QorIQ LS1021A-IOT Gateway Reference Design Board Reference Manual

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Chapter 1
Introduction

The LS1021A-IoT gateway reference design is a purpose-built, small footprint hardware platform equipped with a wide array of both high speed connectivity and low speed serial interfaces engineered to support the secure delivery of IoT services to end-users in a home, business, or other commercial location. The LS1021A-IOT Gateway reference design offers an affordable, ready-made platform for rapidly deploying a secure, standardized, and open infrastructure gateway platform for deployment of IoT services. The reference design combines standards-based, open source software together with a feature-rich IoT gateway design, to establish a common, open framework for secure IoT service delivery and management.

Setting the LS1021A-IOT gateway platform apart is the wide assortment of high-speed and serial-based connectivity it offers in a compact, highly secure design, delivering a truly impressive level of versatility. An additional innovation of the gateway reference design is its support for Arduino Shield^{TM} modules, which further enable the board to support a wide variety of communication solutions offered by the family of Arduino modules. High efficiency is achieved through the use of Freescale's new ARM-based LS1021A embedded processor, which delivers over 5,000 Coremarks of performance at a typical power of under 3 watts. In addition to it's outstanding performance efficiency and high level of integration, the LS1021A-IoT gateway design offers HDMI, SATA2, and USB3 connectors as well as a complete Linux software developer's package.

In addition to high efficiency, integration, and reliability, the LS1021A-IOT reference platform supports a comprehensive level of security, which includes secure boot, Trust Architecture, and tamper detection for both standby and active power modes. Together, these features safeguard customer designs from the point of manufacture to the point of deployment, providing continuous protection from malicious attacks and ensures end products deliver the highest level of security and reliability.

The LS1021A-IOT board is lead-free and RoHS-compliant.

1.1 Related documentation

For more information on the LS1021A-IOT board, see the additional resources listed in the table below.

NOTE

Some of the documents listed below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer or sales representative.

Table 1-1. Related documents

Document	Description
LS1021A QorIQ Advanced Multicore Processor Data Sheet	Provides information about electrical characteristics, hardware design considerations, pin assignments, package, and ordering information.
LS1021A QorIQ Integrated Multicore Processor Reference Manual (LS1021ARM)	Provides a detailed description about LS1021A QorIQ multicore processor and its features, such as memory map, serial interfaces, power supply, chip features, and clock information.
The SystemID Format for Power Architecture™ Development Systems (AN3638)	Freescale Semiconductor Power Architecture™ technology-based evaluation and development platforms may optionally implement a "System ID" non-volatile memory device. This device stores important configuration data about the board.
QorIQ LS1021A IOT Gateway Getting Started Guide (LS1021A-IOTGS)	Explains how to connect the LS1021A-IOT card (700-28203 Rev B) and verify its basic operation. This document shows the settings for switches, connectors, jumpers, push buttons, and LEDs, and the instructions for getting a U-Boot terminal up and running.
MBED documents	https://developer.mbed.org/handbook/Serial

NOTE

Freescale Semiconductor, Inc. does not own the MBED documents and they are mentioned solely for reference purposes.

1.2 Silicon features

The LS1021A processor includes the following functions and features:

- Two (LS1021A) ARM Cortex-A7 cores based on Harvard architecture including AMBA4 MPCORE™ Virtualization, each with separate ECC protected L1 32 KB I cache and 32 KB D cache and a shared 512 KB L2 cache with ECC protection

    - Up to 1.0 GHz at 1.0 V with 32-bit ISA support
    - Three levels of instructions: user, supervisor, and hypervisor
    - Independent boot and reset
    - Secure boot capability with QorIQ Trust Architecture and ARM TrustZone® support
- Hierarchical interconnect fabric
    - Cache Coherency Interconnect (CCI-400)
- 16 or 32-bit DDR3LP/DDR4 SDRAM memory controller with ECC
- Encryption/Decryption (SEC 5.x)
- RegEx pattern matching (PME 2)
- VeTSEC Ethernet interfaces
    - Three 1 Gbit/s Ethernet controllers with IEEE 1588
- High speed peripheral interfaces
    - Two PCI Express 2.0 controllers/ports running at up to 5 GHz
- Additional peripheral interfaces
    - One SATA2 controller supporting up to 3 Gbit/s operation
    - One USB 2.0/3.0 controller with integrated PHY and one USB 2.0 controller with ULPI interface
    - SD/SDXC/eMMC
    - Two SPI controllers and one QuadSPI controller
    - Three I2C controllers
    - Four 16550-compliant UARTs and 6 LPUARTs
    - Integrated flash controller (IFC)
    - Integrated LCD controller 2D-ACE (only on LS1021A)
    - Four FlexCAN controllers (only on LS1021A and LS1022A)
- Multicore programmable interrupt controller (PIC)
- One 8-channel DMA engine
- QUICC Engine block (LS1021A and LS1020A only)
    - 32-bit RISC controller for flexible support of the communications peripherals
    - Serial DMA channel for receive and transmit on all serial channels
    - Two universal communication controllers, supporting TDM, HDLC, UART, and ISDN

1.3 Board features

The features of the LS1021A-IOT reference board are as follows:

- Four lanes of SerDes connections supporting:
    - Two PCI Express buses that support Gen 1 and Gen 2

    - One Gbit Ethernet SGMII interfaces
    - One muxed SATA or Gbit Ethernet SGMII interface
- Integrated USB3 PHY with dedicated SerDes lane
- DDR Controller
    - Supports data rates up to 1600 MHz
    - Supports 1 GB un-buffered DDR3L SDRAM discrete devices (32-bit bus) with 4 bit ECC
    - DDR power supplies 1.35 V to all devices with automatic tracking of VTT
- IFC/Local Bus
    - QSPI: Serial NOR 128 MB
    - CPLD: 8-bit registers in CPLD for system configuration
- Ethernet
    - One Gbit Ethernet RGMII interface to 4-port switch with 4x 10/100/1000 RJ45 ports
    - Two onboard SGMII PHYs with up to two 10/100/1G RJ45 ports (one muxed with SATA)
- System logic CPLD
    - Manages system power and reset sequencing
    - Latch IFC address/data multiplexed signals for 8 bit config register access
    - Signal mux/demux function (for example, LCD and UCC)
    - GPIO routing
    - IRQ routing
    - Level shifter 3.3 V to 1.8 V (for example, JTAG)
    - Switch control
- Clocks
    - DDR clock (DDRCLK) - 66.667 MHz
    - System clock (SYSCLK) - switch selectable to one of three settings: 96 MHz, 99 MHz and 100 MHz for system clock
    - 100 MHz single-source DIFF_SYCLK input to processor, which supports core/platform SYSCLK, DDR controller (DDRCLK), and USB controller (USBCLK)
    - SerDes clocks (100 MHz) that provide clocks to all SerDes blocks and slots
- Power supplies
    - 12 V input Supply 12 V @5 A
    - PoE Class 0 (12.9W) - optional
        - LT3976 - 12 V to 3.3 V for PMIC input supply
        - LT3976 - 12 V to 5 V for SATA and USB ports
        - ISL8201MIRZ - 3.3 V board supply including CPLD
- MC34VR500 Power Management IC (PMIC) supplying VDD and VDDC and GVDD, VTT, VREF, O1VDD, OVDD, L1VDD, and LVDD
- 2x MAX8869

    - MPCIe slots 1.5 V
    - USB HUB1.25 V
- Video
    - Silicon Image SiI9022A for HDMI connection on board
    - 12-bit RGB double edge mode support up to 720p
- USB
    - Two USB 3.0 type A ports via HUB
    - Two USB 2.0 connection on two mini PCIE connectors
- SDHC
    - SDHC port connects directly to a full 8-bit SD/MMC slot
    - Support for SDIO devices
- EEPROM
    - Board MAC address configuration
- I/O Expansion
    - Arduino Shield Connector
    - Port 0 - CAN/GPIO/Flextimer
    - Port 1 - GPIO/CPLD Expansion
    - Port 2 - SPI/I2C/UART
- MBED MK22FX512
    - Serial-to-USB converter
    - Run-control debug interface (CMSIS-DAP)
    - Expansion headers exposing ADCs, GPIO, Timer, and so on for future applications

NOTE

All components are lead-free and RoHS-compliant

1.4 Block diagram

This section provides a high-level overview of the LS1021A processor, as well as the LS1021A-IOT/LS1020A platform. The figure below shows the major functional units within the LS1021A device.

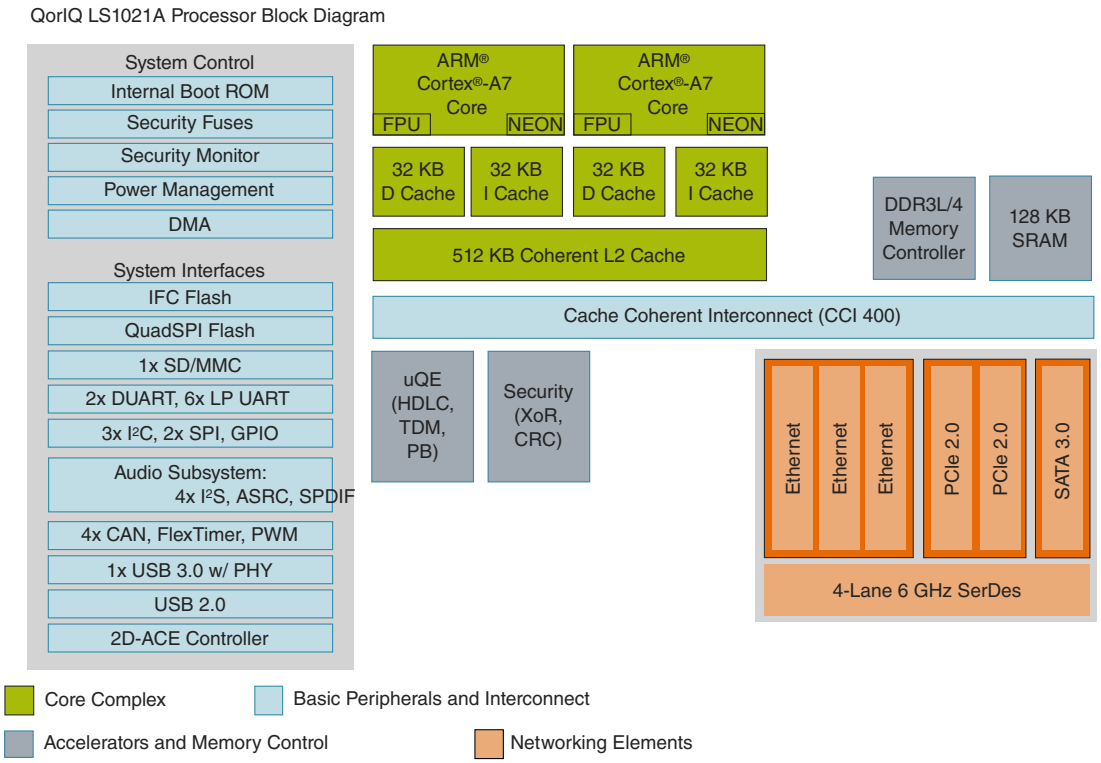

Figure 1-1. LS1021A block diagram

The figure below shows the overall architecture of the LS1021A-IOT/LS1020A platform.

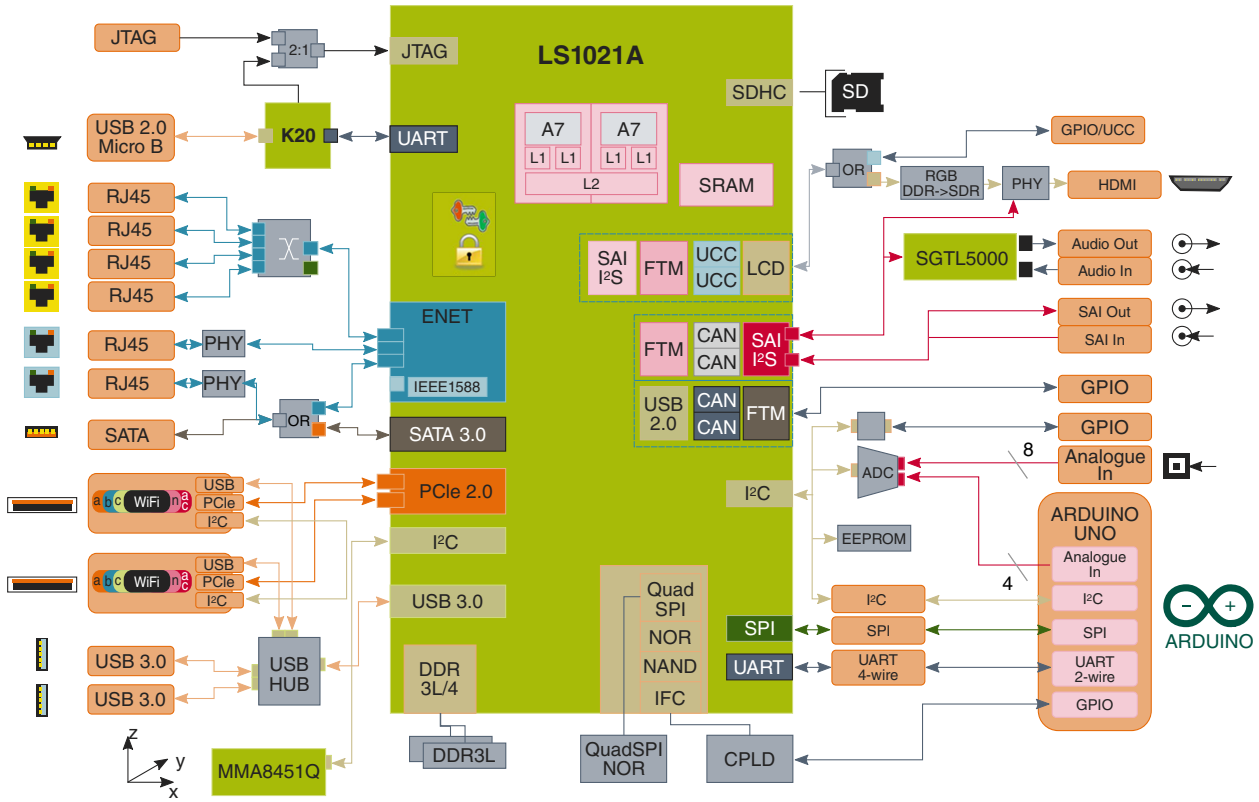

Figure 1-2. LS1021A-IOT System block diagram

Chapter 2
Architecture

The LS1021A-IOT architecture is primarily determined by the processor and by the need to evaluate as many of its features as possible, maximizing testability without impacting the ability to deliver an easily usable off-the-shelf software development platform.

2.1 Processor

The LS1021A-IOT processor supports the features detailed in the following sections.

2.2 Power

The LS1021A-IOT board is powered by an external 12 V at 5 A DC power supply brick. The 12 V is regulated to provide the numerous processor and peripheral device supplies required. The mating plug of the power supply has an inner diameter of 2.1 mm and outer diameter of 5.5 mm. The figure below shows the polarity of the barrel connector.

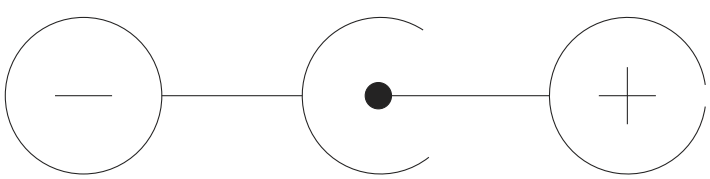

Figure 2-1. Power supply barrel connector polarity

The LS1021A-IOT board requires several power rails to supply the power for the LS1021A and its associated peripheral circuitry. Figure 2-2 shows the board power tree. The 12 V can either be supplied from the barrel connector or alternatively from a Power Over Ethernet (PoE) source plugged into the ETH3 RJ45 port.

CAUTION

When powered from the PoE, the LS1021A-IOT board supports 12.9 W operation. Therefore, care must be taken that this limit is not exceeded.

The +12V0 supplies the following.

Table 2-1. +12V0 distribution

Reference designator	Description	Voltage generated	Supplies
J7	SATA connector	N/A	-
U3	Intersil ISL8201MIRZ	+3V3	+3V3 board power to LS1201A and peripherals
U11	Linear technology LT3976	+5V0	USB Ports, SATA Connector, U502, U30
U12	Linear technology LT3976	+3V3_PMIC	MC34VR500 PMIC (U13)

The +5V0 supplies the following.

Table 2-2. +5V0 distribution

Reference designator	Description	Voltage generated	Supplies
U30	MAX8869EU25	+1V5_MPCIE	MiniPCIe Slots P1 and P2
U502	MAX8869EU25	+1V25	USB HUB - USB5534B (U503)
J25	USB Port 1 and 2	N/A	-
J7	SATA connector	N/A	-

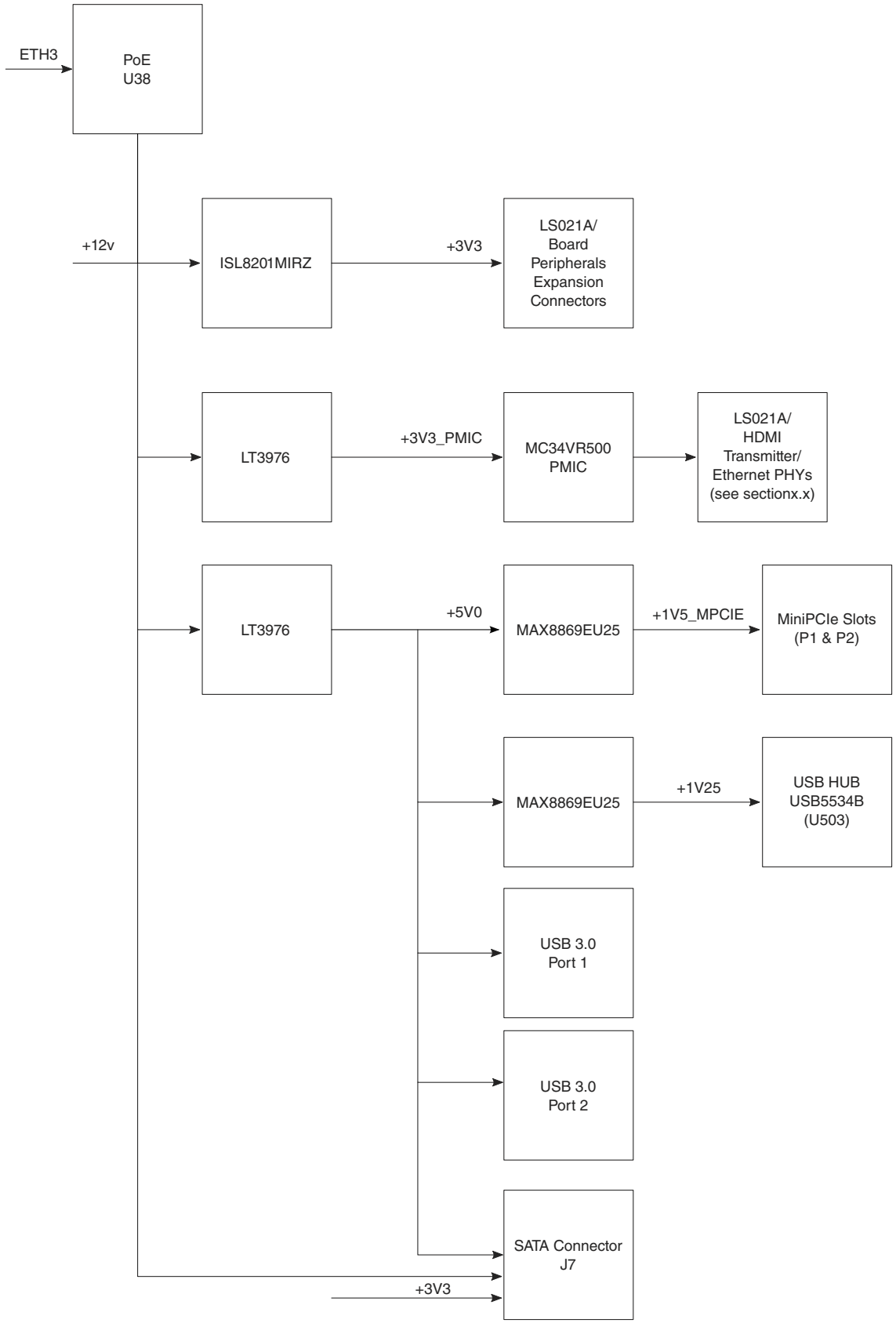

Figure 2-2. LS1021A-IOT power tree

2.2.1 MC34VR500

The LS1021A-IOT uses an MC34VR500 to provide VDD,VDDC, GVDD, OVDD, BVDD, DVDD, EVDD, LVDD, VTT, and VREF power as well as 1.2 V for the HDMI transmitter.

The figure below shows an overview of this power supply.

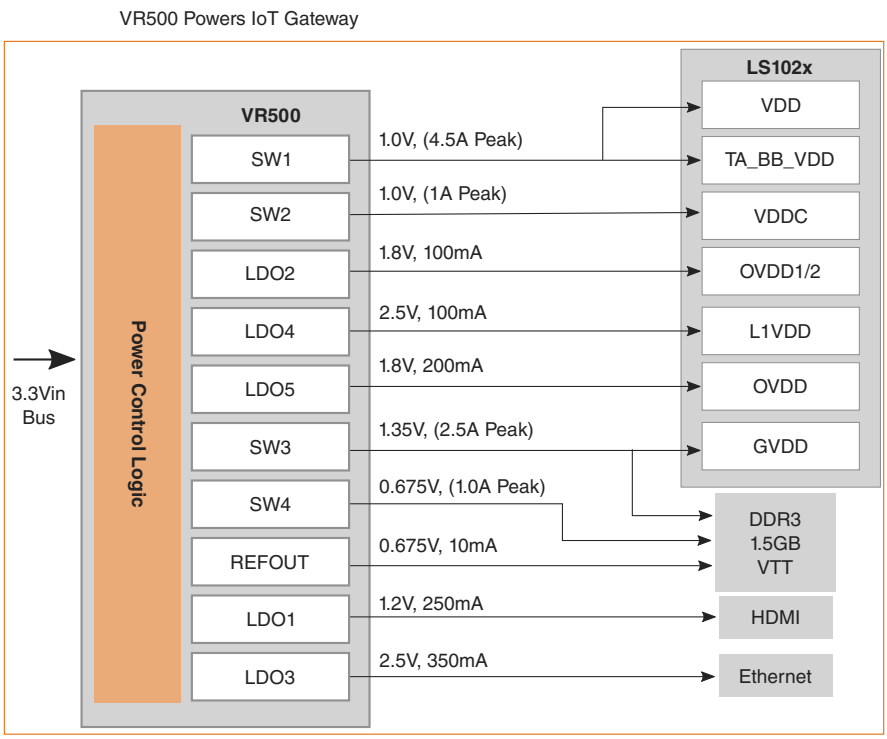

Figure 2-3. LS1021A-IOT powered by MC34VR500

2.2.2 Fuse programming power

Fuse programming power is supplied to allow customer programming of the security fuse processors; this power is normally off to prevent inadvertent fuse programming. Jumpers J19 and J20 should be populated with shunts to connect them to the 1.8 V supply.

2.2.3 Power sequence

Power sequencing is controlled by the CPLD as well as the internal MC34VR500 sequencing. After the 12 V power is supplied to the system, the 3.3 V supply is enabled and the CPLD logic initiates the power sequence. The 3.3 V power to the MC34VR500 PMIC is then enabled and once stable, the MC34VR500 is powered on. The MC34VR500V1 PMIC is programmed to meet the LS1021A power sequence requirements. For more information, see the documentation on MC34VR500.

This power sequence is illustrated in the figure below.

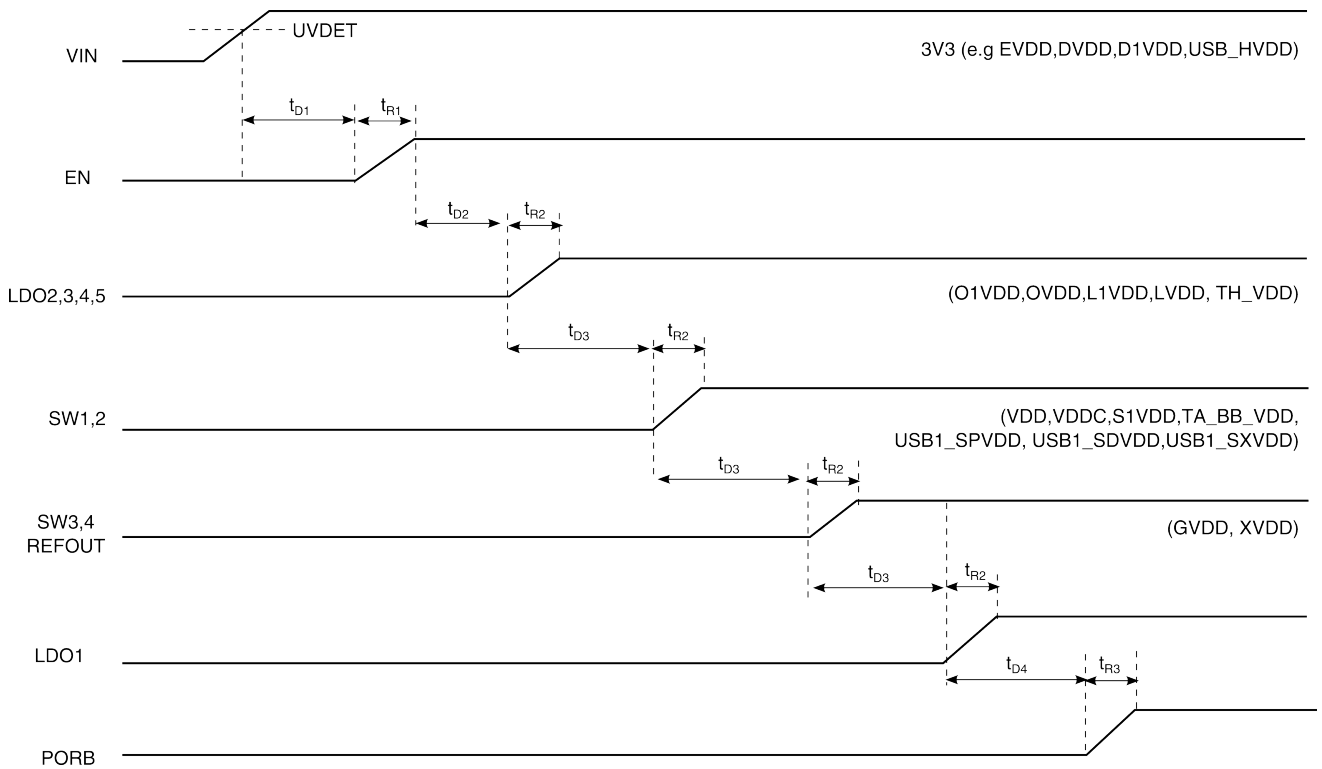

Figure 2-4. LS1021A-IOT power sequence

The table below describes the startup sequence timing.

Table 2-3. 34VR500V1 and V2 startup sequence timing

Parameter	Description	Typ.	Unit
t_{D1}	Turn-on delay	6.0	ms
t_{R1}	Rise time of EN	[1]	ms
t_{D2}	Turn-on delay of first regulator	2.5	ms
t_{R2}	Rise time of regulators [2]	0.2	ms
t_{D3}	Delay between regulators	1.0	ms
t_{D4}	Turn-on delay of PORB	2.0	ms
t_{R3}	Rise time of PORB	0.2	ms

NOTE

[1]: Depends on the external signal driving EN.

[2]: Rise time is a function of slew rate of regulators and nominal voltage selected.

2.3 Deep sleep control

Deep sleep control is not supported on the LS1021A-IOT board.

2.4 Reset

Reset signals to and from the LS1021A board and other devices on LS1021A-IOT are managed by CPLD. The figure below shows an overview of the reset architecture.

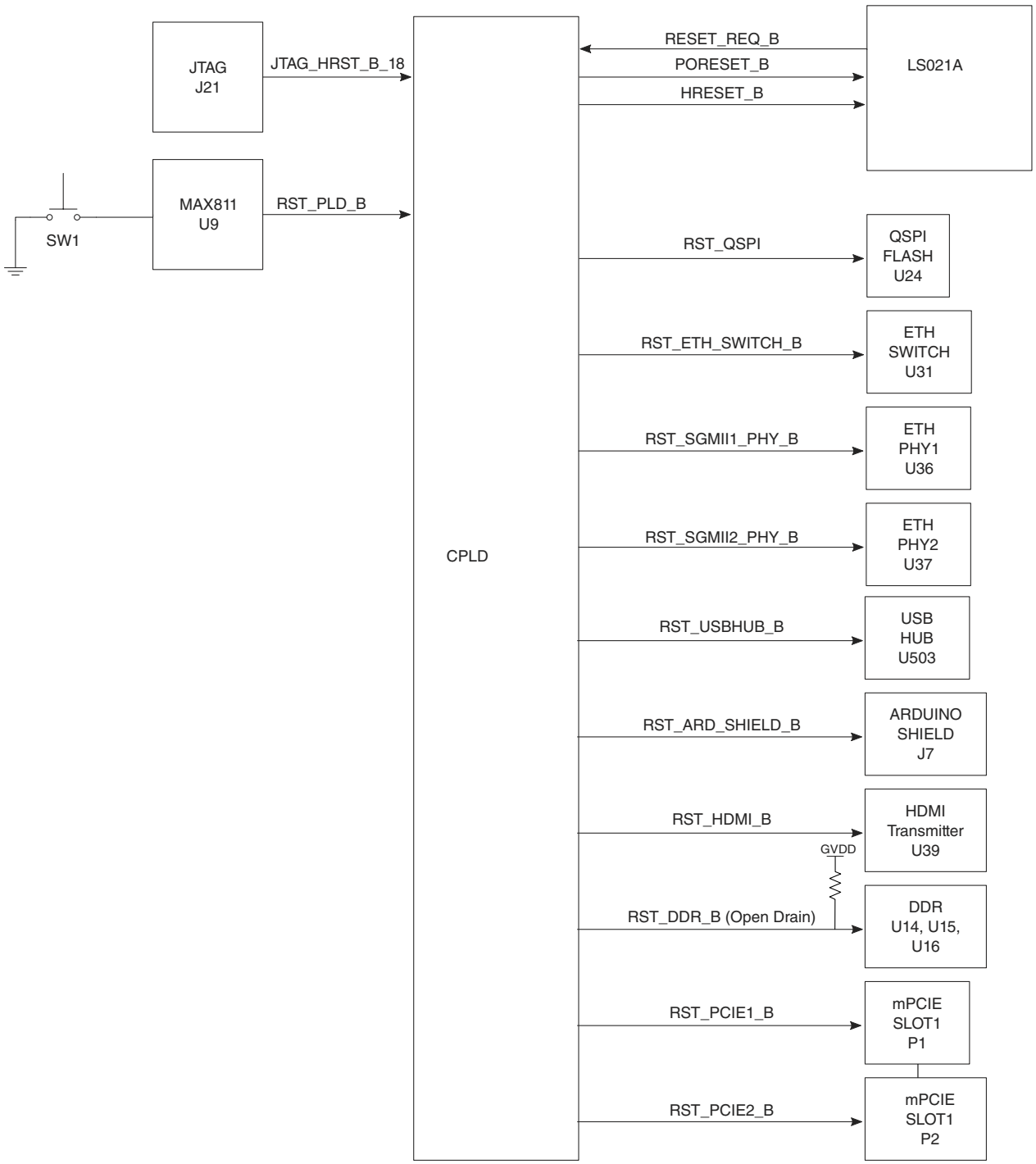

Figure 2-5. Reset architecture

The CPLD implements a reset sequencer, which manages the assertion and release of the reset signals to the system. It also manages the POR configuration and timing to the LS1021A board.

2.4.1 System reset

A system reset is asserted by pressing SW1 located on the rear panel of the chassis. This type of reset power cycles all supplies to the board and asserts all resets in the system. The behavior is the same as cycling the 12 V power.

2.4.2 RESET_REQ reset

The LS1021A RESET_REQ pin can be configured to assert when the chip requires a reset. The LS1021A RESET_REQ pin is routed through the CPLD back to the LS1021A PORESET pin. The CPLD manages the correct POR configuration and timing for the PORESET sequence.

2.4.3 Reset sequence timing

All resets are released simultaneously after the power sequence has completed.

2.5 Device configuration

The processor uses hardware-sampled pins to configure various portions of the device. The remaining configuration is set by the Reset Configuration Word (RCW). These are either driven from the CPLD or hardwired on the board. The LS1021A configuration pins are described in the table below.

Table 2-4. Configuration options

Configuration signal	Nets sampled	Description	Comment
cfg_rcw_src[0:8]	IFC_AD[8:15], IFC_CLE	RCW and Boot Source	SW2[1] - Selectable 0 : QSPI (not supported on revA board) 1 : SDHC (default)
cfg_dram_type	IFC_A[21]		Pulled high on PCB - DDR3L
cfg_ifc_te	IFC_TE	IFC TE signal enable	Driven high during POR by CPLD
cfg_gpinput[0:7]	IFC_AD[0:7]	CPLD Version	MAJOR - AD[0:3] MINOR - AD[4:7]

Table continues on the next page...

Table 2-4. Configuration options (continued)

Configuration signal	Nets sampled	Description	Comment
cfg_eng_use0	IFC_WE0_B	SYSCLK Select	SW2[2] - Selectable 0 : DIFF_SYSCLK 1 : SYSCLK (default)
cfg_eng_use1	IFC_OE_B	-	Reserved

2.6 Clocks

This section describes the clocking scheme on the LS1021A-IOT reference board:

- SYSCLK (single-ended and differential)
- DDRCLK (single-ended)
- SerDes clocks
- Ethernet clocks
- USB clock

The architecture of the clock section is shown in the figure below.

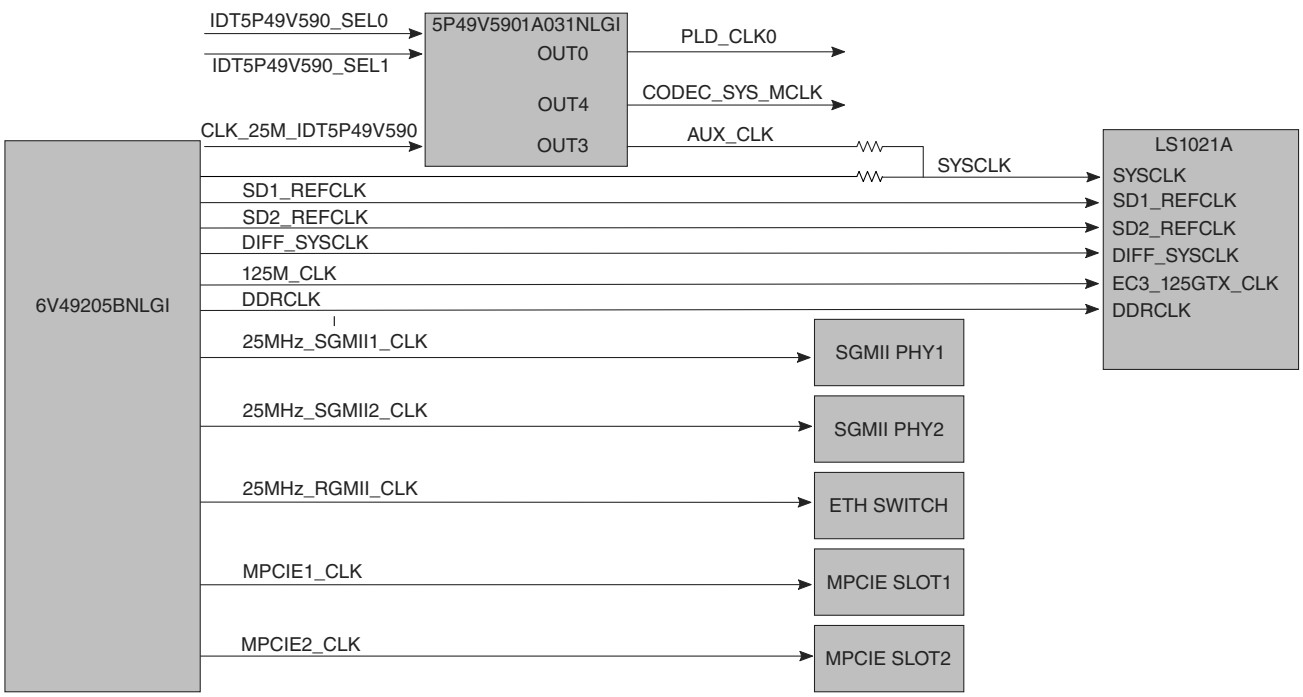

Figure 2-6. Clock architecture

The table below summarizes the board clocking scheme.

Table 2-5. Board clocking scheme

Clock input	Source	Frequency (MHz)	Function	Notes
SYSCLK	6V49205BNLGI	100	For initial debug	
	5P49V5901A031NLGI	.	Selected by S2[6:7]	.
		100	00	Default
		99	01	Alternative HDMI frequency
		96	10	Profibus frequency support
		66.667	11	Reserved
DIFF_SYSCLK	6V49205BNLGI	100		
DDRCLK	6V49205BNLGI	66.667	Pull-up	-
		100	Pull-down	Default
USBCLK	N/A	N/A	USB source lock if DIFF_SYSCLK not used	USB CLK is sourced internally from DIFF_SYSCLK
SERDES_REF_CLK1	6V49205BNLGI	100	S1 SerDes PLL1	
SERDES_REF_CLK2	6V49205BNLGI	100	S1 SerDes PLL2	
EC3_GTX_CLK	6V49205BNLGI	125	RGMII Gigabit CLK	

2.6.1 SYSCLK

SYSCLK is provided either by the IDT6V49205BNLGI or the IDT5P49V5901A031NLGI - both are programmable frequency synthesizers with hardware presets. The IDT5P49V5901A031NLGI is the main source of SYSCLK and the device is strapped depending on the state of SW[6:7]; the default is 100 MHz.

2.6.1.1 Single-Source SYSCLK

A new feature supported on LS1021A is single-source clocking. In this mode, a differential clock is supplied to the DIFF_SYSCLK_P/DIFF_SYSCLK_N inputs on the processor. This will then supply all clocks to the core, platform (SYSCLK), DDR controller (DDRCLK), and USB controller (USBCLK).

2.6.2 DDRCLK

DDRCLK is provided by IDT 6V49205BNLGI, a programmable frequency synthesizer with hardware presets. The device is strapped to provide 100 MHz to DDRCLK during power up.

DDRCLK frequency options are listed in the table below.

Table 2-6. DDRCLK frequency options

DDRCLK pin	DDRCLK	Notes
pull-up	66.67 MHz	n/a
pull-down	100.00 MHz	Default on LS1021A-IOT

2.6.3 SerDes clocks

The LS1021A SerDes port accepts two differential clock inputs (SD1_REFCLK1 and SD1_REFCLK2), allowing the flexibility to use different protocols with different clock rates on the SerDes pins. The clock inputs are provided by the IDT clock generator device, which can generate the required 100.00 or 125.00 frequencies. By default, they are both set to 100 MHz.

2.6.4 Ethernet clocks

An Ethernet clock is also provided by the IDT6V49205BNLGI, which supplies 125.0 MHz to the Ethernet port clock input (EC3_GTXCLK_125), as well as 25 MHz to the separate SGMII PHYs and RGMII PHY.

2.6.5 Codec SYS MCLK

The SGTL5000 audio codec requires a master audio frequency. The IDT5P49V5901A031NLGI is pre-programmed to source 24.576 MHz to it.

2.7 Memory controllers

The LS1021A-IOT board supports high-speed DRAM with 1 GB DDR3L SDRAM discrete devices (32-bit bus) together with 4-bit ECC. The memory interface includes all the necessary termination and I/O power and it is routed so as to achieve maximum performance of the memory bus, as shown in the figure below.

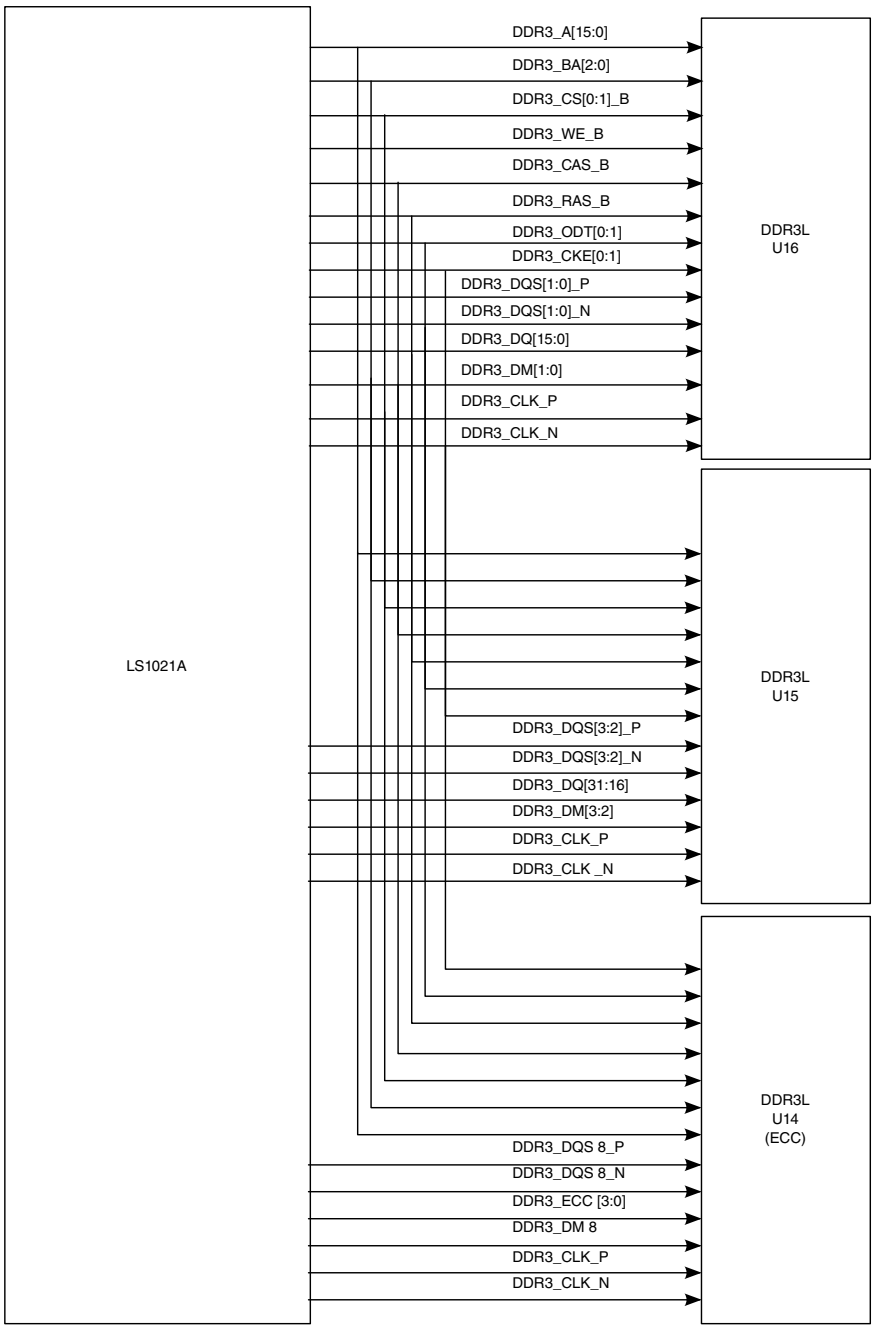

Figure 2-7. Memory controllers

2.8 SerDes port

The LS1021A/LS1020A SerDes block provides four high-speed serial communication lanes supporting a variety of protocols, including:

- SGMII-1.25 / 3.125 Gbit/s
- PCI Express (PEX) Gen 1-1X / 2X / 4X 2.5 Gbit/s
- PCI Express (PEX) Gen 2-1X / 2X / 4X 5 Gbit/s
- SATA-1X1.5 / 3 Gbit/s

An overview of the SerDes protocols supported on LS1021A is shown in the table below.

Table 2-7. LS1021A SerDes protocols

SRDS_PRTCL_S1[128:135] RCW	A	B	C	D
0	PCIe1(x4)			
80	PCIe2(x2)		PCIe2(x2)	
10	PCIe1 (x1)	SATA1	PCIe2(x2)	
20	PCIe1 (x1)	SGMII1	PCIe2 (x1)	SGMII2
30	PCIe1 (x1)	SATA1	SGMII1	SGMII2
40	PCIe1 (x2)		SATA1	SGMII2
50	PCIe1 (x2)		PCIe2 (x1)	SGMII2
60	PCIe1 (x2)		SGMII1	SGMII2
70	PCIe1 (x1)	SATA1	PCIe2 (x1)	SGMII2

The LS1021A-IOT board supports two of these modes (20 and 70). Lanes A, C, and D are routed directly to either the mPCIe slots or to the SGMII2 Ethernet PHY. Lane B is routed through CBTL02043A, a high-speed multiplexer. CBTL02043A allows the Lane B to be routed to either the SATA connector or the SGMII1 Ethernet PHY. The SerDes mux selection is through SW2[5] as described in the table below.

Table 2-8. LS1021A-IOT SerDes Lane B selection

Switch	Setting	Option	Description
.	OFF	.	0 : SerDes Lane 2 - SATA
S2.5	ON	SGMII2_SATA MUX	1 : SerDes Lane 2 - SGMII2 (default)

The user must ensure that the `cfg_srds1_prtcl` field in the RCW is set to the bits shown in Table 2-7 to match the selected SerDes configuration. Software must also configure the appropriate configuration that is selected.

2.8.1 PCI Express support

LS1021A-IOT supports evaluation of two PCI Express slots using mini PCI Express Gen-1 or Gen-2 cards.

Both slots, P1 and P2, have standard mPCIe pinouts as shown in the following table.

Table 2-9. Mini PCIe pinout

Signal	Pin	Pin	Signal
Reserved	51	52	+3.3V
Reserved	49	50	GND
Reserved	47	48	+1.5V_MPCIE
Reserved	45	46	-
Reserved	43	44	-
Reserved	41	42	-
Reserved	39	40	GND
GND	37	38	USB_D+
GND	35	36	USB_D-
PETp0	33	34	GND
PETn0	31	32	SMB_DATA
GND	29	30	SMB_CLK
GND	27	28	+1.5V_MPCIE
PERp0	25	26	GND
PERn0	23	24	+3.3Vaux
GND	21	22	PERST#
Reserved	19	20	Reserved
Reserved	17	18	GND
Mechanical Key			
GND	15	16	Reserved
REFCLK+	13	14	Reserved
REFCLK-	11	12	Reserved
GND	9	10	Reserved
CLKREQ#	7	8	Reserved
Reserved	5	6	1.5V_MPCIE
Reserved	3	4	GND
WAKE#	1	2	3.3V

2.8.2 SGMII support

LS1021A-IOT supports evaluation of the SGMII protocol for serialized Ethernet PHYs. Ethernet data is carried over the SerDes lanes. On the LS1021A-IOT board, two Atheros AR8033 PHYs are used to support SGMII mode.

2.8.3 SATA support

SATA can be evaluated using the onboard SATA header, which provides both power and SerDes lanes to support up to SATA2.0 protocols with a maximum of 3 Gbit/s data rate. The LS1021A-IOT chassis has 4 mounting holes in the lid to accommodate a standard 2.5-inch hard disk drive.

2.9 Ethernet controllers

The LS1021A-IOT board supports three Ethernet Controllers (EC), which can connect to Ethernet PHYs using MII or RGMII protocols. On the LS1021A-IOT board, the EC3 port operates in RGMII mode and is always on, while the EC2 and EC3 ports operate only in SGMII mode. The two SGMII ports connect to Atheros AR8033 PHYs whilst the RGMII is routed to a Realtek RTL8365MB-CG 4 port lightly managed layer 2 Gigabit Ethernet switch. The Ethernet connectivity is shown in the following figure.

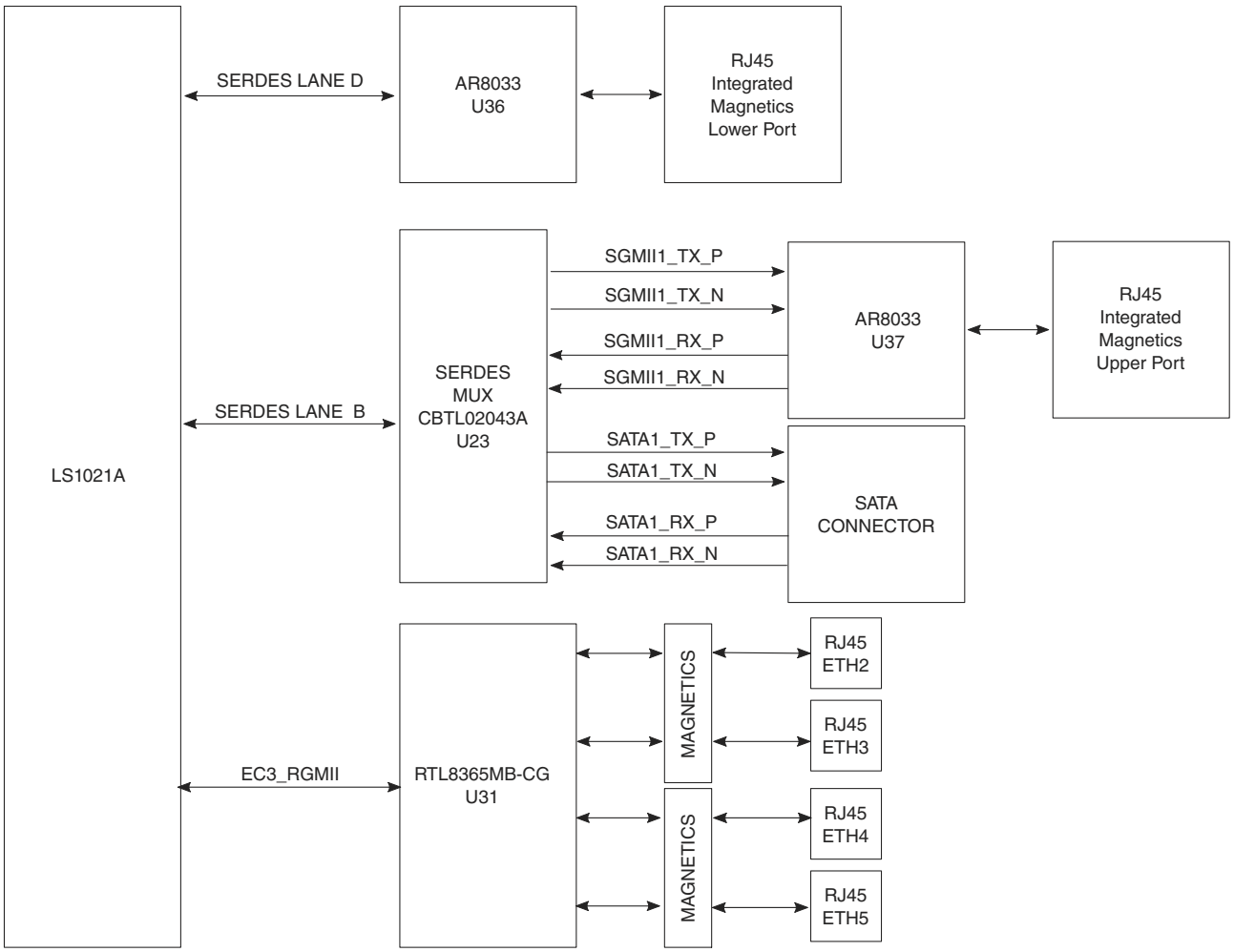

Figure 2-8. Ethernet connectivity

Connections and routing for TSEC are summarized in the following table.

Table 2-10. Ethernet port locations

Description	eTSEC interface voltage	PHY address	Chassis Ref	RJ45 LED color	LED on	LED off
SGMII Ethernet eTSEC1	S1VDD/X1VDD (1.0V/1.35V)	1	ETH0	Green/Orange	On - link Blink - activity	No link
SGMII Ethernet eTSEC2	S1VDD/X1VDD (1.0V/1.35V)	3	ETH1	Green/Orange	ON - link Blink - activity	No link
L2 Switch Ethernet Port1 (via eTSEC3)	LVDD(2.5V)	N/A	ETH2	Green/Orange	On - link Blink - activity	No link
L2 Switch Ethernet Port2 (via eTSEC3)	LVDD(2.5V)	N/A	ETH3	Green/Orange	On - link Blink - activity	No link
L2 Switch Ethernet Port3 (via eTSEC3)	LVDD(2.5V)	N/A	ETH4	Green/Orange	On - link Blink - activity	No link

Table continues on the next page...

Table 2-10. Ethernet port locations (continued)

Description	eTSEC interface voltage	PHY address	Chassis Ref	RJ45 LED color	LED on	LED off
L2 Switch Ethernet Port4 (via eTSEC3)	LVDD(2.5V)	N/A	ETH5	Green/Orange	On - link Blink - activity	No ink

2.10 Ethernet management interfaces

The SGMII PHYs are controlled via the LS1021A Ethernet management interface. The Realtek switch is controlled over the SPI interface. The routing architecture for the both is shown in the following figure.

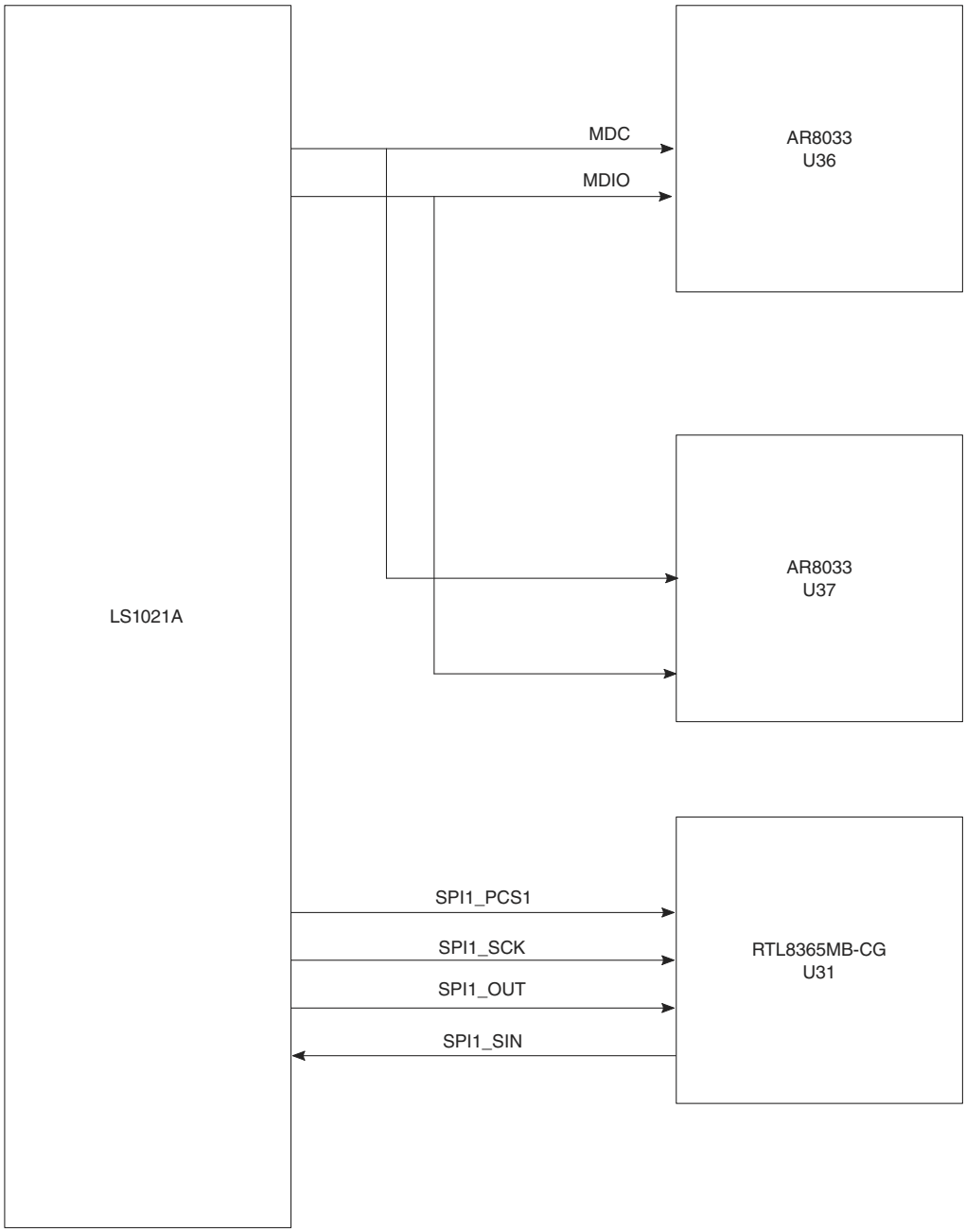

Figure 2-9. Ethernet Management routing

NOTE

IEEE-1588™ is not supported on the LS1021A-IOT board.

2.11 USB interface

The LS1021A-IOT routes the integrated USB 3.0 (USB1) controller on the LS1021A board to the USB5534B 4 port USB 3.0 Hub. Ports 1 and 2 are used in full USB 3.0 mode with both SuperSpeed and traditional USB 2.0 signals being routed to a Dual USB 3.0 Type A connector. Power ON/OFF control to the connector is via the MAX1558H, which is managed by the USB hub. Power fault detection is also monitored by the Hub.

The remaining two ports (3 and 4) use only the USB 2.0 portion of the port and are routed to the two mini PCIe slots.

The following figure illustrates the USB architecture.

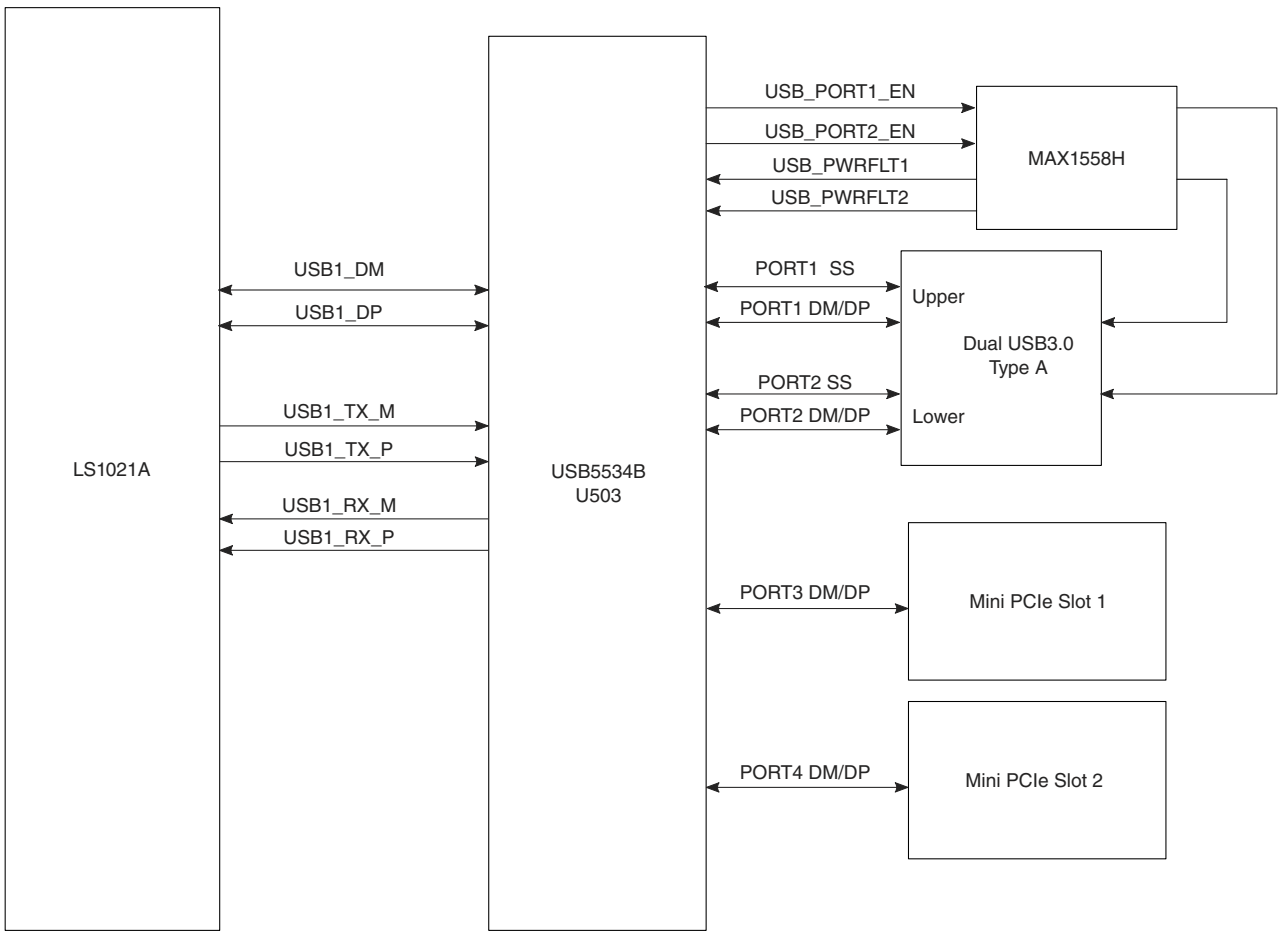

Figure 2-10. USB architecture

NOTE

The USB block requires no board-specific setup or programming.

2.12 Local bus

The LS1021A Integrated Flash Controller (IFC), also called the "local bus", supports 32-bit addressing and 8- or 16-bit data widths for a variety of devices. Due to pin multiplexing restrictions, only limited options are available. On the LS1021A-IOT, Quad SPI Flash was selected, which only leaves the 8 LSB multiplexed IFC_AD lines as well as CS0, WE_B and OE_B. This 8-bit parallel interface is connected to the CPLD and provides one 8-bit wide read register and one 8-bit wide write register.

NOTE

No dedicated address lines are available in the multiplexed mode.

The following figure gives an overview of the IFC bus.

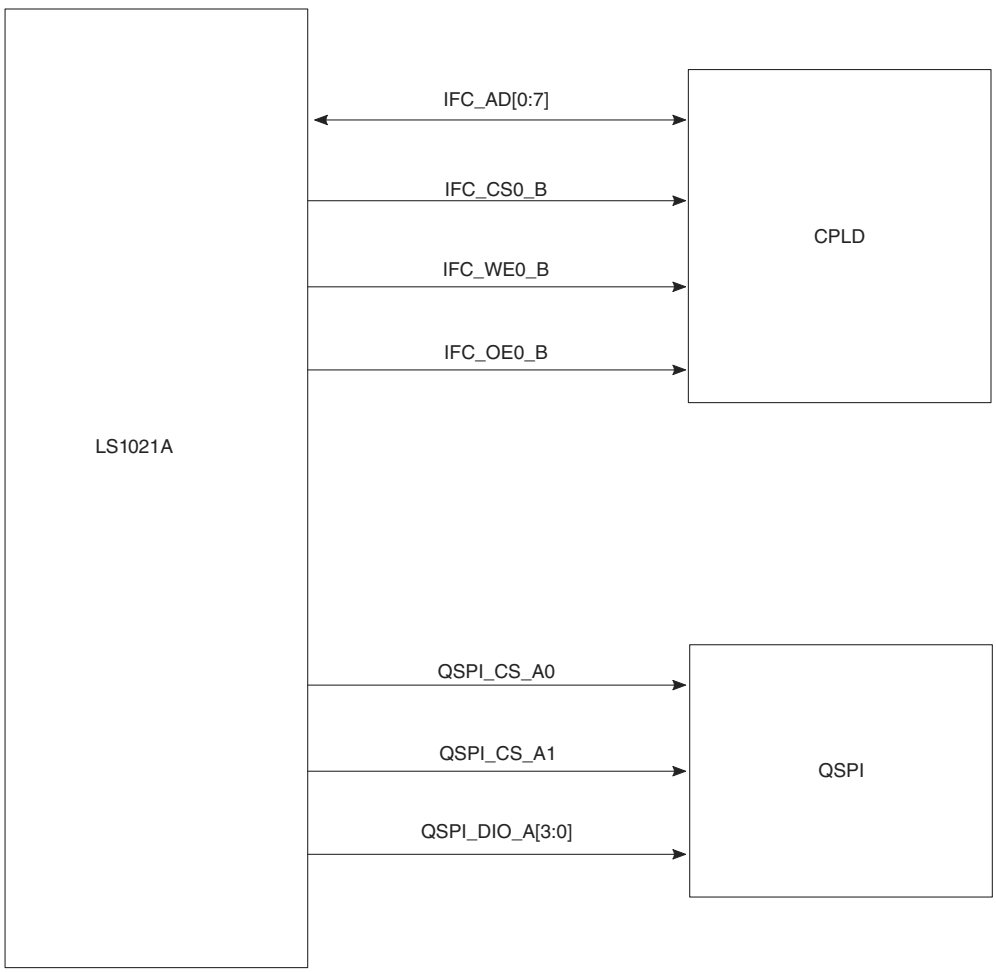

Figure 2-11. IFC architecture

On the LS1021A-IOT board, the devices available on the IFC bus are as follows.

Table 2-11. IFC devices

IFC device	Mfg.	Part number	Description
QSPI	Spansion	S70FL01GS	512 KB QSPI NOR Flash
CPLD registers	Freescale	n/a	1x Read register (DIP switch settings) 1x Write register (TBD)

2.13 2D ACE - display controller port

The LS1021A board has an internal Display Control Unit (2D ACE), suitable for driving video at resolutions up to XVGA (1024 x 768 x 24 bpp x 60 Hz). Higher resolutions, such as UXGA, may be possible, depending on the overall system memory bandwidth. The display buffer resides in the main memory, with the R-G-B pixel data streaming out at a rate sufficient to maintain the LCD raster. Since the DCU handles all the raster generation, all that remains is to convert the data stream into a format suitable for the LCD displays.

The LS1021A board implements a double data rate interface where data is sampled on rising and falling edges. The Sil9022A HDMI transmitter can support this mode directly however for higher resolutions such as 720p/1080p a 24-bit single edge interface must be used. To accommodate these higher resolutions the DCU hardware signals are routed through the CPLD converted to 24-bit single edge mode. The Sil9022A drives a TMDS bus to an HDMI connector as shown in the figure below.

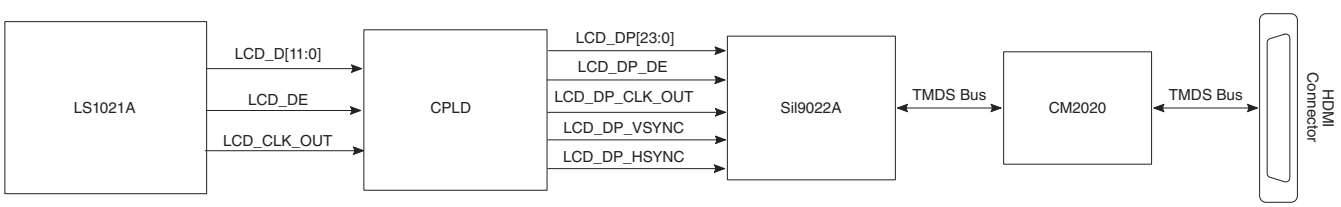

Figure 2-12. DIU architecture

2.13.1 Programming display control unit

The display control unit (2D-ACE) should be programmed to generate the pixel data/ clock/enables in order to properly drive the selected encoder.

- Program the DCU with the following information:
  - Raster (framebuffer) width, height, and depth
  - An "Area Of Interest" (often equal to the width and height of the display)
- Pixel clock within limits of the monitor
- Horizontal and vertical sync parameters, which include:
  - Polarity (generally positive, but not always)
  - Front/back "porch" - the interval between sync transitions and active pixel data; usually one or two pixel clocks (HSYNC) or one or two lines (VSYNC) are sufficient.
  - Sync assertion time - display width (in pixels) with front and back porch (in pixels) and the sync assertion time should be approximately equal to the horizontal timing parameter stated by the monitor. This could be in units of microseconds, pixels or Hz. A similar process is used for vertical timing.

2.14 I^2C

The LS1021A-IOT board utilizes two of the four I2C busses available on the device.

The devices available on each I2C bus segment are listed in the table below.

NOTE

Due to Rev A silicon errata, the two I2C buses are commoned via zero ohm resistors so that both buses can be accessed via I2C1.

I^2C bus device addresses are summarized in the tables below.

Table 2-12. I2C1 bus device map

7b Addr.	Description	Device	Notes
0x2A	Audio Codec	SGTL5000	n/a
0x51	Board EEPROM	SiI9022A	n/a
	USB Hub	USB5534B (U503)	Isolated from bus, by default

The second I2C1 bus device map is given below.

Table 2-13. Second I2C1 bus device map

7b Addr	Description	Device	Notes
0x08	PMIC	MC34VR500V1ES(U13)	
0x1C	Accelerometer	MMA8451Q (U18)	

Table continues on the next page...

Table 2-13. Second I2C1 bus device map (continued)

7b Addr	Description	Device	Notes
0x23	GPIO Expander	PCA9555BS (U2)	n/a
0x35	12 bit ADC	MAX1239 (U6)	
0x44	Current monitor	INA220AIDGST (U17)	1V Monitor
0x45	Current monitor	INA220AIDGST (U1)	12V Monitor
0x48	Thermal Monitor	LM75BD (U7)	Case
0x4C	Thermal Monitor	ADT7461(U32)	LS1021A
0x72	HDMI Transmitter	SiI9022A (U39)	TPI
0x7A	HDMI Transmitter	SiI9022A (U39)	Internal registers
0xC0	HDMI Transmitter	SiI9022A (U39)	Transmitter CPI
	IDT 5P Clock Driver	IDT5P49V5901A031NLGI(U21)	Isolated from bus, by default
	IDT 6V Clock Driver	IDT6V49205BNLGI (U29)	
-	Arduino Shield	J8	
-	Arduino Shield	J15	Via I2C Expander
-	miniPCIe1 Slot	P1	
-	miniPCIe2 Slot	P2	
-	I2C Repeater	PCA9515 (U10)	

NOTE

The 7b addresses do not include the R/W bit as an address member, though some datasheets might do so. For consistency, all I2C addresses are of 7 bits only.

2.15 SPI interface

The LS1021A board has two serial peripheral interfaces (SPI). It uses SPI1 to control several onboard peripherals as well as being made available on connectors for external peripheral use. SPI2 is not available due to pin multiplexing.

The figure below shows the overall connections of the SPI.

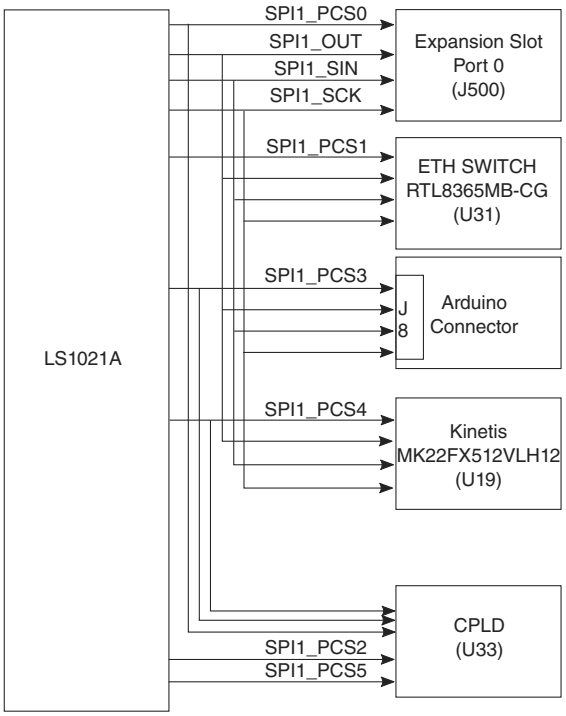

Figure 2-13. SPI architecture

2.16 SDHC interface

The LS1021A SDHC interface supports a large variety of devices, with the LS1021A-IOT board supporting a subset as follows:

- MMC cards, 1x, 4x or 8x wide, 3.3 V only
- Legacy MMC cards: 1x, 4x or 8x wide, 3.3 V only
- SDHC card, 1x or 4x wide, 3.3 V only
- SDIO cards, 1x, 4x, 8x wide, 3.3 V only

To handle all these options, LS1021A-IOT system features a full-sized SDHC connector.

NOTE

SDHC_WP and SDHC_CD_N are multiplexed with I2C2 signals. Therefore, by default, they are not supported.

The following figure shows the overall connections of the SDHC portion.

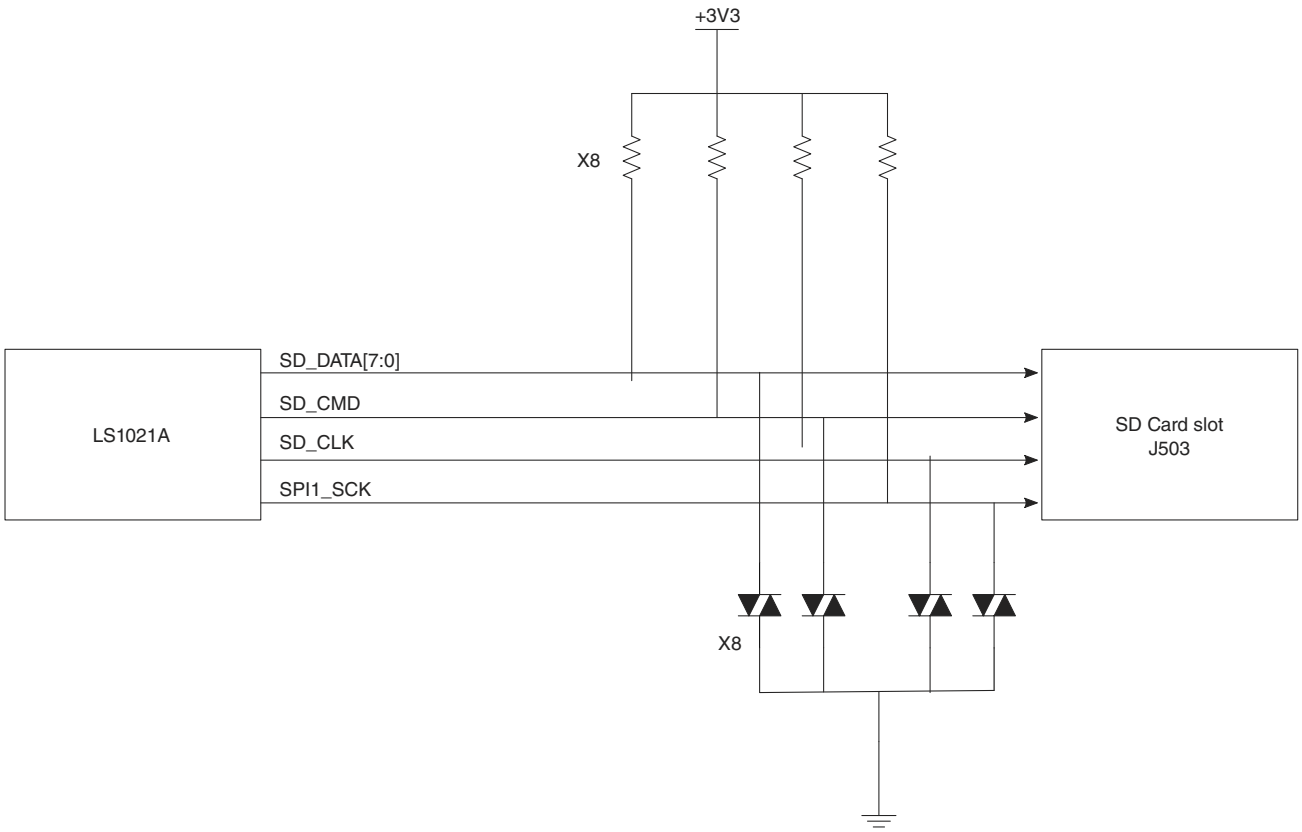

Figure 2-14. SDHC architecture

2.17 Interrupt controller

As the LS1021A board has only six external interrupt pins, they are connected to the CPLD so that the various board interrupt sources can be consolidated to individual interrupt pins as well as provided with appropriate voltage level conversion.

The figure below shows the interrupt architecture.

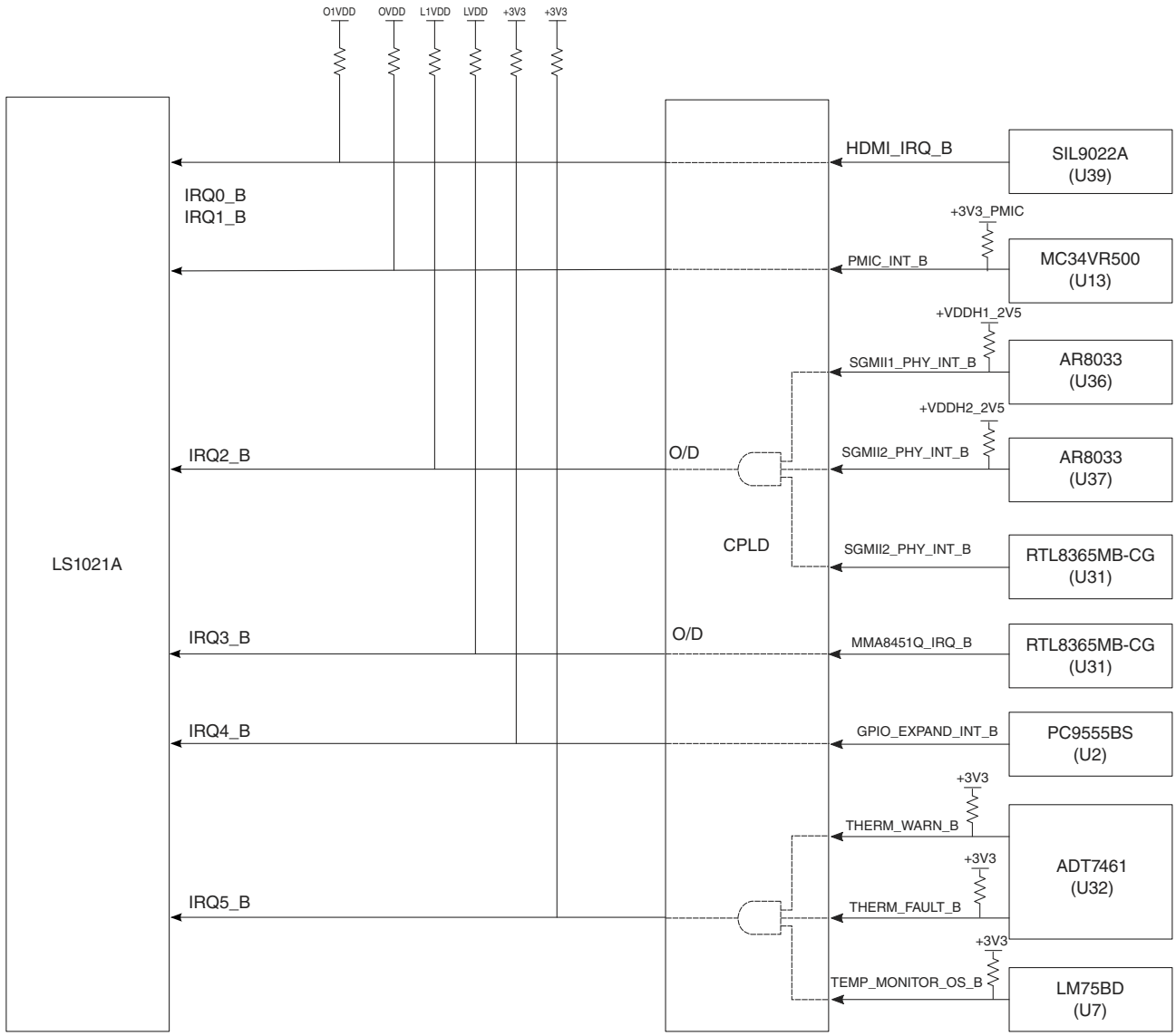

Figure 2-15. Interrupt architecture

The connection from external interrupts to the external MPIC pins is shown in the table below.

NOTE

IRQ2_B and IRQ3_B are tri-stated on the CPLD and pulled to the appropriate voltage rail.

Table 2-14. Interrupt connections

Signal names	Connected devices	CPLD O/D	Note
IRQ0_B	HDMI Interrupt	NO	+1.8V O1VDD, Pull-up on board

Table continues on the next page...

Table 2-14. Interrupt connections (continued)

Signal names	Connected devices	CPLD O/D	Note
IRQ1_B	PMIC Interrupt	NO	+1.8V OVDD, Pull-up on board
IRQ2_B	Ethernet Interrupts	YES	+2.5V L1VDD, Pull-up on board IRQ2_B = SGMII1_PHY_INT_B & SGMII2_PHY_INT_B & ETH_SW_INT_B
IRQ3_B	Accelerometer	YES	+2.5V LVDD, Pull-up on board
IRQ4_B	GPIO Expander	NO	+3.3V DVDD, Pull-up on board
IRQ5_B	Thermal monitors	NO	+3.3V DVDD, Pull-up on board IRQ5_B = THERM_WARN_B & THERM_FAULT_B & TEMP_MONITOR_OS_B

2.18 Event pins

The Event pins are not currently used on the LS1021A-IOT board and are connected to the CPLD for future use.

Table 2-15. Event Pin connections (continued)

Signal names	Connected devices	Note
EVT0_B	N/A	Unused
EVT1_B	N/A	Unused
EVT2_B	N/A	Unused
EVT3_B	N/A	Unused
EVT4_B	N/A	Unused
EVT9_B	N/A	Unused

2.19 Serial ports

Two of the LS1021A UARTS are available on the LS1021A-IOT board. UART1 is configured as a 2-wire serial port to an MBED enabled Kinetis MK22 circuit, which provides UART over USB. The Kinetis USB is accessed via a Micro-B connector (J25) and can be used as a console UART using a program such as Teraterm on a host PC. The second UART on the LS1021A-IOT board is the 4-wire LPUART1, which is routed to

the Arduino header (J17) and expansion port 0 (J500). Note that the Arduino header only supports the TXD and RXD signals with Port 0 adding CTS and RTS control signals. The following figure shows an overview of the serial ports.

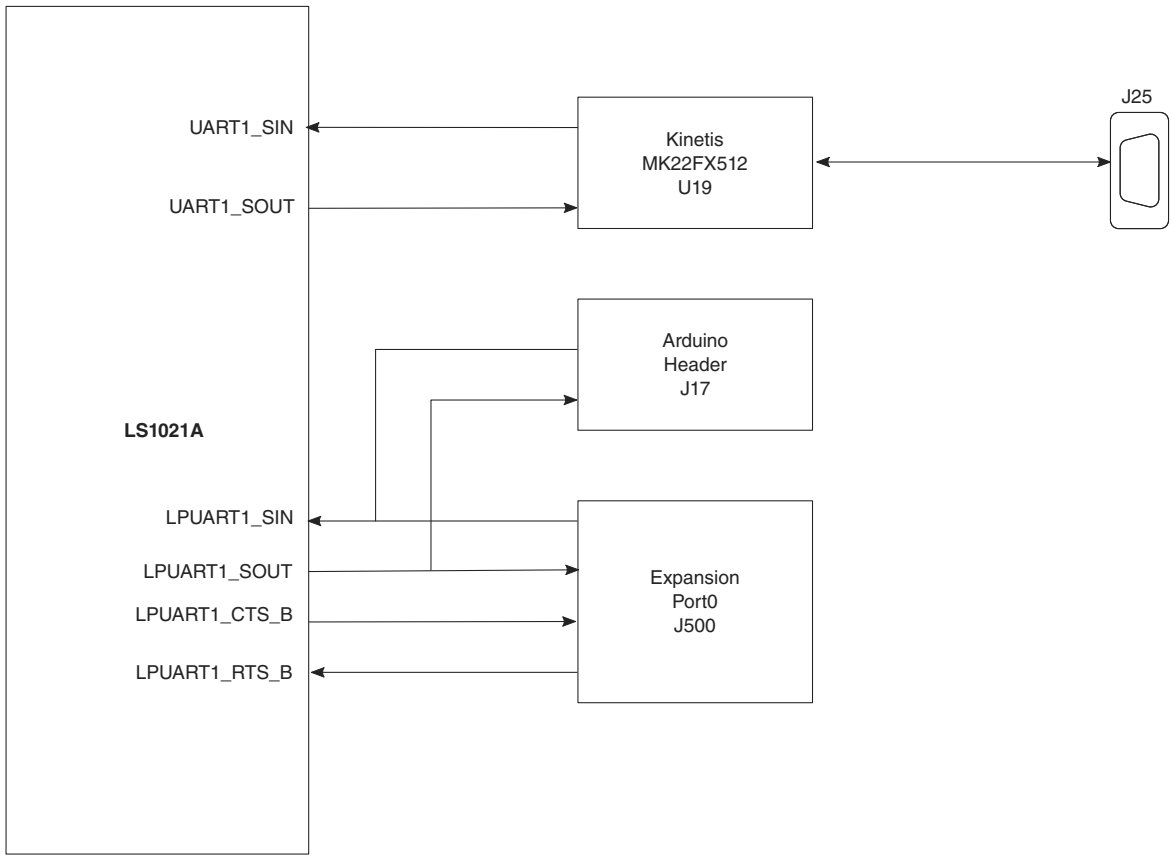

Figure 2-16. Serial architecture

2.20 Audio port

The Synchronous Audio Interface (SAI) architecture can be illustrated as shown in the figure below.

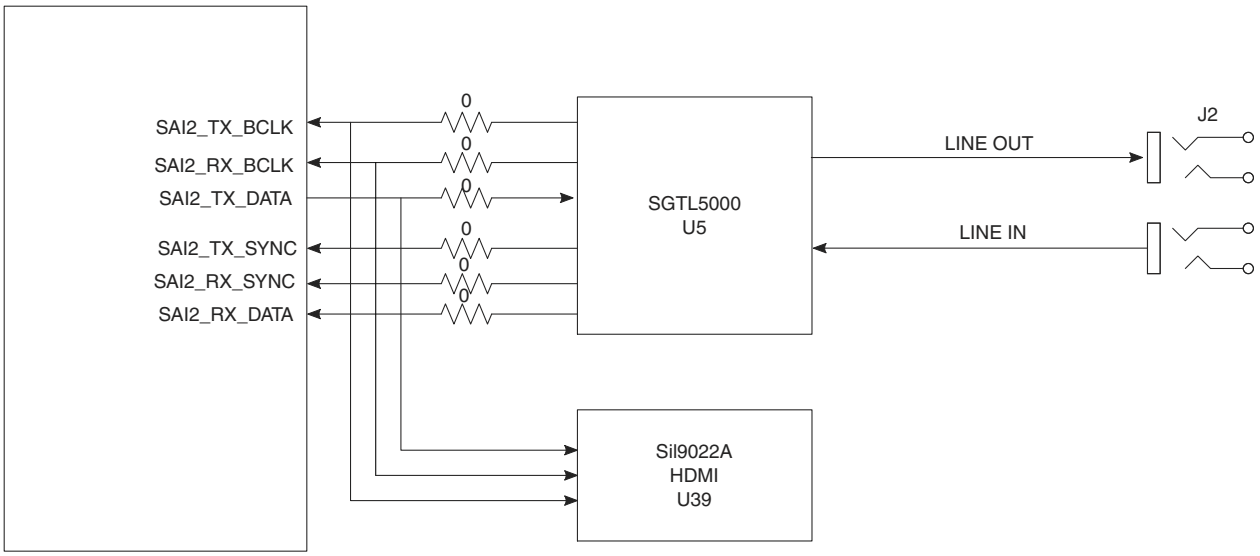

Figure 2-17. Audio port architecture

The LS1021A board supports four full duplex Synchronous Audio Interface (SAI) ports. The LS1-21A-IOT uses one of these ports (SAI2) in I2S mode. A bidirectional connection to the Freescale SGTL5000-32QFN CODEC (U5) provides Line IN, Line OUT functionality to J2 available on the rear panel.

NOTE

By default, the SGTL5000 is configured to be the Master of the bus and therefore, generates CLK and SYNCs for both transmit and receive directions.

SAI2 transmit is also routed to the HDMI transmitter to supply audio output.

2.21 JTAG port

The LS1021A board has a JTAG port for debug purposes. Access to the JTAG port is either through an ARM Cortex 10-pin header or via the CMSIS-DAP implemented in the Kinetis MK22FX512. Using the standard 10-pin header requires an external piece of hardware such as the Codewarrior TAP for ARM. The CMSIS-DAP provides an alternative via a USB cable.

The COP/JTAG architecture is shown in the figure below.

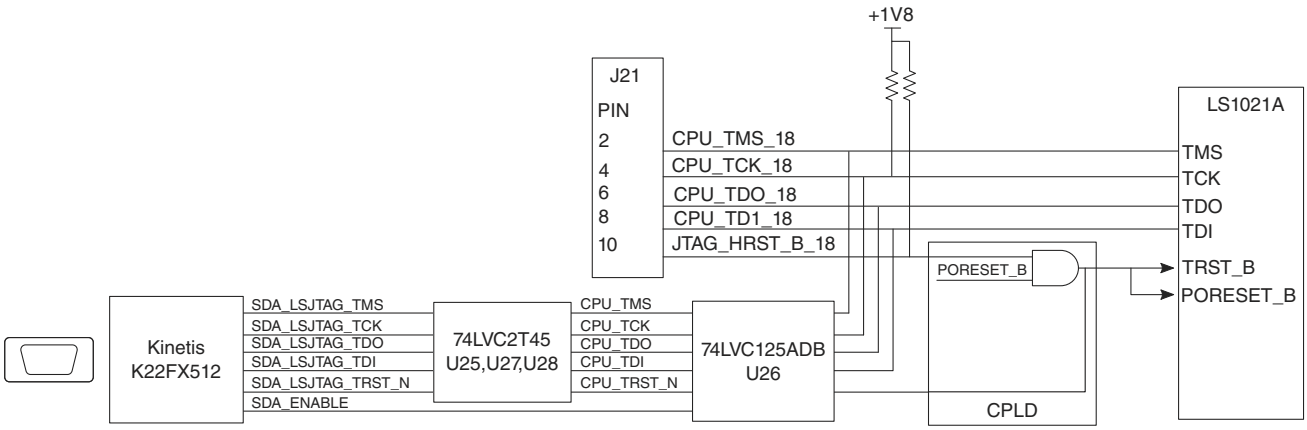

Figure 2-18. JTAG/COP connections

2.22 GPIO pins

The LS1021A board has no dedicated GPIO pins; instead, GPIO functions are multiplexed internally on other signals, which must be disabled before using the GPIO functions.

The LS1021A-IOT board provides the following GPIO options.

Table 2-16. GPIO mapping

GPIO availability	Notes
GPIO3{27:15]	Available on back panel Port 2 (J502). Muxed on LS1021A with CAN/USB2/FTM/RGMII functionality selected through RCW.
GPIO_EXPAND[7:0]	Controlled via I2C. Available on back panel Port 1 (J501).
CPLD_EXPAND[5:0]	Connected to CPLD. Available on back panel Port 1 (J501) Functionality reserved for future use.

2.23 Monitoring LEDs

The LEDs on the LS1021A-IOT board can be used to monitor various functions of the system as described in the table below.

Table 2-17. Monitoring LEDs

Description	Ref	Color	LED on	LED off
K22 MBED status	D5	Green	MBED mode LED ON - MBED driver running LED Blink - UART/ CMSIS-DAP activity Bootloader mode LED BLINK SLOW - Bootloader running LED BLINK FAST - Application image flashed	
LS1021A ASLEEP	D6	Red	ASLEEP	Out of asleep
+3V3	D7	Green	3V3 Power ON	3V3 Power OFF
Reset Complete	D8	Green	Reset Sequence Completed Successfully	Reset not complete
SGMII Ethernet eTSEC1	ETH0	Green/ Orange	ON - Link blink - Activity	No link
SGMII Ethernet eTSEC3	ETH1	Green/ Orange	ON - Link blink - Activity	No link
L2 Switch Ethernet Port1	ETH2	Green/ Orange	ON - Link blink - Activity	No link
L2 Switch Ethernet Port2	ETH3	Green/ Orange	ON - Link blink - Activity	No link
L2 Switch Ethernet Port3	ETH4	Green/ Orange	ON - Link blink - Activity	No link
L2 Switch Ethernet Port4	ETH5	Green/ Orange	ON - Link blink - Activity	No link

2.24 MBED

This section describes the MBED circuit on the LS1021A-IOT board. MBED is an open-standard serial and debug adapter. It bridges serial and debug communications between a USB host and an embedded target processor as shown in the figure below.

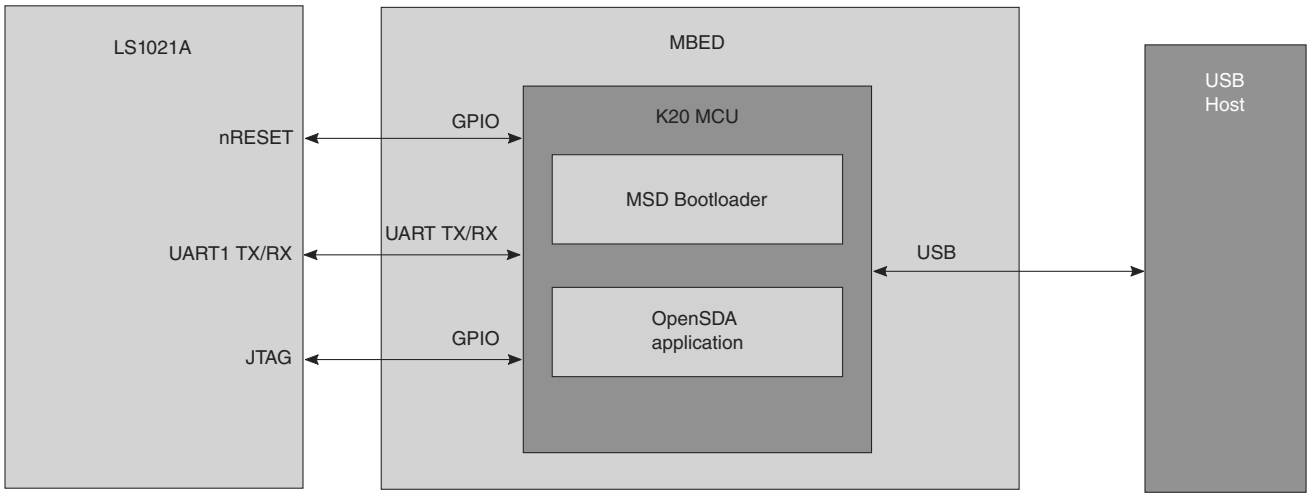

Figure 2-19. MBED architecture

MBED is managed by a Kinetis K22 MCU built on the ARM® Cortex™-M4 core. The Kinetis K22 includes an integrated USB controller that can operate at clock rates up to 50 MHz. The MBED circuit includes a status LED and a pushbutton. The pushbutton asserts the Reset signal to the target processor. GPIO signals provide an interface to the JTAG debug port on a target processor. Additionally, signal connections are available to implement a UART serial channel.

MBED features a mass storage device (MSD) bootloader, which provides a quick and easy mechanism for loading different MBED applications, such as flash programmers, run-control debug interfaces, serial-to-USB converters, and more.

Chapter 3
Expansion Headers and Ports

The LS1021A-IOT board features numerous expansion options to provide additional interfacing options. This chapter describes Pinouts for the various headers and expansion ports.

3.1 K22 expansion (internal)

The K22 is primarily used for UART-to-USB conversion as well as JTAG access. However, it has numerous additional IOs that are made available on two headers (J4 and J9). Currently, these are defined as reserved, as no software is in place to utilize them.

The following two tables detail the connectivity to the K22.

Table 3-1. J4 Pinout

Pin	Net name	K22 PIN number	K22 Pin name	Pin	Net name	K22 PIN number	K22 Pin name
1	SDA_PTA5	27	PTA5	2	GND	-	-
3	SDA_PTA12	28	PTA12	4	SDA_PTBB0	35	SDA_PTB0
5	GND	-	-	6	SDA_PTB2	37	SDA_PTB2
7	SDA_PTA13	29	PTA13	8	+3V3	-	-
9	SDA_PTC0	43	PTC0	10	SDA_PTB3	38	SDA_PTB3
11	SDA_PTC8	53	PTC8	12	SDA_PTB16	39	SDA_PTB16
13	GND	-	-	14	SDA_PTB17	40	SDA_PTB17
15	SDA_PTC9	54	PTC9	16	GND	-	-
17	SDA_PTC10	55	PTC10	18	SDA_PTB18	41	SDA_PTB18
19	SDA_PTC11	56	PTC11	20	SDA_PTB19	42	SDA_PTB19

The following table details the J9 Pinout connectivity to the K22.

Table 3-2. J9 Pinout

Pin	Net name	K22 PIN number	K22 Pin name	Pin	Net name	K22 PIN number	K22 Pin name
1	K20_VREFH	14	VREFH	2	K20_VDDA	13	VDDA
3	SDA_VREF_OUT	17	VREF_OUT	4	K20_VSSA	16	VSSA
5	GND	-	-	6	+3V3	-	-
7	SDA_DACO_OUT	18	DACO_OUT	8	SDA_PTE0	1	PTE0
9	GND	-	-	10	SDA_PTE1	2	PTE1
11	SDA_ADC0_DP3	11	ADC0_DP3	12	GND	-	-
13	SDA_ADC0_DM3	12	ADC0_DM3	14	-	-	-
15	GND	-	-	16	+3V3	-	-
17	SDA_ADC0_DP0	9	ADC0_DP0	18	GND	-	-
19	SDA_ADC0_DM0	10	ADC0_DM0	20	GND	-	-

3.2 Audio expansion (internal)

The LS1021A Serial Audio Interface 1 (SAI1) is brought to a six-pin header - reserved for future use.

Table 3-3. J6 Pinout

Pin	Net name	LS1021A Pin number	LS1021A Pin name	Pin	Net name	LS1021A Pin number	LS1021A Pin name
1	SAI1_TX_SYNC	Y6	SAI1_TX_SYNC	2	SAI1_RX_SYNC	AC5	SAI1_RX_SYNC
3	SAI1_TX_DATA	W5	SAI1_TX_DATA	4	SAI1_RX_DATA	AB4	SAI1_RX_DATA
5	SAI1_TX_BCLK	W6	SAI1_TX_BCLK	6	SAI1_RX_BCLK	AC3	SAI1_RX_BCLK

3.3 Arduino expansion (internal)

The LS1021A-IOT board implements an Arduino Uno pinout to allow connection of SPI/ UART and I2C shields. Typically, this slot will be used for low power radios such as ZigBee or 6LoPan.

J7 provides power to the Arduino shield. J8 has SPI1 and I2C2. Four ADC channels from the MAX1239 (U6) are made available on J15 as well as an alternative source for I2C2. SPI1 is also available on J16. J17 contains GPIOs that are connected to the CPLD.

NOTE

These signals are not implemented in the CPLD logic and are reserved for future use.

Table 3-4. J7 Pinout

Pin	Net name	Source	Pin	Net name	Source
1	N/C	-	2	+3V3	Power
3	RST_ARD_SHIELD	CPLD	4	+3V3	Power
5	+5V0	Power	6	GND	Power
7	GND	Power	8	+12V	Power

Table 3-5. J8 Pinout

Pin	Net name	Source	Pin	Net name	Source
1	N/C	-	2	N/C	-
3	SPI1_PCS3	LS1021A SPI1	4	SPI1_OUT	LS1021A SPI1
5	SPI1_SIN	LS1021A SPI1	6	SPI1_SCK	LS1021A SPI1
7	GND	Power	8	AREF	TP2
9	I2C2_SDA_EXP	I2C2 bus Expander (U10)	10	I2C2_SCL_EXP	I2C2 bus Expander (U10)

Table 3-6. J15 Pinout

Pin	Net name	Source	Pin	Net name	Source
1	ADC_CH0	MAX1239 ADC (U6)	2	ADC_CH1	MAX1239 ADC (U6)
3	ADC_CH2	MAX1239 ADC (U6)	4	ADC_CH3	MAX1239 ADC (U6)
5	I2C2_SDA_EXP	I2C2bus Expander (U10)	6	I2C2_SDA_EXP	I2C2bus Expander (U10)

Table 3-7. J16 Pinout

Pin	Net name	Source	Pin	Net name	Source
1	SPI1_SIN	LS1021A SPI1	2	+5V0	Power
3	SPI1_SCK	LS1021A SPI1	4	SPI1_OUT	LS1021A SPI1
5	RST_ARD_SHIELD	CPLD	6	GND	Power

Table 3-8. J17 Pinout

Pin	Net name	Source	Pin	Net name	Source
1	LPUART1_SIN	LS1021A LPUART1	2	LPUART1_SOUT	LS1021A LPUART1
3	ARD_PD2	CPLD	4	ARD_PD3	CPLD
5	ARD_PD4	CPLD	6	ARD_PD5	CPLD
7	ARD_PD6	CPLD	8	ARD_PD7	CPLD
9	ARD_PD8	CPLD	10	ARD_PD9	CPLD

3.4 Rear panel expansion ports (external)

The LS1021A-IOT board provides 3 Ports (0-2) to connect externally. Port 0 (J500) provides SPI1, LPUART1 and 8 ADC channels. Port 1 (J501) contains eight GPIOs from the GPIO Expander and 6 GPIOs to the CPLD.

NOTE

The CPLD GPIO is not implemented in the CPLD and is reserved for future use.

Table 3-9. Port 0 (J500) Pinout

Pin	Net name	Source	Pin	Net name	Source
1	+3V3	Power	2	ADC_CH8	MAX1239 ADC (U6)
3	ADC_CH4	MAX1239 ADC (U6)	4	ADC_CH9	MAX1239 ADC (U6)
5	ADC_CH5	MAX1239 ADC (U6)	6	ADC_CH10	MAX1239 ADC (U6)
7	ADC_CH6	MAX1239 ADC (U6)	8	ADC_CH11	MAX1239 ADC (U6)
9	ADC_CH7	MAX1239 ADC (U6)	10	+3V3	Power
11	GND	Power	12	SPI1_PCS0	LS1021A SPI1
13	LPUART1_CTS_B	LS1021A LPUART1	14	SPI1_OUT	LS1021A SPI1
15	LPUART1_RTS_B	LS1021A LPUART1	16	SPI1_SIN	LS1021A SPI1
17	LPUART1_SIN	LS1021A LPUART1	18	SPI1_SCK	LS1021A SPI1
19	LPUART1_SOUT	LS1021A LPUART1	20	GND	Power

Table 3-10. Port 1 (J501) Pinout

Pin	Net name	Source	Pin	Net name	Source
1	+3V3	Power	2	CPLD_EXPAND0	CPLD
3	GPIO_EXPAND0	GPIO EXPANDER PCA9555BS (U2)	4	+5V0	Power

Table continues on the next page...

Table 3-10. Port 1 (J501) Pinout (continued)

Pin	Net name	Source	Pin	Net name	Source
5	GPIO_EXPAND1	GPIO EXPANDER PCA9555BS (U2)	6	CPLD_EXPAND1	CPLD
7	GND	Power	8	CPLD_EXPAND2	CPLD
9	GPIO_EXPAND2	GPIO EXPANDER PCA9555BS (U2)	10	CPLD_EXPAND3	CPLD
11	GPIO_EXPAND3	GPIO EXPANDER PCA9555BS (U2)	12	GND	Power
13	GPIO_EXPAND4	GPIO EXPANDER PCA9555BS (U2)	14	CPLD_EXPAND4	CPLD
15	GND	Power	16	CPLD_EXPAND5	CPLD
17	GPIO_EXPAND5	GPIO EXPANDER PCA9555BS (U2)	18	GPIO_EXPAND7	GPIO EXPANDER PCA9555BS (U2)
19	GPIO_EXPAND6	GPIO EXPANDER PCA9555BS (U2)	20	GND	Power

Table 3-11. Port 2 (J502) Pinout

Pin	Net name	Source	Pin	Net name	Source
1	+2V5	Power	2	+5V0	Power
3	GPIO3_25	LS1021A	4	GND	Power
5	GPIO3_24	LS1021A	6	GPIO3_19	LS1021A
7	GND	Power	8	GPIO3_20	LS1021A
9	GPIO3_18	LS1021A	10	GPIO3_21	LS1021A
11	GPIO3_17	Power	12	GND	Power
13	GPIO3_26	LS1021A	14	GPIO3_27	LS1021A
15	GND	Power	16	GPIO3_16	LS1021A
17	GPIO3_22	LS1021A	18	GPIO3_23	LS1021A
19	GPIO3_15	LS1021A	20	GND	Power

Chapter 4
CPLD System Controller Architecture

This chapter explains the CPLD system controller architecture. The figure below illustrates the detailed block diagram of the CPLD.

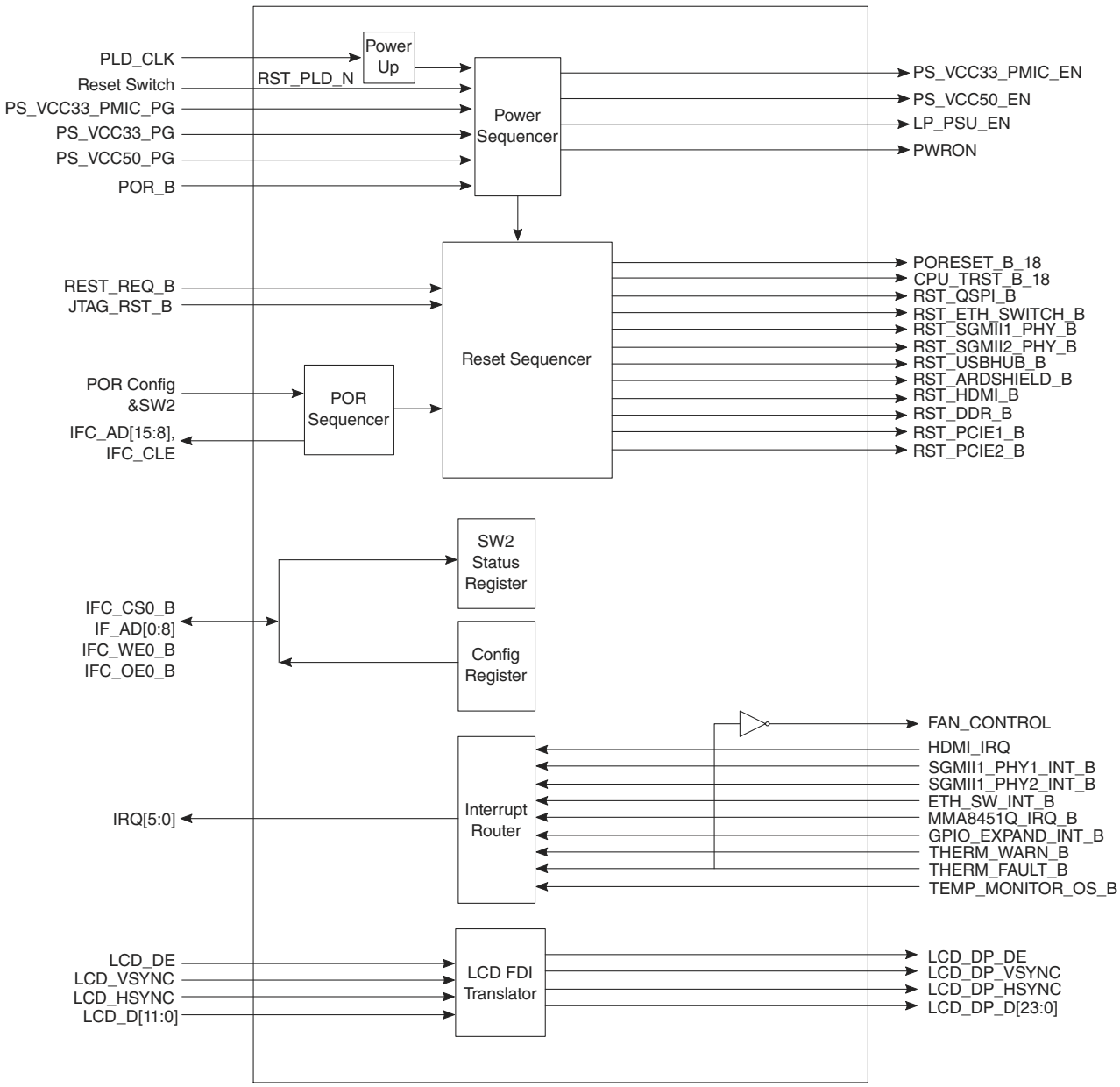

Figure 4-1. CPLD overview

4.1 Key features of CPLD

This CPLD includes the following features:

- Control power on sequence
  - Power on CPU VDD, GVDD, and others powers.

- Reset signal generation and distribution. System reset features are:
  - Power on reset for LS1021A, QSPI flash, PCIe, DDR, and PHY devices.
  - Manual reset: System will power, sequence, reset, and initialize all CPLD registers to default value after pressing reset button.
- Control POR sequence
  - Configure POR signals according to external DIP switches.
- Select Multiplexed pins
  - Mux QE and LCD
  - Mux SerDes configurations
- IFC Bus
  - Read/write CPLD status registers.
- LCD FDI translator
  - Translate 2-bit FDI signals to 1-bit FDI signals.

4.2 Reset

The reset controller manages not only asserting reset to LS1021A, but to the rest of the system as well. It also maintains the assertion timing of the configuration drive signal (PORESET_b), which causes the CPLD to drive configuration values onto the pin-sampled nets.

The following figure illustrates the reset sequences.

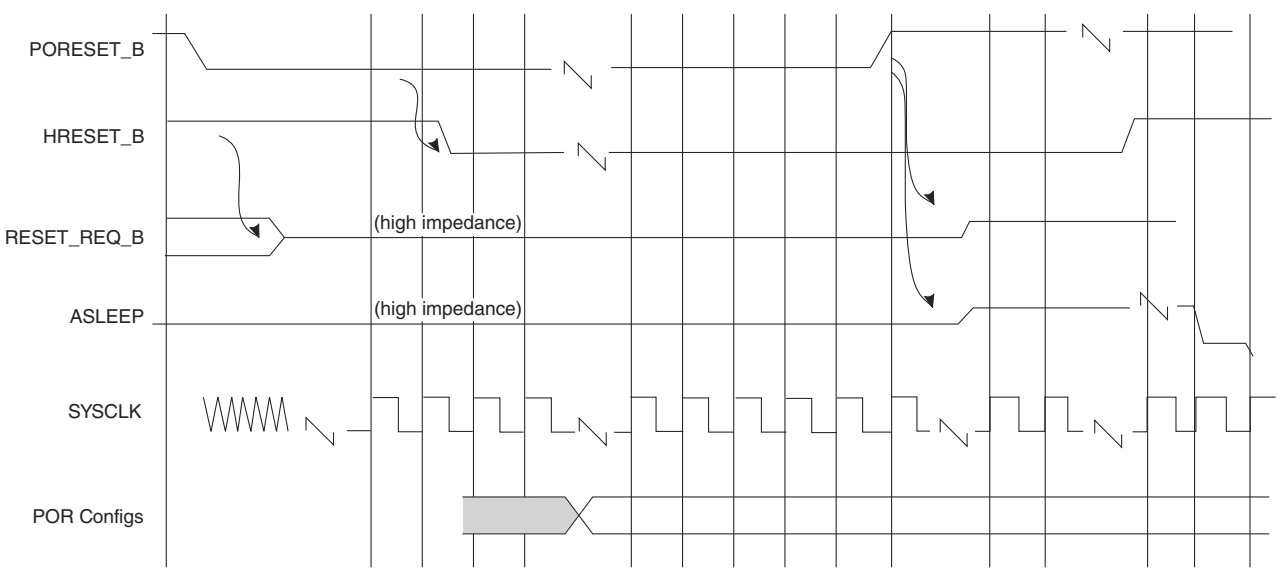

Figure 4-2. Reset power sequencing

4.3 CPLD register map

This section explains the memory mapping of the CPLD registers to LS1021A and also BCSR registers mapping.

4.3.1 Memory map

Two eight-bit CPLD registers are memory mapped to LS1021A using IFC_CS0_B. Address 0x7fb00000 can either be read or written to. When reading, the status of the DIP switches is presented. When writing, certain signals within the CPLD can be controlled. See Table 4-1 and Table 4-2 for more information.

4.3.2 BCSR registers map

The BCSR (Board and Control Register) contains many registers that are accessible from the device over IFC. The table below summarizes all the CPLD registers.

Table 4-1. CPLD read register details

Bit	Access	Description	Default value
0	R	SW2[1] Status	SW2[1] Status
1	R	SW2[2] Status	SW2[2] Status
2	R	SW2[3] Status	SW2[3] Status
3	R	SW2[4] Status	SW2[4] Status
4	R	SW2[5] Status	SW2[5] Status
5	R	SW2[6] Status	SW2[6] Status
6	R	SW2[7] Status	SW2[7] Status
7	R	SW2[8] Status	SW2[8] Status

The following table shows a detailed address map description.

Table 4-2. CPLD write register details

Bit	Access	Description	Options	Default value
0	W	LED0 Control	0 LED OFF 1 LED ON	0

Table continues on the next page...

Table 4-2. CPLD write register details (continued)

Bit	Access	Description	Options	Default value
1	W	Sata/SGMII Mux Control	0 SATA 1 SGMII	1
2	W	QE_/LCD MUX	0 QE 1 LCD	1
3	W	SERDES MUX SHUTDOWN	0 ENABLED 1 DISABLED	0
4	W	Reserved	-	1
5	W	Reserved	-	1
6	W	Reserved	-	1
7	W	Reserved	-	1

4.4 LCD FDI translator

The LCD interfaces to the tower system or HDMI transmitter (SiI9022A) through a 24-bit RGB interface, 8-bit R, 8-bit G, and 8-bit B. This is needed to translate LCD signals from FDI 2-bits to 1-bit.

The following figure shows the timing for LCD FDI translation.

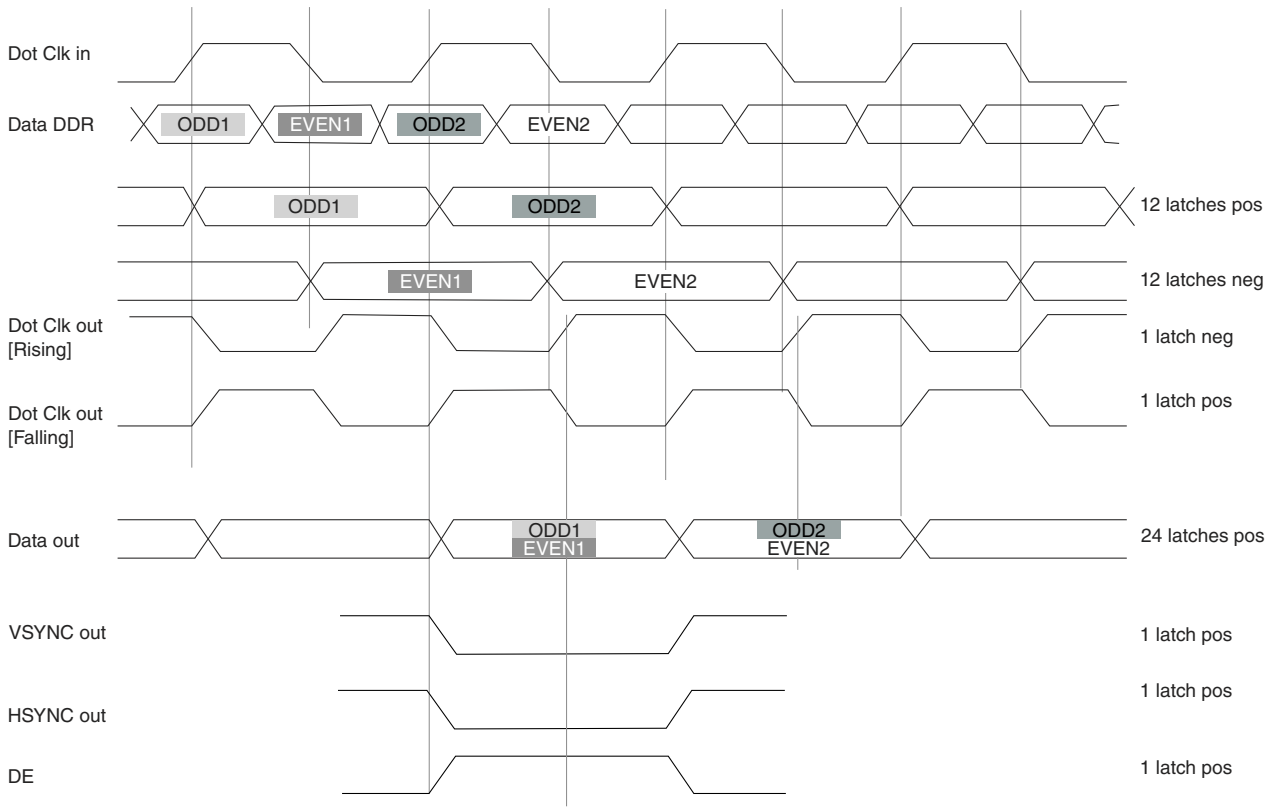

Figure 4-3. Timing of FDI translation

Chapter 5
Board Configuration and Debug Support

This chapter describes the necessary steps to configure the board for normal operation and also illustrates the connections to the board that are required for the bare boards.

5.1 Kit contents

This section illustrates the contents of LS1021A-IOT Gateway box, front and rear elevations, as well as the main features of the top and bottom side of the LS1021A-IOT Printed Circuit Board (PCB).

The LS1021A-IOT Gateway Reference design board is supplied with the following contents as shown in the figure below.

- 1x LS1021A-IOT Gateway
- 1x 12 V at 5 A PSU
- 1x Micro-B USB cable
- 1x HDMI cable
- 1x 8 GB SDHC card

Figure 5-1. LS1021A-IOT kit contents

5.2 Case and PCB description

The LS1021A-IOT is contained within an enclosure. The following figures of the front and rear panels are annotated to describe the I/O functions and indicators.

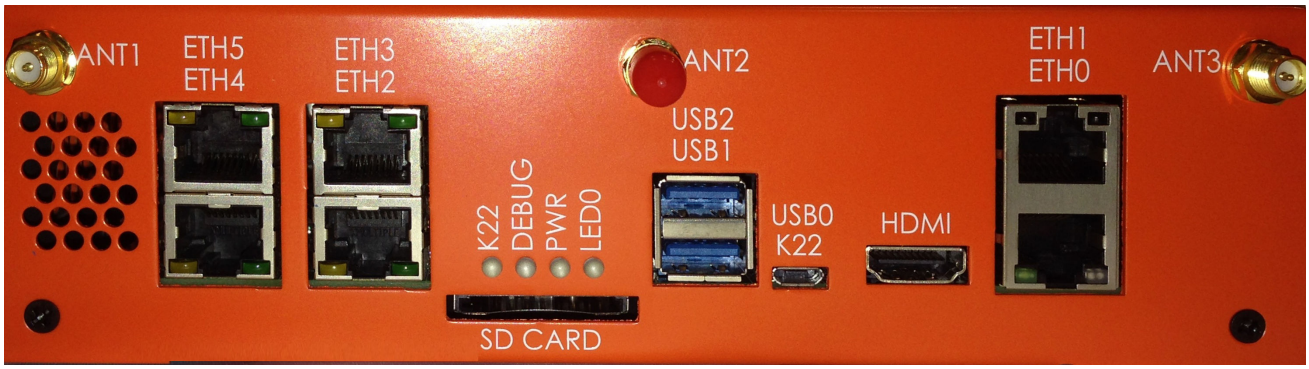

Figure 5-2. LS1021A-IOT Chassis - Front

Figure 5-3. LS1021A-IOT Chassis - Rear

The features of the board are shown in the following figures.

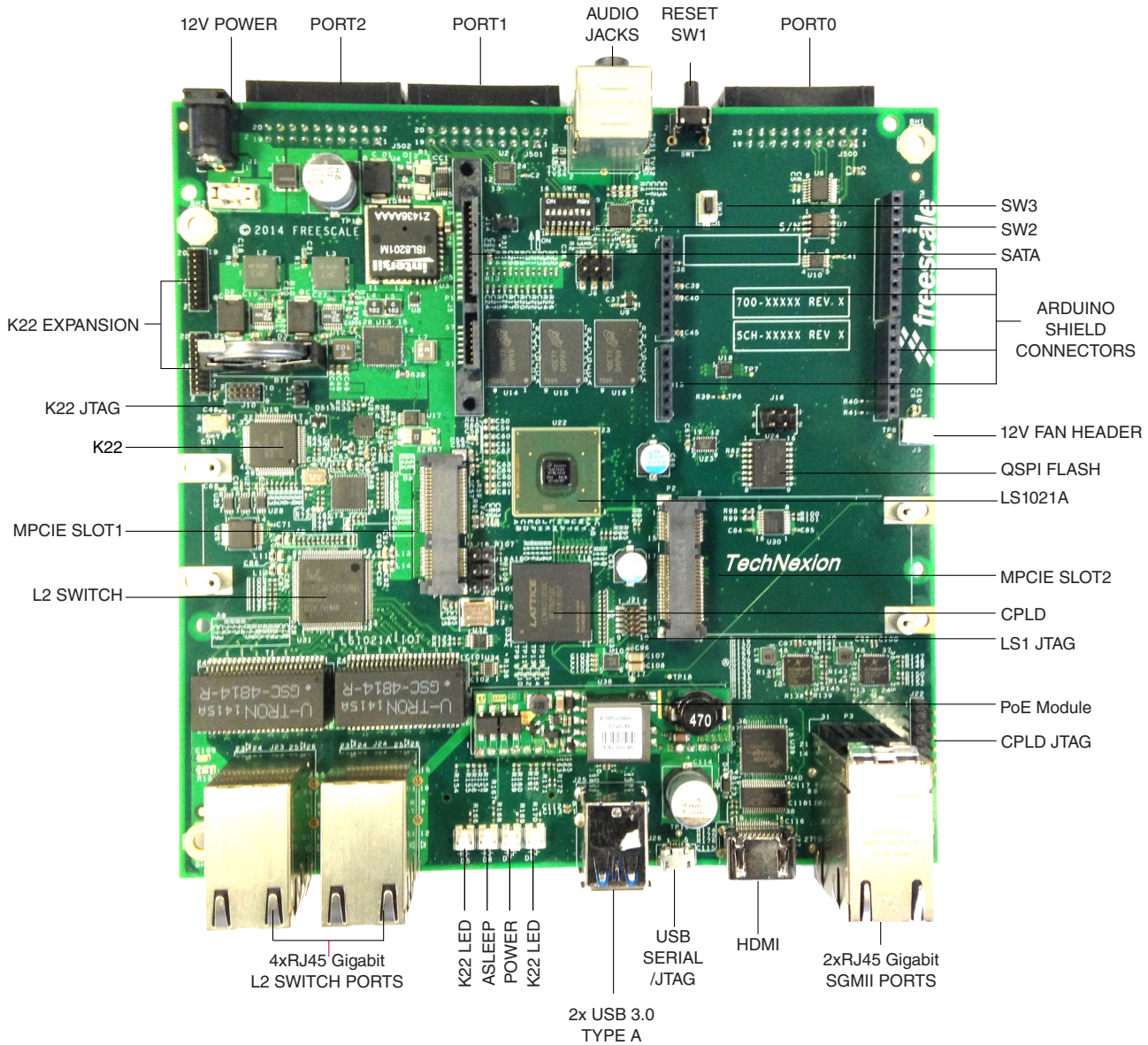

Figure 5-4. LS1021A-IOT PCB - top side

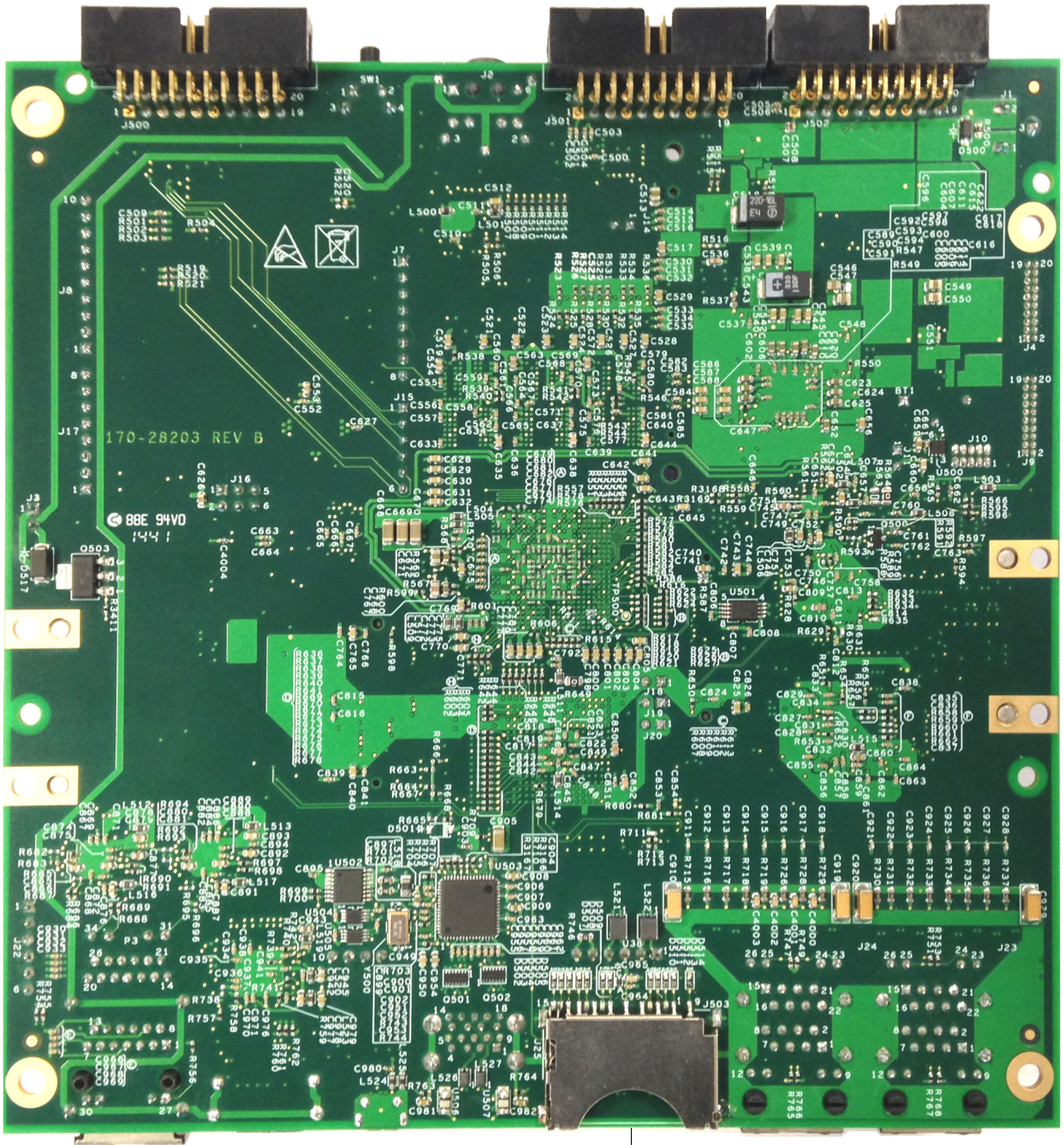

Figure 5-5. LS1021A-IOT PCB - bottom side

5.3 Configuring switches and jumpers

To configure the LS1021A-IOT board, use the default switch settings listed in the table below.

NOTE

The default switch settings are indicated by » symbol.

Table 5-1. Default switch settings

Feature	Settings (OFF=1, ON=0)	Option	Comments
S2.1	OFF	RCW & Boot Source	0 : QSPI (not supported on revA board) » 1 : SDHC (default)
S2.2	OFF	SYSCLK Select	0 : DIFF_SYSCLK »1 : SYSCLK (default)
S2.3	OFF	Reserved	0 : Reserved »1 : Reserved (default)
S2.4	OFF	Reserved	0 : Reserved »1 : Reserved (default)
S2.5	OFF	SGMII2_SATA MUX	0 : SerDes Lane 2 - SATA »1 : SerDes Lane 2 – SGMII2 (default)
S2.[6 :7]	ON:ON	SYSCLK Frequency Select	»00 : 100MHz (default) 01 : 99MHz 10 : 96MHz 11: Reserved
S2.8	OFF	SDA_SWD_EN Control	0 : K22 CMSIS-DAP »1 : JTAG HEADER (default)

The following table lists the jumper settings.

Table 5-2. Jumper settings

Jumpers	Default settings on LS1021A-IOT	Description
J11	OFF	VDD_LP Source Select OFF – Battery ON - +1V0_VDDC
J18	OFF	Reserved
J19	OFF	Reserved
J20	OFF	Reserved

The following figure shows the jumper locations.

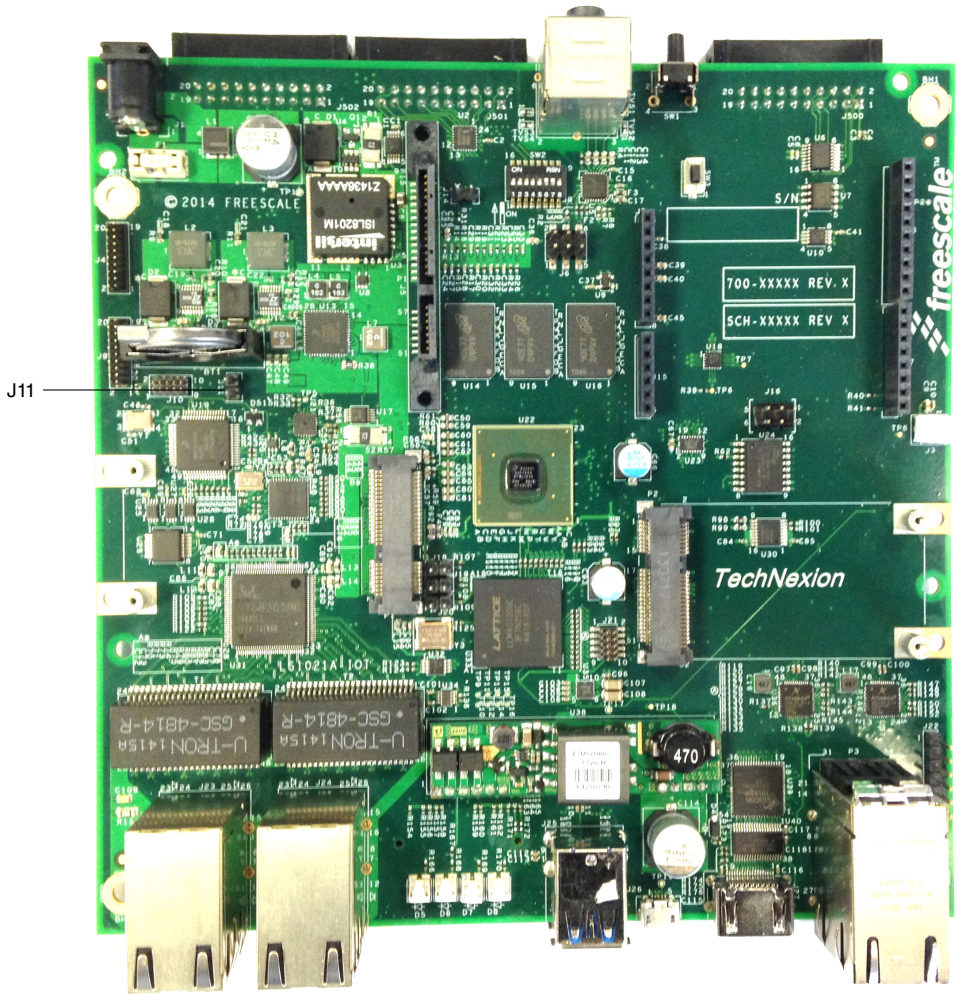

Figure 5-6. Jumper settings

5.4 Memory map

This section explain the default memory map for the system.

The following table illustrates the default memory map for the system.

Table 5-3. Memory map

Start Physical Address	End Physical Address	Memory Type	Size
0x0100_0000	0x0FFF_FFFF	CCSR Space	240MB
0x4000_0000	0x43FF_FFFF	QSPI (Chip select 0)	64GB
0x4400_0000	0x47FF_FFFF	QSPI (Chip select 1)	64GB
0x7FB0_0000	0x7FB0_0004	CPLD register	4B
0x8000_0000	0xBFFF_FFFF	DDR	1GB

NOTE

In SDK 1.7 and previous releases, only the first 16 MB of QSPI is available due to limitations in the driver. This will be fixed in a future release.

5.5 CMSIS-DAP debug support

JTAG connectivity to the LS1021A on the LS1021A-IOT board is available from two sources:

- CMSIS-DAP via USB0 – the onboard TAP (slower and limited features)
- JTAG Header – Internal 10pin ARM Debug Header – requires a Debugger such as the Freescale CodeWarrior TAP

Both methods require debug software, such as Freescale CodeWarrior to work with the board.

CMSIS-DAP via USB0

NOTE

When USB0 is connected to the host PC via a Micro-B connector, in addition to the UART bridge functionality, a JTAG bridge is provided. Both can run concurrently.

1. Open the case.
2. Ensure SW2.8 is in the ON position to select CMSIS-DAP operation.
3. Close the lid, if desired.
4. Connect the USB0 to the host PC USB port using Micro-B cable.
5. Switch on the power supply to the board.
6. Check for completion of the reset sequence.
7. Check the device manager on a Windows machine, to verify that the CMSIS-DAP device is installed correctly.

NOTE

For further information, see the Debugger User Manual.

JTAG Header

1. Ensure the board is not switched on.
2. Open the case.
3. Set SW2.8 in OFF position to select JTAG header operation.

4. Connect the JTAG connectivity unit to the LS1021A JTAG connector J21. Pin 1 is marked on the board.
5. Switch on the power supply to the board.
6. Check for completion of the reset sequence.

NOTE

For further information, see the Debugger User Manual.

Appendix A
Revision History

The table below provides revision history of this document.

Table A-1. Revision history

Revision	Date	Description
Rev 0	03/2015	Initial public release

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