

COMPLIANT

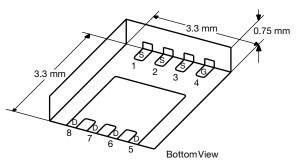
HALOGEN FREE

**Vishay Siliconix** 

## P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω) Max.	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)	
	0.0036 at V <sub>GS</sub> = - 10 V	- 40 <sup>e</sup>		
- 20	0.0048 at V <sub>GS</sub> = - 4.5 V	- 40 <sup>e</sup>	72 nC	
	0.0085 at $V_{GS}$ = - 2.5 V	- 40 <sup>e</sup>		

#### PowerPAK 1212-8S

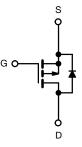


#### **FEATURES**

- TrenchFET<sup>®</sup> Power MOSFET
- Low Thermal Resistance PowerPAK® Package with Small Size and Low 0.75 mm Profile
- 100 % R<sub>g</sub> and UIS Tested
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

#### **APPLICATIONS**

- Smart Phones, Tablet PCs, Mobile Computing
  - Battery Switch
  - Load Switch



P-Channel MOSFET

Ordering Information: Si7655DN-T1-GE3 (Lead (Pb)-free and Halogen-free)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V <sub>DS</sub>	- 20	V
Gate-Source Voltage		V <sub>GS</sub>	± 12	V
	T <sub>C</sub> = 25 °C		- 40 <sup>e</sup>	
Continuous Droin Current (T 150 °C)	T <sub>C</sub> = 70 °C		- 40 <sup>e</sup>	
Continuous Drain Current ( $T_J = 150 \ ^{\circ}C$ )	T <sub>A</sub> = 25 °C	I <sub>D</sub>	- 31 <sup>a, b</sup>	
	T <sub>A</sub> = 70 °C		- 25 <sup>a, b</sup>	
Pulsed Drain Current (t = 300 μs)		I <sub>DM</sub>	- 100	— A
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C	la la	- 40 <sup>e</sup>	
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	- 4 <sup>a, b</sup>	
Avalanche Current	$T_{A} = 25 \text{ °C}$ $I_{AS}$ $L = 0.1 \text{ mH}$	- 20		
Single-Pulse Avalanche Energy	L = 0.11111	E <sub>AS</sub>	20	mJ
	T <sub>C</sub> = 25 °C		57	
Mauiaum Daura Diasiastian	T <sub>C</sub> = 70 °C	P_	36	w
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	4.8 <sup>a, b</sup>	VV
	T <sub>A</sub> = 70 °C		3 <sup>a, b</sup>	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 50 to 150	J°
Soldering Recommendations (Peak Temperature) <sup>c, d</sup>			260	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. t = 10 s.

c. See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

e. Package limited.

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## Vishay Siliconix



# THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a, b</sup>	t ≤ 10 s	R <sub>thJA</sub>	21	26	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	1.7	2.2	0/00

Notes:

a.Surface mounted on 1" x 1" FR4 board. b.Maximum under steady state conditions is 63 °C/W.

**SPECIFICATIONS** (T<sub>1</sub> = 25 °C, unless otherwise noted) Parameter Symbol **Test Conditions** Min. Тур. Max. Unit Static Drain-Source Breakdown Voltage  $V_{GS} = 0 V, I_D = -250 \mu A$ - 20 v V<sub>DS</sub> V<sub>DS</sub> Temperature Coefficient  $\Delta V_{DS}/T_J$ - 12 mV/ I<sub>D</sub> = - 250 μA V<sub>GS(th)</sub> Temperature Coefficient °C 2.6  $\Delta V_{GS(th)}/T_J$  $V_{DS} = V_{GS}, I_D = -250 \ \mu A$ ٧ Gate-Source Threshold Voltage - 0.5 - 1.1 V<sub>GS(th)</sub>  $V_{DS} = 0 V, V_{GS} = \pm 12 V$ ± 100 Gate-Source Leakage IGSS nA  $V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}$ - 1 Zero Gate Voltage Drain Current μA IDSS  $V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 \text{ }^{\circ}\text{C}$ - 10  $V_{DS} \leq$  - 5 V,  $V_{GS}$  = - 10 V On-State Drain Current<sup>a</sup> I<sub>D(on)</sub> - 20 А  $V_{GS}$  = - 10 V,  $I_{D}$  = - 20 A 0.0030 0.0036 Drain-Source On-State Resistance<sup>a</sup>  $V_{GS}$  = - 4.5 V,  $I_{D}$  = - 15 A 0.0039 0.0048 R<sub>DS(on)</sub> 0  $V_{GS} = -2.5 \text{ V}, I_D = -10 \text{ A}$ 0.0062 0.0085 Forward Transconductance<sup>a</sup>  $V_{DS} = -15 \text{ V}, I_{D} = -20 \text{ A}$ 90 S g<sub>fs</sub> Dynamic<sup>b</sup> 6600 Input Capacitance Ciss 890 pF **Output Capacitance**  $V_{DS} = -10 V$ ,  $V_{GS} = 0 V$ , f = 1 MHzCoss **Reverse Transfer Capacitance** 930 Crss  $V_{DS} = -10 \text{ V}, V_{GS} = -10 \text{ V}, I_{D} = -20 \text{ A}$ 150 225 **Total Gate Charge** Qg 110 72 nC  $V_{DS} = -10 \text{ V}, \text{ V}_{GS} = -4.5 \text{ V}, \text{ I}_{D} = -20 \text{ A}$ Gate-Source Charge Q<sub>gs</sub> 12 Gate-Drain Charge 19 Q<sub>ad</sub> Gate Resistance Rg f = 1 MHz0.5 2.6 5.2 Ω Turn-On Delay Time 45 90 t<sub>d(on)</sub> 90  $V_{DD}$  = - 10 V,  $R_L$  = 1  $\Omega$ 45 **Rise Time** tr Turn-Off DelayTime  $I_D \cong$  - 10 A,  $V_{GEN}$  = - 4.5 V,  $R_a$  = 1  $\Omega$ 200 100 t<sub>d(off)</sub> Fall Time 35 70 t<sub>f</sub> ns Turn-On Delay Time 13 25 t<sub>d(on)</sub> **Rise Time** 10 20 tr  $V_{DD}$  = - 10 V,  $R_L$  = 1  $\Omega$  $I_D \cong$  - 10 Å,  $V_{GEN}$  = - 10 V,  $R_q$  = 1  $\Omega$ Turn-Off DelayTime 220 t<sub>d(off)</sub> 110 Fall Time 25 50 t<sub>f</sub> **Drain-Source Body Diode Characteristics** Continuous Source-Drain Diode Current T<sub>C</sub> = 25 °C - 40<sup>c</sup>  $I_S$ А Pulse Diode Forward Current<sup>a</sup> - 100 I<sub>SM</sub> V - 0.75 Body Diode Voltage V<sub>SD</sub>  $I_{F} = -10 \text{ A}$ - 1.2 Body Diode Reverse Recovery Time 30 60 ns t<sub>rr</sub> Body Diode Reverse Recovery Charge 26 Q<sub>rr</sub> 17 nC  $I_F = -10 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, \text{ T}_J = 25 \text{ }^\circ\text{C}$ Reverse Recovery Fall Time 15 ta ns **Reverse Recovery Rise Time** 15 tb

Notes:

a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %. b. Guaranteed by design, not subject to production testing.

c. Package limited.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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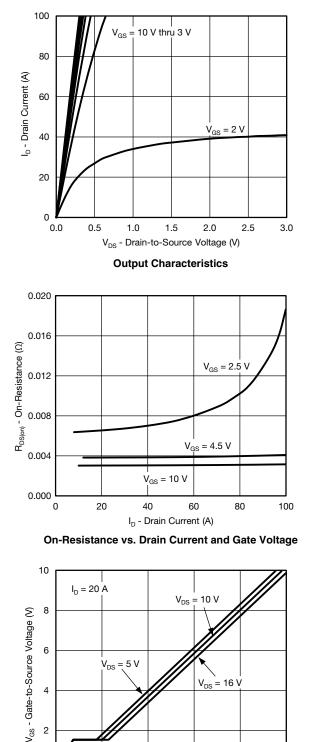
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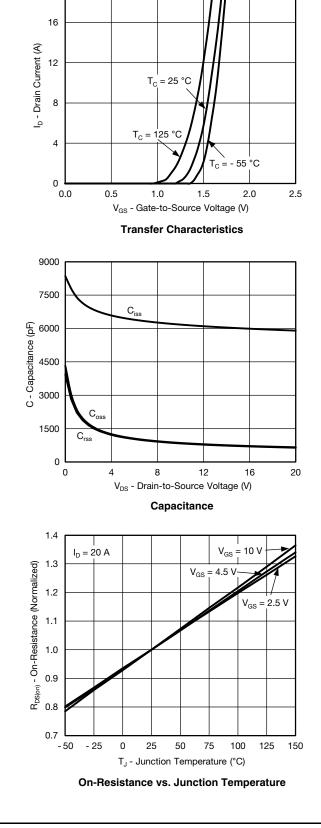


## Si7655DN

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4

2

0

0

 $V_{DS} = 5 V$ 

30

V<sub>DS</sub> = 16 V

120

150

90

Q<sub>a</sub> - Total Gate Charge (nC)

**Gate Charge** 

60

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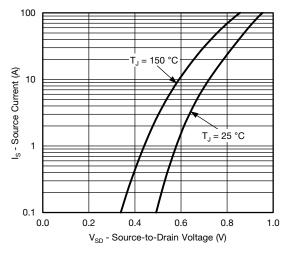
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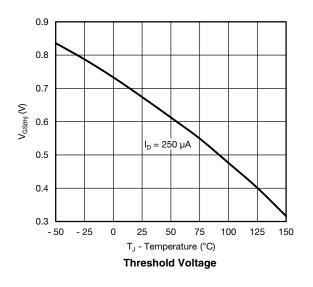
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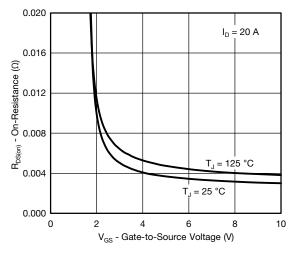


### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

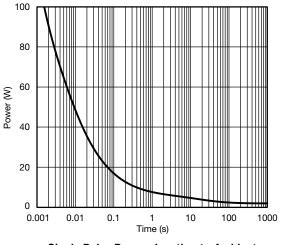


Source-Drain Diode Forward Voltage

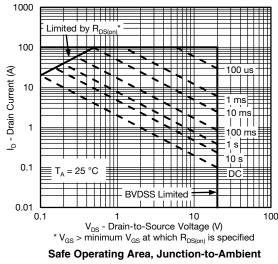




**On-Resistance vs. Gate-to-Source Voltage** 



Single Pulse Power, Junction-to-Ambient



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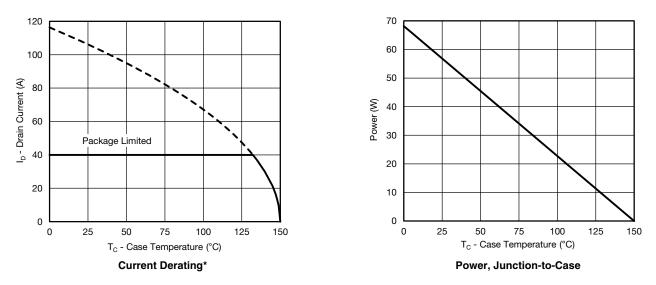
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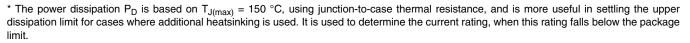
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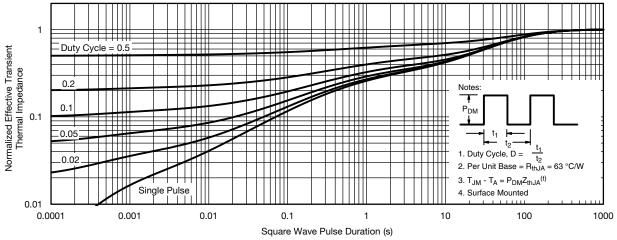


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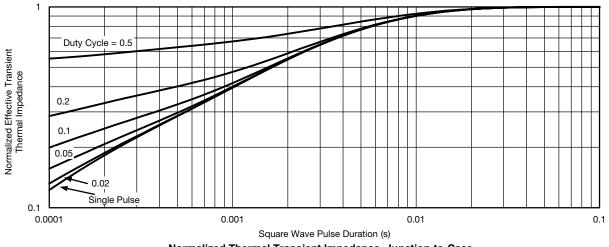


Normalized Thermal Transient Impedance, Junction-to-Ambient

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#### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





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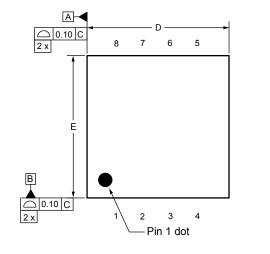
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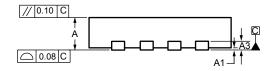


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# Case Outline for PowerPAK<sup>®</sup> 1212-8S







DIM.		MILLIMETERS		INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
А	0.67	0.75	0.83	0.026	0.030	0.033
A1	0.00	-	0.05	0.000	-	0.002
A3		0.20 ref.		0.008 ref		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.15	2.25	2.35	0.085	0.089	0.093
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	1.60	1.70	1.80	0.063	0.067	0.071
е		0.65 bsc.		0.026 bsc.		
К		0.76 ref.		0.030 ref.		
K1		0.41 ref.		0.016 ref.		
L	0.33	0.43	0.53	0.013	0.017	0.021
Z		0.525 ref.		0.021 ref.		
N: C20-0862-Re G: 6008	v. B, 20-Jul-2020					

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### RECOMMENDED MINIMUM PADS FOR PowerPAK<sup>®</sup> 1212-8 Single



Recommended Minimum Pads Dimensions in Inches/(mm)

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