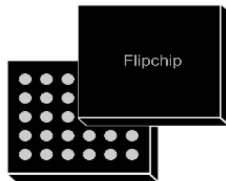


## Li-Ion linear battery charger with LDO and load switches



### Maturity status link

[STBC03](#)

### Device summary

Order code	STBC03JR
LDO	3.0 V
Package	400 $\mu$ m pitch

### Features

- Charges single-cell Li-Ion batteries with CC/CV algorithm and charge termination
- Fast charge current up to 650 mA adjustable by external resistor
- Pre-charge current from 1 mA
- Adjustable floating voltage up to 4.45 V
- Integrated low quiescent LDO regulator
- Automatic power path management
- Auto-recharge function
- Embedded protection circuit module (PCM) featuring battery overcharge, battery over-discharge and battery overcurrent protections
- Charging timeout
- Shipping mode feature allows battery low leakage when over-discharged
- Very low battery leakage in over-discharge and shutdown mode
- Charger enable input
- Charge/fault status output
- Battery voltage pin to allow external gauging
- Two 3  $\Omega$  SPDT load switches
- Available in Flip Chip 30, 400  $\mu$ m pitch package
- Rugged  $\pm 4$  kV HBM, ESD protection on the most critical pins

### Applications

- Smart watches and wearable devices
- Fitness and medical accessories
- Li-Ion and other Li-Poly battery rechargeable equipment

### Description

The **STBC03** is a highly integrated power management, embedding a linear battery charger, a 150 mA LDO, 2 SPDT load switches, and a protection circuit module (PCM) to prevent the battery from being damaged under fault conditions.

The **STBC03** uses a CC/CV algorithm to charge the battery; the fast charge and the pre-charge current can be both independently programmed using dedicated resistors. The termination current is set to 5% of the programmed fast charge current, but has fixed values for fast charge currents lower than 20 mA. The battery floating voltage value is programmable and can be set to a value up to 4.45 V.

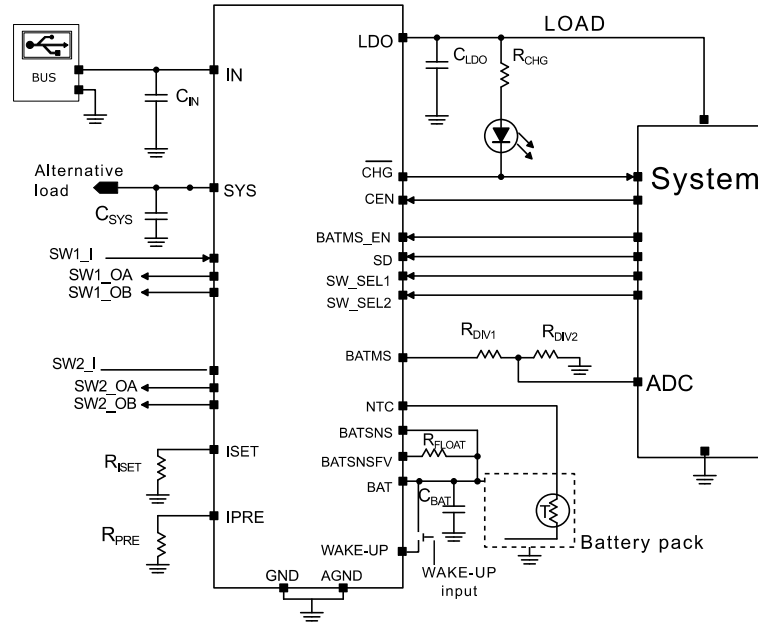
The **STBC03** also features a charger enable input to stop the charging process anytime.

The **STBC03** is automatically powered off from the connected battery when the IN pin is not connected to a valid power source (battery mode).

A battery under/overtemperature condition can be detected by using an external circuitry (NTC thermistor).

The **STBC03** draws less than 10 nA from the connected battery in shipping mode conditions, so to maximize the battery life during shelf life of the final application. The device is available in the Flip Chip 30 package.

# 1 Application schematic

**Figure 1. STBC03 application schematic**

**Table 1. Typical bill of material (BOM)**

Symbol	Value	Description	Note
C <sub>IN</sub>	10 μF (16 V)	Input supply voltage capacitor	Ceramic type
C <sub>SYS</sub>	1 μF (10 V)	System output capacitor	Ceramic type
R <sub>ISET</sub>	Refer to I <sub>SET</sub>	Charge current programming resistor	Film type
R <sub>IPRE</sub>	Refer to I <sub>PRE</sub>	Pre-charge current programming resistor	Film type
C <sub>BAT</sub>	4.7 μF (6.3 V)	Battery positive terminal capacitor	Ceramic type
R <sub>FLOAT</sub>	BATSNSFV	Floating voltage programming resistor	Film type
R <sub>DIV1, DIV2</sub>	100-200 kΩ	Battery monitor resistor divider	Film type
R <sub>CHG</sub>	10 kΩ	Charging/fault pull-up resistor <sup>(1)</sup>	Film type
C <sub>LDO</sub>	1.0 μF (10 V)	LDO output capacitor	Ceramic type

1. R<sub>CHG</sub> must be calculated according to the external LED electrical characteristics.

## 2 Pin configuration

**Figure 2. Pin configuration top through view**

	1	2	3	4	5
A	A1 SD	A2 BATSNSFV	A3 GND	A4 ISET	A5 BAT
B	B1 CEN	B2 SW_SEL1	B3 BATSNS	B4 AGND	B5 BAT
C	C1 SW_SEL2	C2 BATMS_EN	C3 NC	C4 BATMS	C5 SYS
D	D1 NTC	D2 WAKE_UP	D3 NC	D4 IPRE	D5 SYS
E	E1 CHG	E2 SW_I	E3 SW1_OB	E4 SW1_OA	E5 IN
F	F1 SW2_OB	F2 SW2_OA	F3 SW1_I	F4 LDO	F5 IN

**Table 2. Pin description**

Bump		Bump name	Description
Power	IN	E5-F5	Input supply voltage. Bypass this pin to ground with a 10 $\mu$ F capacitor
	BAT	A5-B5	Battery positive terminal. Bypass this pin to GND with a 4.7 $\mu$ F ceramic capacitor
	SYS	C5-D5	System output. Bypass this pin to ground with 1 $\mu$ F ceramic capacitor
	LDO	F4	LDO output. Bypass this pin to ground with 1 $\mu$ F ceramic capacitor
	NTC	D1	Battery temperature monitor pin
	AGND	B4	Analog ground
	GND	A3	GROUND
			Connect together with the same ground layer
Programming	ISET	A4	Fast charge current programming resistor
	IPRE	D4	Pre-charge current programming resistor
Sensing	BATMS	C4	Battery voltage measurement pin
	BATSNS	B3	Battery voltage sensing. Connect as close as possible to the battery positive terminal
	BATSNSFV	A2	Floating voltage sensing. Connect as close as possible to the battery positive terminal
Digital I/Os	CEN	B1	Charger enable pin. Active high. 500 k $\Omega$ internal pull-up (to LDO)
	CHG	E1	Charging/fault flag. Active low (open drain output)
	WAKE-UP	D2	Shipping mode exit input pin. Active high. 50 k $\Omega$ internal pull-down
	SW_SEL2	C1	Load switch 2 selection input (refer to LDO level)
	BATMS_EN	C2	Battery monitor enable input (refer to LDO level)
	SW_SEL1	B2	Load switch 1 selection input (refer to LDO level)
	SD	A1	Shutdown input signal (refer to LDO level). When low, the STBC03 exits ship mode. It cannot be left floating
Switch matrix	SW1_I	F3	Load switch SPDT1 input (1.8 V to 5 V range)
	SW1_OA	E4	Load switch SPDT1 output A
	SW1_OB	E3	Load switch SPDT1 output B
	SW2_I	E2	Load switch SPDT2 input (1.8 V to 5 V range)
			If SPDT switches are used, decoupling capacitors are recommended on input and output. Capacitor values depend on application conditions and requirements. If not used, connect inputs and outputs to GND

Bump		Bump name	Description	
Switch matrix	SW2_OA	F2	Load switch SPDT2 output A	If SPDT switches are used, decoupling capacitors are recommended on input and output. Capacitor values depend on application conditions and requirements. If not used, connect inputs and outputs to GND
	SW2_OB	F1	Load switch SPDT2 output B	
	NC	C3-D3	Not connected	Leave floating

### 3 Maximum ratings

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Test conditions	Value	Unit
$V_{IN}$	Input supply voltage pin	DC voltage	-0.3 to +10.0	V
		Non repetitive, 60 s pulse length	-0.3 to +16.0	V
$V_{LDO}$	LDO output pin voltage	DC voltage	-0.3 to +4.0	V
$V_{SYS}$	SYS pin voltage	DC voltage	-0.3 to +6.5	V
$V_{SW}$	Switch pin voltage (SW1_I, SW2_I, SW1_OA, SW1_OB, SW2_OA, SW2_OB)	DC voltage	-0.3 to +6.5	V
$V_{CHG}$	CHG pin voltage	DC voltage	-0.3 to +6.5	V
$V_{Wake-up}$	WAKE-UP pin voltage	DC voltage	-0.3 to +4.6	V
$V_{LGC}$	Voltage on logic pins (CEN, SW_SEL1, SW_SEL2, SD, BATMS_EN)	DC voltage	-0.3 to +4.0	V
$V_{ISET}, V_{IPRE}$	Voltage on ISET, IPRE pins	DC voltage	-0.3 to +2	V
$V_{NTC}$	Voltage on NTC pin	DC voltage	-0.3 to $V_{LDO}$	V
$V_{BAT}, V_{BATSNS}, V_{BATSNSFV}$	Voltage on BAT, BATSNS and BATSNSFV pins	DC voltage	-0.3 to +5.5	V
$V_{BATMS}$	Voltage on BATMS pin	DC voltage	-0.3 to $V_{BAT}+0.3$	V
ESD	Human body model (IN, SYS, WAKE-UP, LDO, BAT, BATSNS, BATSNSFV)	JS-001-2012 vs. AGND PGND and GND	±4000	V
	Human body model (all the others)	JS-001-2012	±2000	V
$T_{AMB}$	Operating ambient temperature		-40 to +85	°C
$T_J$	Maximum junction temperature		+125	°C
$T_{STG}$	Storage temperature		-65 to +150	°C

**Note:** Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

**Table 4. Thermal data**

Symbol	Parameter	Flip Chip 30 (2.25x2.59 mm)	Unit
$R_{THJB}^{(1)}$	Junction-to-pcb board thermal resistance	50	°C/W

1. Standard FR4 pcb board.

## 4 Electrical characteristics

$V_{IN}=5\text{ V}$ ,  $V_{BAT} = 3.6\text{ V}$ ,  $C_{LDO} = 1\ \mu\text{F}$ ,  $C_{BAT} = 4.7\ \mu\text{F}$ ,  $C_{IN} = 10\ \mu\text{F}$ ,  $C_{SYS} = 1\ \mu\text{F}$ ,  $R_{ISET} = 1\ \text{k}\Omega$ ,  $SD = \text{GND}$ ,  $CEN = \text{high}$ ,  $R_{IPRE} = 4.7\ \text{k}\Omega$ ,  $T_A = 25\ ^\circ\text{C}$ ,  $SW\_SEL1 = SW\_SEL2 = \text{GND}$ ,  $BATMS\_EN = \text{GND}$ , WAKE-UP floating unless otherwise specified.

**Table 5. Electrical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IN}$	Operating input voltage	$V_{FLOAT}$ set 4.2 V, $I_{FAST} < 250\ \text{mA}$	4.55		5.4	V
		$V_{FLOAT}$ set 4.45 V, $I_{FAST} < 450\ \text{mA}$ , $I_{SYS} = I_{LDO} = 0\ \text{mA}$	4.75		5.4 <sup>(1)</sup>	V
$V_{INOVP}$	Input overvoltage protection	$V_{IN}$ rising	5.6	5.9	6.4	V
$V_{INOVP}$	Input overvoltage protection hysteresis	$V_{IN}$ falling		200		mV
$V_{UVLO}$	Undervoltage lock-out	$V_{IN}$ falling		3.9		V
$V_{UVLOH}$	Undervoltage lock-out hysteresis	$V_{IN}$ rising		300		mV
$I_{IN}$	IN supply current	Charger disabled mode ( $CEN = \text{low}$ ), $I_{SYS} = I_{LDO} = 0\ \text{A}$		600		$\mu\text{A}$
		Charging, $V_{HOT} < V_{NTC} < V_{COLD}$ , including $R_{ISET}$ current		1.4		mA
$V_{FLOAT}$	Battery floating voltage	$I_{BAT} = 1\ \text{mA}$ , $BATSNS$ and $BATSNSFV$ short to battery terminal	4.179	4.2	4.221	V
$I_{BAT}$	BAT pin supply current	Battery-powered mode ( $V_{IN} < V_{UVLO}$ ), $I_{LDO} = 0\ \text{A}$		4	8	$\mu\text{A}$
		Charge terminated		9	12	$\mu\text{A}$
		Shutdown mode (by $SD$ pin)		10	50	nA
		Over-discharge mode ( $V_{BAT} < V_{ODC}$ , $V_{IN} < V_{UVLO}$ )		10	50	nA
$I_{FAST}$	Fast charge current	$R_{ISET} = 300\ \Omega$		650 <sup>(1)</sup>		mA
		$R_{ISET} = 430\ \Omega$ , constant-current mode $I_{LDO} + I_{SYS} < 150\ \text{mA}$		450 <sup>(1)</sup>	500	
		$R_{ISET} = 1\ \text{k}\Omega$ , constant-current mode		200		
$I_{PRE}$	Pre-charge current	$R_{IPRE} = 10\ \text{k}\Omega$ , constant-current mode		20		mA
$V_{ISET}$	$I_{SET}$ regulated voltage			1		V
$V_{IPRE}$	$I_{PRE}$ regulated voltage			1		V
$V_{PRE}$	Pre-charge to fast charge battery voltage threshold	Charger active		3		V
$I_{END}$	End-of-charge current	Charging in CV mode for $20\ \text{mA} < I_{FAST}$		5		$\%I_{FAST}$
		Charging in CV mode for $I_{FAST} < 20\ \text{mA}$	See Table 10. $I_{FAST}$ and $I_{END}$			
$V_{OCHG}$	Battery voltage overcharge threshold	$V_{BAT}$ rising, $BATSNSFV$ short to battery terminal	4.245	4.275	4.305	V
		$V_{BAT}$ rising, external resistor between $BATSNSFV$ and battery terminal		$V_{FLOAT} + 75$		mV
$V_{ODC}$	Battery voltage over-discharge threshold	$V_{IN} < V_{UVLO}$ , $I_{LDO} = 150\ \text{mA}$ , $BATSNSFV$ and $BATSNS$ short to battery terminal	2.750	2.8	2.850	V
$V_{ODCR}$	Battery voltage over-discharge release threshold	$V_{UVLO} < V_{IN} < V_{OVP}$ , $I_{LDO} = 150\ \text{mA}$ , $BATSNSFV$ and $BATSNS$ short to battery terminal	3.0			V
$V_{WAKE-UP}$	Wake-up voltage threshold	$V_{BAT} > 3\ \text{V}$ rising, $I_{LDO} = 150\ \text{mA}$	2.2			V

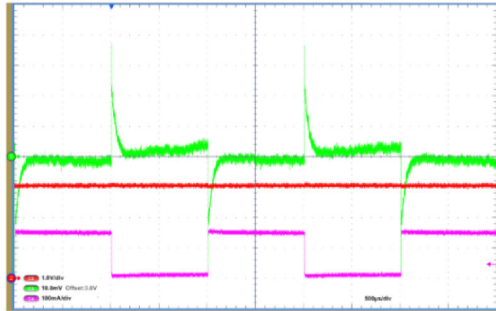
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R <sub>ON-IS</sub>	Input to SYS on-resistance			0.25	0.35	Ω
R <sub>ON-BS</sub>	Battery to SYS on-resistance			0.35	0.4	Ω
R <sub>ON-BATMS</sub>	BATSNS to BATMS on-resistance	I <sub>SINK</sub> = 500 μA	290		550	Ω
R <sub>ON-LOADSW1</sub>	Input to output load switch 1 resistance	V <sub>SW1_I</sub> = 1.8 V to 5 V SW1_OA or SW1_OB test current = 50 mA	2.0		3.8	Ω
R <sub>ON-LOADSW2</sub>	Input to output load switch 2 resistance	V <sub>SW2_I</sub> = 1.8 V to 5 V SW2_OA or SW2_OB test current = 50 mA	2.0		3.4	Ω
V <sub>OL</sub>	Output low level (CHG)	I <sub>SINK</sub> = 5 mA			0.4	V
I <sub>OHZ</sub>	High level open drain output current (CHG)	V <sub>OH</sub> = 5 V			1	μA
V <sub>IL</sub>	Logic low input level (CEN, SW_SEL1, SW_SEL2, BATMS_EN, SD)				0.4	V
V <sub>IH</sub>	Logic high input level (CEN, SW_SEL1, SW_SEL2, BATMS_EN, SD)		1.6			V
R <sub>UP</sub>	CEN pull-up resistor		375	500	625	kΩ
V <sub>LDO</sub>	LDO output voltage	I <sub>LDO</sub> = 1 mA	2.9	3.0	3.1	V
ΔV <sub>OUT-LOAD</sub>	LDO static load regulation	I <sub>LDO</sub> = 1 mA to 150 mA		±0.002	±0.003	%/mA
I <sub>SC</sub>	LDO short-circuit current	R <sub>LOAD</sub> = 0 Ω	250	350		mA
t <sub>ON</sub>	LDO turn-on time	0 to 95% V <sub>LDO</sub> , I <sub>OUT</sub> = 150 mA		210		μs
I <sub>BATOCP</sub>	Battery discharge overcurrent protection	V <sub>IN</sub> < V <sub>UVLO</sub> (powered from BAT)		900		mA
I <sub>INLIM</sub>	Input current limitation	V <sub>SYS</sub> > V <sub>ILIMSCTH</sub> ; V <sub>UVLO</sub> < V <sub>IN</sub> < V <sub>INOVP</sub> (powered from IN)		1.7		A
V <sub>ILIMSCTH</sub>	SYS voltage threshold for input current limitation short-circuit detection	V <sub>UVLO</sub> < V <sub>IN</sub> < V <sub>INOVP</sub>		2		V
V <sub>SCSYS</sub>	SYS short-circuit protection threshold	V <sub>IN</sub> < V <sub>UVLO</sub> or V <sub>IN</sub> > V <sub>INOVP</sub> (powered from BAT)		V <sub>BAT</sub> -0.8		V
I <sub>NTCB</sub>	NTC pin bias current	V <sub>NTC</sub> = 0.25 V	45	50	55	μA
V <sub>HOT</sub>	Thermal hot threshold	Increasing NTC temperature	0.234	0.246	0.258	V
V <sub>COLD</sub>	Thermal cold threshold	Decreasing NTC temperature	1.28	1.355	1.43	V
T <sub>HYST</sub>	Hot/cold temperature thresholds hysteresis	10 kΩ NTC, β = 3370		3		°C
T <sub>SD</sub>	Thermal shutdown die temperature			155		°C
T <sub>WRN</sub>	Thermal warning die temperature			135		°C
t <sub>PW-VIN</sub>	Minimum input voltage connection time to exit from shutdown mode	V <sub>BAT</sub> = 3.5 V, R <sub>NTC</sub> = 10 kΩ		350		ms
t <sub> OCD</sub>	Overcharge detection delay	V <sub>BAT</sub> > V <sub>OCHG</sub> , V <sub>UVLO</sub> < V <sub>IN</sub> < V <sub>INOVP</sub>		1.2		s
t <sub>ODD</sub>	Over-discharge detection delay	V <sub>BAT</sub> < V <sub>ODC</sub> and V <sub>IN</sub> < V <sub>UVLO</sub> or V <sub>IN</sub> > V <sub>INOVP</sub>		60		ms
t <sub>DOD</sub>	Discharge overcurrent detection delay	I <sub>BAT</sub> > I <sub>BATOCP</sub> , V <sub>IN</sub> < V <sub>UVLO</sub> or V <sub>IN</sub> > V <sub>INOVP</sub>		10		ms
t <sub> PFD</sub>	Pre-charge to fast charge transition deglitch time	Rising		100		ms

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{FPD}$	Fast charge to pre-charge fault deglitch time			10		ms
$t_{END}$	End-of-charge deglitch time			100		ms
$t_{PRE}$	Pre-charge timeout	$V_{BAT} = 2\text{ V}$ , charging		1800		s
$t_{FAST}$	Fast charge timeout		14000	18000	22000	s
$t_{CRDD}$	Charger restart deglitch time	After end-of-charge, $V_{BAT} < 3.9\text{ V}$ restart enabled		1200		ms
$V_{REC}$	Charger restart threshold	After end-of-charge, restart enabled		3.9		V
$t_{NTCD}$	Battery temperature transition deglitch time			100		ms
$t_{PW}$	CEN valid input pulse width		15			ms
$t_{PW-WA}$	WAKE-UP valid input pulse width		1200			ms

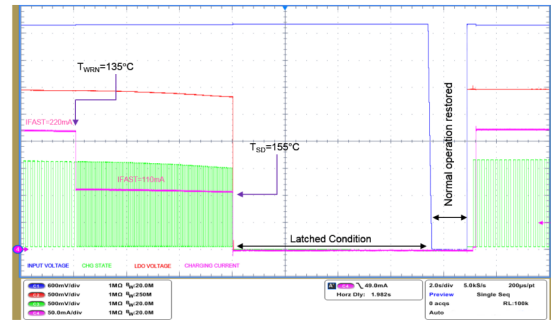
1. If the internal thermal temperature of the STBC03 reaches  $T_{WRN}$ , then the programmed  $I_{FAST}$  is halved until the internal temperature drops below  $T_{WRN} - 10\text{ °C}$  typically. A warning is signaled via the CHG output.



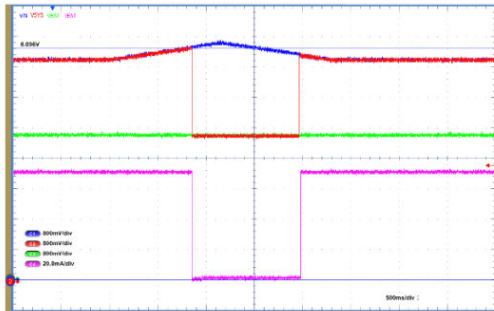
## 5 Typical performance characteristics

**Figure 3. Battery mode 3 V LDO load transient response**

 $V_{BAT} = 3.7\text{ V}$ , 10 mA to 150 mA, slope 150 mA/1  $\mu\text{s}$ 

CH2 (red) = LDO 1 V/div  
 CH3 (green) = LDO 10 mV/div  
 CH4 (pink) = LDO load variation

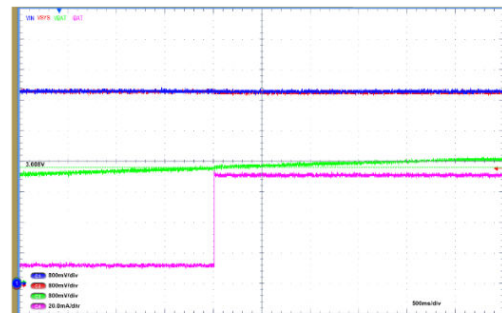
**Figure 4. Thermal management**

 $V_{BAT} = 3.7\text{ V}$ ,  $V_{IN} = 5.0\text{ V}$ 

CH1 (blue) =  $V_{IN}$   
 CH2 (red) = LDO  
 CH3 (green) = CHG  
 CH4 (pink) =  $I_{BAT}$

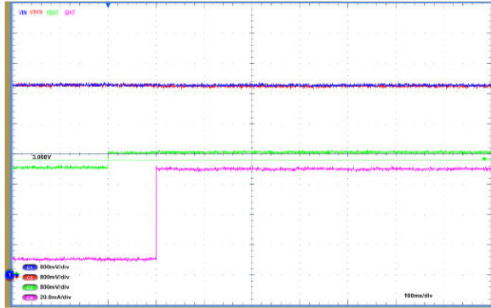
**Figure 5.  $V_{IN}$  mode, overvoltage protection**


Charging is resumed when OVP disappears

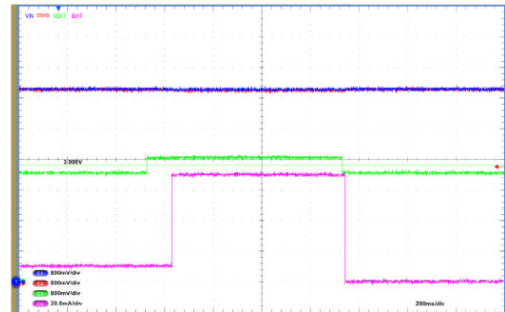
CH1 (blue) =  $V_{IN}$  800 mV/div  
 CH2 (red) =  $V_{SYS}$  800 mV/div  
 CH3 (green) =  $V_{BAT}$  800 mV/div  
 CH4 (pink) =  $I_{BAT}$  20 mA/div

**Figure 6. Pre-charge to fast charge mode transition threshold**


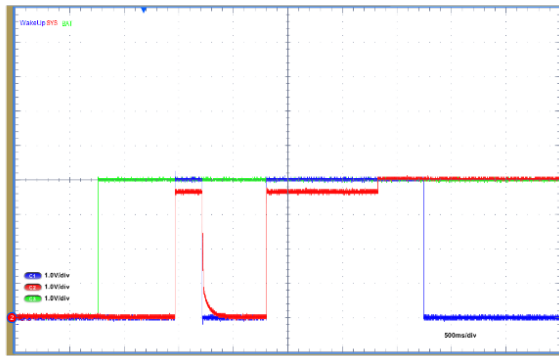
CH1 (blue) =  $V_{IN}$  800 mV/div  
 CH2 (red) =  $V_{SYS}$  800 mV/div  
 CH3 (green) =  $V_{BAT}$  800 mV/div  
 CH4 (pink) =  $I_{BAT}$  20 mA/div

**Figure 7. Pre-charge to fast charge mode transition deglitch**


CH1 (blue) =  $V_{IN}$  800 mV/div  
 CH2 (red) =  $V_{SYS}$  800 mV/div  
 CH3 (green) =  $V_{BAT}$  800 mV/div  
 CH4 (pink) =  $I_{BAT}$  20 mA/div

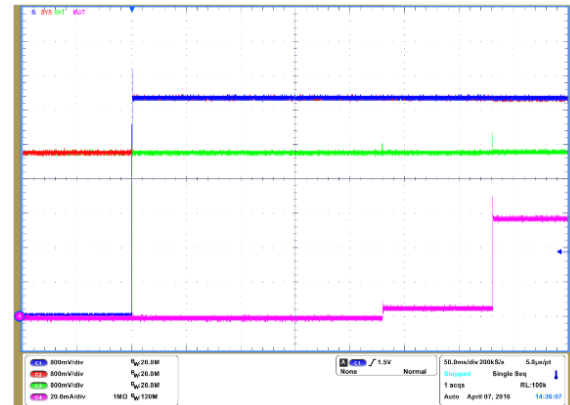
**Figure 8. Pre-charge to fast charge mode to no charge mode transition**


CH1 (blue) =  $V_{IN}$  800 mV/div  
 CH2 (red) =  $V_{SYS}$  800 mV/div  
 CH3 (green) =  $V_{BAT}$  800 mV/div  
 CH4 (pink) =  $I_{BAT}$  20 mA/div

**Figure 9. Wake-up pin operation**


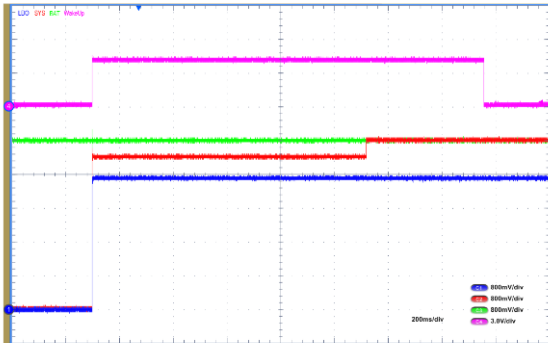
Shutdown mode to battery mode transition.  $V_{IN}$  floating

CH1 (blue) = WAKE-UP pin 800 mV/div  
 CH2 (red) =  $V_{SYS}$  800 mV/div  
 CH3 (green) =  $V_{BAT}$  800 mV/div

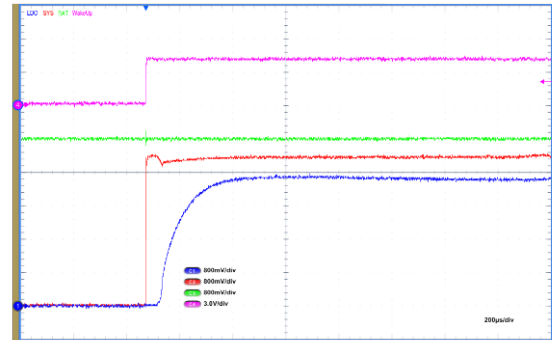
**Figure 10.  $V_{IN}$  plug, charging initialization**


Shutdown mode to  $V_{IN}$  mode transition

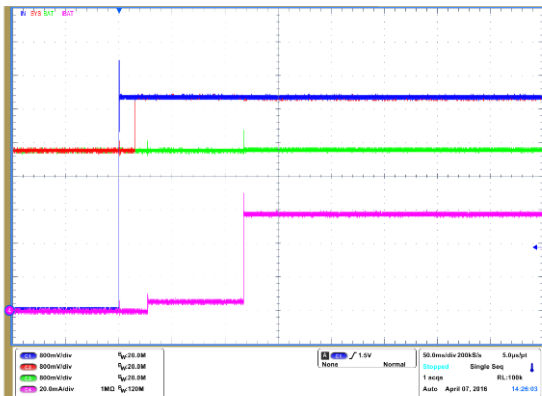
CH1 (blue) =  $V_{IN}$  800 mV/div  
 CH2 (red) =  $V_{SYS}$  800 mV/div  
 CH3 (green) =  $V_{BAT}$  800 mV/div  
 CH4 (pink) =  $I_{BAT}$  20 mA/div

**Figure 11. Wake-up operation,  $V_{SYS}$  and LDO rise overview**


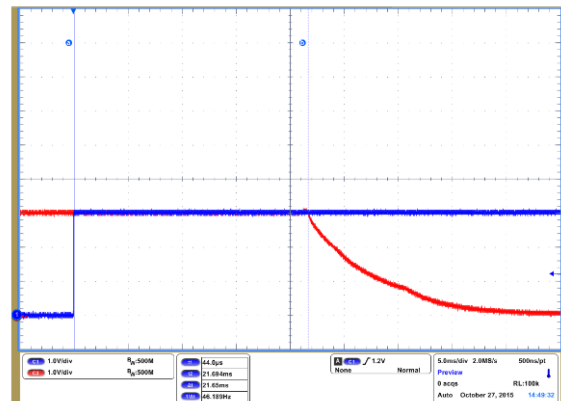
CH1 (blue) =  $V_{LDO}$  800 mV/div  
 CH2 (red) =  $V_{SYS}$  800 mV/div  
 CH3 (green) =  $V_{BAT}$  800 mV/div  
 CH4 (pink) = Wake-up 3 V/div

**Figure 12. Wake-up operation,  $V_{SYS}$  and LDO rise detail**


CH1 (blue) =  $V_{LDO}$  800 mV/div  
 CH2 (red) =  $V_{SYS}$  800 mV/div  
 CH3 (green) =  $V_{BAT}$  800 mV/div  
 CH4 (pink) = Wake-up 3 V/div

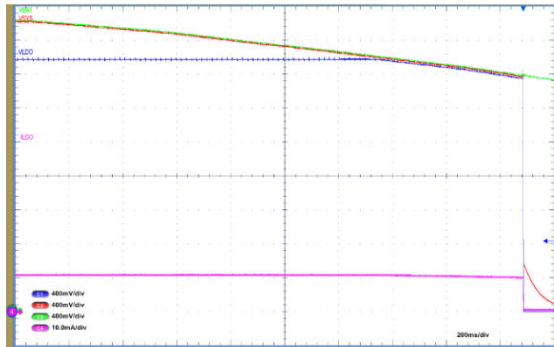
**Figure 13.  $V_{IN}$  plug, charging initialization battery mode to  $V_{IN}$  mode transition**


CH1 (blue) =  $V_{IN}$  800 mV/div  
 CH2 (red) =  $V_{SYS}$  800 mV/div  
 CH3 (green) =  $V_{BAT}$  800 mV/div  
 CH4 (pink) =  $I_{BAT}$  20 mA/div

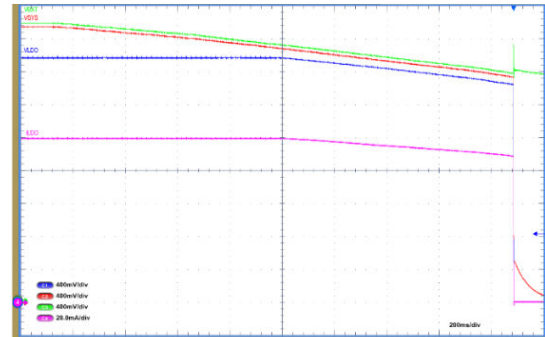
**Figure 14. Shutdown mode entry**


By SD pin

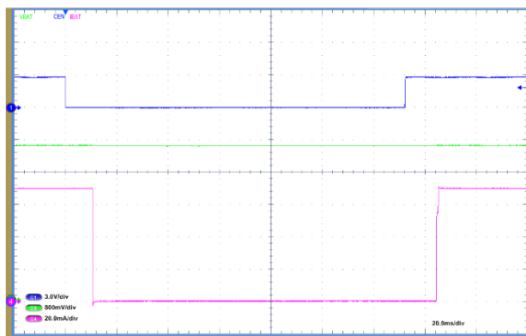
CH1 (blue) = SD pin, 1 V/div  
 CH2 (red) = SYS pin, 1 V/div

**Figure 15.  $V_{BAT}$  to  $V_{SYS}$  drop and  $V_{SYS}$  to  $V_{LDO}$  drop (10 mA)**

 LDO loaded by 10 mA;  $V_{ODC}$  cut-off

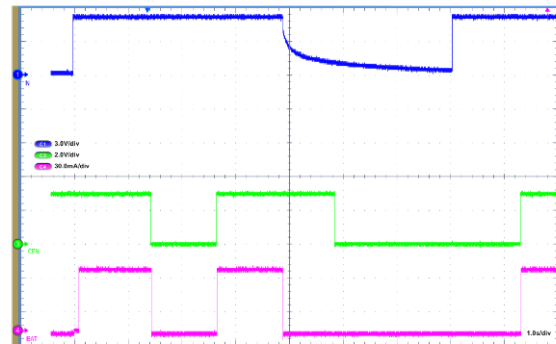
CH1 (blue) =  $V_{LDO}$  400 mV/div  
 CH2 (red) =  $V_{SYS}$  400 mV/div  
 CH3 (green) =  $V_{BAT}$  400 mV/div  
 CH4 (pink) =  $I_{LDO}$  10 mA/div

**Figure 16.  $V_{BAT}$  to  $V_{SYS}$  drop and  $V_{SYS}$  to  $V_{LDO}$  drop (100 mA)**

 LDO loaded by 100 mA;  $V_{ODC}$  cut-off

CH1 (blue) =  $V_{LDO}$  400 mV/div  
 CH2 (red) =  $V_{SYS}$  400 mV/div  
 CH3 (green) =  $V_{BAT}$  400 mV/div  
 CH4 (pink) =  $I_{LDO}$  20 mA/div

**Figure 17.  $C_{EN}$  operation**


CH1 (blue) =  $C_{EN}$  3 V/div  
 CH3 (green) =  $V_{BAT}$  800 mV/div  
 CH4 (pink) =  $I_{BAT}$  20 mA/div

**Figure 18.  $C_{EN}$  operation,  $V_{IN}$  plug/unplug**


CH1 (blue) = IN pin 3.0 V/div  
 CH3 (green) =  $C_{EN}$  2.0 V/div  
 CH4 (pink) =  $I_{BAT}$  30 mA/div

## 6 Functional pin description

### 6.1 GND, AGND

The STBC03 ground pins.

### 6.2 NTC

The battery temperature monitoring pin. Connect the battery NTC thermistor to this pin. The charging cycle stops when the battery temperature is outside of the safe temperature range (0 °C to 45 °C). When the charging cycle is completed, the NTC pin goes to a high impedance state, therefore the NTC thermistor can be also used, together with an external circuitry, to monitor the battery temperature while it is being discharged. If the NTC thermistor is not used, a 10 kΩ resistor must be connected to ensure proper IC operations.

### 6.3 ISET, IPRE

Fast and pre-charge current programming pins. Connect two resistors ( $R_{ISET}$ ,  $R_{IPRE}$ ) to ground to set the fast and pre-charge current ( $I_{FAST}$ ,  $I_{PRE}$ ) according to the following equation (valid for  $I_{FAST}$ ,  $I_{PRE} > 5$  mA):

**Equation 1:**

$$I_{PRE} = \frac{V_{IPRE}}{R_{IPRE}} * K; \quad I_{FAST} = \frac{V_{ISET}}{R_{ISET}} * K \quad (1)$$

Where  $V_{ISET} = V_{IPRE} = 1$  V and  $K = 200$ . Fast charge and pre-charge currents can be independently set from 1 mA to 650 mA. End-of-charge current value is typically 5% of the fast charging current value being set.

For low charging current ( $I_{FAST}$ ,  $I_{PRE} < 5$  mA), the  $R_{ISET}$  and  $R_{IPRE}$  values in the following table must be used.

**Table 6. Charging current setting**

$I_{FAST}$ , $I_{PRE}$	$R_{ISET}$ , $R_{IPRE}$
5 mA	40.5 k
2 mA	110 k
1 mA	260 k

Both  $R_{ISET}$  and  $R_{IPRE}$  must be always used. Short-circuit to ground or open circuit are not allowed options.

### 6.4 BATMS, BATMS\_EN

Battery voltage measurement. If BATMS\_EN is high, the BATMS pin is internally shorted to the BATSNS pin during normal conditions to monitor the battery voltage using external components ( $\mu$ C and embedded ADC). The internal path from BATMS pin to the battery is opened in case any of the following conditions occur: overcurrent, battery over-discharge, shutdown mode, short-circuit on SYS or LDO. To minimize overall system power consumption, this function must be disabled. BATMS\_EN pin should be pulled low.

### 6.5 BATSNS, BATSNSFV

Battery voltage sense pin. The BATSNS pin must be connected as close as possible to the battery positive terminal to ensure the maximum accuracy on the floating voltage and on the battery voltage protection thresholds. The BATSNSFV pin can be used to fix the  $V_{FLOAT}$  value by connecting a proper external series resistor to BATSNSFV. The battery floating voltage can be set up to 4.45 V according to the following equation:

**Equation 2:**

$$V_{float_{adj}} = V_{float_{def}} * \left(1 + \frac{R_{float}}{1M\Omega}\right) V = 4.2 * \left(1 + \frac{R_{float}}{1M\Omega}\right) V \quad (2)$$

Example: to set the battery floating voltage for 4.35 V, refer to the following equation.

**Equation 3:**

$$R_{ext} = 1M\Omega * \left(\frac{V_{float_{adj}}}{4.2V} - 1\right) = 1M\Omega * \left(\frac{4.35V}{4.2V} - 1\right) = 35.7K\Omega \quad (3)$$

If the BATSNSFV pin is connected to the battery positive terminal, the floating voltage is set for its 4.2 V default value.

## 6.6 BAT

External battery connection pin (positive terminal). A 4.7  $\mu\text{F}$  ceramic bypass capacitor must be connected to GND.

## 6.7 IN

5 V input supply voltage pin. The **STBC03** is powered off from this pin when a valid voltage source is detected, meaning a voltage higher than  $V_{UVLO}$  and lower than  $V_{INOVP}$ . A 10  $\mu\text{F}$  ceramic bypass capacitor must be connected to GND.

## 6.8 SYS

The internal LDO input voltage and external unregulated supply pin. The maximum current deliverable through this pin depends on the following two conditions: LDO load and battery status. However, if none of the above loads sinks current, the maximum SYS current budget is 650 mA, provided that the input voltage source can deliver that amount of current.

SYS voltage source can be either IN or BAT, depending on the operating conditions (refer to the following table). A ceramic bypass capacitor of 1  $\mu\text{F}$  must be connected to GND.

**Table 7. SYS voltage source**

$V_{IN}$	$V_{BAT}$	SYS status	LDO status
$< V_{UVLO}$	$< V_{ODC}^{(1)}$	Not powered	Off
$< V_{UVLO}$	$> V_{ODC}$	$V_{BAT}$	On
$> < V_{UVLO}$ and $< V_{INOVP}$	X (don't care) <sup>(3)</sup>	$V_{IN}$	On
$> V_{INOVP}$	$< V_{ODC}$	Not powered	Off
$> V_{INOVP}$	$> V_{ODC}$	$V_{BAT}$	On

- $V_{ODCR}$  if the shutdown mode or the over-discharge protection has been previously activated.
- Voltage drop over internal MOSFET is not included.
- Battery disconnected (0 V) or fully discharged. Resistive short-circuit is not supported for safety reasons.

## 6.9 LDO

LDO output voltage pin. The maximum current capability is anyhow 150 mA. A 1  $\mu\text{F}$  ceramic bypass capacitor must be connected to GND.

## 6.10 WAKE-UP

Wake-up input pin. To restore normal operations of the **STBC03**, so to exit from a shutdown condition, connect the WAKE-UP pin to the battery voltage. The **STBC03** is enabled to operate in normal conditions again, only if the battery voltage is higher than  $V_{ODCR}$  (3 V). A deglitch delay is implemented to prevent unwanted false operations. The above-described WAKE-UP pin functionality is disabled when a valid VIN voltage source is detected. The pin has an internal 50 k $\Omega$  pull-down resistor.

## 6.11 CHG

Active low, open drain charging/fault flag output pin. The CHG provides status information about VIN voltage level, battery charging and faults by toggling at different frequencies as reported in the table below.

**Table 8. CHG pin state**

Device state	CHG pin state	Note
Not valid input ( $V_{IN} < V_{BAT}$ or $V_{IN} > V_{INOVP}$ or $V_{IN} < V_{INUVLO}$ )	High Z (high by external pull-up)	
Valid input ( $V_{IN} > V_{INUVLO}$ , $V_{IN} < V_{INOVP}$ , $V_{BAT} < V_{IN}$ and CEN low)	Low	
End-of-charge (EOC)	Toggling 4.1 Hz (until USB is disconnected)	<p>In case of synchronous alarm events, the highest toggling frequency has higher priority.</p> <p>Example: NTC warning and EOC are concurrent events. NTC warning, signaled by toggling CHG at 16.2 Hz is the only signal available till the battery temperature goes back to a safe range (0 °C to 45 °C). If an EOC condition is still present then a 4.1 Hz toggling signal is present.</p>
Charging phase (pre and fast)	Toggling 6.2 Hz	
Overcharge fault	Toggling 8.2 Hz	
Charging timeout (pre-charge, fast charge)	Toggling 10.2 Hz	
Battery voltage below $V_{PRE}$ after the fast charge starts	Toggling 12.8 Hz	
Charging thermal limitation (thermal warning)	Toggling 14.2 Hz	
Battery temperature fault (NTC warning)	Toggling 16.2 Hz	

## 6.12 CEN

Internal CC/CV charger block enable pin. A low logic level on this pin disables the internal CC/CV charger block. Transitioning CEN from high to low and then back to high, allows the CC/CV charger block to be restarted if it was stopped due to one of the following conditions:

- Charging timeout (pre-charge, fast charge)
- Battery voltage below  $V_{PRE}$  after the fast charge has already started
- End-of-charge

CEN has no effect if the charging cycle has been stopped by a battery overcharge condition.

If the CC/CV charger stops the charging cycle due to an out of range battery temperature, a low logic level on the CEN pin disables the CC/CV charger and resets the charging timeout timers. If CEN is set high, the CC/CV charger restarts normal operations, assuming that no fault condition is detected. CEN is internally pulled up to LDO via a 500 kΩ resistor and must be either left floating or tied to LDO when the STBC03 is powered for the first time.

The auto-recharge function is always enabled so, the CC/CV charger restarts automatically charging the battery if  $V_{BAT}$  goes below 3.9 V; a deglitch time delay has been added to prevent unwanted charging cycle from restarting.

## 6.13 SD

The shutdown pin. In battery mode (if no valid VBUS voltage is present) a logic high level on this pin asserts the low power consumption mode. If SD is kept high when a pulse is applied to WAKE-UP pin the device exits the shutdown condition for the duration of the WAKE-UP pulse. In shutdown mode, the battery drain is then reduced to less than 50 nA. If a valid VBUS voltage is present, the SD pin status has no effect and the device is always out of the shutdown condition.

### 6.14 SW1\_OA, SW1\_OB, SW1\_I, SW2\_OA, SW2\_OB, SW2\_I

SPDT load switch pins. Both of SPDT load switches are controlled by the digital control pins (see section below). Each SPDT features a typical  $R_{DS(on)}$  of 3  $\Omega$ . SPDT load switches can be paralleled to reduce the series resistor as well as to increase the allowable flowing current.

### 6.15 SW\_SEL1 and SW\_SEL2

SW\_SEL1 and SW\_SEL2 drive the SPDT switches according to the following table. They should be connected to GND if not used.

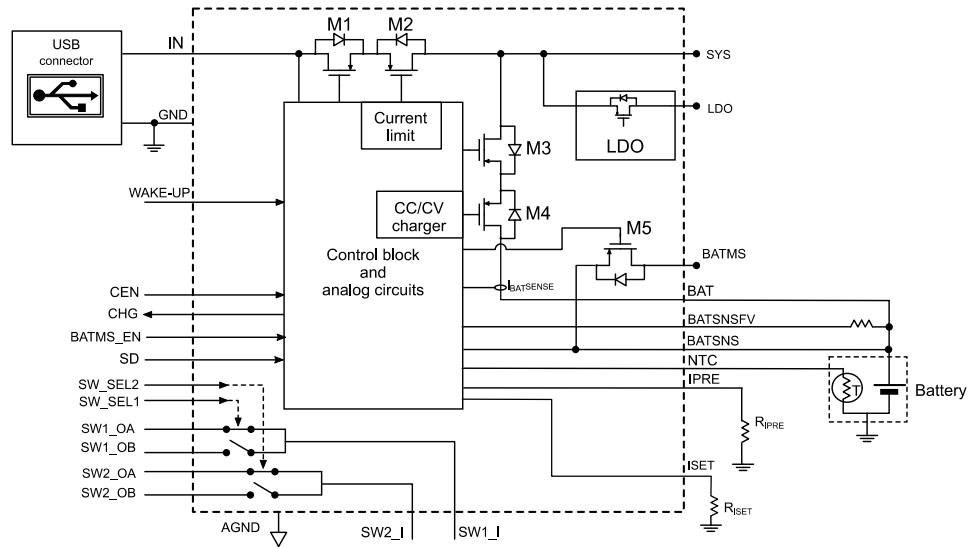
**Table 9. SW\_SEL1, SW\_SEL2 operation**

INPUTS		OUTPUTS			
SW_SEL 1	SW_SEL2	SW1_OA	SW1_OB	SW2_OA	SW2_OB
0	0	SW1_I	Hi-Z	SW2_I	Hi-Z
1	0	Hi-Z	SW1_I	SW2_I	Hi-Z
0	1	SW1_I	Hi-Z	Hi-Z	SW2_I
1	1	Hi-Z	SW1_I	Hi-Z	SW2_I



## 7 Block diagram

Figure 19. STBC03 block diagram



## 8 Operation description

The **STBC03** is a power management IC integrating a battery charger with an embedded power path function, a 150 mA low quiescent LDO, two SPDT load switches and a protection circuit module (PCM) to prevent the battery from being damaged.

When powered off from a single-cell Li-Ion or Li-Poly battery, and after having performed all the safety checks, the **STBC03** starts charging the battery using a constant-current and constant-voltage algorithm.

The embedded power path allows simultaneously the battery to be charged and the overall system to be supplied. By contrast, when the input voltage is above the valid range, the battery supplies the LDO as well as every load connected to SYS.

The **STBC03** also protects the battery in case of:

- Overcharge
- Over-discharge
- Charge overcurrent
- Discharge overcurrent

If a fault condition is detected when the input voltage is valid ( $V_{UVLO} < V_{IN} < V_{INOVLP}$ ), the CHG pin starts toggling, signaling the fault.

The device can also be in shutdown mode (shutdown  $I_{BAT} < 50$  nA) maximizing the battery life of the end-product during its shelf life.

### 8.1 Power-on

When the **STBC03** is in shutdown mode, any load connected to LDO and to SYS is not supplied.

An applied valid input voltage ( $V_{UVLO} < V_{IN} < V_{INOVLP}$ ) for at least 250 ms, regardless the presence of a battery or if the battery is fully depleted, allows the loads connected to SYS and LDO to be supplied, thus enabling proper system operations.

The CEN pin must be left floating or tied high (LDO level) during the power-on for proper operations. The **STBC03** can be also turned on when  $V_{IN}$  is outside the valid range, below the conditions that the battery has at least a remaining charge of 3 V and the wake-up input is properly triggered. The **STBC03** features an UVLO circuit that prevents oscillations if the input voltage source is unstable. The CEN pin must be left floating or tied to a high level (LDO) when the **STBC03** is powered.

### 8.2 Battery charger

The **STBC03** allows single-cell Li-Ion and Li-Poly battery chemistry to be charged up to a 4.45 V using a CC/CV charging algorithm. The charging cycle starts when a valid input voltage source ( $V_{UVLO} < V_{IN} < V_{INOVLP}$ ) is detected and signaled by the CHG pin toggling from a high impedance state to a low logic level.

If the battery is deeply discharged (the battery voltage is lower than  $V_{PRE}$ ), the **STBC03** charger enters the pre-charge phase and starts charging in constant-current mode with the pre-charge current ( $I_{PRE}$ ) set. In case the battery voltage does not reach the  $V_{PRE}$  threshold within the  $t_{PRE}$  time, the charging process is stopped and a fault is signaled.

By contrast, as soon as the battery voltage reaches the  $V_{PRE}$  threshold, the constant-current fast charge phase starts operating, and the relevant charging current increases to the  $I_{FAST}$  level.

Likewise, if the constant current fast charge phase is not completed within  $t_{FAST}$ , meaning that  $V_{BAT} < V_{FLOAT}$ , the charging process is stopped and a fault is signaled (CHG starts toggling at 10.2 Hz as long as a valid  $V_{IN}$  is present).

Should the battery voltage decrease below  $V_{PRE}$  during the fast charge phase, the charging process is halted and a fault is signaled. The constant-current fast charge phase lasts until the battery voltage is lower than  $V_{FLOAT}$ . After that, the charging algorithm switches to a constant-voltage (CV) mode.

During the CV mode, the battery voltage is regulated to  $V_{FLOAT}$  and the charging current starts decreasing over time. As soon as it goes below  $I_{END}$ , the charging process is considered to be completed (EOC, end-of-charge) and the relevant status is signaled via a 4.1 Hz toggling signal on the CHG pin, again as long as there is a valid input source applied ( $V_{UVLO} < V_{IN} < V_{INOVLP}$ ).

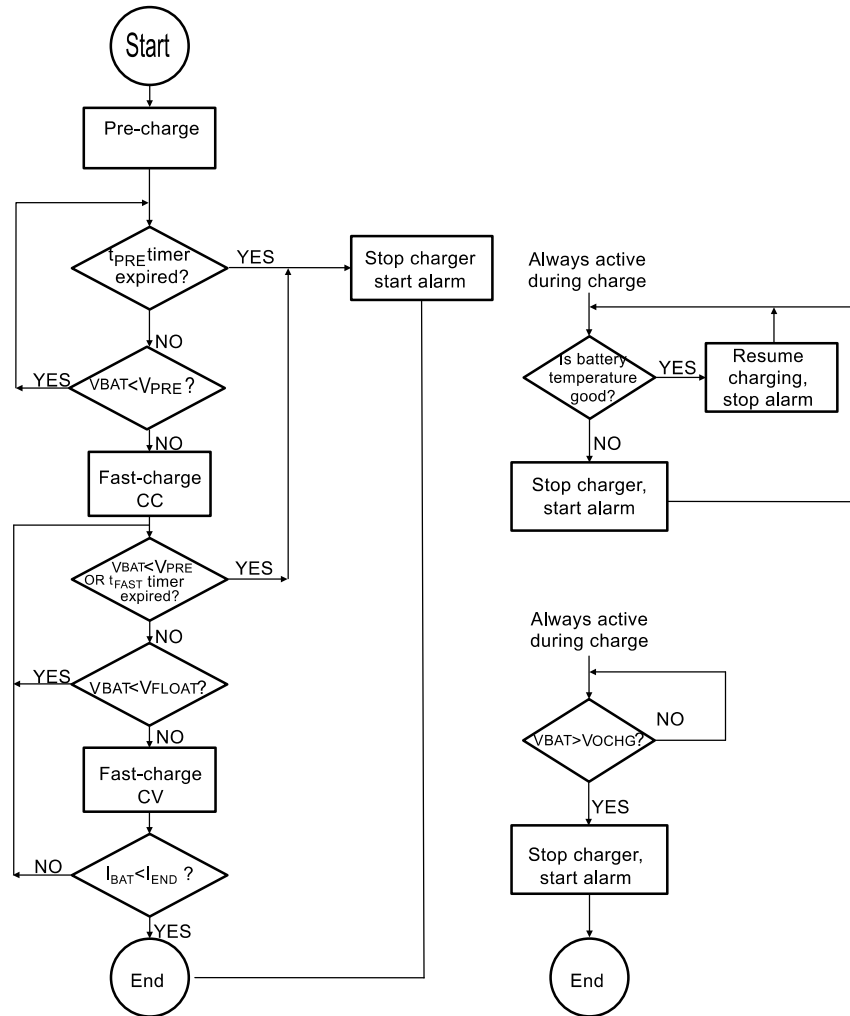
Both  $I_{PRE}$  and the  $I_{FAST}$  values can be programmed from 1 mA to 450 mA via an external resistor, as described in the ISET pin description.

For any  $I_{FAST}$  programmed value above 20 mA, the  $I_{END}$  value can be set either 5% or 2.5% of the  $I_{FAST}$  level.  
 For any  $I_{FAST}$  programmed value below 20 mA, the relevant  $I_{END}$  value is set as per the following table:

**Table 10.  $I_{FAST}$  and  $I_{END}$** 

$I_{FAST}$	$I_{END}$
20 mA	1.7 mA
10 mA	1.1 mA
5 mA	0.65 mA
2 mA	0.4 mA
1 mA	0.2 mA

The battery temperature is monitored throughout the charging cycle for safety reasons.

**Figure 20. Charging flowchart**


Actions:

- Pre-charge starts  $t_{PRE}$  timer, starts charging in CC mode at  $I_{PRE}$
- Fast-charge CC starts  $t_{FAST}$  timer, increases charge current to  $I_{FAST}$
- Fast-charge CV activates the constant-voltage control loop
- Start alarm: the CHG pin starts toggling

Figure 21. End-of-charge flowchart

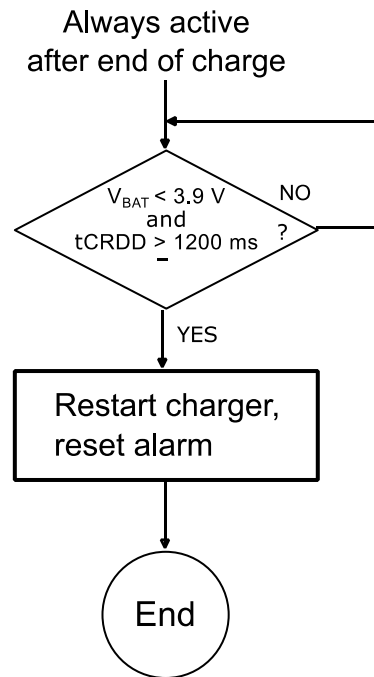
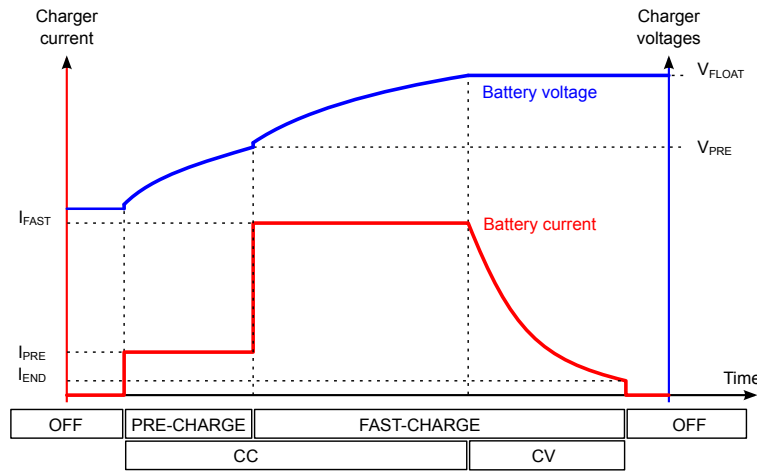


Figure 22. CC/CV charging profile (not in scale)



### 8.3 Battery temperature monitoring

The STBC03 integrates all the needed blocks to monitor the battery temperature through an external NTC resistor. The battery temperature monitoring is enabled only during the battery charging process, in order to save power when the system is supplied from the battery.

When the battery temperature is outside the normal operating range (0-45 °C), the charging process is halted, an alarm signal is activated (the CHG pin toggles at 16.2 Hz) but the charging timeout timers are not stopped.

If the temperature goes back to the normal operating range, before the maximum charging time has elapsed, the charging process is resumed and the alarm signal is cleared.

In case of the charging timeout expires and the temperature is still outside the normal operating range, the charging process is stopped but it can be still restarted using the CEN pin.

Both temperature thresholds feature a 3 °C hysteresis. The battery temperature monitoring block is designed to work with an NTC thermistor having  $R_{25} = 10 \text{ k}\Omega$  and  $\beta = 3370$  (Mitsubishi TH05-3H103F). If an NTC thermistor is not used, 10 kΩ resistor must be connected to ensure the proper IC operation.

### 8.4 Battery overcharge protection

The battery overcharge protection is a safety feature, active when a valid input voltage is connected, preventing the battery voltage from exceeding a  $V_{OCHG}$  value. Should an overcharge condition be detected, the current path from the input to the battery is opened and a fault signal is activated (the CHG pin toggles at 8.2 Hz). When the battery voltage goes below  $V_{OCHG}$ , normal operations can only be restarted by disconnecting and connecting back again the input voltage ( $V_{IN}$ ).

## 8.5 Battery over-discharge protection

The battery over-discharge protection is a safety feature enabled only when no valid input voltage source ( $V_{UVLO} < V_{IN} < V_{INOVP}$ ) is detected. Therefore, when the STBC03 and the system are powered off from the battery, an over-discharge of the battery itself is avoided. Should the battery voltage level be below  $V_{ODC}$  for more than  $t_{ODD}$  (over-discharge state), the STBC03 turns off and current sunk from the battery is reduced to less than 50 nA. When a valid input voltage source is detected, while the battery is in an over-discharge state, the STBC03 charger, SYS and LDO outputs are enabled. This condition persists until the battery voltage has exceeded the over-discharge released threshold ( $V_{ODCR}$ ), otherwise any other disconnection of a valid input voltage source brings back the STBC03 to a battery over-discharge state.

## 8.6 Battery discharge overcurrent protection

When the STBC03 is powered off from the battery connected to the BAT pin, a discharge overcurrent protection circuit disables the STBC03 if the current sunk from the battery is in excess of  $I_{BATOCP}$  (900 mA typical) for more than  $t_{DOD}$ .

The presence of a valid input voltage source or triggering the WAKE-UP input pin, allows normal operating conditions to be restored.

## 8.7 Battery fault protection

The STBC03 features a battery fault protection. The STBC03 charger is stopped if the battery voltage remains below 1 V for at least 16 seconds.

## 8.8 Floating voltage adjustment

The STBC03 features a floating voltage adjustment, controlled via the external resistor  $R_{FLOAT}$  connected between battery and BATSNSFV. For safety reasons, the battery voltage overcharge threshold level ( $V_{OCHG}$ ) is linked to any floating voltage set.

## 8.9 Input overcurrent protection

When the STBC03 is powered off from a valid input voltage source, a current limitation circuit prevents the input current from increasing in an uncontrolled manner in case of excessive load. In fact, when  $V_{SYS}$  is lower than  $V_{ILIMSCTH}$ , the input current is limited so to have a reduced power dissipation. As soon as  $V_{SYS}$  increases over  $V_{ILIMSCTH}$ , the input current limit value is increased to  $I_{INLIM}$ .

## 8.10 SYS short-circuit protection, LDO current limitation

In battery mode condition, if a short-circuit on the SYS pin happens, the STBC03 is turned off (no deglitch). This short-circuit protection occurs until the SYS voltage drops below  $V_{SCSYS}$ .

If the LDO output is in a short-circuit condition, the maximum delivered current is limited to  $I_{SC}$ .

## 8.11 IN overvoltage protection

Should the input voltage source temporarily be  $V_{IN} > V_{INOVP}$  (for example due to a poorly regulated voltage source), then the STBC03 is powered off from the battery, thus any load connected to SYS is protected.

As soon as the input voltage source goes back within a valid input range ( $V_{UVLO} < V_{IN} < V_{INOVP}$ ), the STBC03 is then powered off again from  $V_{IN}$ .

## 8.12 Shutdown mode

Asserting the SD pin high forces the STBC03 to enter in shutdown mode (low power), the current sunk from the battery is reduced to less than 50 nA. Both SYS and LDO pins are not supplied. Normal operating conditions are restored either by connecting a valid input voltage source ( $V_{UVLO} < V_{IN} < V_{INOVP}$ ) for at least  $t_{PW-VIN}$  or by connecting the WAKE-UP pin to  $V_{BAT}$  for at least  $t_{PW-WA}$ .

### 8.13 Thermal shutdown

The STBC03 is fully protected against overheating. During the charging process, if a  $T_{WRN} < T_{SD}$  temperature level is detected, a warning is signaled via the CHG output (toggling at 14.2 Hz). In this condition, the programmed  $I_{PRE}$  and  $I_{FAST}$  are temporary halved. In case of a further temperature increase (up to  $T_{SD}$ ) the STBC03 turns off, thus stopping the charging process. This condition is latched and normal operation can be restored only by disconnecting and reconnecting back again a valid input voltage source on the  $V_{IN}$  pin.

### 8.14 Reverse current protection

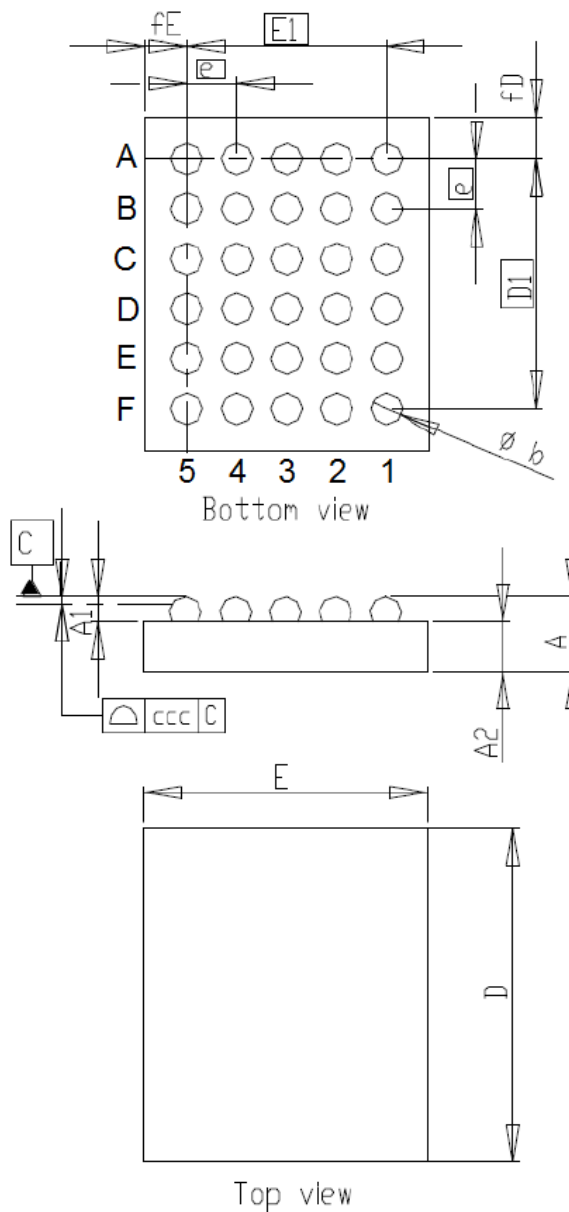
When the input voltage ( $V_{IN}$ ) is higher than  $V_{UVLO}$ , but lower than the battery voltage  $V_{BAT}$  ( $V_{UVLO} < V_{IN} < V_{BAT}$ ) the current path from BAT to IN is opened so to stop any reverse current flowing from the battery to the input voltage source. This event is signaled through the CHG flag.

## 9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 9.1 Flip Chip 30 (2.59x2.25 mm) package information

Figure 23. Flip Chip 30 (2.59x2.25 mm) package outline

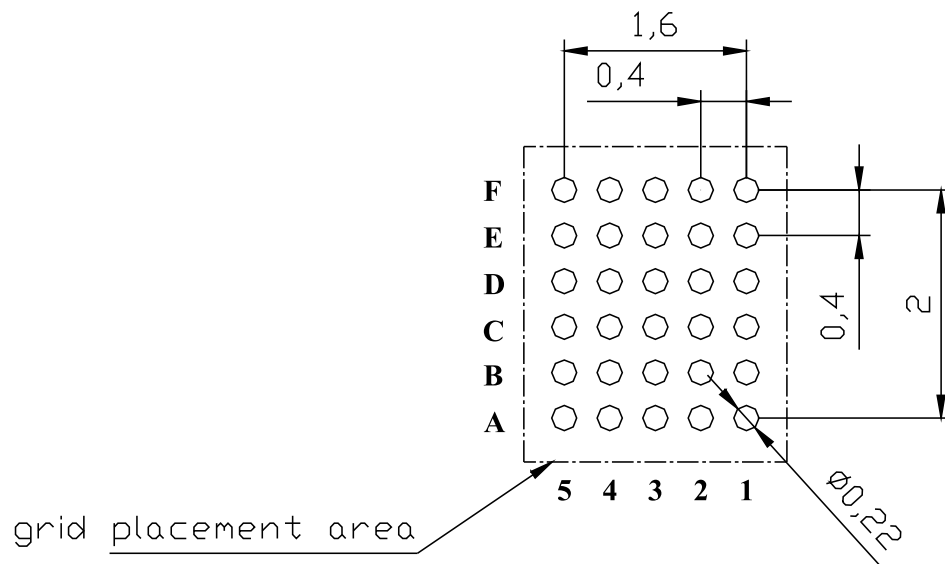




**Table 11. Flip Chip 30 (2.59x2.25 mm) package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.50	0.55	0.60
A1	0.17	0.20	0.23
A2	0.33	0.35	0.37
b	0.23	0.26	0.29
D	2.56	2.59	2.62
D1		2	
E	2.22	2.25	2.28
E1		1.6	
e		0.40	
SE		0.20	
SD		0.20	
fD	0.285	0.295	0.305
fE	0.315	0.325	0.335
ccc		0.075	

**Note:** The terminal A1 on the bumps side is identified by a distinguishing feature (for instance by a circular "clear area", typically 0.1 mm diameter) and/or a missing bump. The terminal A1 on the backside of the product is identified by a distinguishing feature (for instance by a circular "clear area", typically between 0.1 and 0.5 mm diameter, depending on the die size).

**Figure 24. Flip Chip 30 (2.59x2.25 mm) recommended footprint**


## Revision history

**Table 12. Document revision history**

Date	Revision	Changes
10-Nov-2016	1	Initial release.
07-Feb-2017	2	Datasheet promoted from preliminary to production data.
28-Aug-2017	3	Updated Table 5: "Electrical characteristics". Updated Figure 19: "STBC03 block diagram".
06-Mar-2018	4	Updated Figure 4. Thermal management.
26-May-2020	5	Updated Section 6.12 CEN
03-Mar-2022	6	Updated $t_{PW-VIN}$ Typical value in Table 5

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