PCA9538A

Low-voltage 8-bit I²C-bus I/O port with interrupt and reset

Rev. 1 — 28 September 2012 Product data sheet

1. General description

The PCA9538A is a low-voltage 8-bit General Purpose Input/Output (GPIO) expander with interrupt and reset for I²C-bus/SMBus applications. NXP I/O expanders provide a simple solution when additional I/Os are needed while keeping interconnections to a minimum, for example, in ACPI power switches, sensors, push buttons, LEDs, fan control, etc.

In addition to providing a flexible set of GPIOs, the wide V_{DD} range of 1.65 V to 5.5 V allows the PCA9538A to interface with next-generation microprocessors and microcontrollers where supply levels are dropping down to conserve power.

The PCA9538A contains the PCA9538A register set of four 8-bit Configuration, Input, Output, and Polarity Inversion registers.

The PCA9538A is a pin-to-pin replacement for the PCA9538 and other industry-standard devices. A more fully functional device, the PCAL9538A, is available with Agile I/O features. See the respective data sheet for more details.

The PCA9538A open-drain interrupt ($\overline{INT}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

$\overline{INT}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus. Thus, the PCA9538A can remain a simple slave device.

The device outputs have 25 mA sink capabilities for directly driving LEDs while consuming low device current.

The power-on reset sets the registers to their default values and initializes the device state machine. In the PCA9538A, the $\overline{RESET}$ pin causes the same reset/default I/O input configuration to occur without de-powering the device, holding the registers and I²C-bus state machine in their default state until the $\overline{RESET}$ input is once again HIGH. This input requires a pull-up to V_{DD}.

Two hardware pins (A0, A1) select the fixed I²C-bus address and allow up to four devices to share the same I²C-bus/SMBus.

2. Features and benefits

- I²C-bus to parallel port expander
- Operating power supply voltage range of 1.65 V to 5.5 V
- Low standby current consumption:
  - 1.5 μA (typical at 5 V V_{DD})
  - 1.0 μA (typical at 3.3 V V_{DD})
- Schmitt-trigger action allows slow input transition and better switching noise immunity at the SCL and SDA inputs
  - $V_{hys} = 0.10 \times V_{DD}$ (typical)
- 5 V tolerant I/Os
- Active LOW reset input ($\overline{RESET}$)
- Open-drain active LOW interrupt output ($\overline{INT}$)
- 400 kHz Fast-mode I²C-bus
- Internal power-on reset
- Power-up with all channels configured as inputs
- No glitch on power-up
- Latched outputs with 25 mA drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA per JESD78, Class II
- ESD protection exceeds JESD22
  - 2000 V Human Body Model (A114-A)
  - 1000 V Charged-Device Model (C101)
- Packages offered: TSSOP16 and HVQFN16

3. Ordering information

Table 1. Ordering information

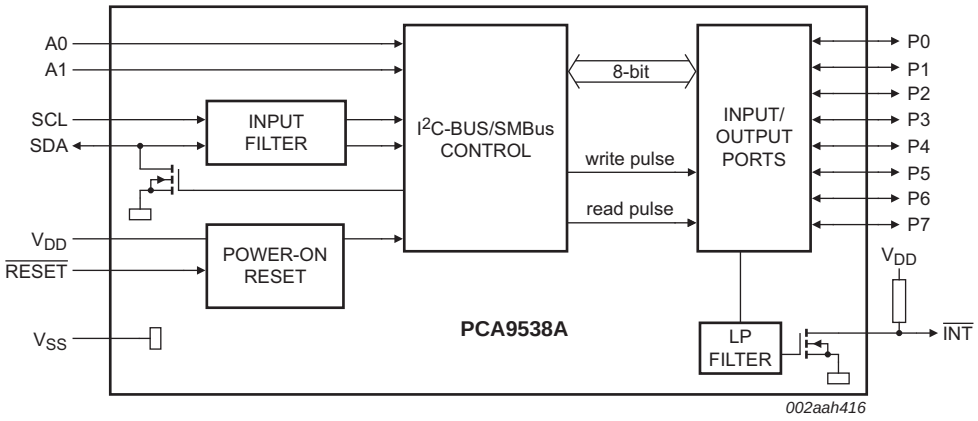
Type number	Topside mark	Package		
		Name	Description	Version
PCA9538ABS	P3A	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 × 3 × 0.85 mm	SOT758-1
PCA9538APW	PA9538A	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA9538ABS	PCA9538ABSHP	HVQFN16	Reel pack, SMD, 13-inch, Turned	6000	T_{amb} = –40 °C to +85 °C
PCA9538APW	PCA9538APWJ	TSSOP16	Reel pack, SMD, 13-inch	2500	T_{amb} = –40 °C to +85 °C

4. Block diagram



Remark: All I/Os are set to inputs at reset.

Fig 1. Block diagram of PCA9538A

5. Pinning information

5.1 Pinning

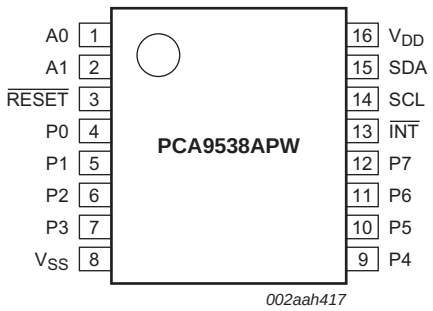


Fig 2. Pin configuration for TSSOP16

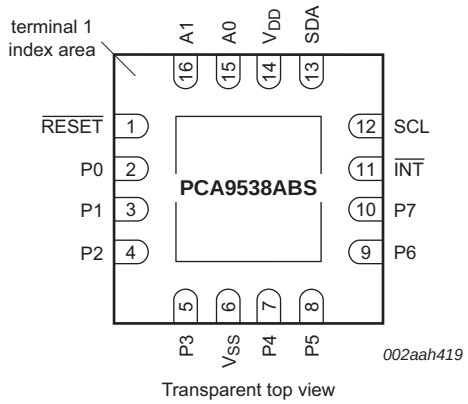


Fig 3. Pin configuration for HVQFN16

5.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	TSSOP16	HVQFN16	
A0	1	15	address input 0
A1	2	16	address input 1
$\overline{\text{RESET}}$	3	1	active LOW reset input
P0[1]	4	2	Port P input/output 0
P1[1]	5	3	Port P input/output 1
P2[1]	6	4	Port P input/output 2
P3[1]	7	5	Port P input/output 3
V_{SS}	8	6[2]	supply ground
P4[1]	9	7	Port P input/output 4
P5[1]	10	8	Port P input/output 5
P6[1]	11	9	Port P input/output 6
P7[1]	12	10	Port P input/output 7
$\overline{\text{INT}}$	13	11	interrupt output (open-drain)
SCL	14	12	serial clock line
SDA	15	13	serial data line
V_{DD}	16	14	supply voltage

[1] All I/O are configured as input at power-on.

[2] HVQFN16 package die supply ground is connected to both the V_{SS} pin and the exposed center pad. The V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

6. Functional description

Refer to Figure 1 “Block diagram of PCA9538A”.

6.1 Device address

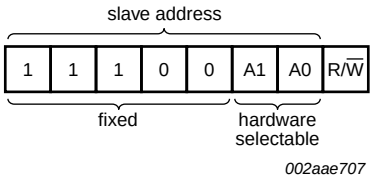


Fig 4. PCA9538A address

A1 and A0 are the hardware address package pins and are held to either HIGH (logic 1) or LOW (logic 0) to assign one of the four possible slave addresses. The last bit of the slave address (R/$\overline{W}$) defines the operation (read or write) to be performed. A HIGH (logic 1) selects a read operation, while a LOW (logic 0) selects a write operation.

6.2 Pointer register and command byte

Following the successful acknowledgement of the address byte, the bus master sends a command byte, which is stored in the Pointer register in the PCA9538A. Two bits of this data byte state the operation (read or write) and the internal registers (Input, Output, Polarity Inversion, or Configuration) that will be affected. Bit 6 in conjunction with the lower three bits of the Command byte are used to point to the extended features of the device (Agile I/O). This register is write only.

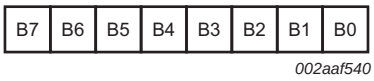


Fig 5. Pointer register bits

Table 4. Command byte

Pointer register bits								Command byte (hexadecimal)	Register	Protocol	Power-up default
B7	B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	0	00h	Input port	read byte	xxxx xxxx[1]
0	0	0	0	0	0	0	1	01h	Output port	read/write byte	1111 1111
0	0	0	0	0	0	1	0	02h	Polarity Inversion	read/write byte	0000 0000
0	0	0	0	0	0	1	1	03h	Configuration	read/write byte	1111 1111

[1] Undefined.

6.3 Interface definition

Table 5. Interface definition

Byte	Bit							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C-bus slave address	H	H	H	L	L	A1	A0	R/$\overline{W}$
I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

6.4 Register descriptions

6.4.1 Input port register (00h)

The Input port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. The Input port register is read only; writes to this register have no effect. The default value 'X' is determined by the externally applied logic level. An Input port register read operation is performed as described in Section 7.2 "Read commands".

Table 6. Input port register (address 00h)

Bit	7	6	5	4	3	2	1	0
Symbol	I7	I6	I5	I4	I3	I2	I1	I0
Default	X	X	X	X	X	X	X	X

6.4.2 Output port register (01h)

The Output port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from this register reflect the value that was written to this register, **not** the actual pin value.

Table 7. Output port register (address 01h)

Bit	7	6	5	4	3	2	1	0
Symbol	O7	O6	O5	O4	O3	O2	O1	O0
Default	1	1	1	1	1	1	1	1

6.4.3 Polarity inversion register (02h)

The Polarity inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with '1'), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a '0'), the corresponding port pin's original polarity is retained.

Table 8. Polarity inversion register (address 02h)

Bit	7	6	5	4	3	2	1	0
Symbol	N7	N6	N5	N4	N3	N2	N1	N0
Default	0	0	0	0	0	0	0	0

6.4.4 Configuration register (03h)

The Configuration register (register 3) configures the direction of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

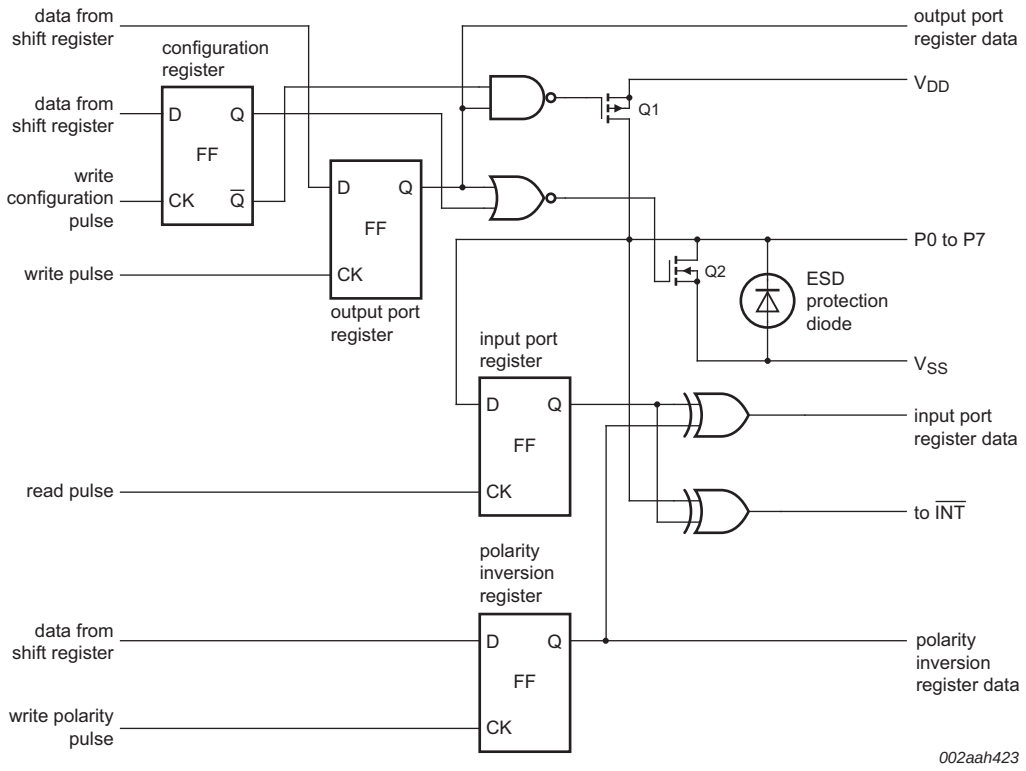
Table 9. Configuration register (address 03h)

Bit	7	6	5	4	3	2	1	0
Symbol	C7	C6	C5	C4	C3	C2	C1	C0
Default	1	1	1	1	1	1	1	1

6.5 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above V_{DD} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output port register. In this case, there are low-impedance paths between the I/O pin and either V_{DD} or V_{SS}. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.



On power-up or reset, all registers return to default values.

Fig 6. Simplified schematic of the I/Os (P0 to P7)

6.6 Power-on reset

When power (from 0 V) is applied to V_{DD}, an internal power-on reset holds the PCA9538A in a reset condition until V_{DD} has reached V_{POR}. At that time, the reset condition is released and the PCA9538A registers and I²C-bus/SMBus state machine initialize to their default states. After that, V_{DD} must be lowered to below V_{PORF} and back up to the operating voltage for a power-reset cycle. See Section 8.3 “Power-on reset requirements”.

6.7 Reset input ($\overline{\text{RESET}}$)

The $\overline{\text{RESET}}$ input can be asserted to initialize the system while keeping the V_{DD} at its operating level. A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin LOW for a minimum of $t_{w(rst)}$. The PCA9538A registers and I²C-bus/SMBus state machine are changed to their default state once $\overline{\text{RESET}}$ is LOW (0). When $\overline{\text{RESET}}$ is HIGH (1), the I/O levels at the P port can be changed externally or through the master. This input requires a pull-up resistor to V_{DD} if no active connection is used.

6.8 Interrupt output ($\overline{\text{INT}}$)

An interrupt is generated by any rising or falling edge of the port inputs in the Input mode. After time $t_{v(INT)}$, the signal $\overline{\text{INT}}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or when data is read from the port that generated the interrupt (see Figure 10). Resetting occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{\text{INT}}$.

A pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input port register.

The $\overline{\text{INT}}$ output has an open-drain structure and requires a pull-up resistor to V_{DD}. $\overline{\text{INT}}$ should be connected to the voltage source of the device that requires the interrupt information. When using the input latch feature, the input pin state is latched. The interrupt is reset only when data is read from the port that generated the interrupt. The reset occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal.

7. Bus transactions

The PCA9538A is an I²C-bus slave device. Data is exchanged between the master and PCA9538A through write and read commands using I²C-bus. The two communication lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1 Write commands

Data is transmitted to the PCA9538A by sending the device address and setting the Least Significant Bit (LSB) to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission.

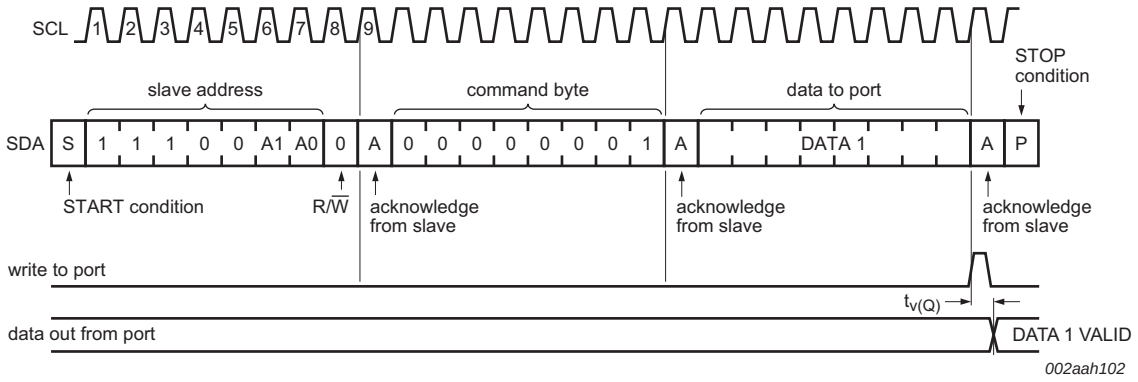


Fig 7. Write to Output port register

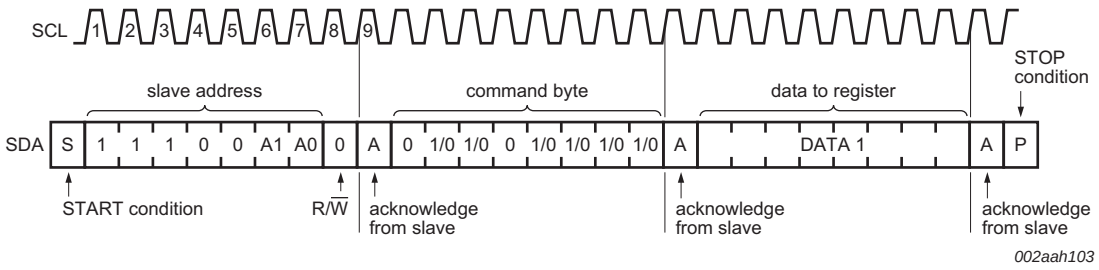


Fig 8. Write to Configuration or Polarity inversion registers

7.2 Read commands

To read data from the PCA9538A, the bus master must first send the PCA9538A address with the least significant bit set to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register is to be accessed.

After a restart the device address is sent again, but this time the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9538A (see Figure 9 and Figure 10).

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limit on the number of data bytes received in one read transmission, but on the final byte received the bus master must not acknowledge the data.

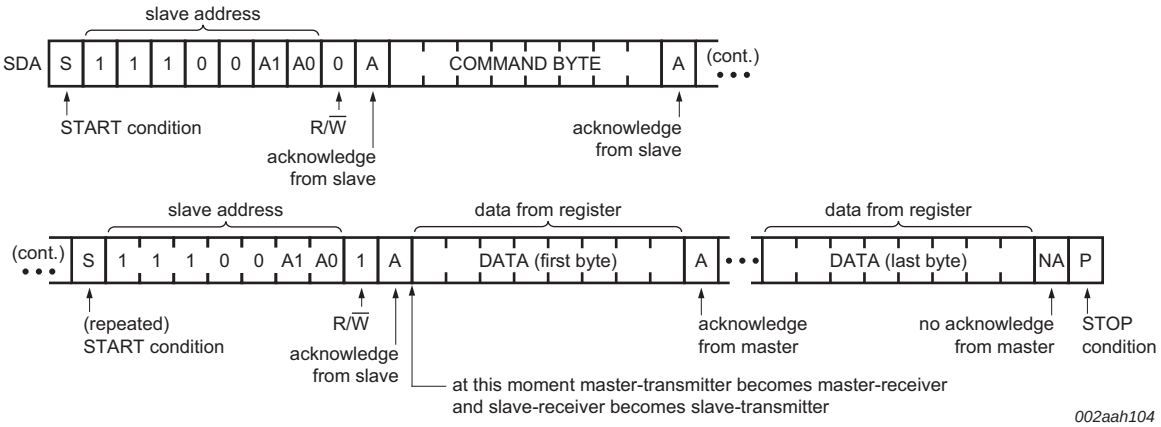
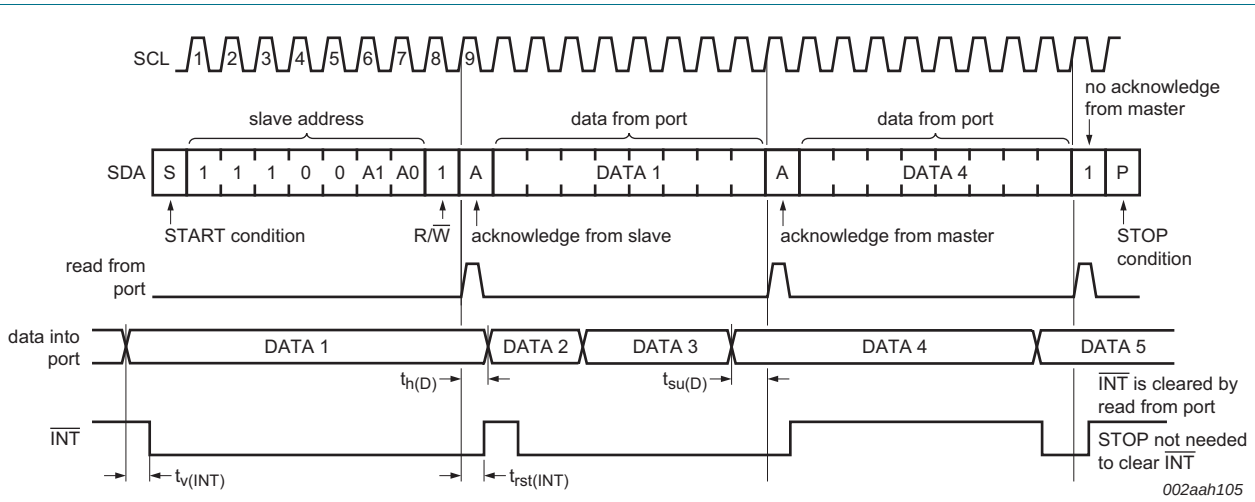


Fig 9. Read from register

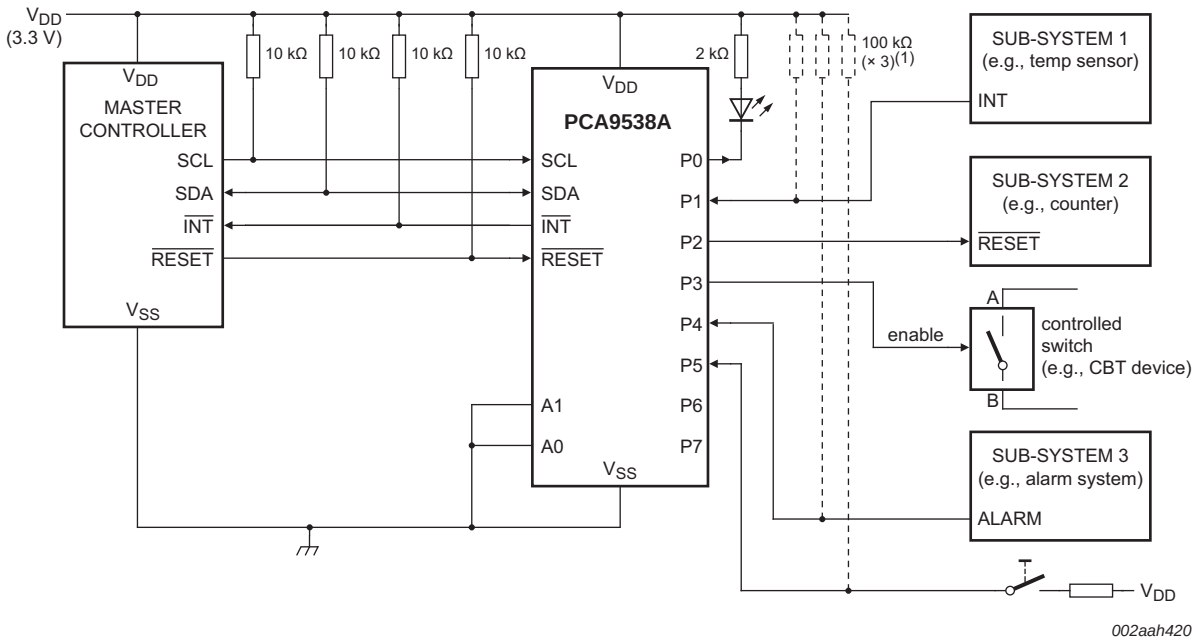


Transfer of data can be stopped at any time by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been programmed with 00h (read Input port register).

This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from P port (see Figure 9).

Fig 10. Read Input port register

8. Application design-in information



Device address is 1110 000x for this example.

P0, P2, P3 configured as outputs.

P1, P4, P5 configured as inputs.

P6, P7 are not used and need 100 kΩ pull-up resistors to protect them from floating or the internal pull-up or pull-down selected.

(1) Resistors are required for inputs (on P port) that may float. If a driver to an input will never let the input float, a resistor is not needed. Outputs (in the P port) do not need pull-up resistors.

Fig 11. Typical application

8.1 Minimizing I_{DD} when the I/Os are used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{DD} through a resistor as shown in Figure 11. Since the LED acts as a diode, when the LED is off the I/O V_I is about 1.2 V less than V_{DD}. The supply current, I_{DD}, increases as V_I becomes lower than V_{DD}.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{DD} when the LED is off. Figure 12 shows a high value resistor in parallel with the LED. Figure 13 shows V_{DD} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_I at or above V_{DD} and prevents additional supply current consumption when the LED is off.

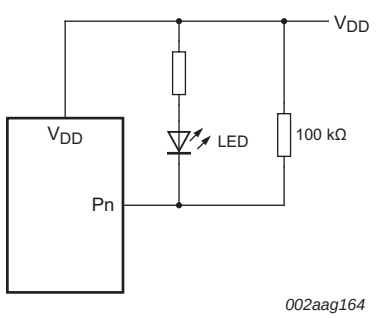


Fig 12. High value resistor in parallel with the LED

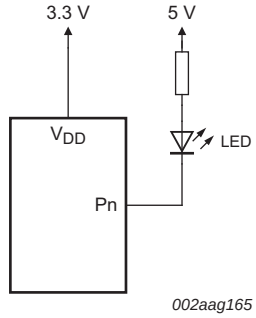


Fig 13. Device supplied by a lower voltage

8.2 12 V tolerant I/Os

The PCA9538A device SCR group reference diode can go up to 10 V before latch back to 8 V. The ESD gate oxide will protect the device, but not if used continually. Therefore, to achieve 12 V tolerant I/Os, the external protection circuitry (diode) must be used as shown in Figure 14.

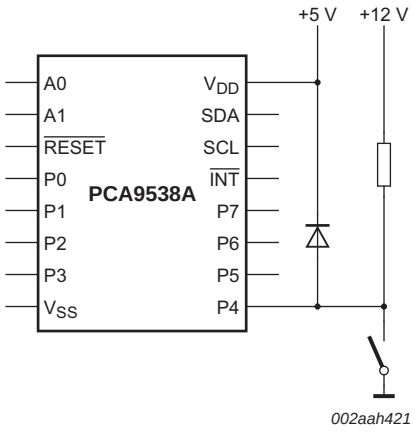


Fig 14. External protection circuitry

8.3 Power-on reset requirements

In the event of a glitch or data corruption, PCA9538A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 15 and Figure 16.

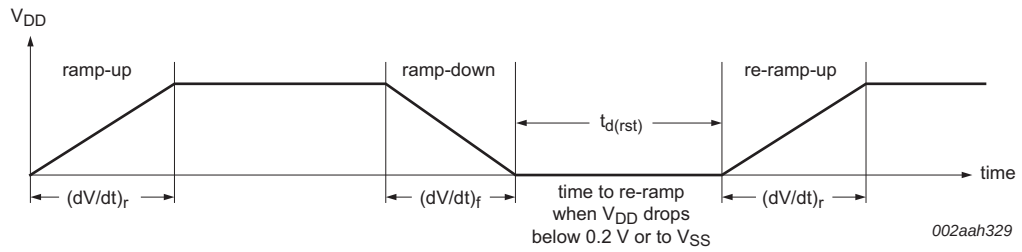


Fig 15. V_{DD} is lowered below 0.2 V or 0 V and then ramped up to V_{DD}

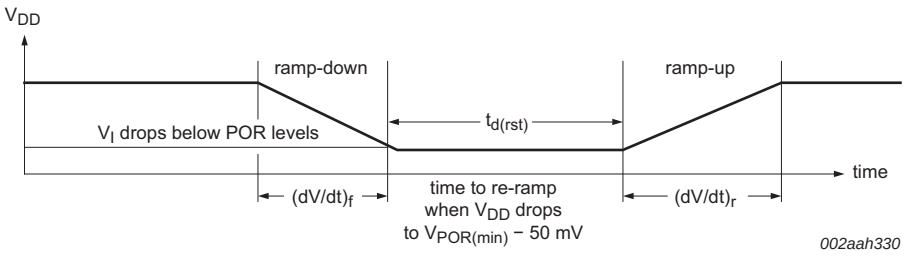


Fig 16. V_{DD} is lowered below the POR threshold, then ramped back up to V_{DD}

Table 10 specifies the performance of the power-on reset feature for PCA9538A for both types of power-on reset.

Table 10. Recommended supply sequencing and ramp rates

T_{amb} = 25 °C (unless otherwise noted). Not tested; specified by design.

Symbol	Parameter	Condition		Min	Typ	Max	Unit
$(dV/dt)_f$	fall rate of change of voltage	Figure 15		0.1	-	2000	ms
$(dV/dt)_r$	rise rate of change of voltage	Figure 15		0.1	-	2000	ms
$t_{d(rst)}$	reset delay time	Figure 15; re-ramp time when V_{DD} drops to V_{SS}		1	-	-	µs
		Figure 16; re-ramp time when V_{DD} drops to $V_{POR(min)}$ − 50 mV		1	-	-	µs
$\Delta V_{DD(gl)}$	glitch supply voltage difference	Figure 17	[1]	-	-	1.0	V
$t_{w(gl)VDD}$	supply voltage glitch pulse width	Figure 17	[2]	-	-	10	µs
$V_{POR(trip)}$	power-on reset trip voltage	falling V_{DD}		0.7	-	-	V
		rising V_{DD}		-	-	1.4	V

[1] Level that V_{DD} can glitch down to, but not cause a functional disruption when $t_{w(gl)VDD} < 1$ µs.

[2] Glitch width that will not cause a functional disruption when $\Delta V_{DD(gl)} = 0.5 \times V_{DD}$.

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ($t_{w(gl)VDD}$) and glitch height ($\Delta V_{DD(gl)}$) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 17 and Table 10 provide more information on how to measure these specifications.

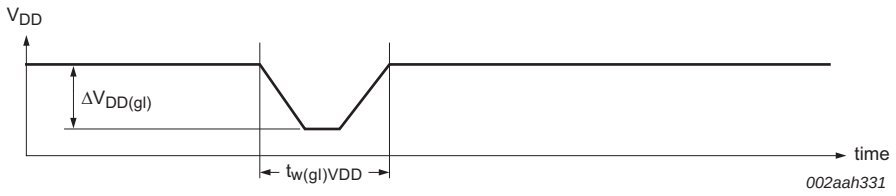


Fig 17. Glitch width and glitch height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I²C-bus/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{DD} being lowered to or from 0 V. Figure 18 and Table 10 provide more details on this specification.

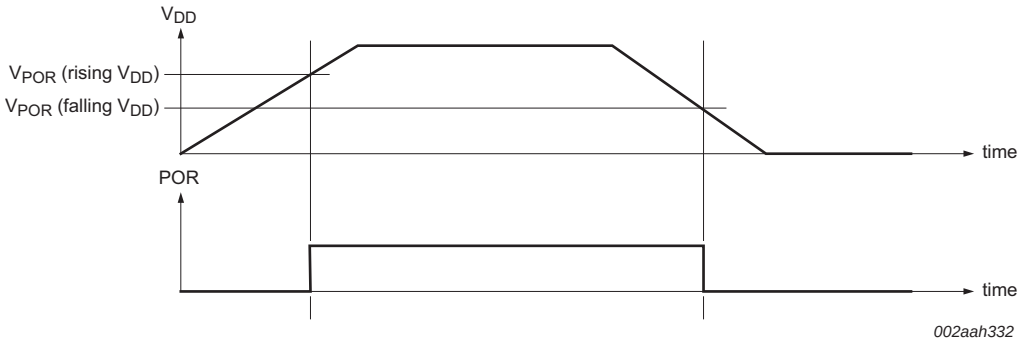


Fig 18. Power-on reset voltage (V_{POR})

9. Limiting values

Table 11. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+6.5	V
V_I	input voltage		[1]	–0.5	+6.5	V
V_O	output voltage		[1]	–0.5	+6.5	V
I_{IK}	input clamping current	A0, A1, $\overline{RESET}$, SCL; $V_I < 0$ V		-	±20	mA
I_{OK}	output clamping current	$\overline{INT}$; $V_O < 0$ V		-	±20	mA
I_{IOK}	input/output clamping current	P port; $V_O < 0$ V or $V_O > V_{DD}$		-	±20	mA
		SDA; $V_O < 0$ V or $V_O > V_{DD}$		-	±20	mA
I_{OL}	LOW-level output current	continuous; I/O port		-	50	mA
		continuous; SDA, $\overline{INT}$		-	25	mA
I_{OH}	HIGH-level output current	continuous; P port		-	25	mA
I_{DD}	supply current			-	160	mA
I_{SS}	ground supply current			-	200	mA
P_{tot}	total power dissipation			-	200	mW
T_{stg}	storage temperature			–65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	125	°C

[1] The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

10. Recommended operating conditions

Table 12. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		1.65	5.5	V
V_{IH}	HIGH-level input voltage	SCL, SDA, $\overline{RESET}$	$0.7 \times V_{DD}$	5.5	V
		A0, A1, P port	$0.7 \times V_{DD}$	5.5	V
V_{IL}	LOW-level input voltage	SCL, SDA, $\overline{RESET}$	–0.5	$0.3 \times V_{DD}$	V
		A0, A1, P port	–0.5	$0.3 \times V_{DD}$	V
I_{OH}	HIGH-level output current	P port	-	10	mA
I_{OL}	LOW-level output current	P port	-	25	mA
T_{amb}	ambient temperature	operating in free air	–40	+85	°C

11. Thermal characteristics

Table 13. Thermal characteristics

Symbol	Parameter	Conditions		Max	Unit
$Z_{th(j-a)}$	transient thermal impedance from junction to ambient	HVQFN16 package	[1]	53	K/W
		TSSOP16 package	[1]	108	K/W

[1] The package thermal impedance is calculated in accordance with JESD 51-7.

12. Static characteristics

Table 14. Static characteristics

T_{amb} = −40 °C to +85 °C; V_{DD} = 1.65 V to 5.5 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{IK}	input clamping voltage	I_I = −18 mA		−1.2	-	-	V
V_{POR}	power-on reset voltage	$V_I = V_{DD}$ or V_{SS}; I_O = 0 mA		-	1.1	1.4	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 1.65 V to 5.5 V					
		SDA		3	-	-	mA
		$\overline{INT}$		3	15[2]	-	mA
		P port					
		V_{OL} = 0.5 V; V_{DD} = 1.65 V	[3]	8	10	-	mA
		V_{OL} = 0.7 V; V_{DD} = 1.65 V	[3]	10	13	-	mA
		V_{OL} = 0.5 V; V_{DD} = 2.3 V	[3]	8	10	-	mA
		V_{OL} = 0.7 V; V_{DD} = 2.3 V	[3]	10	13	-	mA
		V_{OL} = 0.5 V; V_{DD} = 3.0 V	[3]	8	14	-	mA
		V_{OL} = 0.7 V; V_{DD} = 3.0 V	[3]	10	19	-	mA
		V_{OL} = 0.5 V; V_{DD} = 4.5 V	[3]	8	17	-	mA
		V_{OL} = 0.7 V; V_{DD} = 4.5 V	[3]	10	24	-	mA
V_{OH}	HIGH-level output voltage	P port					
		I_{OH} = −8 mA; V_{DD} = 1.65 V	[4]	1.2	-	-	V
		I_{OH} = −10 mA; V_{DD} = 1.65 V	[4]	1.1	-	-	V
		I_{OH} = −8 mA; V_{DD} = 2.3 V	[4]	1.8	-	-	V
		I_{OH} = −10 mA; V_{DD} = 2.3 V	[4]	1.7	-	-	V
		I_{OH} = −8 mA; V_{DD} = 3.0 V	[4]	2.6	-	-	V
		I_{OH} = −10 mA; V_{DD} = 3.0 V	[4]	2.5	-	-	V
		I_{OH} = −8 mA; V_{DD} = 4.75 V	[4]	4.1	-	-	V
		I_{OH} = −10 mA; V_{DD} = 4.75 V	[4]	4.0	-	-	V
I_I	input current	V_{DD} = 1.65 V to 5.5 V					
		SCL, SDA, $\overline{RESET}$; $V_I = V_{DD}$ or V_{SS}		-	-	0.1	µA
		A0, A1; $V_I = V_{DD}$ or V_{SS}		-	-	±1	µA
I_{IH}	HIGH-level input current	P port; $V_I = V_{DD}$; V_{DD} = 1.65 V to 5.5 V		-	-	1	µA
I_{IL}	LOW-level input current	P port; $V_I = V_{SS}$; V_{DD} = 1.65 V to 5.5 V		-	-	1	µA

Table 14. Static characteristics *...continued*

T_{amb} = −40 °C to +85 °C; V_{DD} = 1.65 V to 5.5 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{DD}	supply current	SDA, P port, A0, A1, $\overline{RESET}$; V_I on SDA, $\overline{RESET}$ = V_{DD} or V_{SS}; V_I on P port and A0, A1, A2 = V_{DD}; I_O = 0 mA; I/O = inputs; f_{SCL} = 400 kHz				
		V_{DD} = 3.6 V to 5.5 V	-	10	25	µA
		V_{DD} = 2.3 V to 3.6 V	-	6.5	15	µA
		V_{DD} = 1.65 V to 2.3 V	-	4	9	µA
		SCL, SDA, P port, A0, A1, $\overline{RESET}$; V_I on SCL, SDA, $\overline{RESET}$ = V_{DD} or V_{SS}; V_I on P port and A0, A1, A2 = V_{DD}; I_O = 0 mA; I/O = inputs; f_{SCL} = 0 kHz				
		V_{DD} = 3.6 V to 5.5 V	-	1.5	7	µA
		V_{DD} = 2.3 V to 3.6 V	-	1	3.2	µA
		V_{DD} = 1.65 V to 2.3 V	-	0.5	1.7	µA
ΔI_{DD}	additional quiescent supply current	SCL, SDA, $\overline{RESET}$; one input at V_{DD} − 0.6 V, other inputs at V_{DD} or V_{SS}; V_{DD} = 1.65 V to 5.5 V	-	-	25	µA
		P port, A0, A1, $\overline{RESET}$; one input at V_{DD} − 0.6 V, other inputs at V_{DD} or V_{SS}; V_{DD} = 1.65 V to 5.5 V	-	-	80	µA
C_i	input capacitance	V_I = V_{DD} or V_{SS}; V_{DD} = 1.65 V to 5.5 V	-	6	7	pF
C_{io}	input/output capacitance	$V_{I/O}$ = V_{DD} or V_{SS}; V_{DD} = 1.65 V to 5.5 V	-	7	8	pF
		$V_{I/O}$ = V_{DD} or V_{SS}; V_{DD} = 1.65 V to 5.5 V	-	7.5	8.5	pF

[1] For I_{DD}, all typical values are at nominal supply voltage (1.8 V, 2.5 V, 3.3 V, 3.6 V or 5 V V_{DD}) and T_{amb} = 25 °C. Except for I_{DD}, the typical values are at V_{DD} = 3.3 V and T_{amb} = 25 °C.

[2] Typical value for T_{amb} = 25 °C. V_{OL} = 0.4 V and V_{DD} = 3.3 V. Typical value for V_{DD} < 2.5 V, V_{OL} = 0.6 V.

[3] Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.

[4] The total current sourced by all I/Os must be limited to 85 mA.

12.1 Typical characteristics

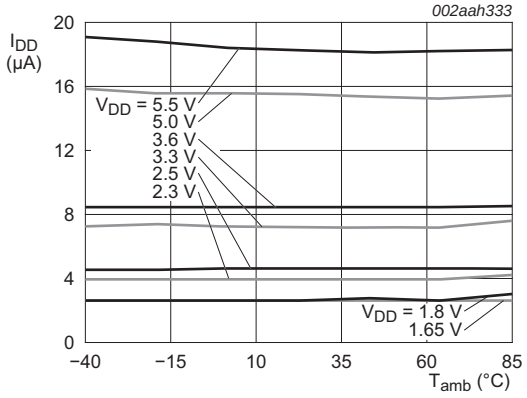


Fig 19. Supply current versus ambient temperature

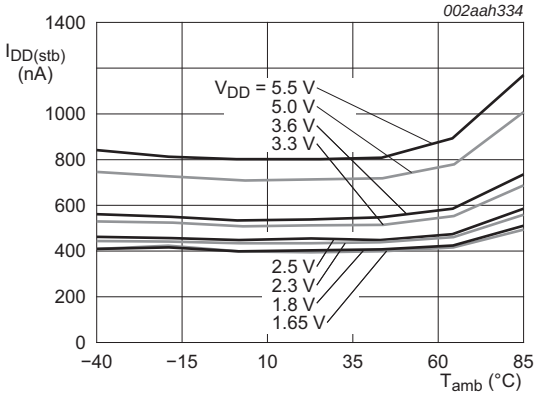
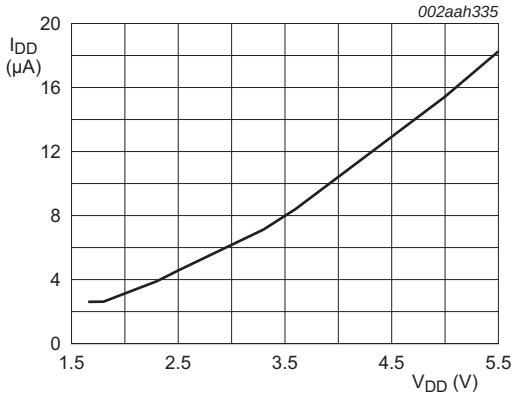
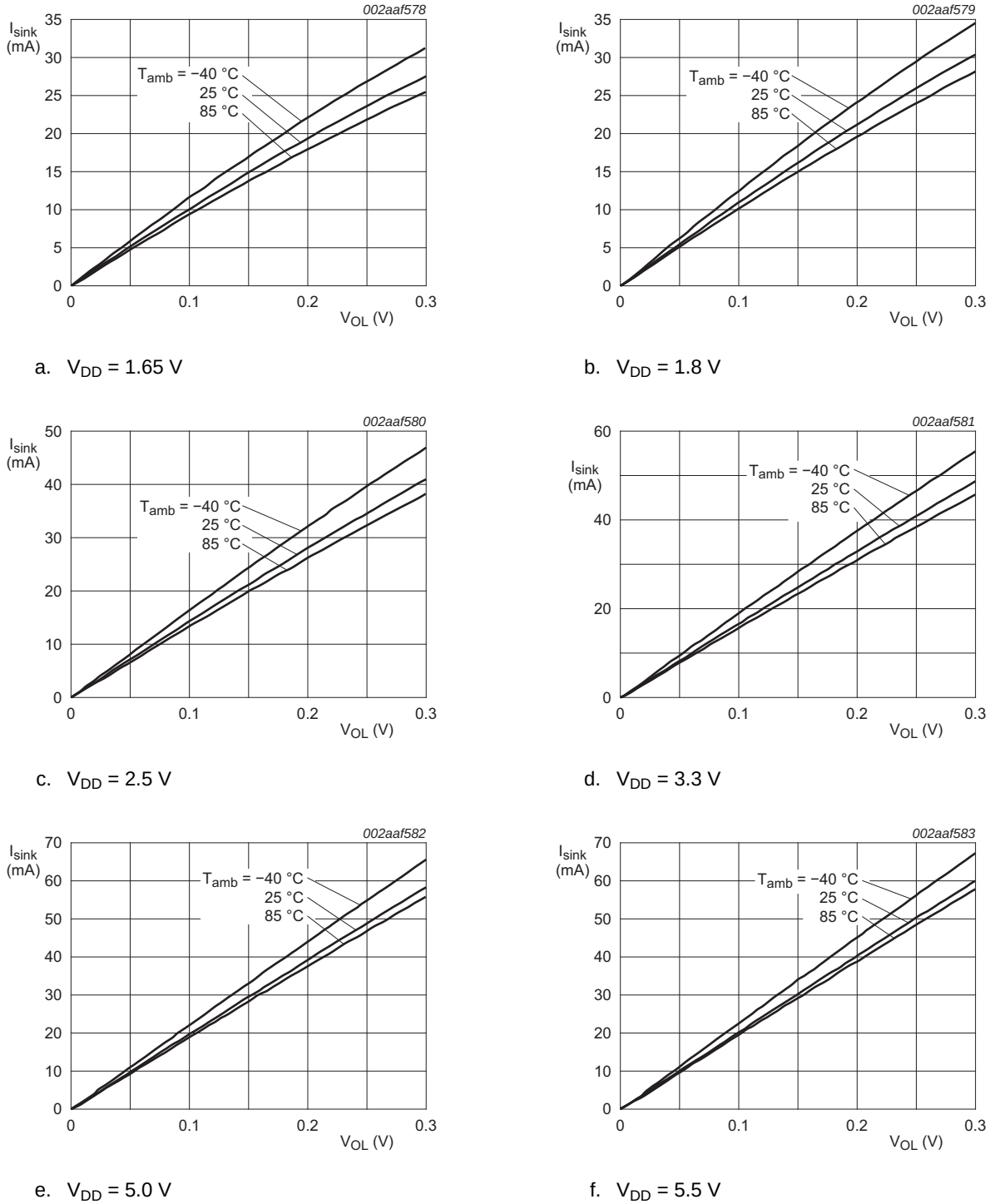


Fig 20. Standby supply current versus ambient temperature



T_{amb} = 25 °C

Fig 21. Supply current versus supply voltage



a. V_{DD} = 1.65 V

b. V_{DD} = 1.8 V

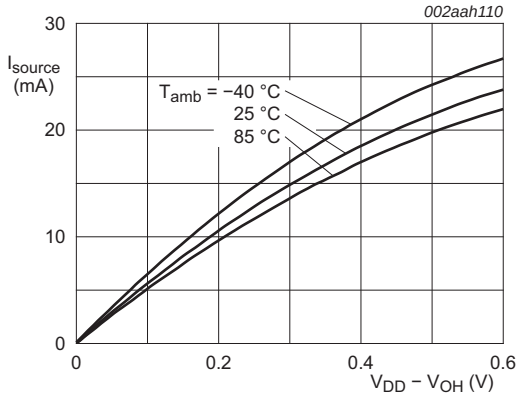
c. V_{DD} = 2.5 V

d. V_{DD} = 3.3 V

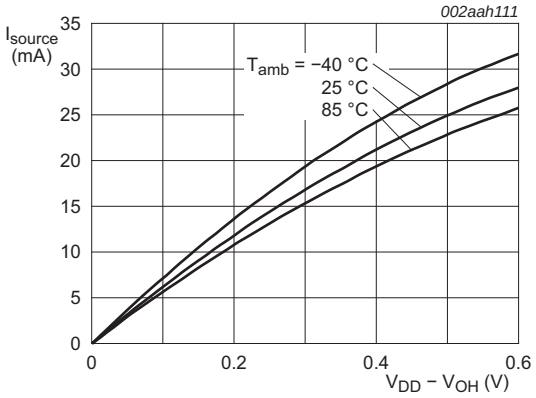
e. V_{DD} = 5.0 V

f. V_{DD} = 5.5 V

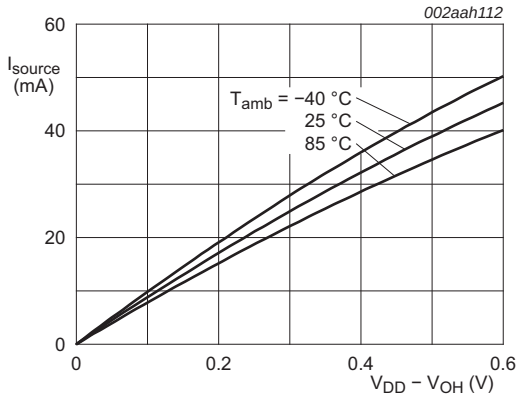
Fig 22. I/O sink current versus LOW-level output voltage



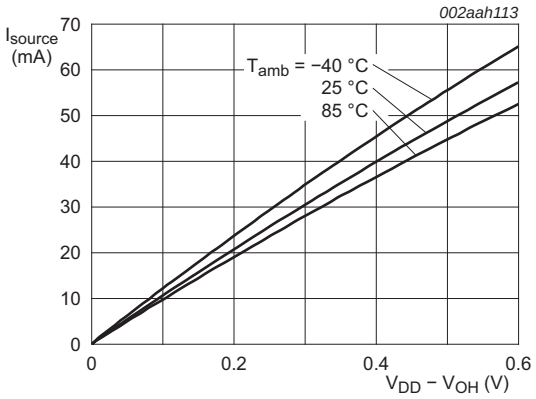
a. V_{DD} = 1.65 V



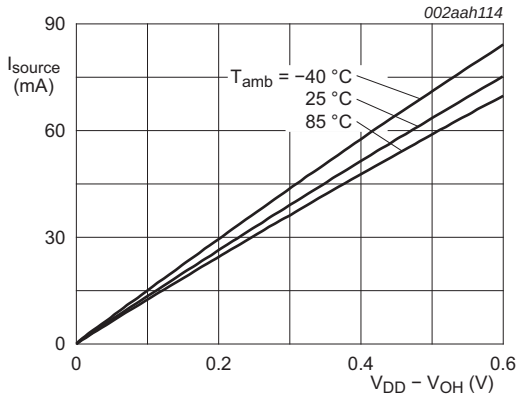
b. V_{DD} = 1.8 V



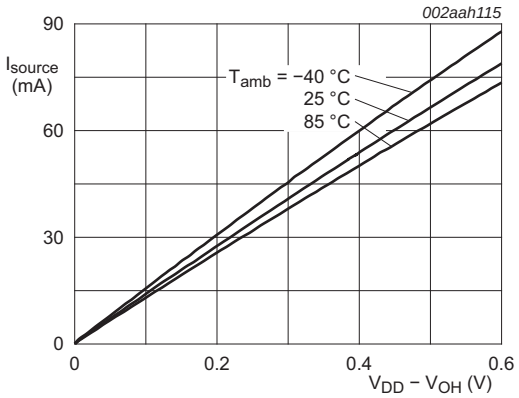
c. V_{DD} = 2.5 V



d. V_{DD} = 3.3 V

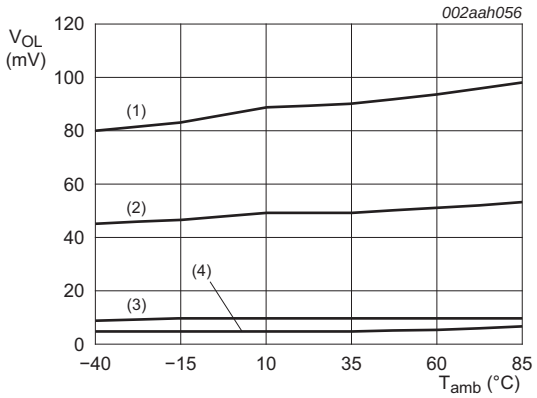


e. V_{DD} = 5.0 V



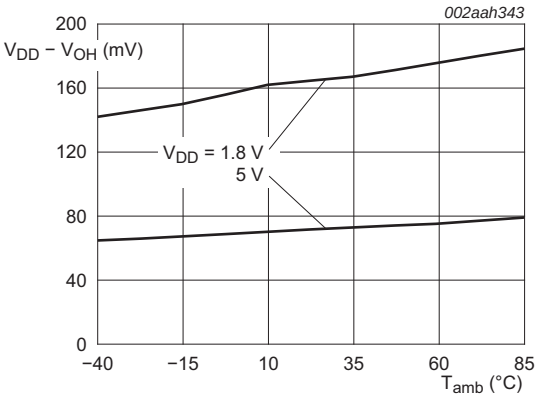
f. V_{DD} = 5.5 V

Fig 23. I/O source current versus HIGH-level output voltage



(1) V_{DD} = 1.8 V; I_{sink} = 10 mA
(2) V_{DD} = 5 V; I_{sink} = 10 mA
(3) V_{DD} = 1.8 V; I_{sink} = 1 mA
(4) V_{DD} = 5 V; I_{sink} = 1 mA

Fig 24. LOW-level output voltage versus temperature



I_{source} = −10 mA

Fig 25. I/O high voltage versus temperature

13. Dynamic characteristics

Table 15. I²C-bus interface timing requirements

Over recommended operating free air temperature range, unless otherwise specified. See Figure 26.

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{HIGH}	HIGH period of the SCL clock		4	-	0.6	-	µs
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	µs
t_{SP}	pulse width of spikes that must be suppressed by the input filter		0	50	0	50	ns
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
$t_{HD;DAT}$	data hold time		0	-	0	-	ns
t_r	rise time of both SDA and SCL signals		-	1000	20	300	ns
t_f	fall time of both SDA and SCL signals		-	300	$20 \times (V_{DD} / 5.5\ V)$	300	ns
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4	-	0.6	-	µs
$t_{VD;DAT}$	data valid time	SCL LOW to SDA output valid	-	3.45	-	0.9	µs
$t_{VD;ACK}$	data valid acknowledge time	ACK signal from SCL LOW to SDA (out) LOW	-	3.45	-	0.9	µs

Table 16. Reset timing requirements

Over recommended operating free air temperature range, unless otherwise specified. See Figure 29.

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
			Min	Max	Min	Max	
$t_{w(rst)}$	reset pulse width		30	-	30	-	ns
$t_{rec(rst)}$	reset recovery time		200	-	200	-	ns
t_{rst}	reset time	[1]	600	-	600	-	ns

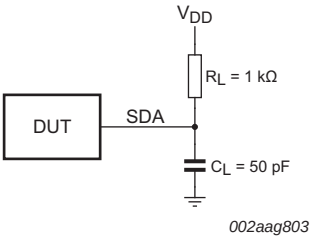
[1] Minimum time for SDA to become HIGH or minimum time to wait before doing a START.

Table 17. Switching characteristics

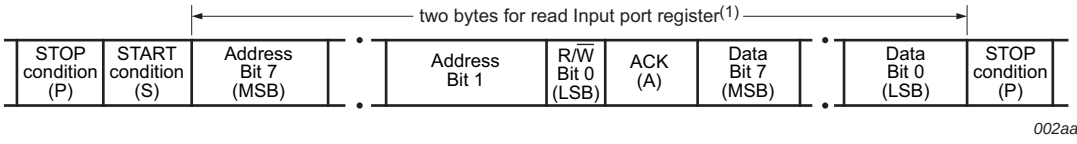
Over recommended operating free air temperature range; $C_L \leq 100$ pF; unless otherwise specified. See Figure 26.

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
			Min	Max	Min	Max	
$t_{v(INT)}$	valid time on pin $\overline{INT}$	from P port to $\overline{INT}$	-	1	-	1	µs
$t_{rst(INT)}$	reset time on pin $\overline{INT}$	from SCL to $\overline{INT}$	-	1	-	1	µs
$t_{v(Q)}$	data output valid time	from SCL to P port	-	400	-	400	ns
$t_{su(D)}$	data input set-up time	from P port to SCL	0	-	0	-	ns
$t_{h(D)}$	data input hold time	from P port to SCL	300	-	300	-	ns

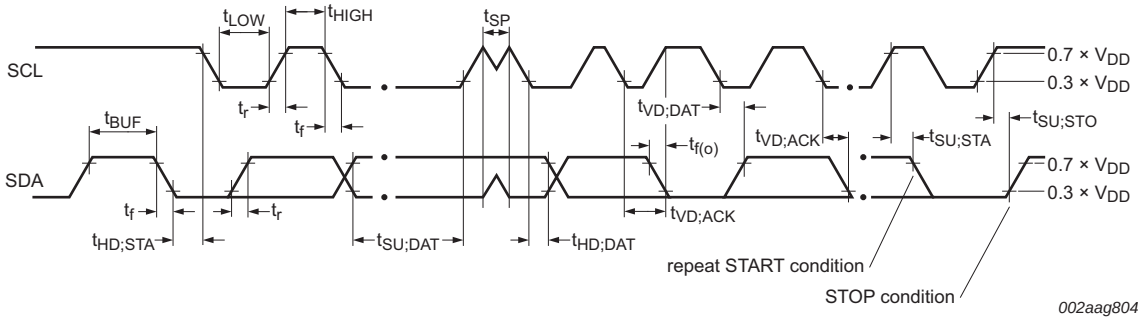
14. Parameter measurement information



a. SDA load configuration



b. Transaction format



c. Voltage waveforms

C_L includes probe and jig capacitance.

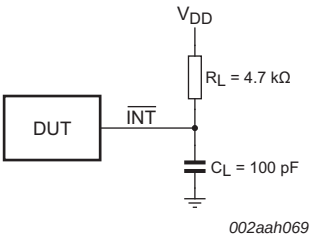
All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; $t_r/t_f \leq 30$ ns.

All parameters and waveforms are not applicable to all devices.

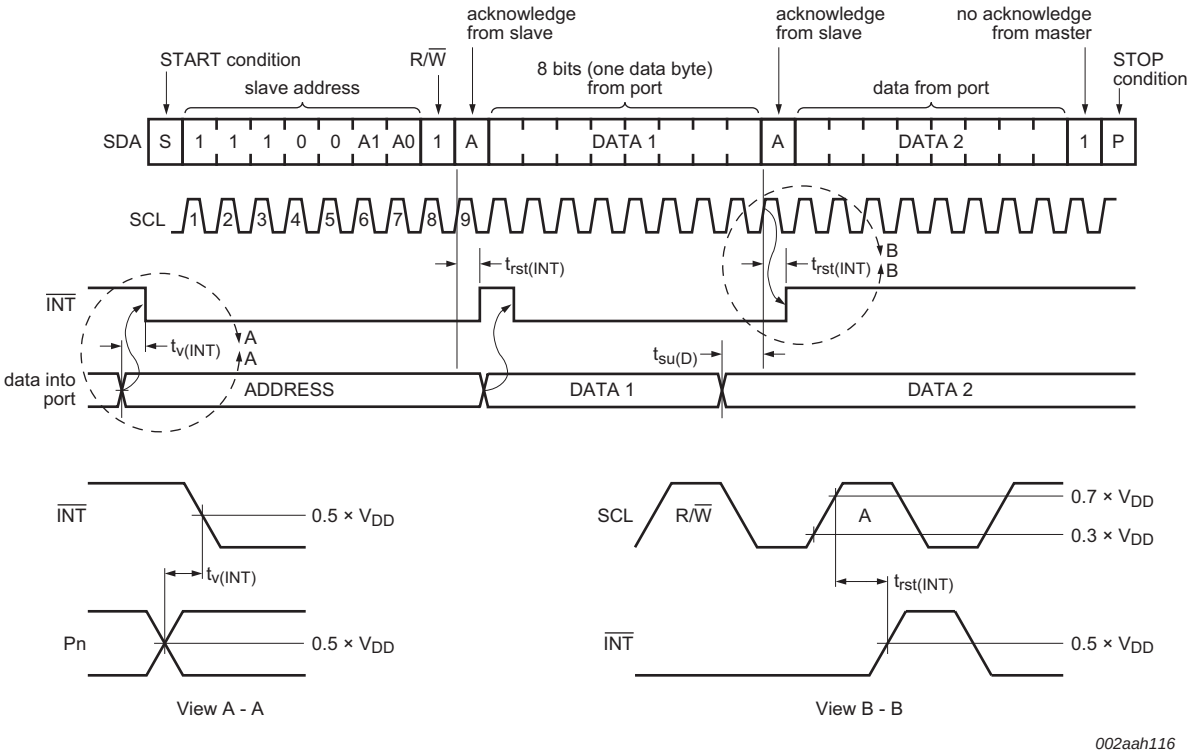
Byte 1 = I²C-bus address; Byte 2, byte 3 = P port data.

(1) See Figure 9.

Fig 26. I²C-bus interface load circuit and voltage waveforms



a. Interrupt load configuration



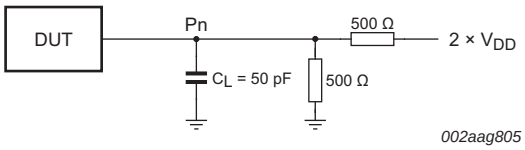
b. Voltage waveforms

C_L includes probe and jig capacitance.

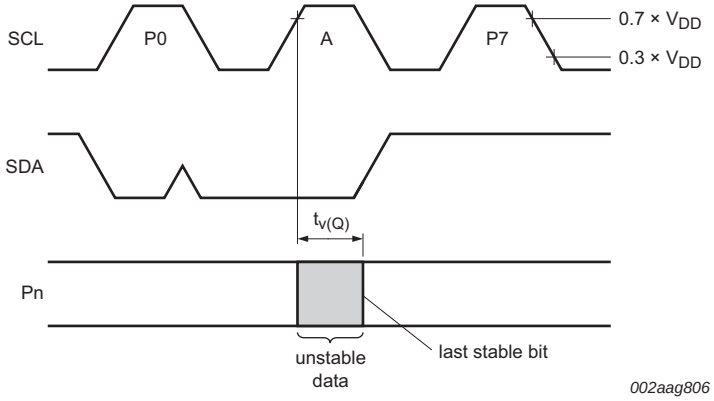
All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

All parameters and waveforms are not applicable to all devices.

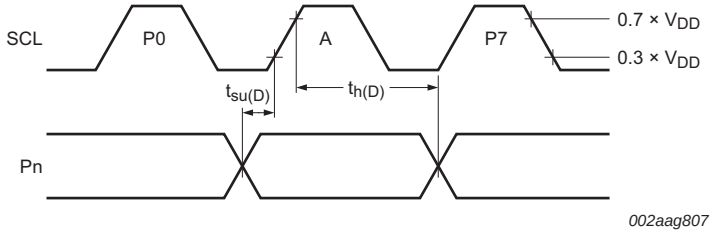
Fig 27. Interrupt load circuit and voltage waveforms



a. P port load configuration



b. Write mode (R/$\overline{W}$ = 0)



c. Read mode (R/$\overline{W}$ = 1)

C_L includes probe and jig capacitance.

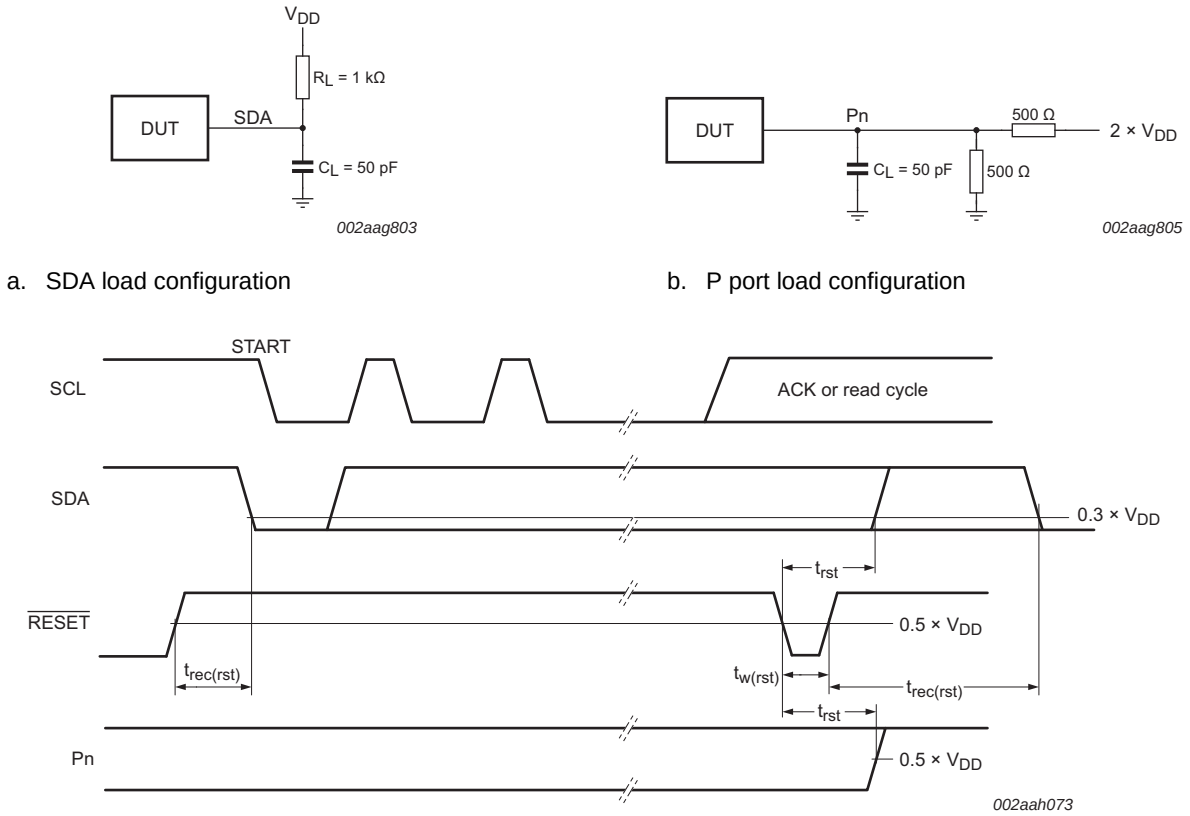
$t_{v(Q)}$ is measured from 0.7 × V_{DD} on SCL to 50 % I/O (Pn) output.

All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

The outputs are measured one at a time, with one transition per measurement.

All parameters and waveforms are not applicable to all devices.

Fig 28. P port load circuit and voltage waveforms



c. $\overline{\text{RESET}}$ timing

C_L includes probe and jig capacitance.

All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

The outputs are measured one at a time, with one transition per measurement.

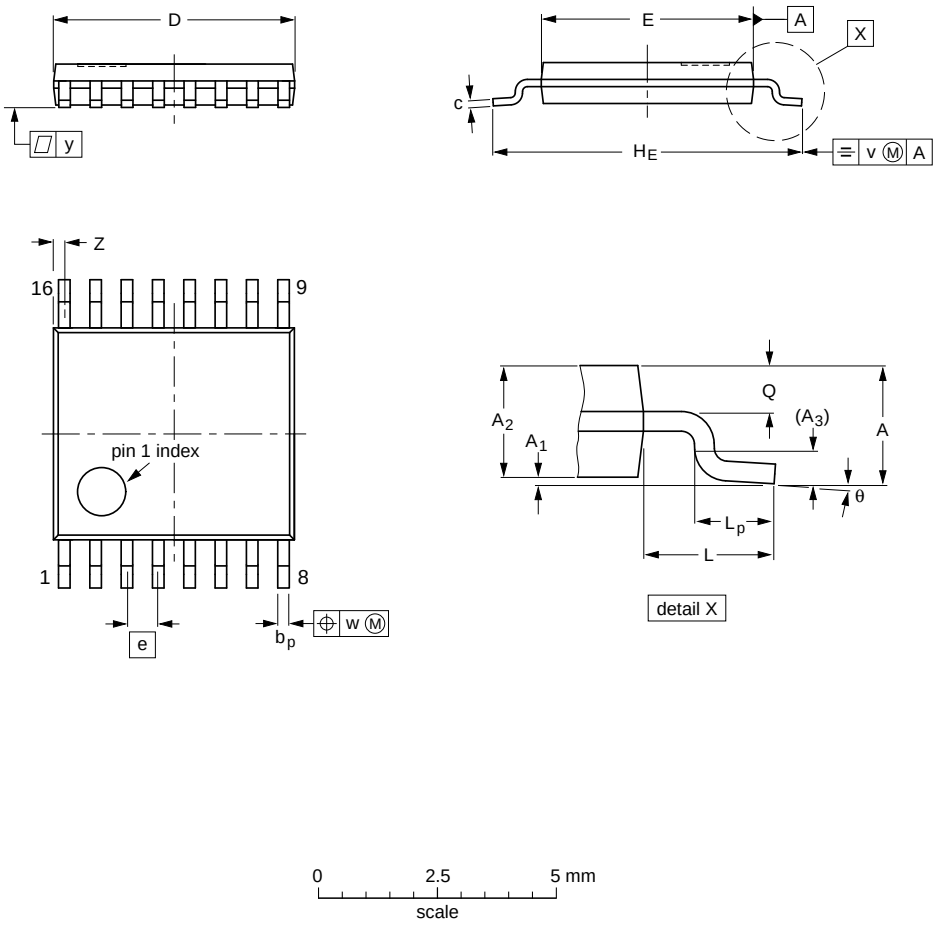
I/Os are configured as inputs.

All parameters and waveforms are not applicable to all devices.

Fig 29. Reset load circuits and voltage waveforms

15. Package outline

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

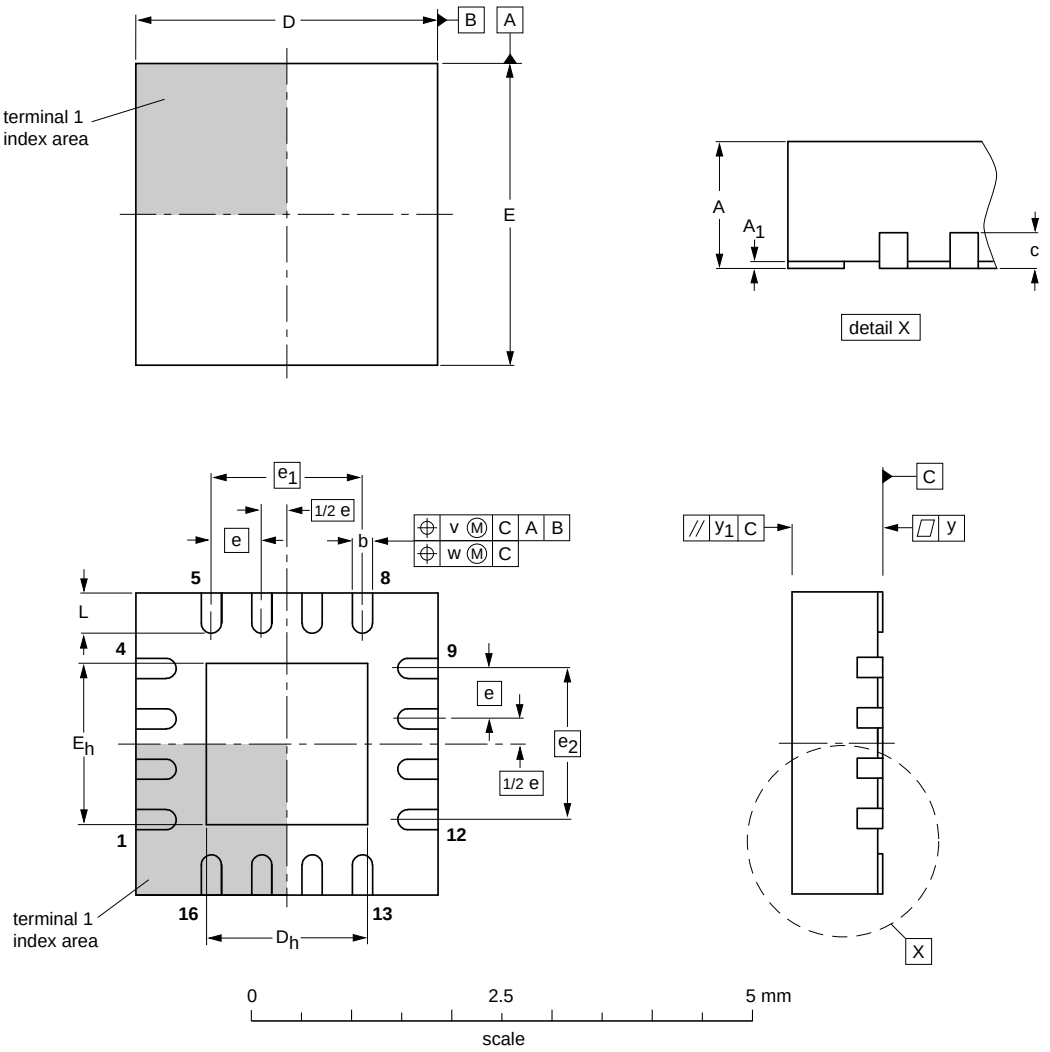
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 30. Package outline SOT403-1 (TSSOP16)

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 x 3 x 0.85 mm **SOT758-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.75 1.45	3.1 2.9	1.75 1.45	0.5	1.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT758-1	- - -	MO-220	- - -			~~02-03-25~~ 02-10-21

Fig 31. Package outline SOT758-1 (HVQFN16)

16. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

17. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 32) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 18 and 19

Table 18. SnPb eutectic process (from J-STD-020C)

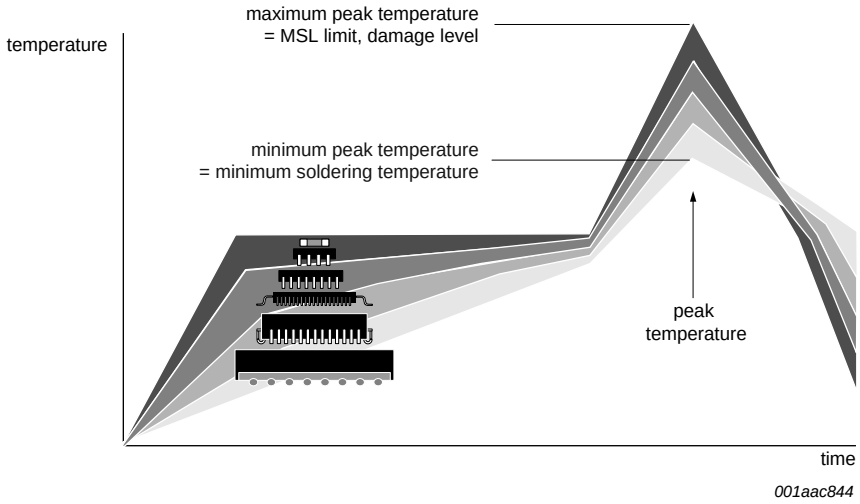
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 19. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 32.



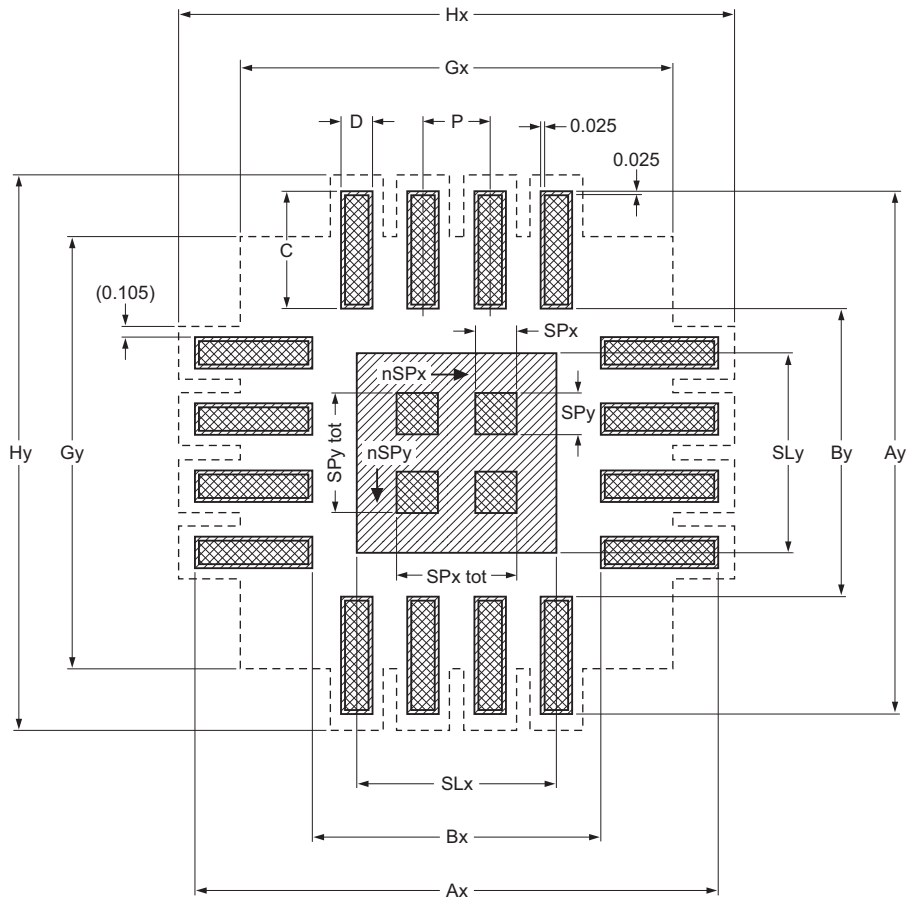
MSL: Moisture Sensitivity Level

Fig 32. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

18. Soldering: PCB footprints

Footprint information for reflow soldering of HVQFN16 package **SOT758-1**



solder land

solder paste deposit

solder land plus solder paste

occupied area

nSPx	nSPy
2	2

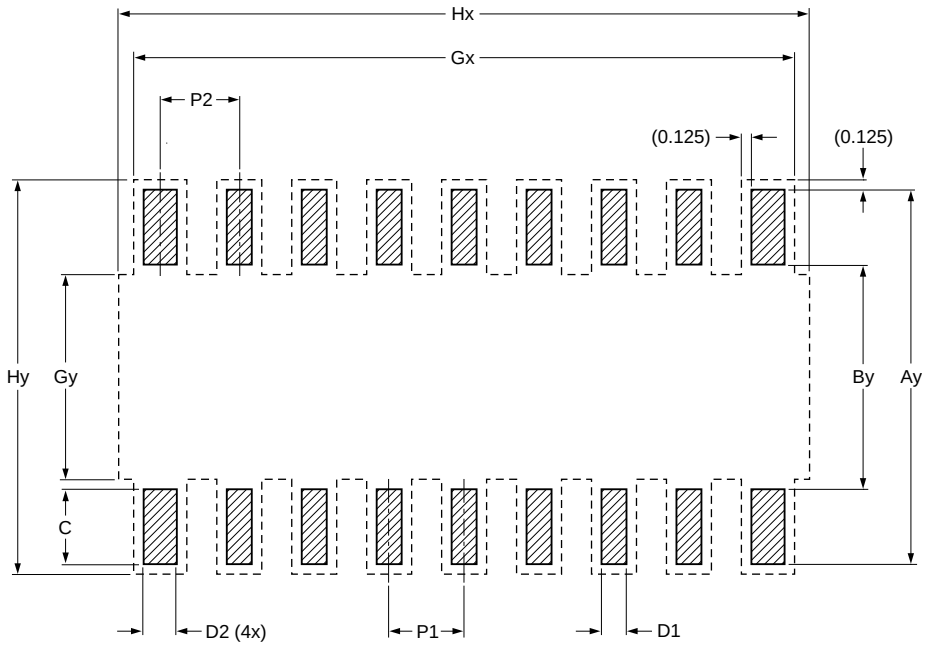
Dimensions in mm

P	Ax	Ay	Bx	By	C	D	SLx	SLy	SPx tot	SPy tot	SPx	SPy	Gx	Gy	Hx	Hy
0.50	4.00	4.00	2.20	2.20	0.90	0.24	1.50	1.50	0.90	0.90	0.30	0.30	3.30	3.30	4.25	4.25

Issue date ~~12-03-07~~ 12-03-08 *sot758-1_fr*

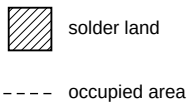
Fig 33. PCB footprint for SOT758-1 (HVQFN16); reflow soldering

Footprint information for reflow soldering of TSSOP16 package **SOT403-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout



DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	5.600	5.300	5.800	7.450

sot403-1_fr

Fig 34. PCB footprint for SOT403-1 (TSSOP16); reflow soldering

19. Abbreviations

Table 20. Abbreviations

Acronym	Description
ACPI	Advanced Configuration and Power Interface
CBT	Cross-Bar Technology
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
FF	Flip-Flop
GPIO	General Purpose Input/Output
HBM	Human Body Model
I^2C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LED	Light Emitting Diode
LP	Low-Pass
LSB	Least Significant Bit
MSB	Most Significant Bit
PCB	Printed-Circuit Board
POR	Power-On Reset
PRR	Pulse Repetition Rate
SCR	Silicon Controlled Rectifier
SMBus	System Management Bus

20. Revision history

Table 21. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9538A v.1	20120928	Product data sheet	-	-

21. Legal information

21.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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