

# CBTL02043A; CBTL02043B

3.3 V, 2 differential channel, 2 : 1 multiplexer/demultiplexer switch

Rev. 4.1 — 30 March 2015

Product data sheet

## 1. General description

CBTL02043A/B is a 2 differential channel, 2-to-1 multiplexer/demultiplexer switch for USB 3.1, PCI Express Generation 3, or other high-speed serial interface applications. The CBTL02043A/B can switch two differential signals to one of two locations. Using a unique design technique, NXP has minimized the impedance of the switch such that the attenuation observed through the switch is negligible, and also minimized the channel-to-channel skew as well as channel-to-channel crosstalk, as required by the high-speed serial interface. CBTL02043A/B allows expansion of existing high-speed ports for extremely low power.

The device's pinouts are optimized to match different application layouts. CBTL02043A has input and output pins on the opposite of the package, and is suitable for edge connector(s) with different signal sources on the motherboard. CBTL02043B has outputs on both sides of the package, and the device can be placed between two connectors to multiplex differential signals from a controller. Please refer to [Section 8](#) for layout examples.

## 2. Features and benefits

- 2 bidirectional differential channel, 2 : 1 multiplexer/demultiplexer
- High-speed signal switching for 10 Gbps applications
- High bandwidth: 10 GHz at –3 dB
- Low insertion loss:
  - ◆ –0.5 dB at 100 MHz
  - ◆ –1.3 dB at 4.0 GHz
- Low return loss: –13.5 dB at 4 GHz
- Low crosstalk: –35 dB at 4 GHz
- Low off-state isolation: –20 dB at 4 GHz
- Low intra-pair skew: 5 ps typical
- Low inter-pair skew: 35 ps maximum
- $V_{DD}$  operating range: 3.3 V  $\pm$  10 %
- Shutdown pin (XSD) for power-saving mode
  - ◆ Standby current less than 1  $\mu$ A
- ESD tolerance:
  - ◆ 2000 V HBM
  - ◆ 1000 V CDM
- DHVQFN20 package



### 3. Applications

- Routing of high-speed differential signals with low signal attenuation
  - ◆ PCIe Gen3
  - ◆ DisplayPort 1.2
  - ◆ USB 3.1
  - ◆ SATA 6 Gbit/s

### 4. Ordering information

**Table 1. Ordering information**

| Type number  | Topside marking | Package  |                                                                                                                                               |          |
|--------------|-----------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------|----------|
|              |                 | Name     | Description                                                                                                                                   | Version  |
| CBTL02043ABQ | TL02043A        | DHVQFN20 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm <sup>[1]</sup> | SOT764-1 |
| CBTL02043BBQ | TL02043B        | DHVQFN20 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm <sup>[1]</sup> | SOT764-1 |

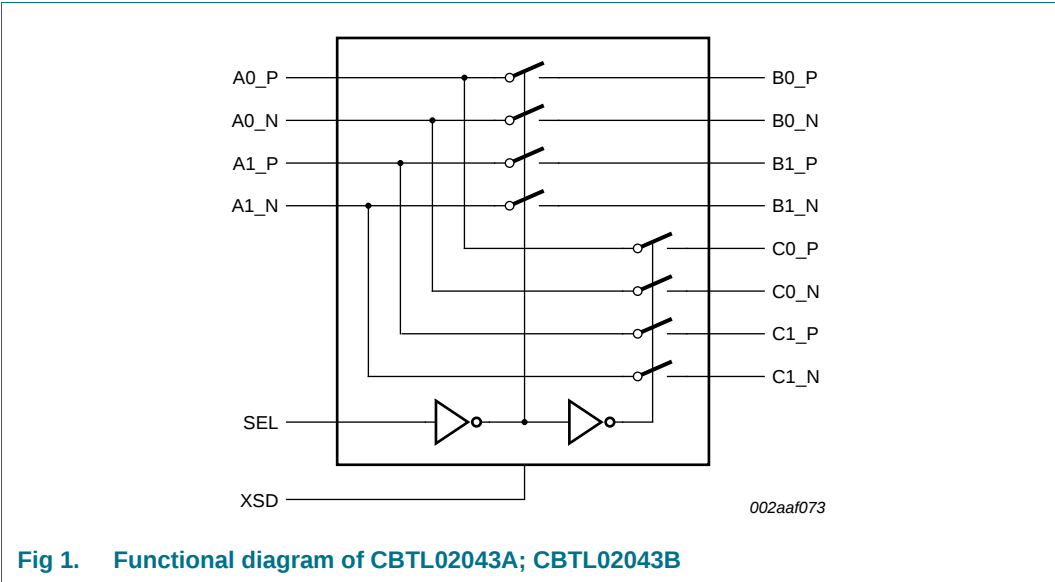
[1] Total height after printed-circuit board mounting = 1.0 mm maximum.

#### 4.1 Ordering options

**Table 2. Ordering options**

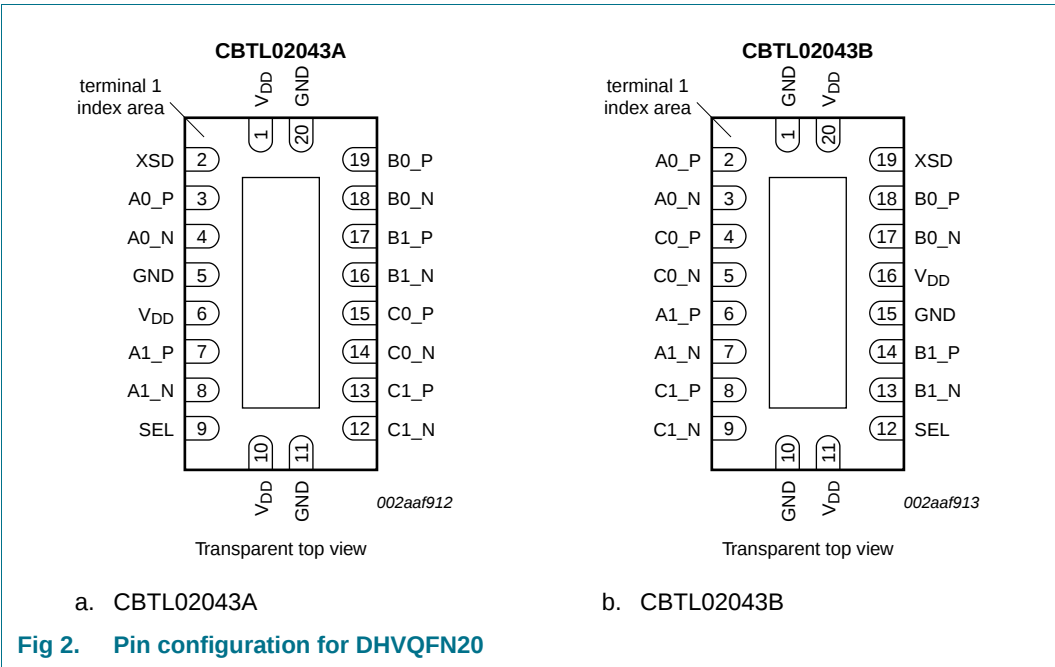
| Type number  | Orderable part number | Package  | Packing method                      | Minimum order quantity | Temperature                         |
|--------------|-----------------------|----------|-------------------------------------|------------------------|-------------------------------------|
| CBTL02043ABQ | CBTL02043ABQ,115      | DHVQFN20 | Reel 7" Q1/T1<br>*standard mark SMD | 3000                   | T <sub>amb</sub> = -40 °C to +85 °C |
| CBTL02043BBQ | CBTL02043BBQ,115      | DHVQFN20 | Reel 7" Q1/T1<br>*standard mark SMD | 3000                   | T <sub>amb</sub> = -40 °C to +85 °C |

5. Functional diagram



6. Pinning information

6.1 Pinning



## 6.2 Pin description

Table 3. Pin description

| Symbol             | Pin                   |                       | Type                    | Description                                                                                                                                                                                                        |
|--------------------|-----------------------|-----------------------|-------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                    | CBTL02043A            | CBTL02043B            |                         |                                                                                                                                                                                                                    |
| A0_P               | 3                     | 2                     | I/O                     | channel 0, port A differential signal input/output                                                                                                                                                                 |
| A0_N               | 4                     | 3                     | I/O                     |                                                                                                                                                                                                                    |
| A1_P               | 7                     | 6                     | I/O                     | channel 1, port A differential signal input/output                                                                                                                                                                 |
| A1_N               | 8                     | 7                     | I/O                     |                                                                                                                                                                                                                    |
| B0_P               | 19                    | 18                    | I/O                     | channel 0, port B differential signal input/output                                                                                                                                                                 |
| B0_N               | 18                    | 17                    | I/O                     |                                                                                                                                                                                                                    |
| B1_P               | 17                    | 14                    | I/O                     | channel 1, port B differential signal input/output                                                                                                                                                                 |
| B1_N               | 16                    | 13                    | I/O                     |                                                                                                                                                                                                                    |
| C0_P               | 15                    | 4                     | I/O                     | channel 0, port C differential signal input/output                                                                                                                                                                 |
| C0_N               | 14                    | 5                     | I/O                     |                                                                                                                                                                                                                    |
| C1_P               | 13                    | 8                     | I/O                     | channel 1, port C differential signal input/output                                                                                                                                                                 |
| C1_N               | 12                    | 9                     | I/O                     |                                                                                                                                                                                                                    |
| SEL                | 9                     | 12                    | CMOS single-ended input | operation mode select<br>SEL = LOW: A ↔ B<br>SEL = HIGH: A ↔ C                                                                                                                                                     |
| XSD                | 2                     | 19                    | CMOS single-ended input | Shutdown pin; should be driven LOW or connected to V <sub>SS</sub> for normal operation. When HIGH, all paths are switched off (non-conducting high-impedance state), and supply current consumption is minimized. |
| V <sub>DD</sub>    | 1, 6, 10              | 11, 16, 20            | power                   | positive supply voltage, 3.3 V (± 10 %)                                                                                                                                                                            |
| GND <sup>[1]</sup> | 5, 11, 20, center pad | 1, 10, 15, center pad | power                   | supply ground                                                                                                                                                                                                      |

- [1] DHVQFN20 package die supply ground is connected to both GND pins and exposed center pad. GND pins and the exposed center pad must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

7. Functional description

Refer to [Figure 1 “Functional diagram of CBTL02043A; CBTL02043B”](#).

7.1 Function selection and shutdown function

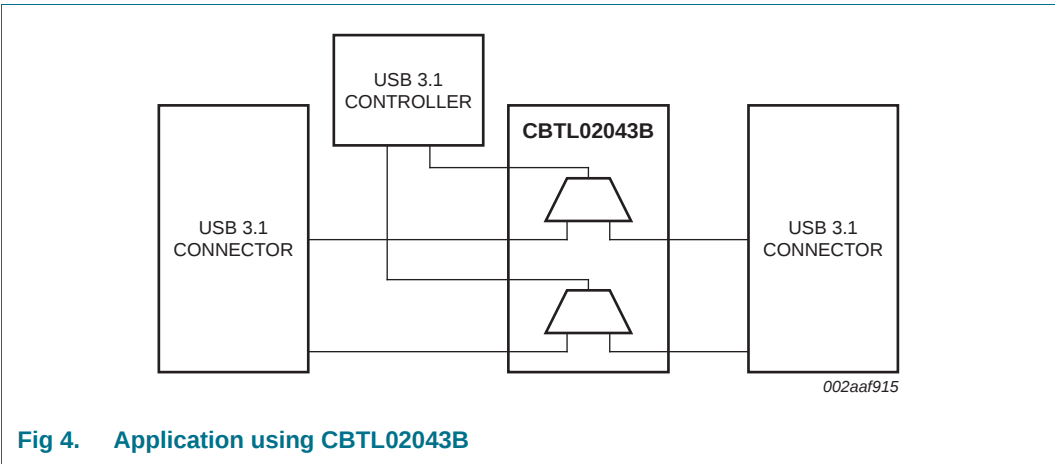
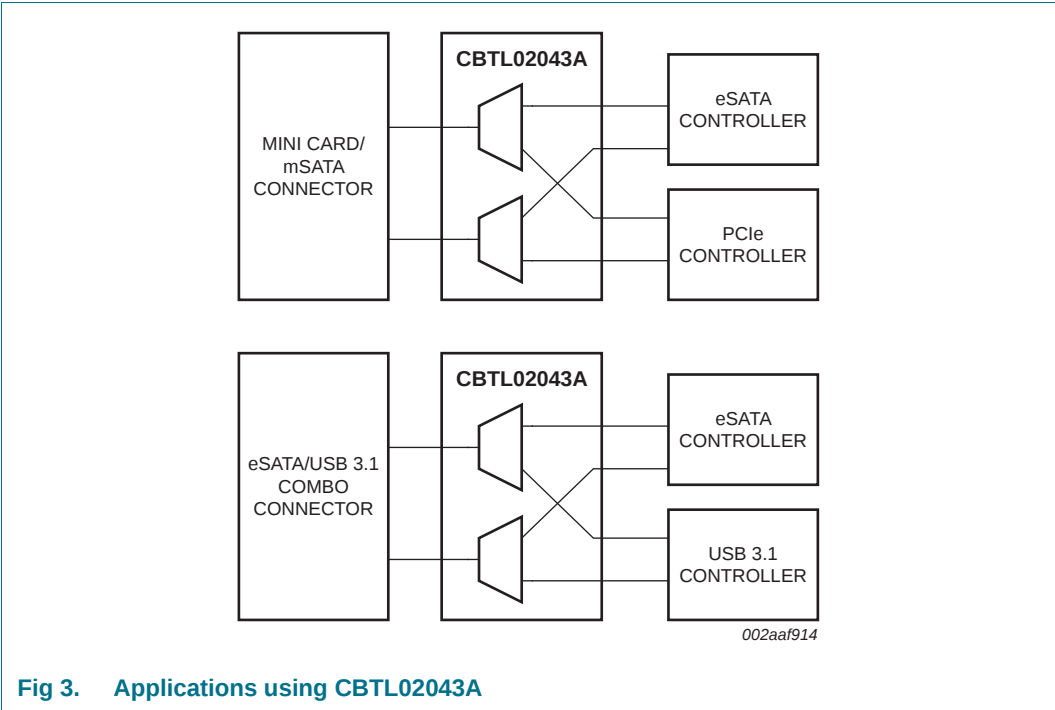
The CBTL02043A/B provides a shutdown function to minimize power consumption when the application is not active, but power to the CBTL02043A/B is provided. The XSD pin (active HIGH) places all channels in high-impedance state (non-conducting) while reducing current consumption to near-zero. When XSD pin is LOW, the device operates normally.

Table 4. Function selection

X = Don't care.

| XSD  | SEL  | Function                      |
|------|------|-------------------------------|
| HIGH | X    | An, Bn and Cn pins are high-Z |
| LOW  | LOW  | An to Bn and vice versa       |
| LOW  | HIGH | An to Cn and vice versa       |

8. Application design-in information



## 9. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol     | Parameter                       | Conditions | Min   | Max  | Unit |
|------------|---------------------------------|------------|-------|------|------|
| $V_{DD}$   | supply voltage                  |            | -0.3  | +4.6 | V    |
| $T_{case}$ | case temperature                |            | -40   | +85  | °C   |
| $T_{stg}$  | storage temperature             |            | -65   | +150 | °C   |
| $V_{ESD}$  | electrostatic discharge voltage | HBM        | [1] - | 2000 | V    |
|            |                                 | CDM        | [2] - | 1000 | V    |

[1] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[2] Charged Device Model: ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged Device Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

## 10. Recommended operating conditions

**Table 6. Recommended operating conditions**

| Symbol    | Parameter           | Conditions            | Min | Typ | Max      | Unit |
|-----------|---------------------|-----------------------|-----|-----|----------|------|
| $V_{DD}$  | supply voltage      |                       | 3.0 | 3.3 | 3.6      | V    |
| $V_I$     | input voltage       |                       | -   | -   | $V_{DD}$ | V    |
| $T_{amb}$ | ambient temperature | operating in free air | -40 | -   | +85      | °C   |

## 11. Static characteristics

**Table 7. Static characteristics**

$V_{DD} = 3.3 \text{ V} \pm 10\%$ ;  $T_{amb} = -40 \text{ °C to } +85 \text{ °C}$ ; unless otherwise specified.

| Symbol   | Parameter                  | Conditions                                            | Min          | Typ <sup>[1]</sup> | Max                    | Unit |
|----------|----------------------------|-------------------------------------------------------|--------------|--------------------|------------------------|------|
| $I_{DD}$ | supply current             | operating mode;<br>$V_{DD} = \text{max.}$ ; XSD = LOW | -            | 1.35               | 2.5                    | mA   |
|          |                            | shutdown mode;<br>$V_{DD} = \text{max.}$ ; XSD = HIGH | -            | -                  | 1                      | μA   |
| $I_{IH}$ | HIGH-level input current   | $V_{DD} = \text{max.}$ ; $V_I = V_{DD}$               | -            | -                  | $\pm 5$ <sup>[2]</sup> | μA   |
| $I_{IL}$ | LOW-level input current    | $V_{DD} = \text{max.}$ ; $V_I = \text{GND}$           | -            | -                  | $\pm 5$ <sup>[2]</sup> | μA   |
| $V_{IH}$ | HIGH-level input voltage   | SEL, XSD pins                                         | $0.65V_{DD}$ | -                  | -                      | V    |
| $V_{IL}$ | LOW-level input voltage    | SEL, XSD pins                                         | -            | -                  | $0.35V_{DD}$           | V    |
| $V_I$    | input voltage              | differential pins                                     | -            | -                  | 2.4                    | V    |
|          |                            | SEL, XSD pins                                         | -            | -                  | $V_{DD}$               | V    |
| $V_{IC}$ | common-mode input voltage  |                                                       | 0            | -                  | 2                      | V    |
| $V_{ID}$ | differential input voltage | peak-to-peak                                          | -            | -                  | 1.6                    | V    |

[1] Typical values are at  $V_{DD} = 3.3 \text{ V}$ ,  $T_{amb} = 25 \text{ °C}$ , and maximum loading.

[2] Input leakage current is  $\pm 50 \text{ μA}$  if differential pairs are pulled to HIGH and LOW.

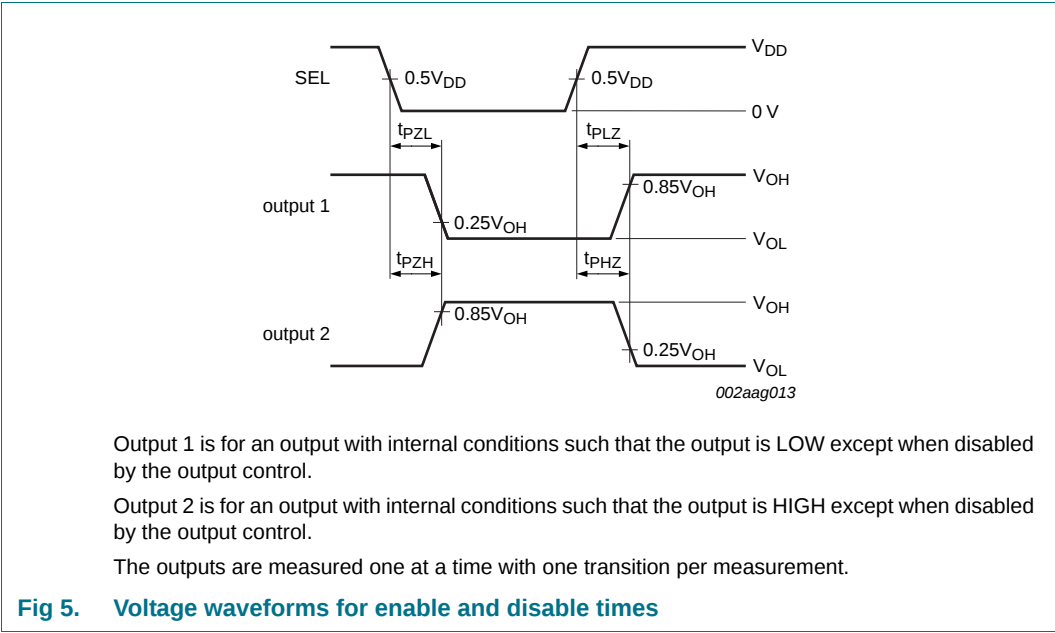
## 12. Dynamic characteristics

**Table 8. Dynamic characteristics**

$V_{DD} = 3.3 \text{ V} \pm 10 \%$ ;  $T_{amb} = -40 \text{ }^{\circ}\text{C}$  to  $+85 \text{ }^{\circ}\text{C}$ ; unless otherwise specified.

| Symbol                           | Parameter                           | Conditions                                                                            | Min | Typ <sup>[1]</sup> | Max | Unit     |
|----------------------------------|-------------------------------------|---------------------------------------------------------------------------------------|-----|--------------------|-----|----------|
| DDIL                             | differential insertion loss         | channel is OFF                                                                        |     |                    |     |          |
|                                  |                                     | f = 4 GHz                                                                             | -   | -20                | -   | dB       |
|                                  |                                     | f = 100 MHz                                                                           | -   | -50                | -   | dB       |
|                                  |                                     | channel is ON                                                                         |     |                    |     |          |
|                                  |                                     | f = 4 GHz                                                                             | -   | -1.3               | -   | dB       |
| DDNEXT                           | differential near-end crosstalk     | adjacent channels are ON                                                              |     |                    |     |          |
|                                  |                                     | f = 4 GHz                                                                             | -   | -35                | -   | dB       |
|                                  |                                     | f = 100 MHz                                                                           | -   | -65                | -   | dB       |
| B <sub>-3dB</sub>                | -3 dB bandwidth                     |                                                                                       | -   | 10                 | -   | GHz      |
| DDRL                             | differential return loss            | f = 4 GHz                                                                             | -   | -13.5              | -   | dB       |
|                                  |                                     | f = 100 MHz                                                                           | -   | -25                | -   | dB       |
| R <sub>on</sub>                  | ON-state resistance                 | $V_{DD} = 3.3 \text{ V}$ ; $V_I = 2 \text{ V}$ ;<br>$I_I = 19 \text{ mA}$             | -   | 6                  | -   | $\Omega$ |
| C <sub>io(on)</sub>              | on-state input/output capacitance   |                                                                                       | -   | 1.5                | -   | pF       |
| t <sub>PD</sub>                  | propagation delay                   | from Port A to Port B, or<br>Port A to Port C, or vice versa                          | -   | 60                 | -   | ps       |
| <b>Switching characteristics</b> |                                     |                                                                                       |     |                    |     |          |
| t <sub>startup</sub>             | start-up time                       | supply voltage valid or<br>XSD going LOW to channel<br>specified operating conditions | -   | -                  | 10  | ms       |
| t <sub>PZH</sub>                 | OFF-state to HIGH propagation delay |                                                                                       | -   | -                  | 300 | ns       |
| t <sub>PZL</sub>                 | OFF-state to LOW propagation delay  |                                                                                       | -   | -                  | 70  | ns       |
| t <sub>PHZ</sub>                 | HIGH to OFF-state propagation delay |                                                                                       | -   | -                  | 50  | ns       |
| t <sub>PLZ</sub>                 | LOW to OFF-state propagation delay  |                                                                                       | -   | -                  | 50  | ns       |
| t <sub>sk(dif)</sub>             | differential skew time              | intra-pair                                                                            | -   | 5                  | -   | ps       |
| t <sub>sk</sub>                  | skew time                           | inter-pair                                                                            | -   | -                  | 35  | ps       |

[1] Typical values are at  $V_{DD} = 3.3 \text{ V}$ ;  $T_{amb} = 25 \text{ }^{\circ}\text{C}$ , and maximum loading.



13. Test information

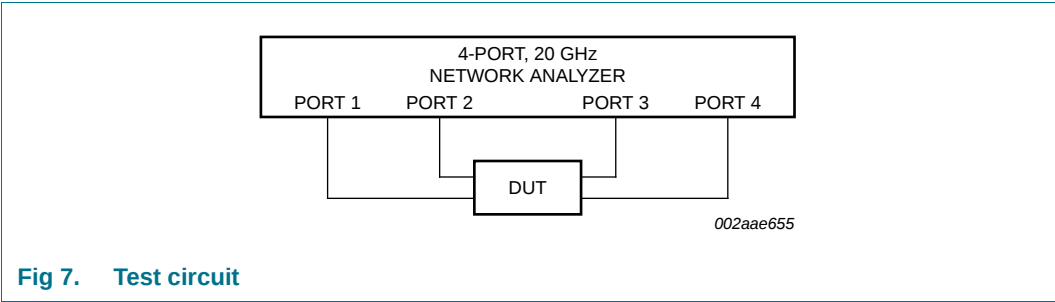
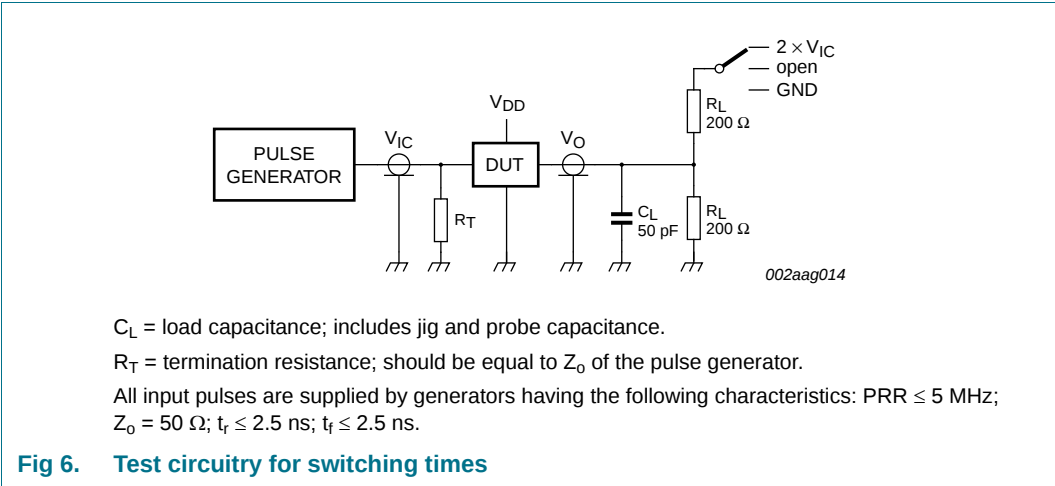


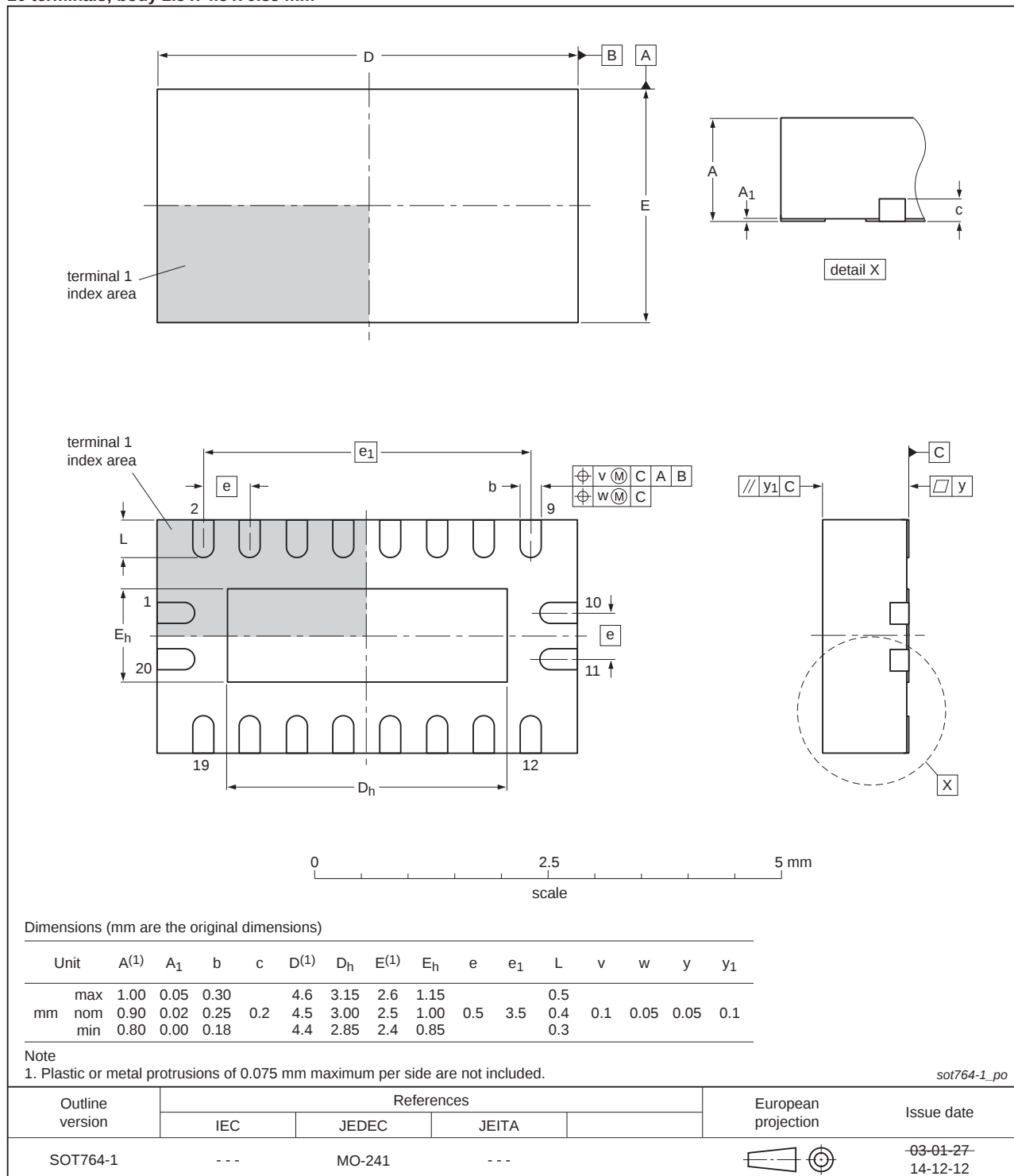
Table 9. Test data

| Test                                     | Load  |              | Switch            |
|------------------------------------------|-------|--------------|-------------------|
|                                          | $C_L$ | $R_L$        |                   |
| $t_{PLZ}$ , $t_{PZL}$ (output on B side) | 50 pF | 200 $\Omega$ | $2 \times V_{IC}$ |
| $t_{PHZ}$ , $t_{PZH}$ (output on B side) | 50 pF | 200 $\Omega$ | GND               |
| $t_{PD}$                                 | -     | 200 $\Omega$ | open              |

## 14. Package outline

**DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm**

**SOT764-1**



**Fig 8. Package outline SOT764-1 (DHVQFN20)**

## 15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note AN10365 "Surface mount reflow soldering description".

### 15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leadless or leaded SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 9](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 10](#) and [11](#)

**Table 10. SnPb eutectic process (from J-STD-020D)**

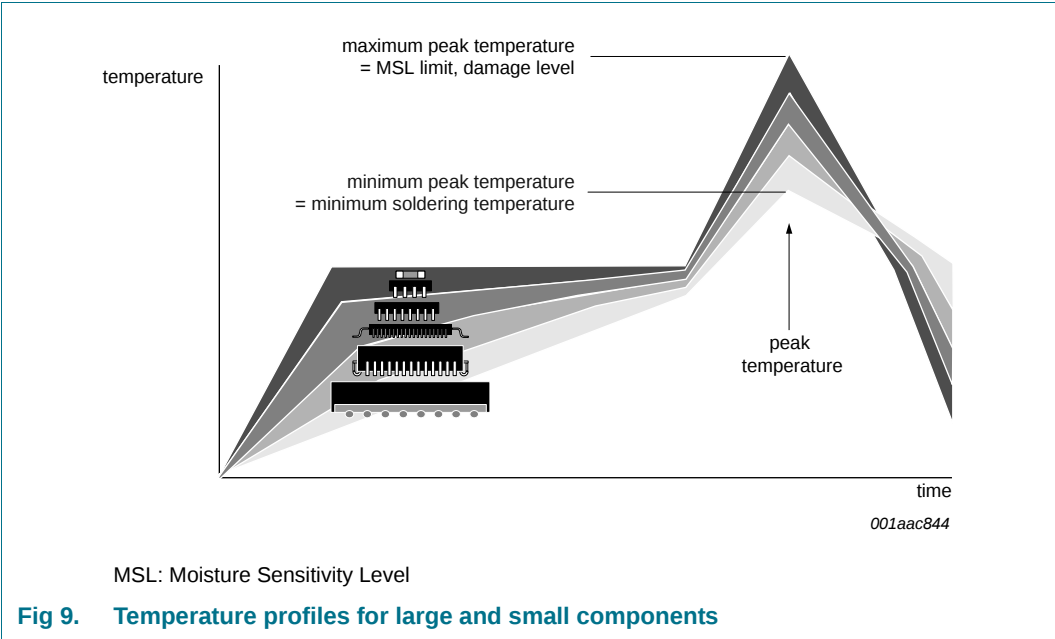
| Package thickness (mm) | Package reflow temperature (°C) |       |
|------------------------|---------------------------------|-------|
|                        | Volume (mm <sup>3</sup> )       |       |
|                        | < 350                           | ≥ 350 |
| < 2.5                  | 235                             | 220   |
| ≥ 2.5                  | 220                             | 220   |

**Table 11. Lead-free process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) |             |        |
|------------------------|---------------------------------|-------------|--------|
|                        | Volume (mm <sup>3</sup> )       |             |        |
|                        | < 350                           | 350 to 2000 | > 2000 |
| < 1.6                  | 260                             | 260         | 260    |
| 1.6 to 2.5             | 260                             | 250         | 245    |
| > 2.5                  | 250                             | 245         | 245    |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 9](#).

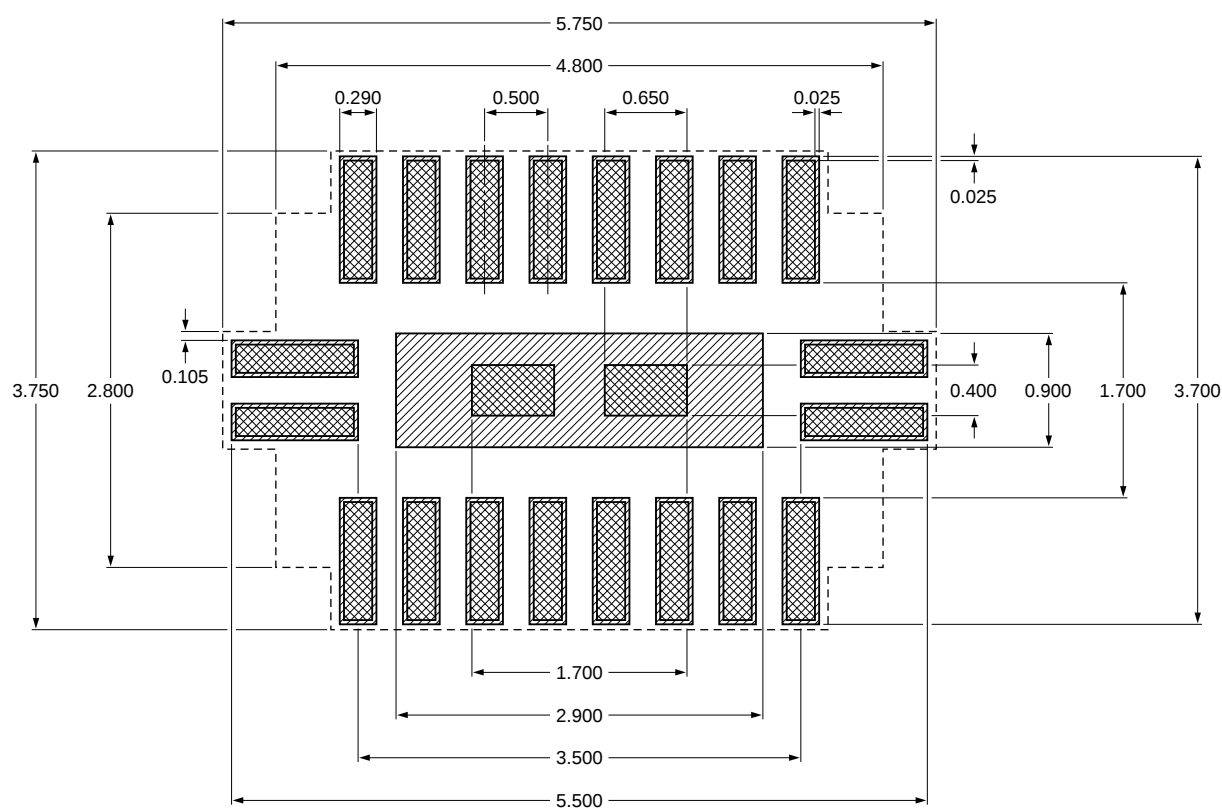


For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 16. Soldering: PCB footprints

### Footprint information for reflow soldering of DHVQFN20 package

**SOT764-1**



Refer to the package outline drawing for actual layout

-  solder land  
 solder paste deposit  
 solder land plus solder paste  
 - - - - occupied area

**Fig 10. PCB footprint for SOT764-1 (DHVQFN20); reflow soldering**

## 17. Abbreviations

Table 12. Abbreviations

| Acronym | Description                           |
|---------|---------------------------------------|
| CDM     | Charged-Device Model                  |
| DUT     | Device Under Test                     |
| ESD     | ElectroStatic Discharge               |
| HBM     | Human Body Model                      |
| I/O     | Input/Output                          |
| PCI     | Peripheral Component Interconnect     |
| PCIe    | PCI Express                           |
| PRR     | Pulse Repetition Rate                 |
| SATA    | Serial Advanced Technology Attachment |
| USB     | Universal Serial Bus                  |

## 18. Revision history

Table 13. Revision history

| Document ID                 | Release date                                | Data sheet status  | Change notice | Supersedes                |
|-----------------------------|---------------------------------------------|--------------------|---------------|---------------------------|
| CBTL02043A_CBTL02043B v.4.1 | 20150330                                    | Product data sheet | -             | CBTL02043A_CBTL02043B v.4 |
| Modifications:              | • Changed "USB 3.0" to "USB 3.1" throughout |                    |               |                           |
| CBTL02043A_CBTL02043B v.4   | 20141219                                    | Product data sheet | -             | CBTL02043A_CBTL02043B v.3 |
| CBTL02043A_CBTL02043B v.3   | 20130305                                    | Product data sheet | -             | CBTL02043A_CBTL02043B v.2 |
| CBTL02043A_CBTL02043B v.2   | 20111110                                    | Product data sheet | -             | CBTL02043A_CBTL02043B v.1 |
| CBTL02043A_CBTL02043B v.1   | 20110310                                    | Product data sheet | -             | -                         |

## 19. Legal information

### 19.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition                                                                            |
|-----------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 19.2 Definitions

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