

# MAX16550

## Integrated Protection IC on 12V Bus with an Integrated MOSFET, Lossless Current Sensing, and PMBus Interface

### General Description

The MAX16550 is a protection IC with an integrated low-resistance MOSFET and lossless current-sense circuitry featuring SMBus/PMBus™ control and reporting. This IC is designed to provide the optimum solution for distribution, control, monitoring and protection of the system's 12V power supply. An internal LDO provides the supply voltage for the protection IC.

If no fault is detected, the IC initiates the startup and has been designed to provide controlled, monotonic startup. Programmable soft-start ramp and delay is implemented to limit the in-rush current during startup.

The IC monitors the current and voltage of the 12V system power rail and provides multiple levels of protection with fast turn-off if a fault is detected.

Maxim's patented, lossless current sense provides high accuracy current sensing over load and temperature, improving overall system-energy efficiency, and reducing dissipation.

Output voltage is monitored at all times. If at any time the output voltage falls below the programmable output undervoltage-lockout threshold, the PWRGD signal is asserted low. If at any time the input voltage falls below the programmable input undervoltage-lockout threshold, the PWRGD signal is asserted low. The IC can be programmed through PMBus to provide input overvoltage protection. Input overvoltage protection is disabled by default. When enabled through PMBus, if the input voltage exceeds a programmable overvoltage threshold, the MOSFET is latched off and a fault indicated.

*PMBus is a trademark of SMIF, Inc.*

**Ordering Information** appears at end of data sheet.

### Benefits and Features

- MAX16550—30A Protection ICn
- High-Density (4mm x 4.5mm for 30A): Less than 25% of the Board Area of Conventional Solutions
  - Monolithic Integration of Power, Control, and Monitoring
  - Integrated Power MOSFET with 1.9mΩ Total Resistance in 12V Power Path ( $R_{DS(ON)}$  Including Package)
  - Integrated Lossless, Precise Current Sensing
  - Integrated LDO Provides  $V_{DD}$  Supply (1.8V Bias Supply)
- Enables Advanced System Power Management—PMBus/SMBus Telemetry with Extensive Status Monitoring and Reporting
  - Load Current Indicator (ILOAD) Pin Provides Analog Output Current Reporting with High Accuracy
  - Programmable Soft-Start for Inrush Current Limiting
  - Increases Power-Supply Reliability with IC Self-Protection Features
    - Very Fast Fault Detection and Isolation
    - $V_{IN}$  to  $V_{OUT}$  Short Protection During Startup
    - Overtemperature Protection
  - Three Levels of Overcurrent Protection
    - Programmable Moderate OCP
    - Programmable Severe OCP Provides Isolation < 5μs.
    - Fail-Safe Safe OCP Provides Isolation < 250ns.

### Additional Features

- Programmable Soft-Start and Delay
- Programmable Input Undervoltage-Lockout Threshold (UVLO)
- Programmable Power-Good Threshold
- PWRGD Pin for Output UVLO/Input UVLO Reporting
- FAULT Pin for Fault Reporting

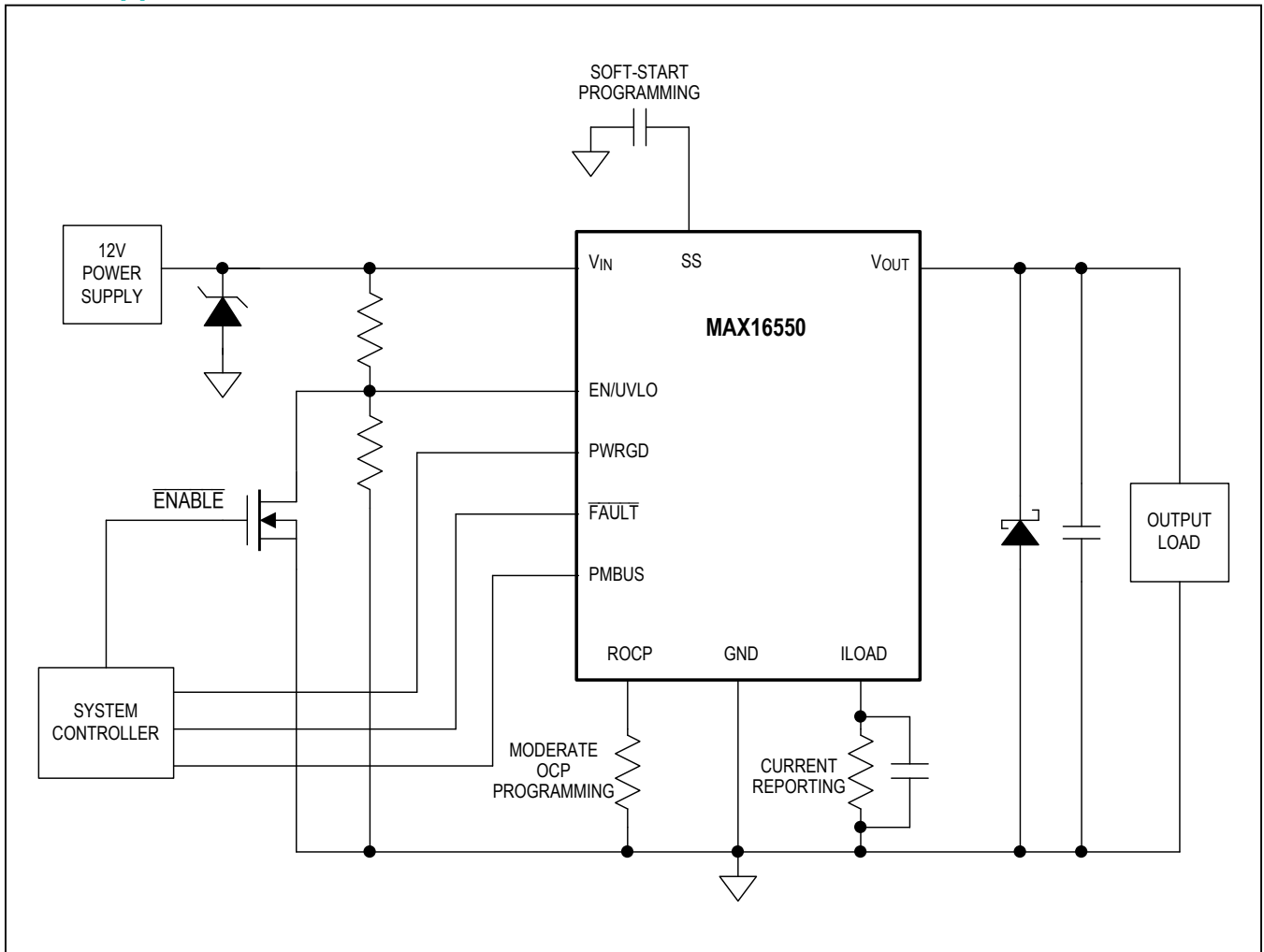
### Systems and Applications

Servers, Networking, Storage, Communication Equipment and AC/DC Power Supplies

- Integrated Protection IC on 12V
  - Circuit Breaker/E-Fuse, Hot Swap



Basic Application Circuit



# MAX16550

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## Absolute Maximum Ratings (Note 1)

Supply Voltage ( $V_{IN}$ ) DC	-0.3V to +16V	ILOAD	-0.3V to +2.5V
Supply Voltage ( $V_{IN}$ ) 150 $\mu$ s	22V	Output Voltage ( $V_{OUT}$ ) DC	-0.3V to +16V
Bias Supply Voltage ( $V_{DD}$ )	-0.3V to +2.5V	BST (Relative to $V_{OUT}$ )	-0.3V to +2.5V
PWRGD, FAULT	-0.3V to +5.5V	SS	-0.3V to +16V
EN/UVLO, R <sub>OCP</sub>	-0.3V to +2.5V	Junction Temperature ( $T_J$ )	150°C
SMBUS_CLK, SMBUS_DATA, SMBUS_ALERT	6V	Storage Temperature Range	-65°C to +165°C
SMBUS_ID	-0.3V to +2.5V	Peak Reflow Temperature	260°C

## Operating Ratings

Supply Voltage ( $V_{IN}$ )	10.8V to 13.2V	Junction Temperature ( $T_J$ )	0°C to +125°C
Bias Supply Voltage ( $V_{DD}$ )	1.76V to 1.94V		

## Package Thermal Characteristics

Junction-to-Case Thermal Resistance ( $\theta_{JC, max}$ ).....0.31°C/W

**Note 1:** These products are completely Halogen-free and Pb-free, employing special materials sets: molding compounds/die attach materials and 100% matte tin plate including anneal. These products are RoHS compliant with an -e3 termination finish and are compatible with both SnPb and Pb-free soldering operations. These products are MSL classified at peak reflow temperatures that meet JEDEC JSTD-020.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Information

<b>PACKAGE TYPE: 18 FCQFN</b>	
Package Code	P184A4F+1
Outline Number	<a href="#">21-1080</a>
Land Pattern Number	<a href="#">90-0529</a>
<b>THERMAL RESISTANCE</b>	
Junction to Case ( $\theta_{JC}$ )	0.31°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

# MAX16550

## Integrated Protection IC on 12V Bus with an Integrated MOSFET, Lossless Current Sensing, and PMBus Interface

### Electrical Characteristics

( $V_{IN} = 12V \pm 10\%$ , unless otherwise noted.  $T_J = 0^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Specifications are 100% production tested at  $T_A = +32^\circ C$ . Limits over operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>12V SUPPLY (<math>V_{IN}</math>)</b>						
Supply Voltage Range	$V_{IN}$		10.8	12	13.2	V
Device Supply Current	$I_{IN}$	FET off	3.0		6.25	mA
		FET on: $I_{OUT} = 0$ (Note 2)	3.7		6.75	
		FET on: $I_{OUT} = 30A$ (Note 2)			10	
<b>INTEGRATED 1.8V LINEAR REGULATOR</b>						
LDO Output Voltage Range	$V_{DD}$		1.76	1.85	1.94	V
$V_{DD}$ Falling		(Note 2)	1.55	1.6	1.7	
$V_{DD}$ Rising		(Note 2)	1.62	1.67	1.73	
Hysteresis		(Note 2)	30	60	80	mV
$V_{DD}$ UVLO Response Time		(Note 2)		2		$\mu s$
<b>UNDERVOLTAGE LOCKOUT: 12V SUPPLY (<math>V_{IN}</math>)</b>						
$V_{IN\_UVLO}$ Rising Threshold	$V_{IN\_UVLO}$	At EN/UVLO pin	0.95	1	1.05	V
$V_{IN\_UVLO}$ Hysteresis				50		
Programmable 12V $V_{IN}$ Undervoltage Threshold for Rising Input	$V_{IN\_UVLO}$	Programmable through resistor-divider, measured at $V_{IN}$	8			V
Response Time	$t_D$	From EN/UVLO = 0V to FET off		2		$\mu s$
<b>EN_ UVLO PIN INTERNAL PARAMETERS</b>						
EN_ UVLO Pin Leakage		EN_ UVLO = 1.8V	5	6.7	11	$\mu A$
EN_ UVLO Internal Pulldown Resistor			110	250	450	k $\Omega$
<b>BOOST VOLTAGE (<math>V_{BST}</math>)</b>						
$V_{BST}$ Charging Time to 1.6V Above $V_{OUT}$	$t_{CHARGE}$	$C_{BST} = 100nF$		150		$\mu s$
BST Voltage Above $V_{OUT}$	$V_{BST}$			1.8		V
Rising UVLO Threshold Above $V_{OUT}$	BOOST UVLO	(Note 2)	0.8	1.2	1.6	V
Falling UVLO Threshold Above $V_{OUT}$		(Note 2)	0.74	1.1	1.5	
UVLO Hysteresis		(Note 2)	60	130	400	mV
Falling Lockout Response Time	$t_D$			1.5		$\mu s$
<b>INTEGRATED MOSFET CHARACTERISTICS</b>						
On-Resistance	$R_{DS(ON)}$	(Note 2)		1.9		m $\Omega$

# MAX16550

## Integrated Protection IC on 12V Bus with an Integrated MOSFET, Lossless Current Sensing, and PMBus Interface

### Electrical Characteristics (continued)

( $V_{IN} = 12V \pm 10\%$ , unless otherwise noted.  $T_J = 0^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Specifications are 100% production tested at  $T_A = +32^\circ C$ . Limits over operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>COMMON OVERCURRENT PROTECTION</b>						
Severe OCP Threshold, % Above Moderate OCP	$I_{OCP(SEVERE)}$	Digitally programmable	130			%
Severe OCP Threshold Accuracy			170			
Severe OCP Delay	$t_{D(SEVERE)}$	From fault threshold exceeded to FET off (Note 3)	5			$\mu s$
Gain from ROCP Pin Current	$G_{OCP}$	(Note 2)	4			A/ $\mu A$
Allowed Range for No-Fault Detection	ROCP		28		360	k $\Omega$
Startup OCP Threshold	$I_{OCP\_STARTUP}$	Programmed through PMBus default setting = 8A (Note 2)	4			A
Startup OCP Threshold Accuracy			8			
			12			
			16			
Startup OCP Threshold Accuracy		$I_{OUT} = 4A$ $I_{OUT} = 8A, 12A, 16A$	$\pm 30$			%
Safe OCP Threshold	$I_{OCP\_SAFE}$	(Note 2)	60			A
Safe OCP Threshold Accuracy		$V_{IN} = 12V, T = +125^\circ C$	$\pm 20$			%
Safe OCP Delay	$t_{D\_SAFE}$	From fault threshold exceeded to FET off	250			ns
<b>OVERCURRENT PROTECTION (MAX16550)</b>						
Gain from ROCP Pin Current	$G_{OCP}$	Gain from ROCP pin current to $I_{OUT}$ (Note 2)	4			A/ $\mu A$
Moderate OCP Voltage Threshold	$V_{OCPM}$	Referred to voltage over ROCP (Note 2)	0.8			V
Moderate OCP Voltage Threshold Accuracy		Referred to $I_{OUT}$ using Equation 1	$\pm 12$			%
Moderate OCP Threshold Range	$I_{OCP(MODERATE)}$	Analog programmable through ROCP	15		35	A
Allowable ROCP Range for ROCP_Fault Detection at Power-Up	ROCP		28		360	k $\Omega$
Moderate OCP Timeout	$t_{OCPM}$	$I_{OUT} > moderate\ OCP,$ $I_{OUT} < severe\ OCP,$ programmable default moderate OCP timeout = 100 $\mu s$ (Note 3)	12.5			$\mu s$
			100			$\mu s$
			100			ms
			250			ms
Moderate OCP Fault-Detect Delay Timeout Accuracy		(Note 3)	$\pm 10$			%
<b>SOFT-START AND <math>C_{OUT}</math></b>						
Soft-Start Discharge Resistance	SS			1	2	k $\Omega$

**Electrical Characteristics (continued)**

( $V_{IN} = 12V \pm 10\%$ , unless otherwise noted.  $T_J = 0^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Specifications are 100% production tested at  $T_A = +32^\circ C$ . Limits over operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Soft-Start Charging Current	$I_{SS}$		20		39	$\mu A$	
Soft-Start Capacitor Value Range	$C_{SS}$	Linear startup ramp	0		75	nF	
Soft-Start Time	$t_{SS}$	$C_{SS} = 0nF$ , $I_{OUT} = 0A$ (Note 3)		1		ms	
Soft-Start Capacitor Discharge Threshold			0.17	0.2	0.25	V	
CSS Discharge Check Duration During Startup		(Note 3)		2.2		s	
Recommended Output Capacitance Range	$C_{OUT}$	(Note 2)	10		10000	$\mu F$	
<b>FET <math>V_{GS}</math> UNDERVOLTAGE LOCKOUT</b>							
$V_{GS}$ Rising UVLO Threshold	$V_{GS\_UVLO}$		0.87	1.3	1.61	V	
$V_{GS}$ Falling UVLO Threshold			0.74	1.17	1.50		
$V_{GS}$ UVLO Hysteresis			87	100	466	mV	
$V_{GS}$ UVLO Masking Time		During startup (Note 3)			100	ms	
$V_{GS}$ UVLO Deglitching		(Note 3)			10	$\mu s$	
<b>PASS FET SHORT DETECTION DURING STARTUP</b>							
Duration of $V_{OUT}$ Discharge Check	$t_{DISCHARGE}$	(Note 3)		2.2		s	
Pulldown Resistance on $V_{OUT}$ During Self-Check	$R_{DISCHARGE}$		400	455	560	$\Omega$	
Threshold for Self-Check Procedure	$V_{OUT\_SELF\_CHECK}$	SMBus/PMBus programmable, default 9V (Note 2)	5.8 6.8 7.7 8.8	6 7 8 9	6.2 7.2 8.2 9.4	V	
Delay from Self-Check Pass to Start $V_{OUT}$ Ramp	$t_D$	Programmable (Note 3)		0 10 20		$\mu s$	
<b>PWRGD PIN</b>							
Max Allowable PWRGD Output High Voltage	$V_{OH}$	External pullup leakage below $1\mu A$		5.5		V	
PWRGD Output Low Voltage	$V_{OL}$	Sinking 4mA			0.4	V	
Propagation Delay from $V_{OUT\_UVLO}$ Detect to PWRGD Pin Asserted Low	$t_D$	(Note 3)		3.2		$\mu s$	
Threshold for PWRGD Asserted High	$V_{TH(PWRGD)}$	SMBus/PMBus programmable, default 11V (Note 2)		8 9 10 11		V	
PWRGD Clear Timing Time Needed to Clear PWRGD after $V_{OUT}$ Has Reached $V_{IN}$		(Note 3)			5		ms
PWRGD Hysteresis		(Note 2)		0.35	0.5	0.63	V

**Electrical Characteristics (continued)**

( $V_{IN} = 12V \pm 10\%$ , unless otherwise noted.  $T_J = 0^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Specifications are 100% production tested at  $T_A = +32^\circ C$ . Limits over operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWRGD Accuracy			-5		+5	%
<b>OVERTEMPERATURE PROTECTION</b>						
Overtemperature-Protection Threshold	$T_{OTP}$	PMBus programmable (Note 2)		140		$^\circ C$
<b>SMBus DATA (SMBUS_DATA) AND CLOCK (SMBUS_CLOCK) PINS</b>						
Leakage Current		For pullup = 5.5V (Note 2)		5.3		$\mu A$
Input Low Voltage	$V_{IL}$				0.8	V
Input High Voltage	$V_{IH}$		2.1			V
Output Low Voltage	$V_{OL}$	SMBUS_DATA, sinking 4mA			0.4	V
Max Allowable External Pullup Voltage	$V_{OH\ MAX}$			5.5		V
<b>SMBus ALERT PIN</b>						
Output Low Voltage	$V_{OL}$	Sinking 4mA			0.4	V
Leakage Current		For pullup = 5.5V (Note 2)			1	$\mu A$
Max Allowable External Pullup Voltage	$V_{OH\ MAX}$			5.5		V
<b>FAULT-ISOLATION DELAY</b>						
Fault-Detection Time	$t_D$	Fault detection to start of gate pulldown (Note 3)		60		ns
Pass FET Turn-Off Time	$t_F$	From start of gate pulldown to pass FET off (Note 3)		50		ns
<b>FAULT PIN</b>						
Input High Voltage	$V_{IH}$	(Note 2)	1			V
Input Low Voltage	$V_{IL}$	(Note 2)			0.66	V
Max Allowable $\overline{FAULT}$ Output High Voltage	$V_{OH}$	External pullup, leakage below $1\mu A$		5.5		V
$\overline{FAULT}$ Output Low Voltage	$V_{OL}$	Sinking 4mA			0.4	V
Propagation Delay from Fault Detect to $\overline{FAULT}$ Asserted Low	$t_D$	(Note 3)		100		ns
<b><math>V_{IN}</math> OVERVOLTAGE PROTECTION</b>						
Programmable Threshold for OVP	$V_{IN\_OVP}$	Measured at $V_{IN}$ , programmable (Note 2)		14 16		V
$V_{IN}$ Overvoltage Accuracy	$V_{IN\_OVP}$		-5		+5	%
Deglitching Time	$t_{FILTER\_OVP}$	(Note 3)		20		$\mu s$
<b>CURRENT REPORTING (ILOAD) PIN</b>						
Linear $I_{OUT}$ Reporting Range		Current-reporting range	0		30	A
Max Allowable Linear Voltage Range				1.35		V
Offset Current		$I_{OUT} = 0A$		0.32		$\mu A$

**Electrical Characteristics (continued)**

( $V_{IN} = 12V \pm 10\%$ , unless otherwise noted.  $T_J = 0^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Specifications are 100% production tested at  $T_A = +32^\circ C$ . Limits over operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current-Reporting Gain	$G_{ILOAD}$	ILOAD current divided by $I_{OUT}$ current (Note 2)		5		$\mu A/A$
Bandwidth		No capacitor in parallel with $R_{LOAD}$ resistor	100			kHz
<b>ANALOG CURRENT-REPORTING ACCURACY</b>						
Current-Reporting Accuracy (Notes 3, 4, 5)	$I_{OUT}$	$I_{OUT} = 4A$	-2.5		+2.5	%
		$I_{OUT} = 30A$	-1.8		+1.8	
<b>SMBus/PMBus TELEMETRY</b>						
Digital Current-Reporting Accuracy	READ_IOUT (8Ch), READ_IIN (89h)	$I_{OUT} = 4A$		$\pm 3$		%
		$I_{OUT} = 30A$		$\pm 2$		
Digital Power-Reporting Accuracy	READ_PIN (97h)	Digital, $I_{OUT} = 4A$ , $V_{IN} = 12V$ , $R_{LOAD} = 9k\Omega$ (MAX16550)		$\pm 5$		%
		Digital, $I_{OUT} = 30A$ , $V_{IN} = 12V$ , $R_{LOAD} = 9k\Omega$ (MAX16550)		$\pm 3.5$		
Digital Input-Voltage Reporting Accuracy	READ_VIN (88h)			$\pm 1.2$		%
Digital Output-Voltage Reporting Accuracy	READ_VOUT (8Bh)			$\pm 1.2$		%
Digital Temperature-Reporting Accuracy	READ_TEMPERA- TURE_1 (8Dh)			$\pm 8$		$^\circ C$
Digital Energy-Reporting Accuracy	READ_EIN (86h)	$I_{OUT} = 4A$		$\pm 5$		%
		$I_{OUT} = 30A$		$\pm 3$		

**Note 2:** Denotes specification that apply for typical operating junction temperature ( $T_J = +25^\circ C$ ).

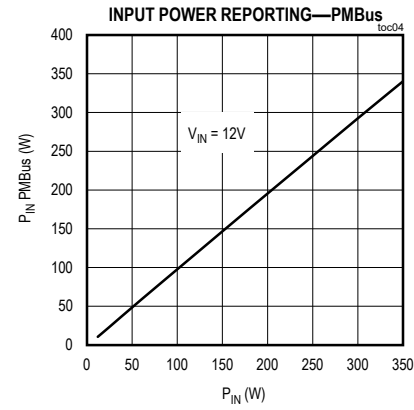
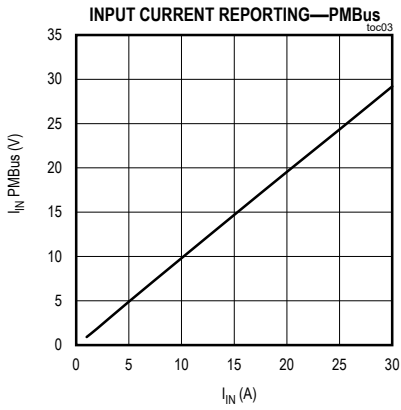
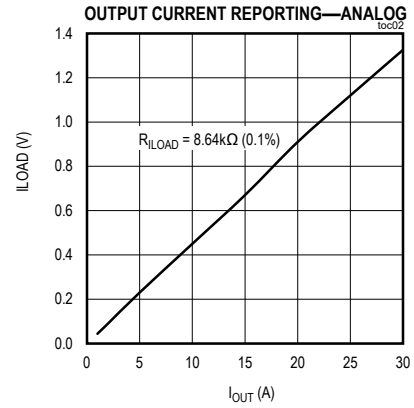
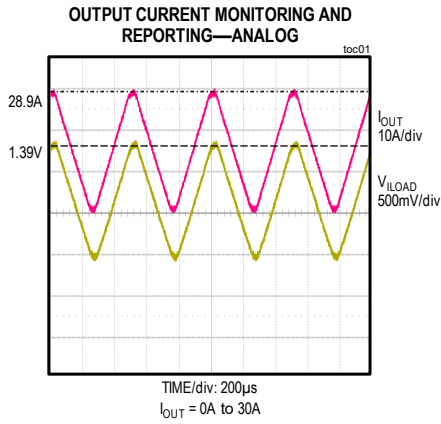
**Note 3:** Guaranteed by design, not production tested.

**Note 4:** Reporting accuracy presented includes 0.1% external resistor tolerance contribution.

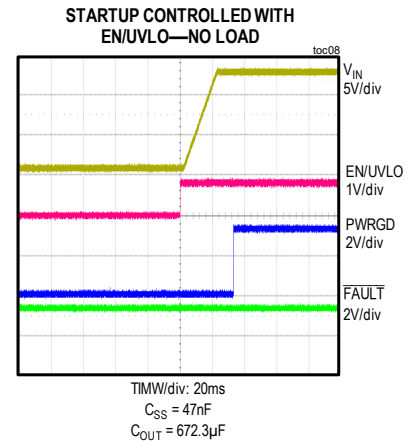
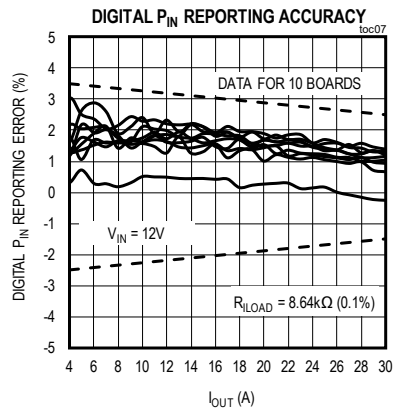
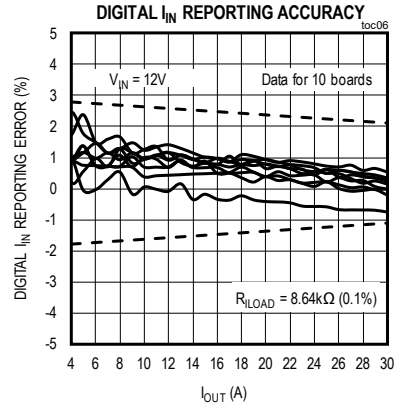
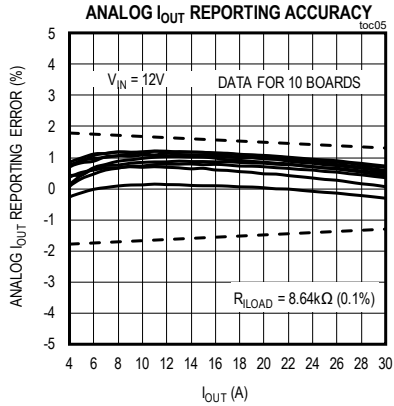
**Note 5:** Min/max limits are  $\geq 4\sigma$  about the mean.



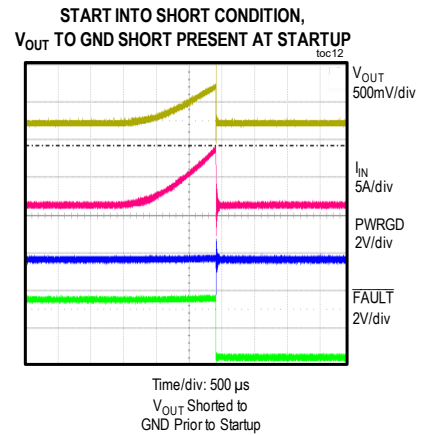
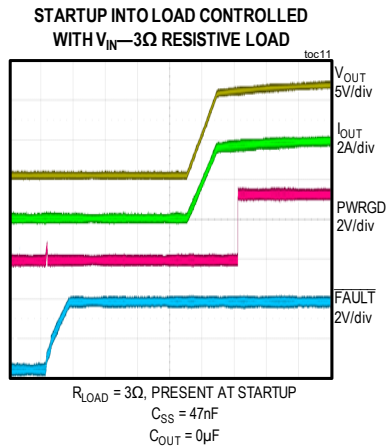
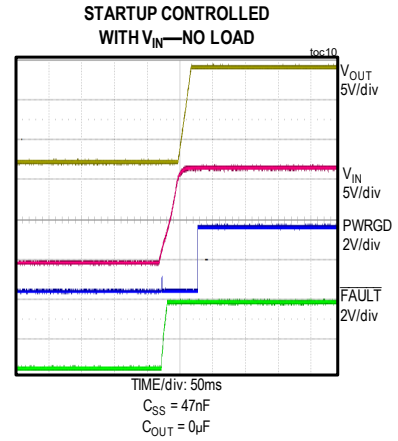
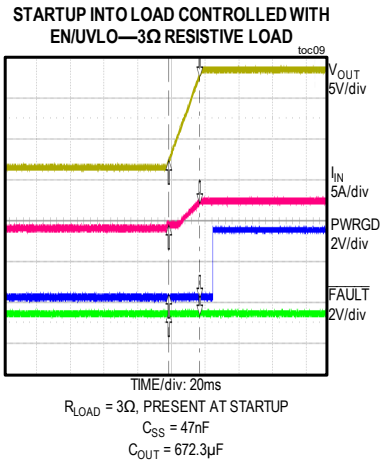
Typical Operating Characteristics



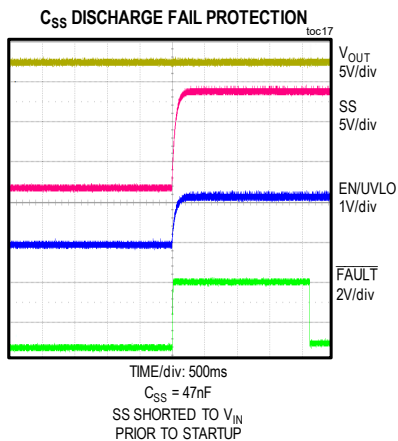
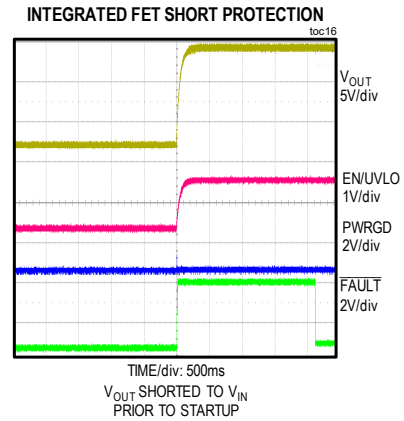
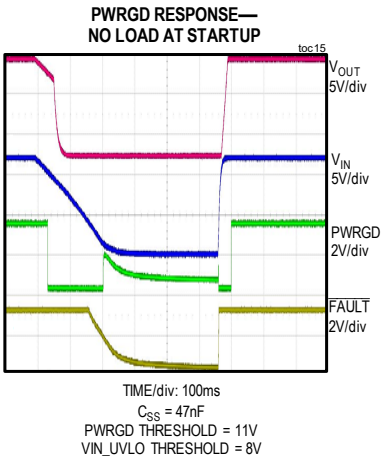
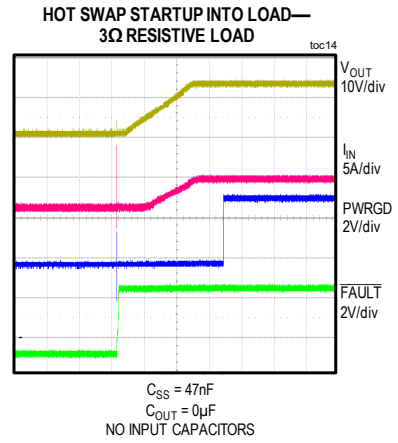
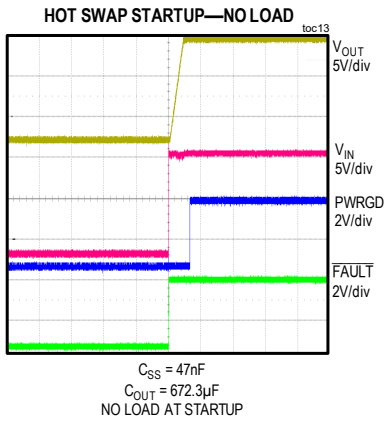
Typical Operating Characteristics (continued)



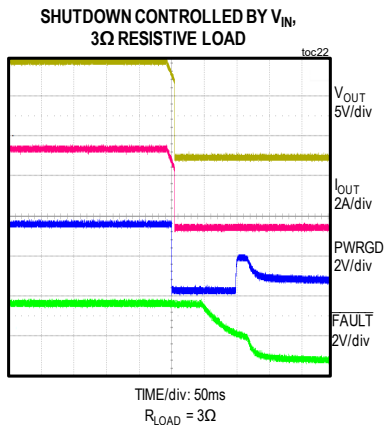
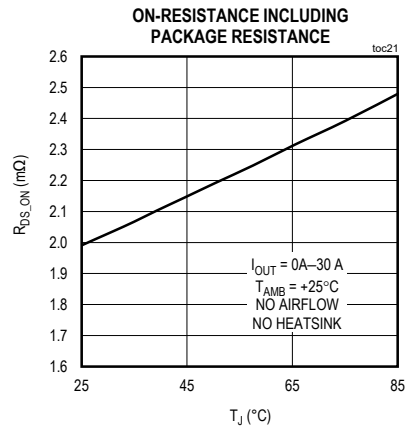
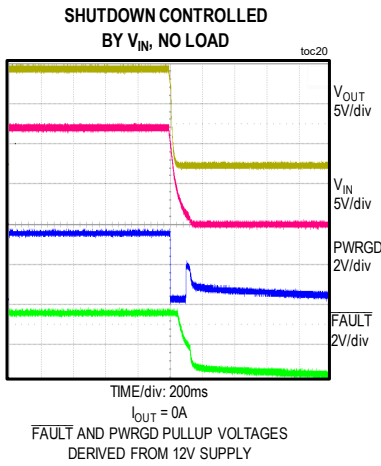
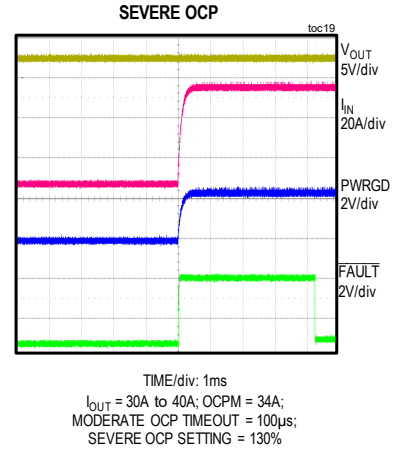
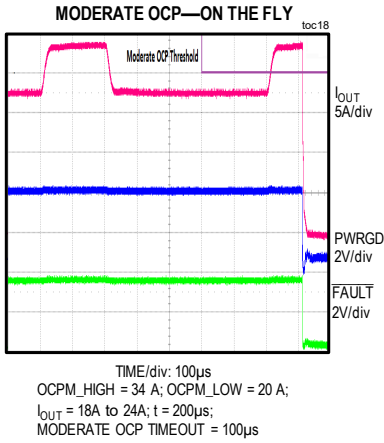
Typical Operating Characteristics (continued)



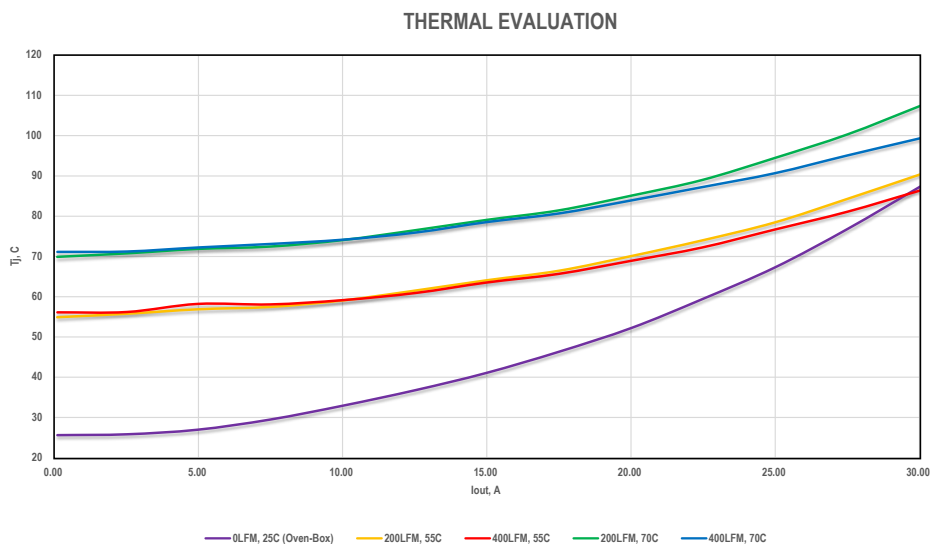
Typical Operating Characteristics (continued)



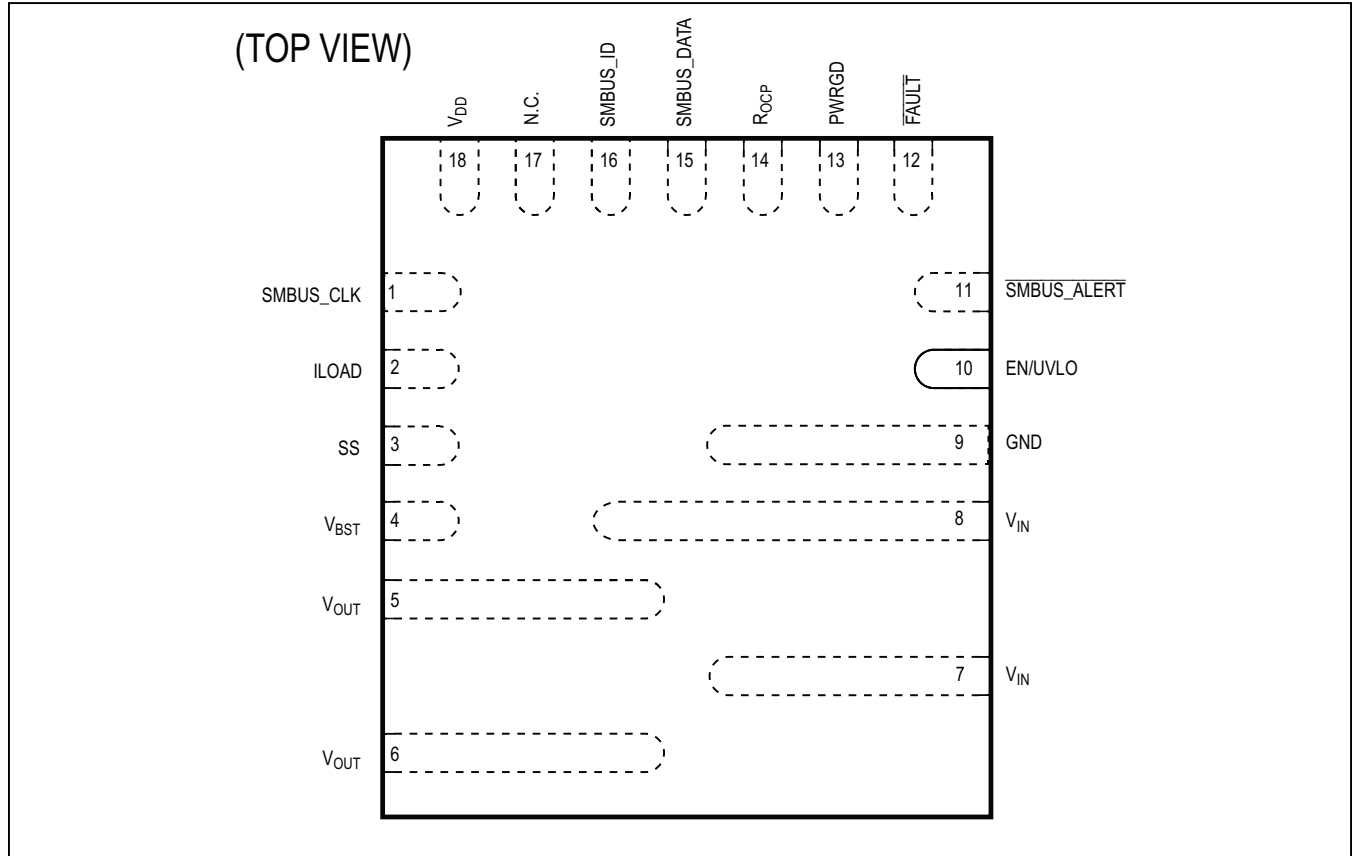
Typical Operating Characteristics (continued)



Typical Operating Characteristics (continued)



Pin Configuration



Pin Description

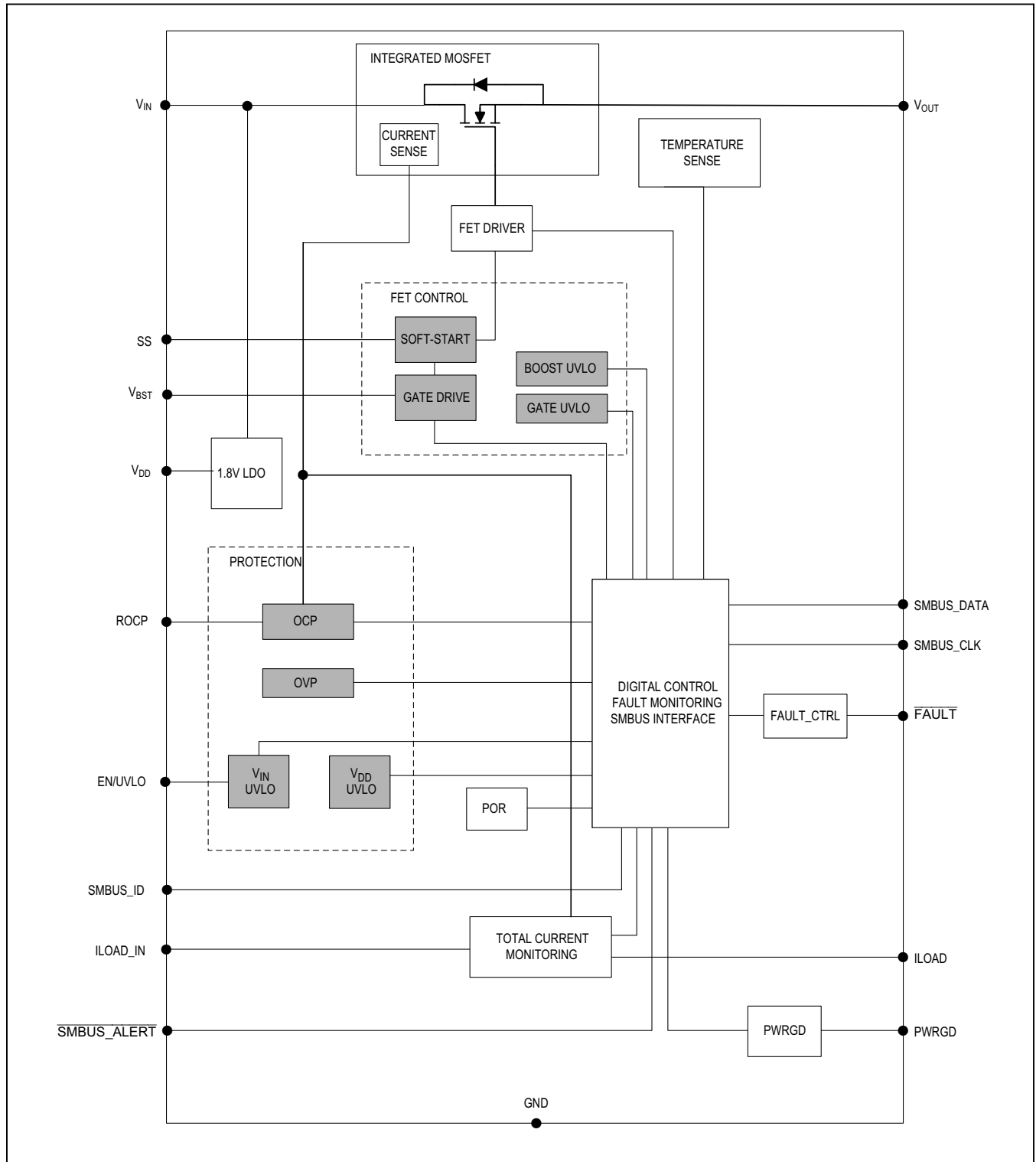
PIN	NAME	FUNCTION
1	SMBUS_CLK	SMBus Clock Pin.
2	ILOAD	Analog Current Representation of the Load Current. Connect the pin to ground through a properly sized resistor for proper voltage representation. Always keep this pin connected to ground through a resistor. A capacitor parallel to the R <sub>ILOAD</sub> resistor is required; see Table 16 for the recommended value.
3	SS	Soft-Start Pin. A capacitor is connected from SS to GND to program soft-start. The soft-start program capacitor should not exceed 75nF. If a fast load transient (di/dt > 2.5A/ms) resulting in fast and large transient output-voltage deviation is possible in the application, an additional capacitor between SS and V <sub>OUT</sub> is recommended to keep the pass FET V <sub>GS</sub> above its UVLO threshold.
4	V <sub>BST</sub>	Charge-Pump Supply for Pass FET Gate Drive. Connect this node to V <sub>OUT</sub> through a 220nF bypass capacitor. This supply is designed to be used by the MAX16550 only. No additional load or external components other than a bypass capacitor are allowed on the V <sub>BST</sub> pin.
5-6	V <sub>OUT</sub>	12V Output Power Pins (Load Side).

## MAX16550/MAX16551 Connection Information (continued)

PIN	NAME	FUNCTION
7-8	$V_{IN}$	12V Input Power Pins (Power Supply Side).
9	GND	IC Ground. Connect this node to GND plane through vias for proper operation.
10	EN/UVLO	12V Input Voltage and UVLO Pin. Normally connected to the center node of a resistor-divider connected from $V_{IN}$ to ground. A properly sized capacitor can be placed in parallel to the bottom resistor of the resistor-divider for additional filtering. In addition to 12V UVLO programming, this node can be used to enable/disable the MAX16550.
11	$\overline{\text{SMBUS\_ALERT}}$	SMBus Alert, Open-Drain, Active-Low Pin.
12	$\overline{\text{FAULT}}$	Fault Communication, Bidirectional Pin. It is used to indicate/receive detection of latching fault. See the <i>FAULT Reporting</i> section for more details. Connect this pin to the system bias supply rail through a 10k $\Omega$ resistor. 5V compliant, active-low pin.
13	PWRGD	Power Good Pin. Used to report $V_{IN}$ and $V_{OUT}$ status. See the <i>Power Good (PWRGD) Output</i> section for more details. Connect this pin to system bias supply rail through a 10k $\Omega$ resistor. This pin is 5V compliant.
14	ROCP	Moderate OCP Threshold Programming Input. Connect this pin to GND using an appropriate programming resistor. See the <i>Moderate OCP Threshold</i> section for additional details. No other components are allowed on this pin.
15	SMBUS_DATA	SMBus Data Pin.
16	SMBUS_ID	SMBus Address Programming and Current Hysteresis Flag Pin. Connect this pin to GND through a properly sized resistor to select desired address setting.
17	N.C.	Not Connected. Connect to GND through a 10k $\Omega$ resistor.
18	$V_{DD}$	Internal 1.8V Linear Regulator (LDO) Output. Connect this pin to GND through a 1 $\mu$ F (or higher) capacitor. See Figure 6 for the correct value. No additional loads or components other than external properly sized capacitor are allowed on the $V_{DD}$ pin.



Block Diagram



### Detailed Description

The MAX16550 integrated power-protection IC is designed to provide a complete, single-chip circuit-breaker protection solution for the 12V power bus. It combines power monitoring and control functions with a low on-resistance pass FET device that acts as a disconnect switch to limit maximum power distributed to the load. The IC implements Maxim's proprietary integrated lossless current sensing techniques to provide a highly accurate and compact protection solution. The ICs integrate PMBus/SMBus interface for digital control and monitoring.

Refer to the IC [Block Diagram](#). An integrated N-channel power MOSFET is driven by the FET control circuit that includes a boost circuit to provide gate drive. An internal LDO provides  $V_{DD}$  IC bias supply, eliminating the need for external bias supply, enabling effective use of the device in hot-swap applications.

### Startup

The IC enables the integrated 1.8V  $V_{DD}$  LDO once the 12V supply voltage is high enough to guarantee LDO operation. Once  $V_{DD}$  is valid, the ICs read the SMBus\_ID programming resistor value to set the PMBus address and initiate. During this period, the gate-drive supply capacitor becomes fully charged. Once these two func-

tions are complete, the ICs can be controlled through the enable input.

The enable input (EN/UVLO) has a precise threshold and provides a  $V_{IN\_UVLO}$  function, where the enable voltage is derived from  $V_{IN}$  through a resistor-divider, with an optional control signal used in conjunction with the divider, as shown in [Figure 5](#). The EN/UVLO pin must not be pulled high externally other than to pull the EN/UVLO pin high through a properly sized resistor-divider from the input supply. Though the enable signal can be pulled low to disable the part, this should only be allowed to occur when the input-voltage supply is within operating range, as specified in the [Electrical Characteristics](#) table.

### Startup Safe Operating Area (SOA)

During soft-start, it is important to keep the FET within its safe operating area. The peak current allowed during startup is shown in [Figure 1](#). In case resistive short is possible in the application, it is required to use startup OCP feature to protect the device. The startup OCP threshold must be programmed to a value lower than safe peak current. [Figure 1](#) assumes pure capacitive or RC load on the output.

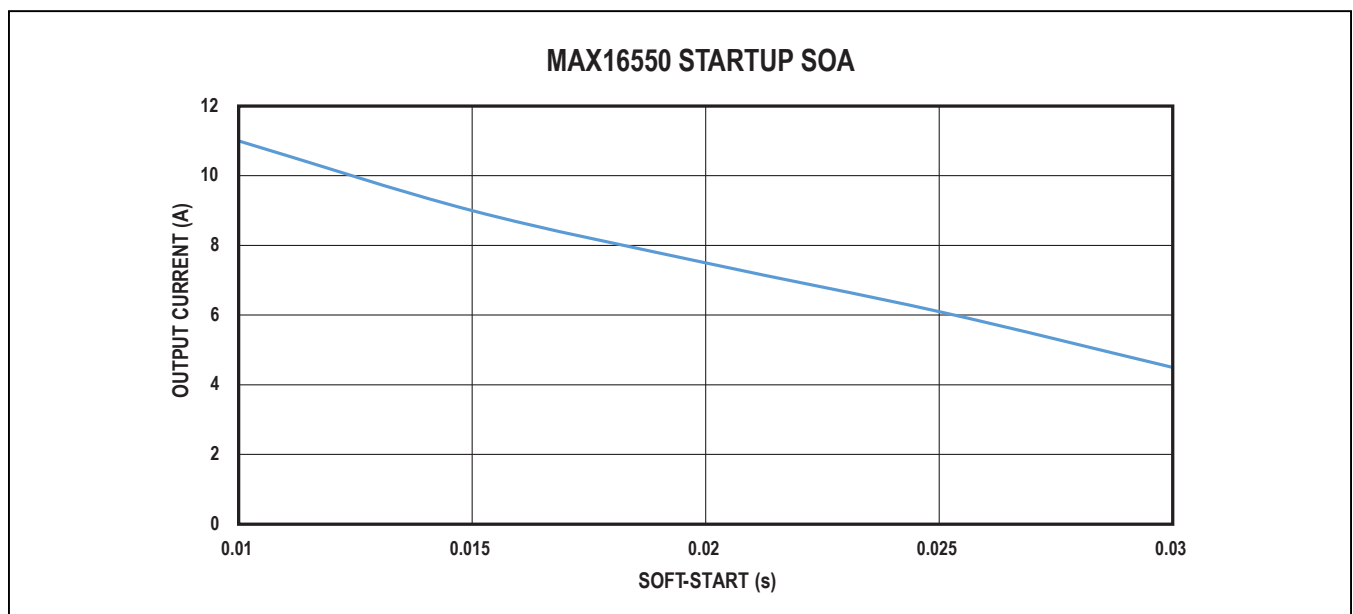


Figure 1. MAX16550 Startup SOA

**Self-Check**

Once  $V_{BST\_UVLO}$  has been cleared, the internal  $V_{DD\_LDO}$  is fully enabled and the EN/UVLO pin is above the enable threshold, the ICs initiate a timed output discharge as a self-check procedure. By default, the ICs initiate this procedure immediately after  $V_{BST\_UVLO}$  has been cleared and the internal  $V_{DD\_LDO}$  is fully enabled. Delay to start this procedure can be reprogrammed through PMBus. If the output does not fall below the programmed  $V_{OUT\_UVLO}$  threshold after a fixed period, the pass FET could potentially be shorted, with the ICs asserting both FAULT and PWRGD pins low. The latched fault condition remains until restart (EN/UVLO or  $V_{IN}$  toggling, restarting through the OPERATIONS command). The threshold ( $V_{OUT\_UVLO}$ ) for the self-check procedure can be programmed to one of three different values through the PMBus. These values are programmed with the corresponding values for the PWRGD threshold. If the output voltage is below the programmed  $V_{OUT\_UVLO}$ , the self-check is considered passed and the ICs proceed with startup.

In addition, a soft-start capacitor discharge procedure is performed during every restart. The ICs utilize an integrated resistive element, with resistance approximately  $1.2k\Omega$ , to discharge the  $C_{SS}$  capacitor. The ICs check if the voltage across the  $C_{SS}$  capacitor is below the soft-start threshold shown in the [Electrical Characteristics](#) table after a fixed period of time. If the voltage across the  $C_{SS}$  capacitor is not below the softstart threshold, the ICs latch the pass FET off and assert the  $\overline{FAULT}$  pin low. The latched fault condition is kept until reset (EN/UVLO or  $V_{IN}$  toggling).

The ICs check the ROCP value at all times, including startup (after the bias supply is valid). This check ensures proper reference OCP threshold selection, which determines startup and severe OCP thresholds. If the wrong ROCP value is detected, the ICs report the fault by asserting the  $\overline{FAULT}$  signal low. The latched fault condition is kept until restart (EN/UVLO or  $V_{IN}$  toggling/restarting through the OPERATIONS command).

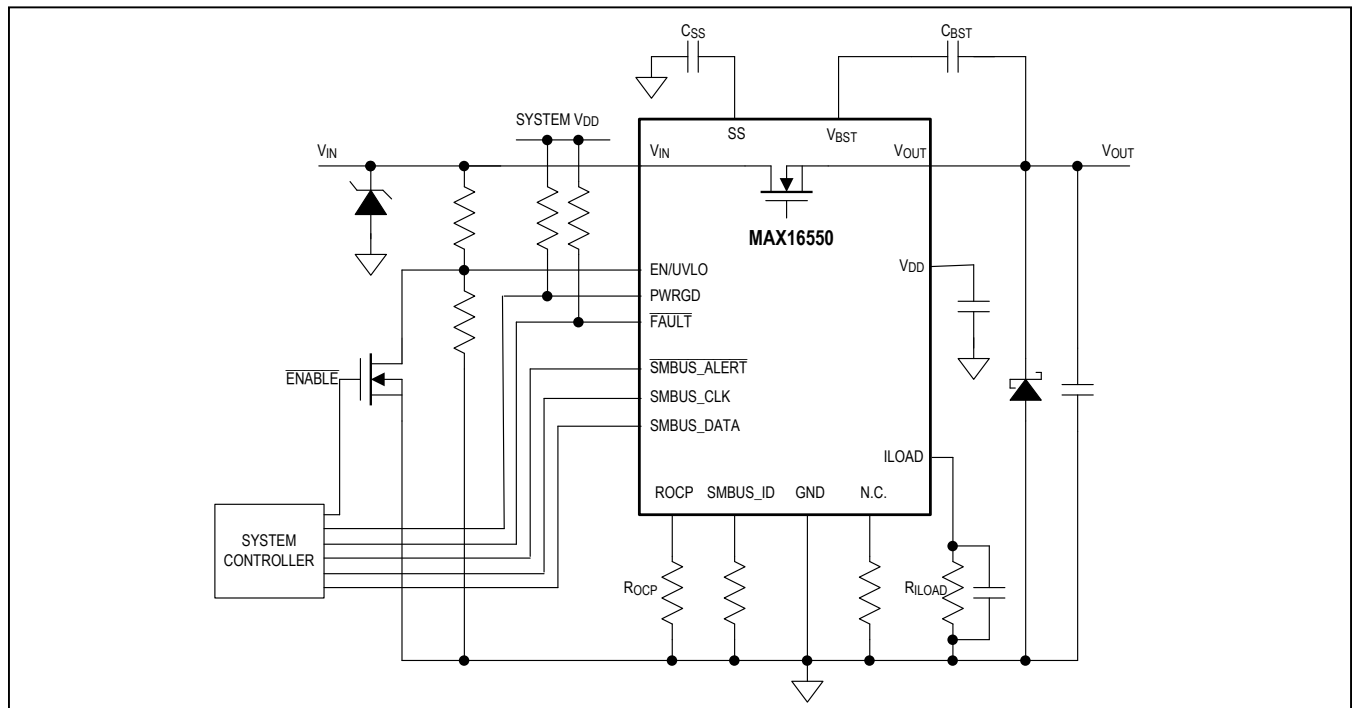


Figure 2. MAX16550 Configuration Example

**Soft-Start**

Once the self-check procedure is complete, the output-voltage soft-start ramp is initiated. During startup, the  $C_{SS}$  capacitor is charged using a constant-current source. Since the integrated FET is configured as a source follower, the output voltage is ramped monotonically at a rate determined by the external soft-start capacitor.

**V<sub>DD</sub> UVLO**

The ICs implement V<sub>DD</sub> UVLO fault monitor and protection. V<sub>DD</sub> is monitored at all times. Startup

procedures are not initiated until V<sub>DD</sub> UVLO is cleared. If V<sub>DD</sub> falls below V<sub>DD</sub> UVLO during normal operation, this fault is latched and V<sub>IN</sub> power cycle/toggle is required to reset this latching fault.

**Current Hysteresis**

The SMBUS\_ID pin is used as a current-hysteresis flag after SMBUS\_ID decoding is completed. If the output current is greater than the MFR\_SPECIFIC\_HYSTH level, the current-hysteresis flag is set to high. If output current is less than the MFR\_SPECIFIC\_HYSTL level, then the current-hysteresis flag is set to low.

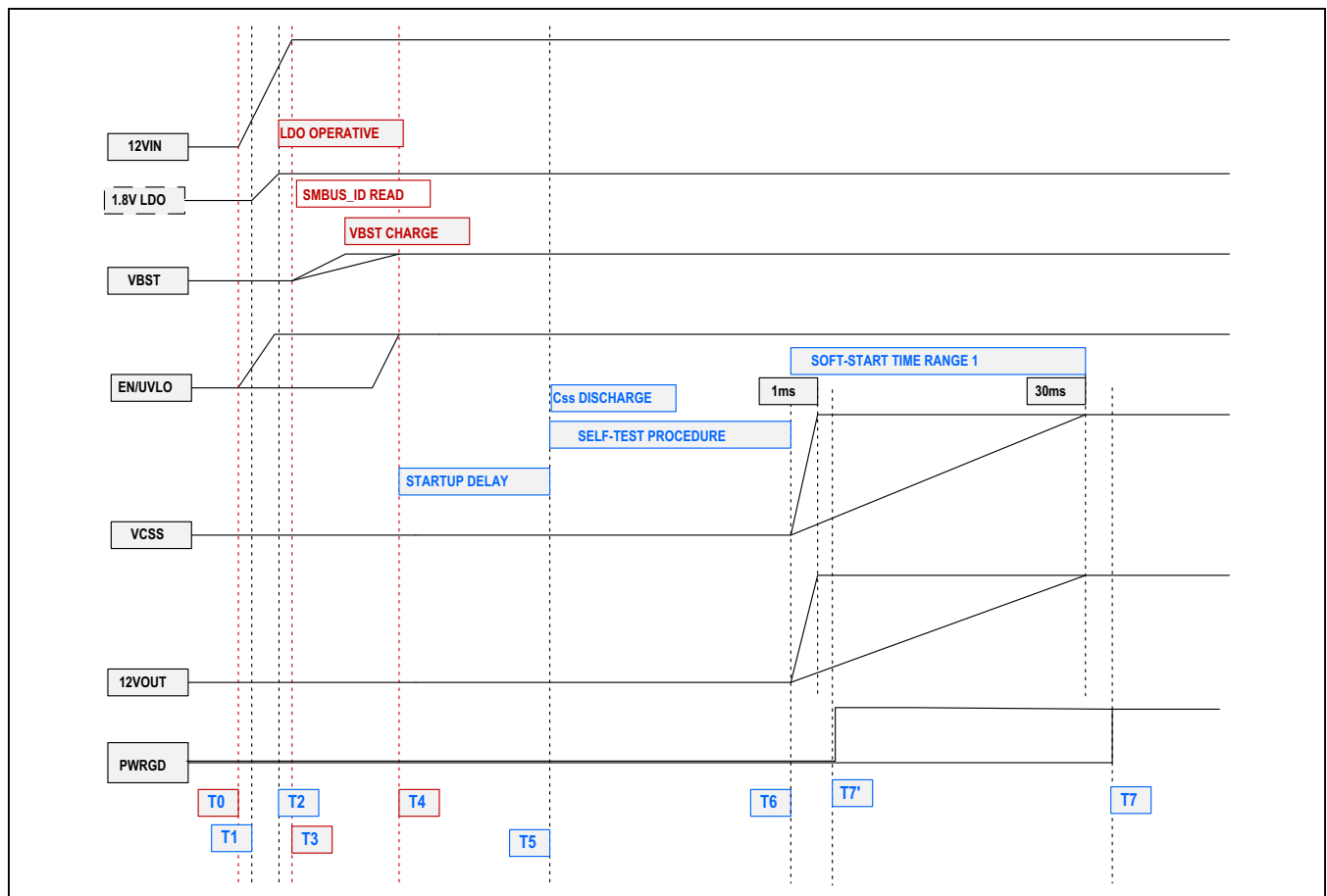


Figure 3. Startup Timing Diagram

**Table 1. Timing Diagram Example Shown  
in Figure 5**

POINT/ PERIOD	DESCRIPTION
t0	12V $V_{IN}$ applied.
t1	The LDO has enough headroom to start up. $V_{IN} > 2V$ (typ).
t2	The internal 1.8V LDO is ready and the MAX16550 logic is fully operational. External bypass capacitors connected to the $V_{DD}$ pin are fully charged. 700 $\mu$ s (typ).
t3, t4	SMBus ID resistor reading and $V_{BST}$ charging. EN/UVLO signal status is ignored from t3 to t4. 150 $\mu$ s (typ).
t4	EN/UVLO is active. Startup check-up procedures can be started after the EN/UVLO is cleared.
t4, t5	User-programmable startup delay (0 to 20 $\mu$ s).
t5, t6	Self-test procedure. $C_{SS}$ discharge.
t6, t7	$V_{OUT}$ ramp (1ms–30ms).
t7	Power-good (PWRGD) output asserted. 6ms (typ).
t7+	PWRGD is high, normal operation starts.

### SMBus ID Resistor Out of Range

After  $V_{DD}$  UVLO is cleared, the SMBus ID programming resistor is read. If it is out of range, a latching fault is tripped. This fault can be cleared by EN/UVLO or  $V_{IN}$  toggling or restarting through the OPERATIONS command. The latter may mean pulling EN/UVLO above the threshold and then low after the fault is detected to reset the fault latch. The value is read again when EN/UVLO goes high for the second time.

### VBOOST, VGS UVLO

$V_{BOOST}$  UVLO is checked when EN/UVLO is above the enable threshold and remains active while the device is enabled. If  $V_{BOOST}$  UVLO is tripped before the FET is turned on, the latching fault can still be reset by EN/UVLO or  $V_{IN}$  toggling or restarting through the OPERATIONS command. The gate-drive ( $V_{GS}$ ) UVLO protection has 10 $\mu$ s internal deglitching filtering, which prevents false tripping due to output-voltage overshoot if a large, fast unloading transient is present. An external capacitance can be placed between the  $V_{OUT}$  and  $V_{SS}$  pins for filtering.  $V_{BOOST}$  and  $V_{GS}$  UVLO are latching faults, which result in the pass FET being latched off and  $\overline{FAULT}$  asserted

low.  $V_{GS}$  UVLO is masked for 100ms during startup to avoid tripping a latching fault.

### $V_{IN}$ UVLO

The  $V_{IN}$  UVLO is fed through a resistor-divider to the EN/UVLO pin and therefore provides a programmable threshold on the 12V input rail. The EN/UVLO pin includes hysteresis and if the pin falls below the programmed value during operation, the device turns the integrated FET off and PWRGD is deasserted. The integrated FET is turned on again if the positive threshold is exceeded and performs self-test and soft-start for each cycle.  $V_{IN}$  UVLO warning is also provided through the PMBus.

### Overcurrent Detection

The MAX16550 actively monitors load current on the 12V power bus load at all times, including startup. Startup OCP is active during startup until the power-good (PWRGD) flag is set. Startup OCP threshold is 8A by default and has much faster reaction time. If, at any time during startup, load current rises above the startup threshold, the integrated pass FET turns off within 10 $\mu$ s and the  $\overline{FAULT}$  pin is asserted low. This is a latching fault.

The MAX16550 provides three levels of overcurrent protection during normal operation (after the startup procedure is complete and the PWRGD flag is set high). The “moderate” OCP threshold is set using an analog external resistor and is therefore programmable over a wide continuous range. This OCP allows a higher current to be sustained for a period less than a programmable timeout period without shutting down the device to allow for short surges that pose no threat to the device and are normal operating conditions. If the load current on the 12V power bus exceeds the moderate OCP threshold for the entire timeout period, but its magnitude is less than a programmable severe overcurrent threshold (Table 3), the integrated pass FET switches off at the end of the timeout period and the  $\overline{FAULT}$  pin is asserted low to indicate a moderate OCP fault condition. Restarting the system requires EN/UVLO or  $V_{IN}$  toggling or restarting through the OPERATIONS command. Moderate OCP timeout is user programmable through SMBus, with four different values.

The second level of OCP protection is a “severe OCP.” Severe OCP threshold is programmed relative to moderate OCP threshold using PMBus. If at any time the load current exceeds the severe OCP threshold, the MAX16550 turns the integrated pass FET off in less than 5 $\mu$ s, and asserts the  $\overline{FAULT}$  pin low. Severe overcurrent protection is a latching fault.

The MAX16550 features a third level of protection against severe overload faults, called “safe OCP,” with 60A internally fixed threshold. It assures that the integrated pass FET is protected from exceeding its safe operating condition at all times. If at any time the load current on the 12V power bus exceeds the safe OCP threshold, the MAX16550 turns the pass FET off within 250ns and asserts the  $\overline{\text{FAULT}}$  pin low. The severe OCP threshold should be set to a value less than the safe OCP threshold.

The MAX16550 supports on-the-fly moderate OCP threshold changes. The concept is shown in Figure 4. If the resistance seen by the ROCP pin is changed during the MAX16550 operation, the MAX16550 adjusts the moderate OCP threshold to match the value selected by the external resistive network.

### Overvoltage Protection

The ICs includes  $V_{IN}$  overvoltage protection to protect the system from an overvoltage event that could harm the downstream circuitry. Overvoltage protection is disabled by default and can be enabled and programmed through PMBus. The input voltage is constantly monitored, and if at any time it rises above the PMBus programmed threshold, the pass FET is latched off,  $\overline{\text{FAULT}}$  asserted low, and a fault reported. This is a latching fault.

### Wrong ROCP Protection

The ICs are protected against out-of-range ROCP values. Protection is enabled at all operating conditions, including startup. Wrong ROCP is considered a severe, latching fault, so if at any time the ROCP value is detected out of the permitted range, the ICs latch the integrated FET off, and assert the  $\overline{\text{FAULT}}$  pin low. An EN/UVLO or  $V_{IN}$  toggling or a restart through the OPERATIONS command must be performed to clear the fault and restart the ICs. If ROCP is changed during operation by the system (see Figure 4), the design must be such that ROCP is within range at all times.

### Overtemperature Protection

The ICs include protection against overtemperature conditions. If the junction temperature exceeds the programmable threshold, the IC latches the integrated FET off and asserts the  $\overline{\text{FAULT}}$  output low. To re-enable the IC, the following options are available:

- Toggling EN/UVLO or  $V_{IN}$
- Restarting through the OPERATIONS command

The overtemperature threshold is user programmable through the PMBus.

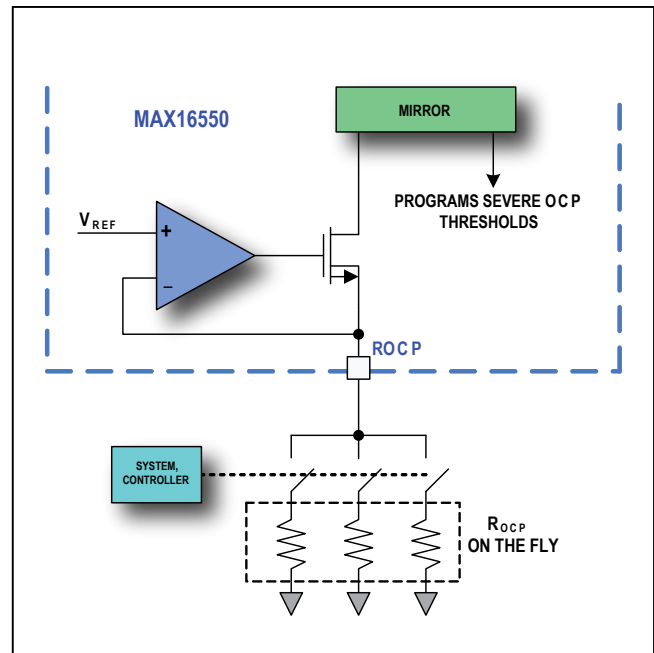


Figure 4. On-The-Fly Analog Programmable Moderate OCP Threshold (MAX16550)

### $\overline{\text{FAULT}}$ Fault Reporting

The ICs provide a dedicated pin ( $\overline{\text{FAULT}}$ ) for fault reporting. If at any time a latching fault is detected, the  $\overline{\text{FAULT}}$  pin is immediately latched low. An EN/UVLO or  $V_{IN}$  toggling or restart through the OPERATIONS command is required to reset the ICs after a latching-fault detection.

### Fault Input and $\overline{\text{FAULT}}$ Pullup

The  $\overline{\text{FAULT}}$  pin is a bidirectional open-drain pin that can be used for fault communication from external circuitry to the ICs. To communicate a fault to the ICs, the external circuitry must pull the  $\overline{\text{FAULT}}$  pin low. If  $\overline{\text{FAULT}}$  is externally pulled low, the ICs treat it as a latching fault; therefore, the pullup voltage source must be considered to ensure the rail is operational and pulled high before the ICs' startup cycle.

These are the options for the pullup rail:

- MAX16550  $V_{DD}$ : 1.8V internal LDO rail. This rail is limited to 1.8V, so the external system has to be compliant with that rail.
- System 3.3V or 5V Rail:  $\overline{\text{FAULT}}$  is 5V compliant; therefore, an external higher voltage rail can be used for pullup. This rail has to be stable when the ICs are initiating their startup procedure. If it is not, a potential false-fault communication may occur.

### Power-Good (PWRGD) Output

The ICs provide a dedicated pin for power-good reporting (PWRGD). PWRGD is asserted high after startup, when the output node is charged above the programmed PWRGD threshold and the FET is fully enhanced and operating in its resistive region. In all the other conditions, the PWRGD pin is deasserted low.

PWRGD is an open-drain pin; thus, an external pullup resistor connected to the pullup supply rail is needed. Different options are available for the pullup rail:

- MAX16550  $V_{DD}$ : 1.8V internal LDO rail. This rail is limited to 1.8V, so the external system has to be compliant with that rail.
- System 3.3V or 5V Rail: PWRGD is 5V compliant; therefore, an external higher voltage rail can be used for pullup.

### Analog Load Current Signal Output

The ICs include an output pin (ILOAD) that allows the user to monitor the load current through the ICs. The current sourced by the ILOAD pin is proportional to the current through the device with the ratio shown in the [Electrical Characteristics](#) table. A properly sized resistor between the ILOAD pin and GND should be added. The ICs report zero current on the ILOAD pin during soft-start, and start reporting load current once the pass FET  $V_{GS}$  is above its UVLO threshold (i.e., the pass FET is in its resistive region).

### PMBus/SMBus Reporting and Warning

The ICs provide PMBus-compliant digital telemetry through the PMBus, as shown in [Table 4](#). The ICs include a digital multiply function that provides a reading for input power and input energy. For average values, the sample size is programmable. Peak values for input/output

**Table 2. Faults Detected and Actions**

PARAMETER	DESCRIPTION	$\overline{\text{FAULT}}$ ASSERTED	LATCHING
$V_{DD}$ UVLO	Internal $V_{DD}$ LDO UVLO	N/A*	N/A*
$V_{BOOST}$ UVLO	UVLO for $V_{BOOST}$ voltage	Yes	Yes
$V_{GS}$ UVLO	UVLO for $V_{GS}$ voltage	Yes	Yes
$V_{IN}$ UVLO	EN/UVLO pin below threshold	No	No
$R_{OCP}$	$R_{OCP}$ detected as being out of valid range	Yes	Yes
R_SMBus_ID	SMBus_ID resistor detected as being out of range	Yes	Yes
$C_{SS}$ Discharge	Soft-start capacitor discharge failed	Yes	Yes
FET Short	Pass FET short detected during startup self-check	Yes	Yes
Startup OCP	Startup overcurrent fault detected	Yes	Yes
Severe OCP	Severe overcurrent fault detected	Yes	Yes
Safe OCP	Safe overcurrent fault detected	Yes	Yes
Power Fault	Power fault detected	Yes	Yes
OTP	Overtemperature-fault threshold exceeded	Yes	Yes
$V_{IN}$ OVP	$V_{IN}$ overvoltage detected	Yes	Yes

**Note 1:** If  $V_{BST\_UVLO}$  fault occurs before startup,  $\overline{\text{FAULT}}$  is not reported and status registers are not updated.

**Note 2:**  $V_{IN\_UVLO}$  clears  $\overline{\text{FAULT}}$  and the latching event.

**Table 3. Requirements for PWRGD Assertion**

PARAMETER	CONDITION
V <sub>OUT</sub>	V <sub>OUT</sub> > PWRGD Threshold
V <sub>IN</sub>	V <sub>IN</sub> > V <sub>IN_UVLO</sub>
Self-Check	MOSFET (V <sub>IN</sub> to V <sub>OUT</sub> ) short not detected during startup.
V <sub>GS</sub>	FET on and in triode region. 5ms delay before PWRGD assertion after this condition is met.

**Table 4. PMBus/SMBus Reporting**

PARAMETER	CONDITION
V <sub>IN</sub>	Input voltage (PMBus compliant)
I <sub>OUT</sub>	Output current (PMBus compliant)
P <sub>IN</sub>	Input power (PMBus compliant)
E <sub>IN</sub>	Input energy (PMBus compliant)
Temperature	MAX16550 chip temperature (PMBus compliant)
Peak V <sub>IN</sub>	Peak value of input voltage (direct reading)
Peak I <sub>OUT</sub>	Peak value of output current (direct reading)
Peak P <sub>IN</sub>	Peak value of input power (direct reading)
Peak Temperature	Peak value of IC temperature (direct reading)
Peak V <sub>OUT</sub>	Peak value of output voltage (direct reading)

voltage, output current, input power, and temperature are stored in dedicated manufacturer-specific registers. The ICs also provide warning functions based on programmable warning thresholds, as specified in the PMBus specification. The sample size for warning flags is also programmable.

## Configuration

The ICs are configured using both analog programming resistors and also through the PMBus. See [Table 5](#) for programmable parameters.

## Reference OCP Threshold

The reference OCP threshold is externally programmable through a resistor connected to the ROCP pin. This threshold is used as reference for startup and severe OCP thresholds. The reference OCP threshold is programmed as shown in Equations 1 and 2 (see the [Electrical Characteristics](#) table for V<sub>OCPM</sub> and GOCP).

**Equation 1:**

$$I_{OCP\_REF} = \frac{V_{OCPM}}{R_{OCP}} \times GOCP$$

where:

I<sub>OCP\_REF</sub> = Reference overcurrent-protection threshold (A)  
V<sub>OCPM</sub> = Overcurrent-protection reference voltage shown in the [Electrical Characteristics](#) table (V)

GOCP = Overcurrent-protection gain shown in the [Electrical Characteristics](#) table (μA/A)

R<sub>OCP</sub> = Value of overcurrent-protection programming resistor (Ω)

**Equation 2:**

$$R_{OCP} = \frac{V_{OCPM}}{I_{OCP\_REF}} \times GOCP$$

where:

I<sub>OCP\_REF</sub> = Reference overcurrent-protection threshold (A)  
V<sub>OCPM</sub> = Overcurrent-protection reference voltage shown in the [Electrical Characteristics](#) table (V)

GOCP = Overcurrent-protection gain shown in the [Electrical Characteristics](#) table (A/A).

R<sub>OCP</sub> = Value of overcurrent-protection programming resistor (Ω)

**Design Example (MAX16550):**

To set moderate OCP to 35A nominal, using Equation 2:

$$R_{OCP} = \frac{0.8V}{35A} \times (4 \times 10^6) \\ = 91.5k\Omega$$

## Startup OCP Threshold

PMBus register DDh is used to set startup OCP threshold. See [Table 14](#) for Reg\_DDh settings.

**Design Example:**

To set Startup OCP to 4A, write 10b to bits Reg\_DDh[5:4].



**Table 5. MAX16550 Programmability**

PARAMETER	PROGRAMMABILITY TYPE	COMPONENT	CONDITION
Moderate (MAX16550) OCP Threshold (sets moderate and severe OCP)	Analog	ROCP	R_OCP
Soft-Start Ramp Rate	Analog	C <sub>SS</sub>	SS
Input UVLO Threshold	Analog	Divider	EN/UVLO
PMBus Address	Programming Resistor	SMBus_ID Resistor	SMBus_ID
Power Fault Timeout	Digital	PMBus_Reg D0h[6:5]	SMB_DATA
Severe OCP Threshold	Digital	PMBus_Reg D0h[7]	SMB_DATA
Startup Delay	Digital	PMBus_Reg D0h[12:11]	SMB_DATA
Input OVP Threshold (OVP feature can be enabled/disabled)	Digital	PMBus_Reg D0h[3:2]	SMB_DATA
Output PWRGD Threshold (sets V <sub>OUT</sub> UVLO and self-test thresholds)	Digital	PMBus_Reg D0h[9:8]	SMB_DATA
Self-Check Threshold	Digital	PMBus_Reg D0h[9:8]	SMB_DATA
Overtemperature Warning and Fault Thresholds	Digital	PMBus_Reg 51h, PMBus_Reg 4Fh	SMB_DATA
Input Overpower Warning Threshold and Fault Thresholds	Digital	PMBus_Reg 6Bh, PMBus_Reg F5h	SMB_DATA
Reporting and Warning Averaging Sample Size	Digital	PMBus_Reg DDh[3:0], PMBus_Reg D0h[1:0]	SMB_DATA
V <sub>IN</sub> Undervoltage Warning and Fault Thresholds	Digital	PMBus_Reg 58h, PMBus_Reg 59h	SMB_DATA
Overcurrent Warning	Digital	PMBus_Reg 4Ah	SMB_DATA
V <sub>OUT</sub> Undervoltage Warning Threshold	Digital	PMBus_Reg 43h	SMB_DATA
ILOAD Voltage Gain	Analog	ILOAD Resistor	ILOAD

**Soft-Start Capacitor (C<sub>SS</sub>)**

During startup, the pass FET device is operated as a source follower. Soft-start capacitor C<sub>SS</sub> is connected between the MOSFET's gate and ground and is charged from a fixed current source. The external C<sub>SS</sub> capacitor therefore charges linearly and this produces a linear monotonic ramp for V<sub>OUT</sub>. The ramp rate is programmable by selecting the appropriate value for C<sub>SS</sub>. The ramp rate for the voltage across C<sub>SS</sub> and V<sub>OUT</sub> is given by Equation 5.

**Equation 5:**

$$\frac{dV}{dt} = \frac{i_{SS}}{C_{SS}}$$

where:

dV/dt = Voltage ramp rate of V<sub>OUT</sub> (V/μs)

i<sub>SS</sub> = Soft-start current source (mA)

C<sub>SS</sub> = External C<sub>SS</sub> capacitor value (nF)

Assuming V<sub>IN</sub> = 12V, Equation 5 can be used to derive the soft-start time given by Equation 6.

**Equation 6:**

$$t_{SS} = \frac{12V \times C_{SS}}{i_{SS}}$$

where:

t<sub>SS</sub> = Ramp duration (μs)

i<sub>SS</sub> = Soft-start current (mA)

C<sub>SS</sub> = External soft-start capacitor value (nF)

Assuming the load inrush current is due to the input capacitance only, the load current is given by Equations 7 and 8.

**Equation 7:**

$$I_{IN} = I_{OUT} = C_{OUT} \times \frac{dV}{dt}$$

where:

I<sub>OUT</sub> = Load inrush current (A)

C<sub>OUT</sub> = Load capacitance (μF)

**Equation 8:**

$$I_{IN} = I_{OUT} = \frac{C_{OUT} \times i_{SS}}{C_{SS}}$$

where:

I<sub>OUT</sub> = Load inrush current (A)

C<sub>OUT</sub> = Load capacitance (μF)

C<sub>SS</sub> = External soft-start capacitor value (nF)

i<sub>SS</sub> = Soft-start current (mA)

Therefore, the soft-start capacitor can be selected based on the design value of inrush current using Equation 9.

**Equation 9:**

$$C_{SS} = \frac{C_{OUT} \times i_{SS}}{I_{INRUSH}}$$

where:

I<sub>INRUSH</sub> = Desired maximum inrush current due to C<sub>LOAD</sub> (A)

C<sub>OUT</sub> = Load capacitance (mF)

C<sub>SS</sub> = External soft-start capacitor value (nF)

i<sub>SS</sub> = MAX16550 soft-start current (μA)

In order to achieve optimal low-loss operation of the pass FET, the ICs monitor the value of the pass FET V<sub>GS</sub>. The V<sub>GS</sub> UVLO is enabled approximately 100ms (according to the [Electrical Characteristics](#) table) after startup initiation. This places an upper limit on C<sub>SS</sub> and t<sub>SS</sub>.

Note that if load unloading transients with di/dt > 2.5A/ms large enough to cause output-voltage transients > ~100mV, an additional capacitor between SS and V<sub>OUT</sub> is recommended to ensure the pass FET V<sub>GS</sub> remains above its UVLO threshold. This capacitor has no noticeable effect on soft-start ramp time as the differential voltage from V<sub>OUT</sub> to SS remains approximately constant in soft-start.

**Design Example:**

Assume a maximum design value for inrush current of 10A, and a load capacitance of 2mF.

$$\begin{aligned} C_{SS} &= \frac{(2\text{mF}) \times (30\mu\text{A})}{10\text{A}} \\ &= 6\text{nF minimum (to meet inrush maximum)} \end{aligned}$$

Use Equation 6 to show that corresponding t<sub>SS</sub> in this example is 2.4ms, which is well below the 100ms limit.

**Input UVLO**

The input UVLO is set using a resistor-divider circuit, as shown in Figure 5. The enable threshold,  $V_{IN\_UVLO}$  is given in the *Electrical Characteristics* table. The corresponding value for the  $V_{IN}$  rail is given by Equation 10.

**Equation 10:**

$$V_{IN} = \frac{V_{IN\_UVLO}}{K}$$

or

**Equation 11:**

$$K = \frac{(V_{IN\_UVLO})}{V_{IN}}$$

where:

$V_{IN}$  = 12V rail input voltage to enable device (V)

$V_{IN\_UVLO}$  = EN/UVLO threshold (V)

K = Resistor-divider ratio,  $R_2/(R_1 + R_2)$

**Design Example:**

To guarantee system startup at 10.8V using Equation 11.

$$K = \frac{1.0V}{10.8V} = 0.926$$

set  $R_2 = 10k\Omega$

$R_1 = 98k\Omega$

**PMBus Address Programming**

The PMBus address is programmed to one of 16 values using the external resistor, as shown in Table 6.

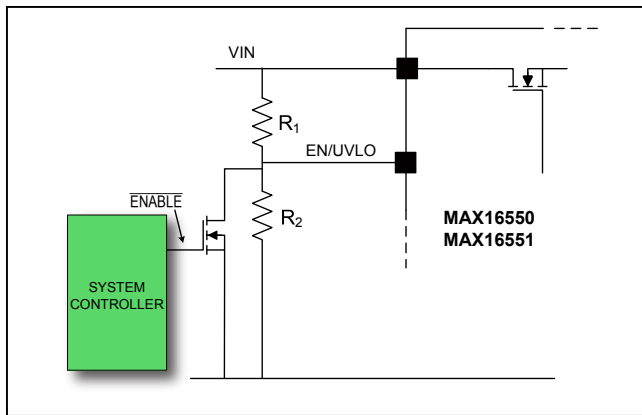


Figure 5. Programming Resistors for Input UVLO

**Table 6. PMBus Address Programming Resistor Values**

VALUE	R_SMBUS_ID (kΩ)	SMBus ID
0	1.78	40h
1	2.37	41h
2	3.16	42h
3	4.22	43h
4	5.62	44h
5	7.5	45h
6	9.76	46h
7	13	47h
8	17.4	10h
9	23.2	11h
10	30.9	12h
11	41.2	13h
12	54.9	50h
13	73.2	51h
14	97.6	52h
15	127	53h

**Note:** RSMBus\_ID should be 1% or better.

**ILOAD Reporting**

The current-reporting voltage is set using an external resistor connected from ILOAD to ground. The maximum voltage is shown in the *Electrical Characteristics* table. The reporting voltage gain is given by Equation 12. Assuming a maximum signal voltage of 1.35V, Equation 14 can be used to select a value for  $R_{ILOAD}$  based on a desired full-scale current.

**Equation 12:**

$$V_{ILOAD} = R_{ILOAD} \times I_{LOAD} \times G_{ILOAD}$$

**Equation 13:**

$$R_{ILOAD} = \frac{1.35V}{I_{LOAD\_FSD} \times G_{ILOAD}}$$

where:

$V_{ILOAD}$  = Current-reporting voltage (V)

$R_{ILOAD}$  = External current-reporting resistor (kΩ)

# MAX16550

## Integrated Protection IC on 12V Bus with an Integrated MOSFET, Lossless Current Sensing, and PMBus Interface

$I_{LOAD}$  = Load current  $I_{OUT} = I_{IN}$  (A)

$I_{LOAD\_FSD}$  = Desired full-scale of current reporting (A)

$G_{ILOAD}$  = Current-reporting gain from the [Electrical Characteristics](#) table

For example, to set the full-scale current reported to 23A:

$$RI_{LOAD} = \frac{1.35V}{23A \times (5 \times 10^{-6})}$$
$$= 11.8K\Omega$$

### MAX16550 PMBus Reporting and Warning Settings

The ICs provide single-sample, averaged and peak values for voltage, current, and power reporting, as well as single reading or averaged readings for warnings. The limits for these parameters and warnings should be set through PMBus prior to operation if a value other than the default is required.

Averaging for voltage, power, and current uses a “accumulate-and-dump” technique, whereas temperature uses a shifting window/rolling average. Power is calculated for every voltage and current sample (as opposed to using averaged voltage and current), and the result is accumulated in a dedicated register for averaging.

Two independently programmable averaging sample sizes are used for reporting and warning/status register use for voltage, current and power:

- Reporting:  $2^N$  samples, with  $N = 0$  to 16 (1 sample to 32K samples)
  - Sample size is set using Reg\_DDh (CONFIG\_2, manufacturer-specific register)
- Warning:  $2^M$  samples, with  $M = 0$  to 3 (1 sample to 8 samples)
  - Sample size is set using Reg D0h (CONFIG, manufacturer-specific register)

The ICs support fault and status reporting except for  $V_{BST\_UVLO}$  fault at startup. If the  $V_{BST\_UVLO}$  occurs at startup the device latches off,  $\overline{FAULT}$  is not reported, and status registers are not updated.

### Setting PMBus-Programmable Parameters

See [Table 7](#) for parameters that are programmed through the PMBus. If a setting other than the default shown below is required, it must be programmed through PMBus. Note that some parameters have an enable bit as well as value bits.

**Table 7. Parameters Programmed through PMBus and Default Values**

PARAMETER	DEFAULT VALUE
Overtemperature-Protection Threshold	140°C
$V_{OUT}$ PWRGD/Self-Check Thresholds	11V/9V
Moderate OCP Timeout	100µs (MAX16550)
Startup Delay	0µs
Startup OCP Threshold	8A
Severe OCP Threshold	130%
Input OVP Threshold	14V (Disabled by Default)
Overtemperature Warning Threshold	220°C (Disabled by Default)
Pin Warning Threshold	(Disabled by Default)
Overcurrent Warning	(Disabled by Default)
$V_{IN}$ Undervoltage Warning	(Disabled by Default)
$V_{OUT}$ Undervoltage Warning	(Disabled by Default)
Current Hysteresis	(Disabled by Default)

### SMBus/PMBus Registers

#### STATUS\_MFR\_SPECIFIC Register (80h)

This is a single-byte register used to read the status of the self-check and fault indicators.

#### ALERT Behavior

Any of the STATUS bits (with some exception) assert the alert line low.

Exceptions are:

- Bit OFF of STATUS\_BYTE/STATUS\_WORD
- Bit POWERGOOD#/MFR\_SPECIFIC of STATUS\_WORD

Alert line can be configured to mask any of the STATUS bits using the SMBALERT\_MASK register.

The only ways to release the alert line are:

- CLEAR\_FAULTS command
- ARA (refer to the SMBus spec v2.0)

The MFR\_DATE register returns a byte from which it's possible to recover the manufacture date (monthly) with [Table 10](#).

**Table 8. PMBus/SMBus Registers**

ADDRESS (HEX)	PROGRAMMABILITY (Note 1)	TYPE	BYTES	DEFAULT (HEX)
1	OPERATION	RW	1	80
3	CLEAR_FAULTS	WO	0	0
19	CAPABILITY	RO	1	B0
1B	SMBALERT_MASK	(Note 2)	2	0000
43	VOUT_UV_WARN_LIMIT	RW	2	0000
4A	IOUT_OC_WARN_LIMIT	RW	2	03FF
4F	OT_FAULT_LIMIT	RW	2	0358
51	OT_WARN_LIMIT	RW	2	03FF
58	VIN_UV_WARN_LIMIT	RW	2	0000
59	VIN_UV_FAULT_LIMIT	RW	2	0000
6B	PIN_OP_WARN_LIMIT	RW	2	0000
78	STATUS_BYTE	RO	1	0
79	STATUS_WORD	RO	2	0
7A	STATUS_VOUT	RO	1	0
7B	STATUS_IOUT	RO	1	0
7C	STATUS_INPUT	RO	1	0
7D	STATUS_TEMPERATURE	RO	1	0
7E	STATUS_CML	RO	1	0
80	STATUS_MFR_SPECIFIC	RO	1	0
86	READ_EIN	RO	7	0
88	READ_VIN	RO	2	0
89	READ_IIN	RO	2	0
8B	READ_VOUT	RO	2	0
8C	READ_IOUT	RO	2	0
8D	READ_TEMPERATURE	RO	2	0
97	READ_PIN	RO	2	0
98	PMBUS_REVISION	RO	1	2
99	MFR_ID	BLK	6	MAXIM
9A	MFR_MODEL	BLK	6	16550/ 16551
9B	MFR_REVISION	BLK	2	1
9D	MFR_DATE	RO	1	See Table 10
D0	CONFIG	RW	2	0
D1	PEAK_VIN	RO	2	0

**Table 8. PMBus/SMBus Registers (continued)**

ADDRESS (HEX)	PROGRAMMABILITY (Note 1)	TYPE	BYTES	DEFAULT (HEX)
D2	PEAK_IOUT	RO	2	0
D3	PEAK_PIN	RO	2	0
D4	PEAK_TEMP	RO	2	0
D5	CLEAR_PEAKS	WO	0	0
DD	CONFIG2	RW	1	0
F2	MFR_SPEC_HYSTL	RW	2	03FF
F3	MFR_SPECT_HYSTH	RW	2	03FF
F4	MFR_SPEC_HYST_STAT	RO	1	0
F5	PIN_OP_FAULT_LIMIT	RW	2	5540
FD	PEAK_VOUT	RO	2	0

**Note 1:** Registers shown in bold (1h - 9Dh) comply with PMBus Power Management Management Protocol Specifications. Refer to the PMBus specification and see [Table 15](#) for more details.

**Note 2:** SMBALERT\_MASK is written to a `write_word` command and read with a read from a `write_block_read_process_call` with a `num_bytes` field of 1.

**Table 9. Register 80h**

BIT #	BIT NAME	DESCRIPTION	READING	INDICATION
[7]	SELFCHECK_FAULT	Pass FET and Soft-Start Self-Check	0	Pass
			1	Fail
[6]	ROCP_FAULT	ROCP Check	0	Pass
			1	Fail
[5]	R_SMBUSID_FAULT	SMBus Programming Resistor Check	0	Pass
			1	Fail
[4]	FOLLOWER_FAULT	Fault Input	0	No Fault Input
			1	Fault Input
[3]	GATE_UVLO_FAULT	V <sub>GS</sub> UVLO Fault	0	No Fault
			1	Fault
[2]	BST_UVLO_FAULT	V <sub>BOOST</sub> UVLO Fault	0	No Fault
			1	Fault
[1]	—	Not Used	0	—
			1	—
[0]	PIN_OP_FAULT	PIN_OP_FAULT	0	Pass
			1	Fault

**Table 10. Lookup Table for MFR\_DATE Register 9Dh**

MFR_DATE[5:0] BINARY	MONTH	YEAR
000000	Jan	2014
000001	Feb	2014
—	—	—
111101	Feb	2019
111110	Mar	2019
111111	Apr	2019







Table 11. MAX16550 PMBus Register Map (continued)

ADDRESS	DEC	NAME	TYPE	WIDTH	DEFAULT	LOW BYTE							HIGH BYTE						
						B7	B6	B5	B4	B3	B2	B1	B0	B15	B14	B13	B12	B11	B10
D0	208	CONFIG	RW	2	0	ocp_cfg	enable_ovp	ovp_th[1]	ovp_th[0]	num_aves_alert[1]	num_aves_alert[0]	ocp_severe_filter[1]	ocp_severe_filter[0]	disable_iadc	ss_cfg[1]	ss_cfg[0]	0	pwrgd_cfg[1]	pwrgd_cfg[0]
D1	209	PEAK_VIN	RO	2	0	vadc_peak[7]	vadc_peak[6]	vadc_peak[5]	vadc_peak[4]	vadc_peak[3]	vadc_peak[2]	vadc_peak[1]	vadc_peak[0]	0	0	0	0	vadc_peak[9]	vadc_peak[8]
D2	210	PEAK_IOUT	RO	2	0	iadc_peak[7]	iadc_peak[6]	iadc_peak[5]	iadc_peak[4]	iadc_peak[3]	iadc_peak[2]	iadc_peak[1]	iadc_peak[0]	0	0	0	0	iadc_peak[9]	iadc_peak[8]
D3	211	PEAK_PIN	RO	2	0	pwr_peak[7]	pwr_peak[6]	pwr_peak[5]	pwr_peak[4]	pwr_peak[3]	pwr_peak[2]	pwr_peak[1]	pwr_peak[0]	pwr_peak[14]	pwr_peak[13]	pwr_peak[12]	pwr_peak[11]	pwr_peak[10]	pwr_peak[9]
D4	212	PEAK_TEMP	RO	2	0	iadc_peak[7]	iadc_peak[6]	iadc_peak[5]	iadc_peak[4]	iadc_peak[3]	iadc_peak[2]	iadc_peak[1]	iadc_peak[0]	0	0	0	0	iadc_peak[9]	iadc_peak[8]
D5	213	CLEAR_PEAKS	WO	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—
D8	216	TRANS0	RO	1	0	trans[0]	trans[0]	trans[0]	trans[0]	trans[0]	trans[0]	trans[0]	trans[0]	trans[0]	trans[0]	trans[0]	trans[0]	trans[0]	trans[0]
D9	217	TRANS1	RO	1	0	trans[1]	trans[1]	trans[1]	trans[1]	trans[1]	trans[1]	trans[1]	trans[1]	trans[1]	trans[1]	trans[1]	trans[1]	trans[1]	trans[1]
DA	218	TRANS2	RO	1	0	trans[2]	trans[2]	trans[2]	trans[2]	trans[2]	trans[2]	trans[2]	trans[2]	trans[2]	trans[2]	trans[2]	trans[2]	trans[2]	trans[2]
DB	219	TRANS3	RO	1	0	trans[3]	trans[3]	trans[3]	trans[3]	trans[3]	trans[3]	trans[3]	trans[3]	trans[3]	trans[3]	trans[3]	trans[3]	trans[3]	trans[3]
DC	220	TRANS4	RO	1	0	trans[4]	trans[4]	trans[4]	trans[4]	trans[4]	trans[4]	trans[4]	trans[4]	trans[4]	trans[4]	trans[4]	trans[4]	trans[4]	trans[4]
DD	221	CONFIG_2	RW	2	0	0	0	0	0	num_aves_reporting[3]	num_aves_reporting[2]	num_aves_reporting[1]	num_aves_reporting[0]	—	—	—	—	—	—
F2	242	MFR_SPECIFIC_HYST_L	RW	2	03FF	hyst[7]	hyst[6]	hyst[5]	hyst[4]	hyst[3]	hyst[2]	hyst[1]	hyst[0]	—	—	—	hyst[9]	hyst[8]	
F3	243	MFR_SPECIFIC_HYST_H	RW	2	03FF	hyst[7]	hyst[6]	hyst[5]	hyst[4]	hyst[3]	hyst[2]	hyst[1]	hyst[0]	—	—	—	hyst[9]	hyst[8]	
F4	244	MFR_SPECIFIC_HYST_STATUS	RO	1	0	0	0	0	0	lout > oc_warm_limit	HYST pin status	HYST > reg_F3	HYST > reg_F2	—	—	—	—	—	
F5	245	PIN_OP_FAULT_LIMIT	RW	2	5540	pin_op_fault<7>	pin_op_fault<6>	pin_op_fault<5>	pin_op_fault<4>	pin_op_fault<3>	pin_op_fault<2>	pin_op_fault<1>	pin_op_fault<0>	pin_op_fault<11>	pin_op_fault<10>	pin_op_fault<9>	pin_op_fault<8>	pin_op_fault<7>	
FD	253	PEAK_VOUT	RO	2	0	vout_peak[7]	vout_peak[6]	vout_peak[5]	vout_peak[4]	vout_peak[3]	vout_peak[2]	vout_peak[1]	vout_peak[0]	0	0	0	0	vout_peak[9]	vout_peak[8]

**CONFIG Register (D0h)**

This is a 2-byte register used to configure the MAX16550/MAX16551 ICs. The default value is 0000h. The meaning of the bits of this register are shown in [Table 12](#).

**CONFIG\_2 Register (DDh)**

This single-byte register allows the selection of the number of samples to average for voltage, current and power reporting. Only bits 3:0 are used; bits 7:4 have no effect and should be left as 0000b. The meaning of the bits of this register are shown in [Table 13](#).

**Peak Voltage, Current, and Power Reporting**

The 2-byte registers shown in [Table 14](#) provides readings of the peak values for input voltage, output current, input power, and temperature in 10 bits direct format.

These registers can be reset with the CLEAR\_PEAKS command (send byte D5h) or power cycling the part.

**PMBus Reporting**

For readings other than direct readings (e.g., Registers D1h, D2h, D3h, D4h, and FDh) PMBus specifications specify that the actual readings in their respective units

correlate with the numerical values read from registers, as shown in Equation 14.

- Current/Voltage/Temperature: 10-bit resolution
- Power: 16-bit resolution

**Equation 14:**

$$X = \frac{1}{m}(Y \times 10^{-R} - b)$$

where:

X = Calculated, “real world” value in the appropriate units (A, V, °C, etc.)

m = Slope coefficient (a 2-byte, two’s complement integer)

Y = 2-byte two’s complement integer received from the PMBus device

b = Offset (a 2-byte, two’s complement integer)

R = Exponent (a 1-byte, two’s complement integer)

The values used in the ICs for the parameters above are shown in [Table 15](#). Note that current and power readings depend on the value of R<sub>LOAD</sub>, the external current reporting resistor.

Table 12. CONFIG Register (D0h)

BIT NO.	BIT NAME	SETTINGS	DESCRIPTION
[15:14]	Ocp_severe_filter[1:0]		Severe OCP deglitch time
		0	0 $\mu$ s
		1	1 $\mu$ s
		10	2 $\mu$ s
[13]	I-ADC disable	11	10 $\mu$ s
		0	I-ADC Enabled (default value)
		1	I-ADC Disabled
		0	Soft-Start Delay = 0ms (default value)
[12:11]	ss_cfg[1:0]	1	Soft-Start Delay = 10ms
		10	Soft-Start Delay = 20ms
		11	Not Used
		0	—
[10]	Not Used	1	—
		0	Power-Good Threshold = 11V, Self-Check Threshold = 9V
[9:8]	pwrzd_th[1:0] (Notes 3, 4)	1	Power-Good Threshold = 10V, Self-Check Threshold = 8V
		10	Power-Good Threshold = 9V, Self-Check Threshold = 7V
		11	Power-Good Threshold = 8V, Self-Check Threshold = 6V
		0	Severe OCP = 130% of Reference OCP (default value)
[7]	ocp_cfg	1	Severe OCP = 170% of Reference OCP
		0	<b>MAX16550</b> – Moderate OCP timeout = 100 $\mu$ s (default value)
[6:5]	mopc_cfg[1:0]	1	<b>MAX16550</b> – Moderate OCP timeout = 250ms
		10	<b>MAX16550</b> – Moderate OCP timeout = 100ms
		11	<b>MAX16550</b> – Moderate OCP timeout = 10 $\mu$ s
		0	V <sub>IN</sub> OVP Protection Disabled (default value)
[4]	enable_ovp	1	V <sub>IN</sub> OVP Protection Enabled
		0	Set V <sub>IN</sub> OVP Threshold = 14V (default value)
[3:2]	ovp_th[1:0]	1	Set V <sub>IN</sub> OVP Threshold = 16V
		10	Set V <sub>IN</sub> OVP Threshold = 18V
		11	Not used
		0	Sets Averaging for PMBus Warning Levels to 1 Sample (default value)
[1:0]	num_aves_alert[1:0]	1	Sets Averaging for PMBus Warning Levels to 2 Samples
		10	Sets Averaging for PMBus Warning Levels to 4 Samples
		11	Sets Averaging for PMBus Warning Levels to 8 Samples
		0	

**Table 13. Averaging Sample Size Settings Using Register DDh**

BITS #	SETTING	STARTUP OCP, NUMBER OF SAMPLES USED FOR REPORTING AVERAGING FOR VOLTAGE, CURRENT AND POWER
[5:4]	su_ocp_cfg	8A 12A 4A 16A
[3:0]	0	1 sample
	1	2 samples
	10	4 samples
	11	8 samples
	100	16 samples
	101	32 samples
	110	64 samples
	111	128 samples
	1000	256 samples
	1001	512 samples
	1010	1024 samples
	1011	2048 samples
	1100	4096 samples
	1101	8192 samples
1110	16384 samples	
1111	32768 samples	

**Table 14. Manufacturer-Specific Direct Reporting Registers**

REGISTER ADDRESS	REGISTER NAME	PARAMETER
D1h	PEAK_VIN	Peak Input Voltage
D2h	PEAK_IOUT	Peak Output Current
D3h	PEAK_PIN	Peak Input Power
D4h	PEAK_TEMP	Peak Temperature
FDh	PEAK_VOUT	Peak Output Voltage

**Table 15. PMBus Equation Parameters**

PMBUS REGISTER	FORMAT	DATA BYTES	m	b	R	UNITS
READ_IOUT (8Ch)*, READ_IIN (89h)*	Direct	2	$3.824 \times R_{LOAD}$	-4300	-3	A
READ_VOUT (8Bh), READ_VIN (88h)	Direct	2	7578	0	-2	V
READ_TEMPERATURE_1 (8Dh)	Direct	2	199	7046	-2	°C
READ_PIN (97h)	Direct	2	$0.895 \times R_{LOAD}$	-9100	-2	W
READ_EIN (86h)**	Direct	2	$3.505 \times R_{LOAD}$	0	-5	**

### Input Capacitance (C<sub>IN</sub>) Selection

Use of input capacitors is highly recommended to guarantee the input voltage is stable and noise free. For applications requiring no input capacitors before the MAX16550, the input-voltage ripple should be less than 300mV peak-to-peak.

### Output Capacitance (C<sub>OUT</sub>) Selection

The maximum output capacitance can be calculated as shown in Equation 15.

**Equation 15:**

$$C_{OUT} = \frac{(I_{INRUSH} \times C_{SS})}{I_{SS}}$$

where:

C<sub>SS</sub> = Soft-start programming capacitance.

I<sub>SS</sub> = Soft-start current, 30μA (typ).

C<sub>OUT</sub> = Maximum load capacitance that can be used at soft-start with a purely capacitive load.

I<sub>INRUSH</sub> = Desired maximum inrush current during start-up. Select I<sub>INRUSH</sub> lower than programmed MAX16550 startup OCP (I<sub>OCP(STARTUP)</sub>) and within MAX16550 startup SOA, refer to [Figure 2](#).

### Design Example

Assume a design value for maximum inrush current of 10A, and a soft-start capacitance of 25nF.

Assume 12V application and 30μA (typ) soft-start current; soft-start time in this case is 0.01ms. The maximum safe operating output current is 11A at 0.01ms (refer to the Startup SOA in [Figure 2](#)) and the default Startup OCP level is 8A (refer to [Table 4](#)).

The designed maximum inrush current of 5A is lower than 8A Startup OCP and within Startup SOA. The designed value is valid. Hence, the maximum load capacitance is calculated as shown in Equation 16.

**Equation 16:**

$$C_{OUT} = \frac{(5A \times 25nF)}{30\mu A} = 4.17mF$$

### Input TVS Diode Selection

The use of a transient voltage suppression (TVS) diode at input is necessary to clamp input-voltage transient within rating of V<sub>IN</sub> pin of MAX16550 (see the [Absolute Maximum Ratings](#) section).

A general guide to select the proper TVS diode is listed below:

- Choose TVS diode reverse-standoff voltage (V<sub>RWM</sub>) ≥ operating voltage of MAX16550, 12V (typ).
- Choose TVS diode peak-pulse current (I<sub>PPM</sub>) ≥ maximum transient peak-pulse current of the MAX16550, 30A (typ).
- Choose TVS clamping voltage (V<sub>C</sub>) ≤ maximum voltage-handling capability of the MAX16550, 22V (typ) for 150μs.

Recommend SMCJ13A based on selection criteria above.

### Output Schottky Diode Selection

The use of a Schottky diode at output is necessary to clamp the negative output-voltage spike within the rating of V<sub>OUT</sub> pin of the MAX16550 (see the [Absolute Maximum Ratings](#) section). Select the proper Schottky diode with low forward-voltage drop (V<sub>F</sub>) and peak forward-surge current (I<sub>FSM</sub>) higher than the expected inductive current.

**Table 16. R<sub>OCP</sub> and R<sub>ILOAD</sub> Selection**

PART	R <sub>OCP</sub>	R <sub>ILOAD</sub>
MAX16550 (30A)	97kΩ	8.2kΩ

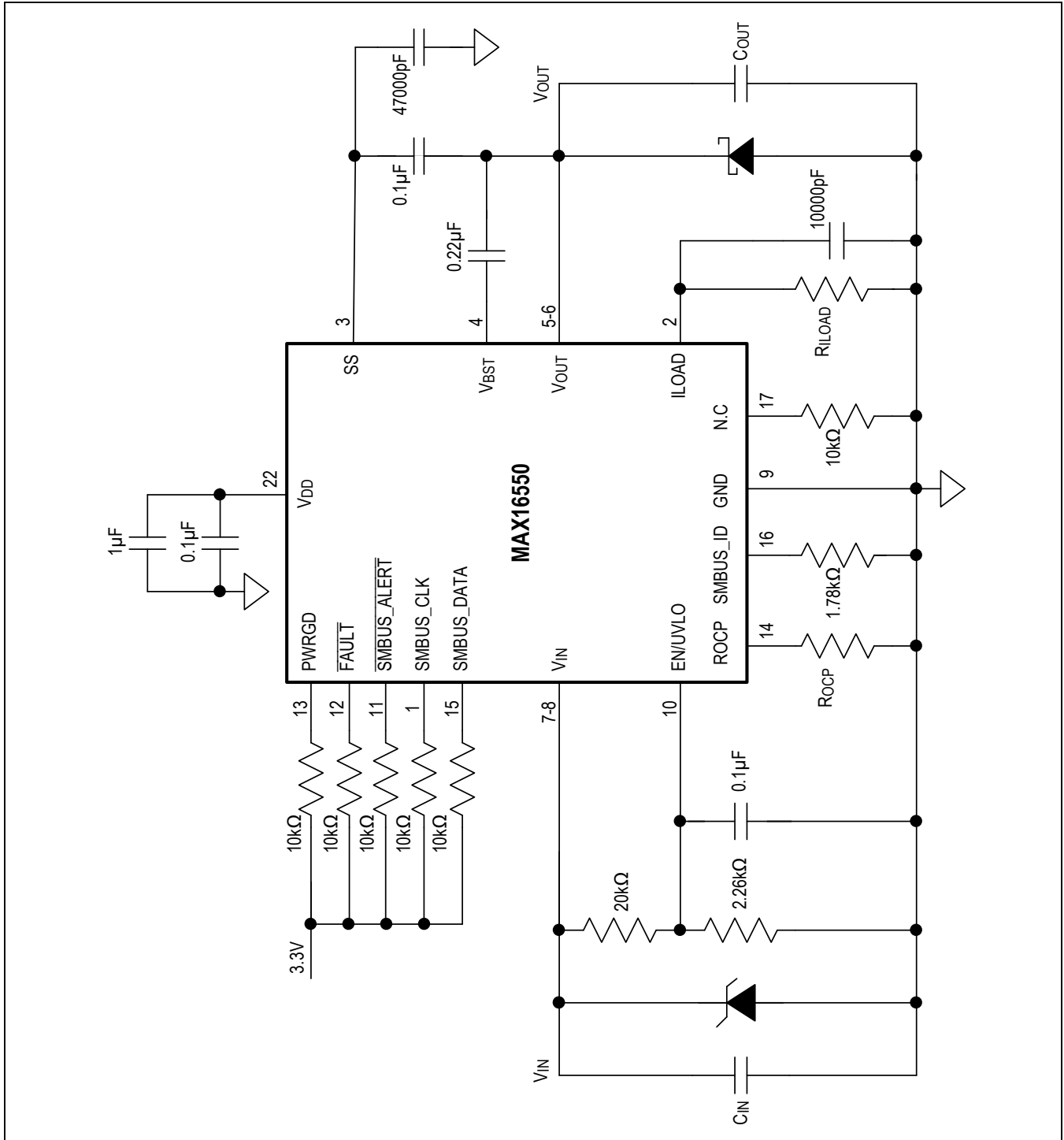


Figure 6. Reference Schematic

## MAX16550 Layout Recommendations

### $V_{IN}$ and $V_{OUT}$

- Minimize input and output trace inductance by using wide and multiple  $V_{IN}$  and  $V_{OUT}$  planes for optimal thermal performance.
- Use multiple vias to connect interlaying power planes.
- Place input capacitors (where applicable) as close to the IC as possible.
- Place output capacitors as close to the IC as possible.
- Place TVS and Schottky diodes close to the IC for tighter coupling to  $V_{OUT}$ , and GND;  $V_{IN}$ , and GND.

### Example

The EV kit layout in [Figure 7](#) shows use of large, wide power planes for  $V_{IN}$  and  $V_{OUT}$  on the top layer.  $C_{IN}$  and  $C_{OUT}$  are close to the IC. The other  $V_{IN}$  and  $V_{OUT}$  power layers are connected with multiple vias between the pins.

### Ground

- Use a trace approximately 1mm wide by 7mm long from the ground pin (pin 13) on the top layer to the underlying ground layers through at least two vias.
- Use a keepout to eliminate all metals directly under the MAX16550 package on the second layer.

### Example

The EV kit layout in [Figure 8](#) and [9](#) show the appropriate ground connection with vias and the ground keepout on Layer 2 (ground). The keepout should extend approximately 30mils outside the MAX16550 package.

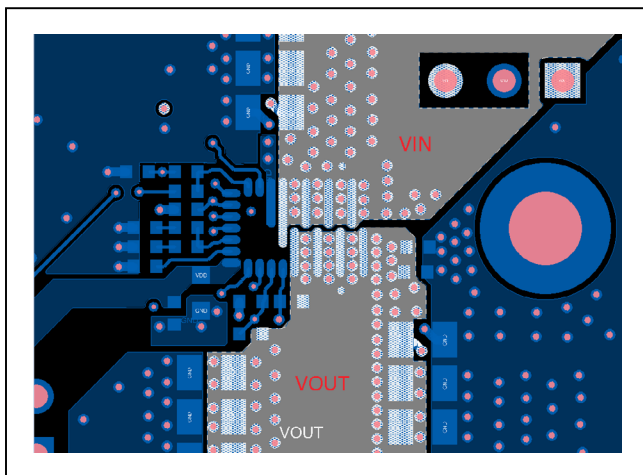


Figure 7. Top Layer (Power)

### $V_{BST}$ and SS

Place the  $V_{BST}$  and SS capacitors on the top layer as close to the pins as possible.

### $V_{DD}$

- Add a  $V_{DD}$  plane on the top layer to decouple the  $V_{DD}$  caps close to the IC to form a tighter loop to ground.
- Place  $V_{DD}$  ground far away from the output capacitor ground.

### ROCP and ILOAD

The ROCP and ILOAD resistors should be placed as close to the IC as possible.

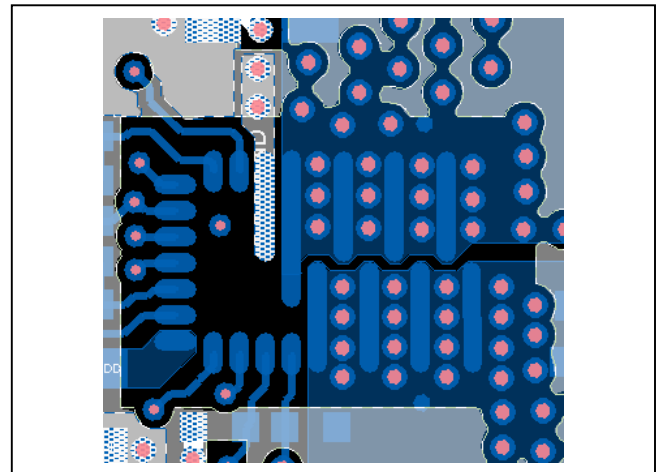


Figure 8. Top Layer (Power) and Layer 2 (GND) with Keepout

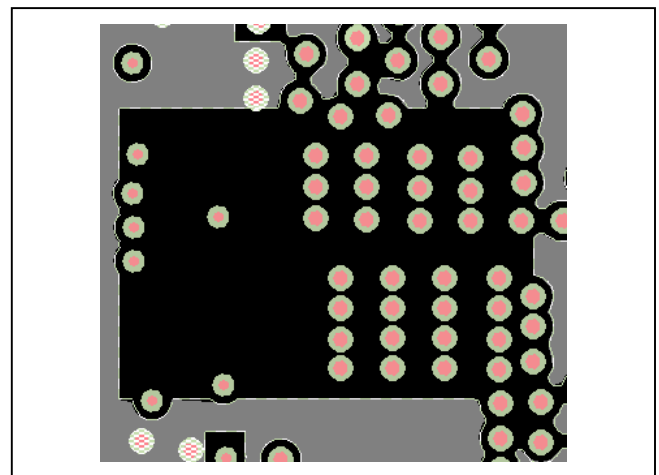


Figure 9. Second Layer (GND) with Keepout



MAX16550

Integrated Protection IC on 12V Bus with an  
Integrated MOSFET, Lossless Current Sensing,  
and PMBus Interface

### Ordering Information

PART*	DESCRIPTION	PACKAGE	SHIPPING METHOD	PACKAGE MARKING
MAX16550GPN+	Protection IC	18 QFN [Type E]	250u Tape & Reel	MAX16550
MAX16550GPN+T			2.5ku Tape & Reel	
MAX16550CGPN+			250u Tape & Reel	MAX16550C
MAX16550CGPN+T			2.5ku Tape & Reel	

*\*These products are completely Halogen-free and Pb-free, employing special materials sets: molding compounds/die attach materials and 100% matte tin plate including anneal. These products are RoHS compliant with an -e3 termination finish and are compatible with both SnPb and Pb-free soldering operations. These products are MSL classified at peak reflow temperatures that meet JEDEC JSTD-020.*

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/16	Initial release	—
1	4/17	Updated <i>Benefits and Features</i> , <i>Absolute Maximum Ratings</i> , <i>Operating Ratings</i> , <i>Typical Operating Characteristics</i> sections, and Equations 2, 6, 9, Equation 9 <i>Design Example</i> , 11, and 13. Updated the <i>Pin Description</i> table, Table 11, and replaced the <i>Basic Application Circuit</i> , Figure 1, and Figure 6. Added <i>Soft-Start</i> , <i>Input Capacitance (C<sub>IN</sub>) Selection</i> , <i>Output Capacitance (C<sub>OUT</sub>) Selection</i> , <i>Input TVS Diode Selection</i> , <i>Output Schottky Diode Selection</i> , and <i>Layout Recommendations</i> sections	1–3, 9–19, 27–29, 32–34, 38–40
2	2/20	Added the MAX16550C part number to the <i>Ordering Information</i> table and added <i>Package Information</i> section	3, 41–43
3	8/20	Removed MAX16551	All

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