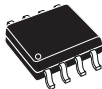


Very high accuracy (70 μ V), high bandwidth (3 MHz), high temperature (175 $^{\circ}$ C), zero-drift operational amplifiers



SOT23-5



SO8


Maturity status link

[TSZ181H1, TSZ182H1](#)

Related products

| | |
|---------------------|-----------------------------------|
| TSZ181H, TSZ182H | For - 40 / 150 $^{\circ}$ C range |
| TSZ181, TSZ182 | For - 40 / 125 $^{\circ}$ C range |

Features

- AEC-Q100 qualified 
- Very high accuracy and stability:
 - 70 μ V max. offset voltage at 25 $^{\circ}$ C
 - 100 μ V offset voltage over full temperature range
- Rail-to-rail input and output
- Low supply voltage: 2.2 - 5.5 V
- Low power consumption: 1 mA max. at 5 V
- Gain bandwidth product: 3 MHz
- Automotive qualification
- Extended temperature range: -40 to 175 $^{\circ}$ C
- Micropackage: SOT23-5, SO8
- Benefits:
 - Higher accuracy without calibration
 - Accuracy virtually unaffected by temperature change

Applications

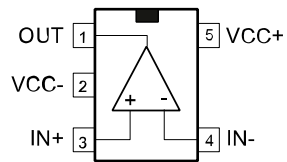
- High accuracy signal conditioning
- Current measurement
- Sensor signal conditioning
- Automotive

Description

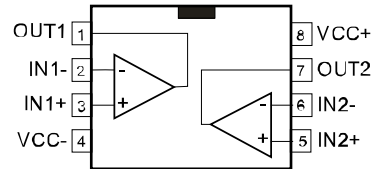
The **TSZ181H1** single and **TSZ182H1** dual operational amplifiers feature very low offset voltages with virtually zero drift versus temperature changes. The **TSZ181H1** and **TSZ182H1** offer rail-to-rail input and output, excellent speed/power consumption ratio, and 3 MHz gain bandwidth product, while consuming just 1 mA at 5 V. The device operates over an extended range of -40 to +175 $^{\circ}$ C and features an ultra-low input bias current. These features make the **TSZ181H1** and **TSZ182H1** ideal for high-accuracy high-bandwidth sensor interfaces for automotive environment.

1 Pin connections

Figure 1. Pin connections (top view)



SOT23-5 (TSZ181H1)



SO8 (TSZ182H1)

2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|-------------|---|--|------|
| V_{CC} | Supply voltage ⁽¹⁾ | 6 | V |
| V_{id} | Differential input voltage ⁽²⁾ | $\pm V_{CC}$ | V |
| V_{in} | Input voltage ⁽³⁾ | $(V_{CC-}) - 0.2$ to $(V_{CC+}) + 0.2$ | V |
| I_{in} | Input current ⁽⁴⁾ | 10 | mA |
| T_{stg} | Storage temperature | -65 to 150 | °C |
| T_j | Junction temperature | 180 | °C |
| R_{th-ja} | Thermal resistance junction to ambient ^{(5) (6)} | | °C/W |
| | SO8 | 125 | |
| | SOT23-5 | 250 | |
| ESD | Human Body Model (HBM) ⁽⁷⁾ | 4 | kV |
| | Charged Device Model (CDM) ⁽⁸⁾ | 1.5 | |

1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. The differential voltage is the non-inverting input terminal with respect to the inverting input terminal.
3. $V_{CC} - V_{in}$ must not exceed 6 V, V_{in} must not exceed 6 V.
4. Input current must be limited by a resistor in series with the inputs.
5. R_{th} are typical values.
6. Short-circuits can cause excessive heating and destructive dissipation.
7. Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
8. Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to ground.

Table 2. Operating conditions

| Symbol | Parameter | Value | Unit |
|-----------|--------------------------------------|--|------|
| V_{CC} | Supply voltage | 2.2 to 5.5 | V |
| V_{icm} | Common mode voltage on input pins | $(V_{CC-}) - 0.1$ to $(V_{CC+}) + 0.1$ | V |
| T | Operating free-air temperature range | -40 to 175 | °C |

3 Electrical characteristics

Table 3. Electrical characteristics at $V_{CC+} = 2.2\text{ V}$, $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, $T = 25\text{ °C}$, $R_L = 10\text{ k}\Omega$ connected to $V_{CC}/2$ (unless otherwise specified)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------------|---|---|------|-----|------|-------------------------|
| DC performance | | | | | | |
| V_{IO} | Input offset voltage | $T = 25\text{ °C}$ | | 3.5 | 70 | μV |
| | | $T_{min} < T < T_{max}$ | | | 100 | |
| $ \Delta V_{IO}/\Delta T $ | Input offset voltage drift ⁽¹⁾ | $T_{min} < T < T_{max}$ | | | 0.26 | $\mu\text{V}/\text{°C}$ |
| I_{IB} | Input bias current ($V_{OUT} = V_{CC}/2$) ⁽²⁾ | $T = 25\text{ °C}$ | | 30 | 200 | pA |
| | | $T_{min} < T < T_{max}$ | | 225 | | |
| I_{IO} | Input offset current ($V_{OUT} = V_{CC}/2$) ⁽²⁾ | $T = 25\text{ °C}$ | | 60 | 400 | pA |
| | | $T_{min} < T < T_{max}$ | | 150 | | |
| CMR1 | Common-mode rejection ratio ⁽³⁾ , $V_{ic} = 0\text{ V to }V_{CC}$, $V_{OUT} = V_{CC}/2$, $R_L > 1\text{ M}\Omega$ | $T = 25\text{ °C}$ | 88 | 115 | | dB |
| | | $T_{min} < T < T_{max}$ | 86 | | | |
| A_{vd} | Large signal voltage gain, $V_{OUT} = 0.5\text{ V to } (V_{CC} - 0.5\text{ V})$ | $T = 25\text{ °C}$ | 102 | 130 | | dB |
| | | $T_{min} < T < T_{max}$ | 92 | | | |
| V_{OH} | High-level output voltage, $V_{OH} = V_{CC} - V_{OUT}$ | $T = 25\text{ °C}$ | | 15 | 40 | mV |
| | | $T_{min} < T < T_{max}$ | | | 70 | |
| V_{OL} | Low-level output voltage | $T = 25\text{ °C}$ | | 10 | 30 | mV |
| | | $T_{min} < T < T_{max}$ | | | 70 | |
| I_{OUT} | $I_{sink} (V_{OUT} = V_{CC})$ | $T = 25\text{ °C}$ | 4 | 6 | | mA |
| | | $T_{min} < T < T_{max}$ | 1.87 | | | |
| | $I_{source} (V_{OUT} = 0\text{ V})$ | $T = 25\text{ °C}$ | 3.5 | 4 | | |
| | | $T_{min} < T < T_{max}$ | 1.4 | | | |
| I_{CC} | Supply current per channel, $V_{OUT} = V_{CC}/2$, $R_L > 1\text{ M}\Omega$ | $T = 25\text{ °C}$ | | 0.7 | 1 | |
| | | $T_{min} < T < T_{max}$ | | | 1.2 | |
| AC performance | | | | | | |
| GBP | Gain bandwidth product, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$ | $T = 25\text{ °C}$ | 1.6 | 2.3 | | MHz |
| | | $T_{min} < T < T_{max}$ | 1 | | | |
| Φ_m | Phase margin | $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$ | | 59 | | degrees |
| G_m | Gain margin | | | 16 | | dB |
| SR | Slew rate ⁽⁴⁾ | $T = 25\text{ °C}$ | 3 | 4.6 | | V/ μs |
| | | $T_{min} < T < T_{max}$ | 2.5 | | | |
| t_s | Settling time | To 0.1%, $V_{in} = 0.8\text{ V}_{pp}$ | | 500 | | ns |
| e_n | Equivalent input noise voltage density | $f = 1\text{ kHz}$ | | 50 | | nV/ $\sqrt{\text{Hz}}$ |
| | | $f = 10\text{ kHz}$ | | 50 | | |
| e_{n-pp} | Voltage noise | $f = 0.1\text{ to }10\text{ Hz}$ | | 0.6 | | μV_{pp} |
| C_S | Channel separation | $f = 1\text{ kHz}$ | | 120 | | dB |
| t_{init} | Initialization time, $G = 100$ ⁽⁵⁾ | $T = 25\text{ °C}$ | | 60 | | μs |
| | | $T_{min} < T < T_{max}$ | | 120 | | |

1. *Input offset measurements are performed on x100 gain configuration. The amplifiers and the gain setting resistors are at the same temperature.*
2. *Guaranteed by design.*
3. *CMR is defined as $20 \times \text{LOG}(\Delta V_{icm} / \Delta V_{io})$.*
4. *Slew rate value is calculated as the average between positive and negative slew rates.*
5. *Initialization time is defined as the delay between the moment when supply voltage exceeds 2.2 V and output voltage stabilization.*

Table 4. Electrical characteristics at $V_{CC+} = 3.3\text{ V}$, $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, $T = 25\text{ }^{\circ}\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_{CC}/2$ (unless otherwise specified)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------------|---|---|-----|-----|------|--------------------------------|
| DC performance | | | | | | |
| V_{IO} | Input offset voltage | $T = 25\text{ }^{\circ}\text{C}$ | | 2 | 70 | μV |
| | | $T_{min} < T < T_{max}$ | | | 100 | |
| $ \Delta V_{IO}/\Delta T $ | Input offset voltage drift ⁽¹⁾ | $T_{min} < T < T_{max}$ | | | 0.26 | $\mu\text{V}/^{\circ}\text{C}$ |
| I_{IB} | Input bias current ($V_{OUT} = V_{CC}/2$) ⁽²⁾ | $T = 25\text{ }^{\circ}\text{C}$ | | 30 | 200 | pA |
| | | $T_{min} < T < T_{max}$ | | 225 | | |
| I_{IO} | Input offset current ($V_{OUT} = V_{CC}/2$) ⁽²⁾ | $T = 25\text{ }^{\circ}\text{C}$ | | 60 | 400 | |
| | | $T_{min} < T < T_{max}$ | | 150 | | |
| CMR1 | Common-mode rejection ratio ⁽³⁾ , $V_{ic} = 0\text{ V to }V_{CC}$, $V_{OUT} = V_{CC}/2$, $R_L > 1\text{ M}\Omega$ | $T = 25\text{ }^{\circ}\text{C}$ | 96 | 120 | | dB |
| | | $T_{min} < T < T_{max}$ | 94 | | | |
| CMR2 | Common-mode rejection ratio ⁽³⁾ , $V_{OUT} = V_{CC}/2$, $R_L > 1\text{ M}\Omega$ | $T = 25\text{ }^{\circ}\text{C}$, $V_{ic} = 0\text{ to }V_{CC} - 1.8\text{ V}$ | 109 | 132 | | dB |
| | | $T_{min} < T < T_{max}$, $V_{ic} = 0\text{ to }V_{CC} - 2\text{ V}$ | 103 | | | |
| A_{vd} | Large signal voltage gain, $V_{OUT} = 0.5\text{ V to } (V_{CC} - 0.5\text{ V})$ | $T = 25\text{ }^{\circ}\text{C}$ | 110 | 138 | | |
| | | $T_{min} < T < T_{max}$ | 95 | | | |
| V_{OH} | High-level output voltage, $V_{OH} = V_{CC} - V_{OUT}$ | $T = 25\text{ }^{\circ}\text{C}$ | | 16 | 40 | mV |
| | | $T_{min} < T < T_{max}$ | | | 70 | |
| V_{OL} | Low-level output voltage | $T = 25\text{ }^{\circ}\text{C}$ | | 11 | 30 | mV |
| | | $T_{min} < T < T_{max}$ | | | 70 | |
| I_{OUT} | $I_{sink} (V_{OUT} = V_{CC})$ | $T = 25\text{ }^{\circ}\text{C}$ | 10 | 15 | | mA |
| | | $T_{min} < T < T_{max}$ | 6.1 | | | |
| | $I_{source} (V_{OUT} = 0\text{ V})$ | $T = 25\text{ }^{\circ}\text{C}$ | 6 | 11 | | |
| | | $T_{min} < T < T_{max}$ | 2.8 | | | |
| I_{CC} | Supply current per channel, $V_{OUT} = V_{CC}/2$, $R_L > 1\text{ M}\Omega$ | $T = 25\text{ }^{\circ}\text{C}$ | | 0.7 | 1 | |
| | | $T_{min} < T < T_{max}$ | | | 1.2 | |
| AC performance | | | | | | |
| GBP | Gain bandwidth product, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$ | $T = 25\text{ }^{\circ}\text{C}$ | 2 | 2.8 | | MHz |
| | | $T_{min} < T < T_{max}$ | 1.2 | | | |
| Φ_m | Phase margin | $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$ | | 56 | | degrees |
| G_m | Gain margin | | | 15 | | dB |
| SR | Slew rate ⁽⁴⁾ | $T = 25\text{ }^{\circ}\text{C}$ | 2.6 | 4.5 | | $\text{V}/\mu\text{s}$ |
| | | $T_{min} < T < T_{max}$ | 2.1 | | | |
| t_s | Settling time | $T_0\text{ to }0.1\%$, $V_{in} = 1.2\text{ V}_{pp}$ | | 550 | | ns |
| e_n | Equivalent input noise voltage density | $f = 1\text{ kHz}$ | | 40 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| | | $f = 10\text{ kHz}$ | | 40 | | |
| e_{n-pp} | Voltage noise | $f = 0.1\text{ to }10\text{ Hz}$ | | 0.5 | | μV_{pp} |
| C_S | Channel separation | $f = 1\text{ kHz}$ | | 120 | | dB |
| t_{init} | Initialization time, $G = 100$ ⁽⁵⁾ | $T = 25\text{ }^{\circ}\text{C}$ | | 60 | | μs |
| | | $T_{min} < T < T_{max}$ | | 120 | | |

1. *Input offset measurements are performed on x100 gain configuration. The amplifiers and the gain setting resistors are at the same temperature.*
2. *Guaranteed by design.*
3. *CMR is defined as $20 \times \text{LOG}(\Delta V_{icm} / \Delta V_{io})$*
4. *Slew rate value is calculated as the average between positive and negative slew rates.*
5. *Initialization time is defined as the delay between the moment when supply voltage exceeds 2.2 V and output voltage stabilization.*

Table 5. Electrical characteristics at $V_{CC+} = 5\text{ V}$, $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, $T = 25\text{ }^{\circ}\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_{CC}/2$ (unless otherwise specified)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------------|---|--|-----|-----|------|--------------------------------|
| DC performance | | | | | | |
| V_{IO} | Input offset voltage | $T = 25\text{ }^{\circ}\text{C}$ | | 1 | 70 | μV |
| | | $T_{min} < T < T_{max}$ | | | 100 | |
| $ \Delta V_{IO}/\Delta T $ | Input offset voltage drift ⁽⁵⁾ | $T_{min} < T < T_{max}$ | | | 0.26 | $\mu\text{V}/^{\circ}\text{C}$ |
| I_{IB} | Input bias current ($V_{OUT} = V_{CC}/2$) ⁽²⁾ | $T = 25\text{ }^{\circ}\text{C}$ | | 30 | 200 | pA |
| | | $T_{min} < T < T_{max}$ | | 225 | | |
| I_{IO} | Input offset current ($V_{OUT} = V_{CC}/2$) ⁽²⁾ | $T = 25\text{ }^{\circ}\text{C}$ | | 60 | 400 | |
| | | $T_{min} < T < T_{max}$ | | 150 | | |
| CMR1 | Common-mode rejection ratio ⁽³⁾ , $V_{ic} = 0\text{ V to }V_{CC}$, $V_{OUT} = V_{CC}/2$, $R_L > 1\text{ M}\Omega$ | $T = 25\text{ }^{\circ}\text{C}$ | 103 | 126 | | |
| | | $T_{min} < T < T_{max}$ | 101 | | | |
| CMR2 | Common-mode rejection ratio ⁽³⁾ , $V_{OUT} = V_{CC}/2$, $R_L > 1\text{ M}\Omega$ | $T = 25\text{ }^{\circ}\text{C}$ $V_{ic} = 0\text{ to }V_{CC} - 1.8\text{ V}$ | 112 | 136 | | |
| | | $T_{min} < T < T_{max}$, $V_{ic} = 0\text{ to }V_{CC} - 2\text{ V}$ | 106 | | | |
| SVR1 | Supply voltage rejection ratio ⁽⁴⁾ , $V_{CC} = 2.2\text{ to }5.5\text{ V}$, $V_{ic} = 0\text{ V}$, $R_L > 1\text{ M}\Omega$ | $T = 25\text{ }^{\circ}\text{C}$ | 101 | 123 | | |
| | | $T_{min} < T < T_{max}$ | 99 | | | |
| A_{vd} | Large signal voltage gain, $V_{OUT} = 0.5\text{ V to }(V_{CC} - 0.5\text{ V})$ | $T = 25\text{ }^{\circ}\text{C}$ | 110 | 144 | | dB |
| | | $T_{min} < T < T_{max}$ | 104 | | | |
| EMIRR | EMI rejection ratio ⁽⁵⁾ | $V_{RF} = 100\text{ mVp}$, $f = 400\text{ MHz}$ | | 52 | | |
| | | $V_{RF} = 100\text{ mVp}$, $f = 900\text{ MHz}$ | | 52 | | |
| | | $V_{RF} = 100\text{ mVp}$, $f = 1800\text{ MHz}$ | | 72 | | |
| | | $V_{RF} = 100\text{ mVp}$, $f = 2400\text{ MHz}$ | | 85 | | |
| V_{OH} | High-level output voltage, $V_{OH} = V_{CC} - V_{OUT}$ | $T = 25\text{ }^{\circ}\text{C}$ | | 18 | 40 | mV |
| | | $T_{min} < T < T_{max}$ | | | 70 | |
| V_{OL} | Low-level output voltage | $T = 25\text{ }^{\circ}\text{C}$ | | 13 | 30 | |
| | | $T_{min} < T < T_{max}$ | | | 70 | |
| I_{OUT} | $I_{sink} (V_{OUT} = V_{CC})$ | $T = 25\text{ }^{\circ}\text{C}$ | 20 | 29 | | mA |
| | | $T_{min} < T < T_{max}$ | 12 | | | |
| | $I_{source} (V_{OUT} = 0\text{ V})$ | $T = 25\text{ }^{\circ}\text{C}$ | 15 | 25 | | |
| | | $T_{min} < T < T_{max}$ | 7 | | | |
| I_{CC} | Supply current per channel, $V_{OUT} = V_{CC}/2$, $R_L > 1\text{ M}\Omega$ | $T = 25\text{ }^{\circ}\text{C}$ | | 0.8 | 1 | |
| | | $T_{min} < T < T_{max}$ | | | 1.2 | |
| AC performance | | | | | | |
| GBP | Gain bandwidth product, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$ | $T = 25\text{ }^{\circ}\text{C}$ | 2 | 3 | | MHz |
| | | $T_{min} < T < T_{max}$ | 1.2 | | | |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------|---|--|-----|-----|-----|------------------------|
| Φ_m | Phase margin | $R_L = 10\text{ k}\Omega, C_L = 100\text{ pF}$ | | 56 | | degrees |
| G_m | Gain margin | | | 15 | | dB |
| SR | Slew rate ⁽⁶⁾ | $T = 25\text{ }^\circ\text{C}$ | 2.9 | 4.7 | | V/ μs |
| | | $T_{\text{min}} < T < T_{\text{max}}$ | 2.4 | | | |
| t_s | Settling time | To 0.1%, $V_{\text{in}} = 1.5\text{ Vpp}$ | | 600 | | ns |
| | | To 0.01%, $V_{\text{in}} = 1\text{ Vpp}$ | | 4 | | μs |
| e_n | Equivalent input noise voltage density | $f = 1\text{ kHz}$ | | 37 | | nV/ $\sqrt{\text{Hz}}$ |
| | | $f = 10\text{ kHz}$ | | 37 | | |
| $e_{n\text{-pp}}$ | Voltage noise | $f = 0.1\text{ to }10\text{ Hz}$ | | 0.4 | | μVpp |
| C_S | Channel separation | $f = 100\text{ Hz}$ | | 135 | | dB |
| t_{init} | Initialization time, $G = 100$ ⁽⁷⁾ | $T = 25\text{ }^\circ\text{C}$ | | 60 | | μs |
| | | $T_{\text{min}} < T < T_{\text{max}}$ | | 100 | | |

1. Input offset measurements are performed on x100 gain configuration. The amplifiers and the gain setting resistors are at the same temperature.
2. Guaranteed by design.
3. CMR is defined as $20 \times \text{LOG}(\Delta V_{\text{icm}} / \Delta V_{\text{io}})$.
4. SVR is defined as $20 \times \text{LOG}(\Delta V_{\text{cc}} / \Delta V_{\text{io}})$.
5. EMIRR is defined as $-20 \text{Log}(V_{\text{RF_Peak}} / \Delta V_{\text{io}})$. Tested on the MiniSO8 package, RF injection on the IN- pin.
6. Slew rate value is calculated as the average between positive and negative slew rates.
7. Initialization time is defined as the delay between the moment when supply voltage exceeds 2.2 V and output voltage stabilization.

4 Typical performance characteristics

Figure 2. Supply current vs. supply voltage

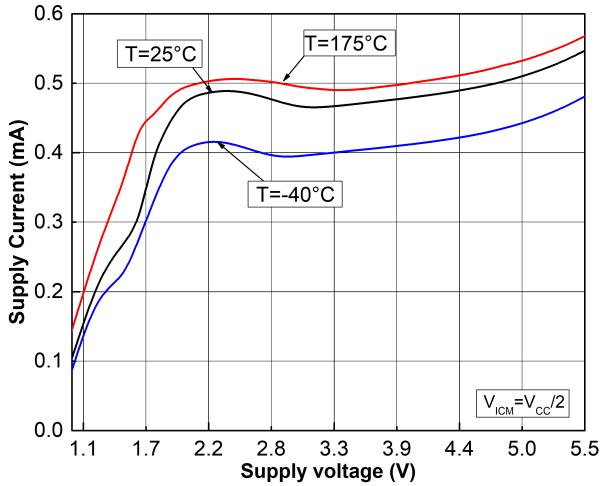


Figure 3. Input offset voltage distribution at $V_{CC} = 5\text{ V}$

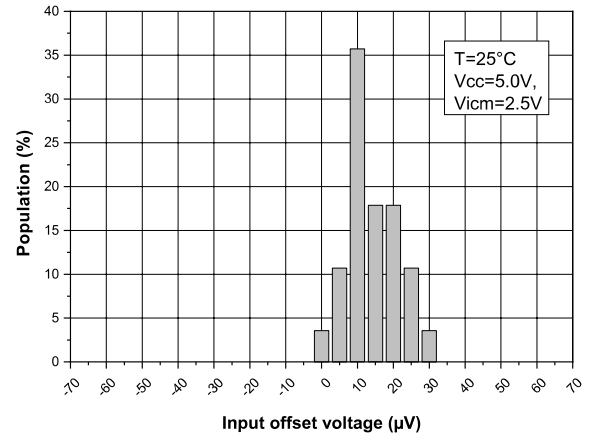


Figure 4. Input offset voltage distribution at $V_{CC} = 3.3\text{ V}$

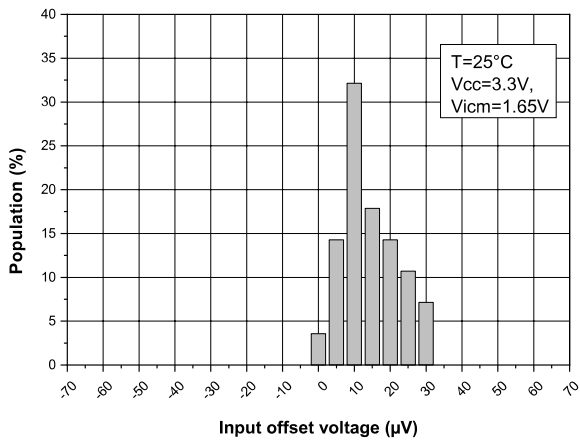


Figure 5. Input offset voltage distribution at $V_{CC} = 2.2\text{ V}$

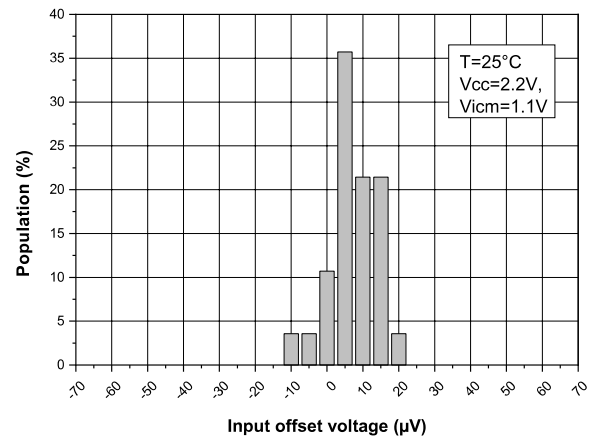


Figure 6. Input offset voltage distribution at $V_{CC} = 5\text{ V}$,
 $T = 175\text{ }^{\circ}\text{C}$

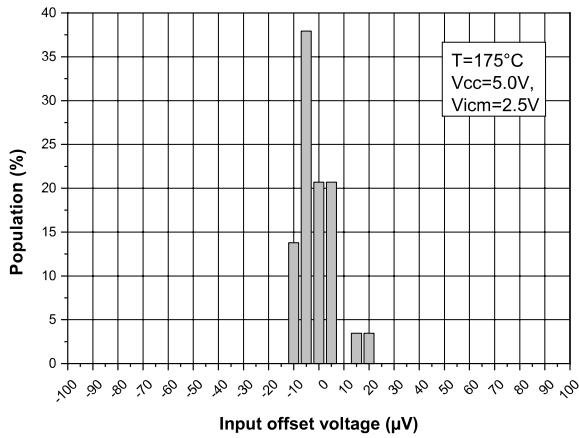


Figure 7. Input offset voltage distribution at $V_{CC} = 5\text{ V}$,
 $T = -40\text{ }^{\circ}\text{C}$

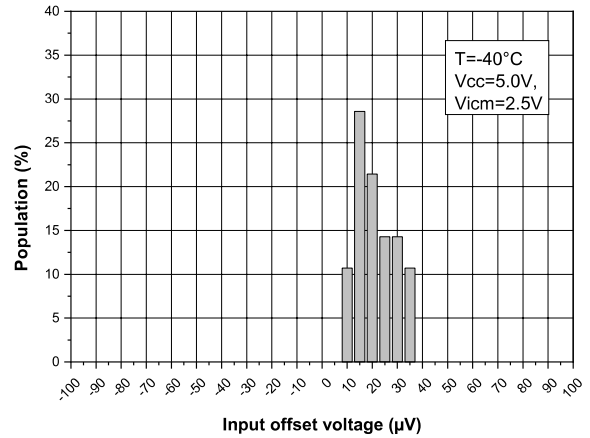


Figure 8. Input offset voltage distribution at $V_{CC} = 2.2\text{ V}$,
 $T = 175\text{ }^{\circ}\text{C}$

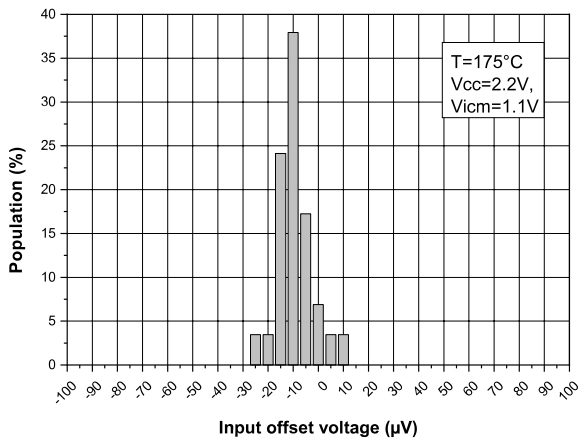


Figure 9. Input offset voltage distribution at $V_{CC} = 2.2\text{ V}$,
 $T = -40\text{ }^{\circ}\text{C}$

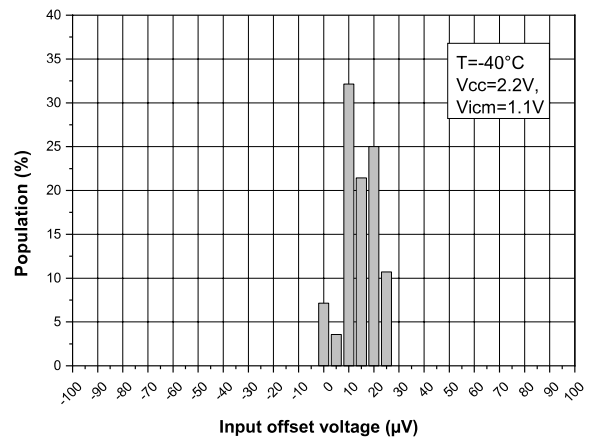


Figure 10. Input offset voltage vs. supply voltage

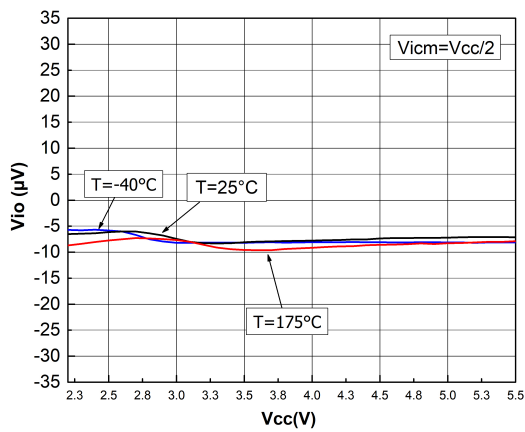


Figure 11. Input offset voltage vs. input common mode at
 $V_{CC} = 5.5\text{ V}$

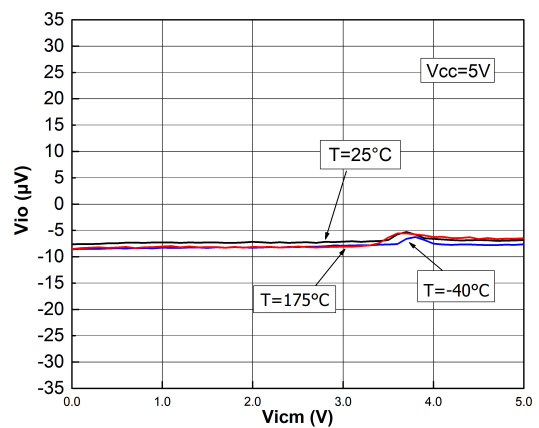


Figure 12. Input offset voltage vs. input common mode at $V_{CC} = 3.3\text{ V}$

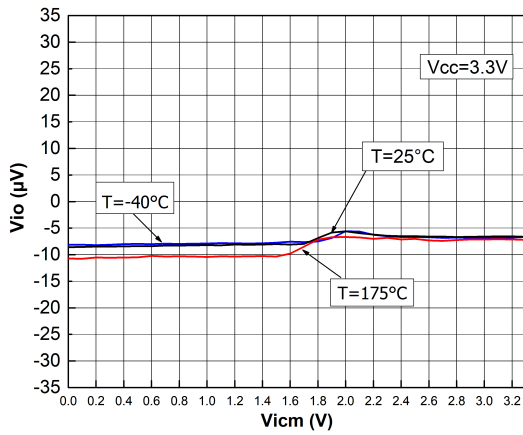


Figure 13. Input offset voltage vs. input common mode at $V_{CC} = 2.2\text{ V}$

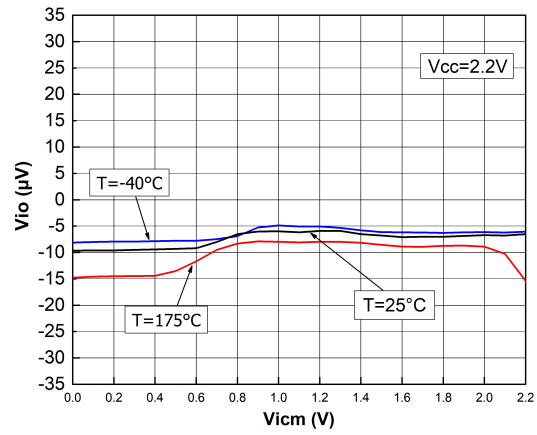


Figure 14. Input offset voltage vs. temperature

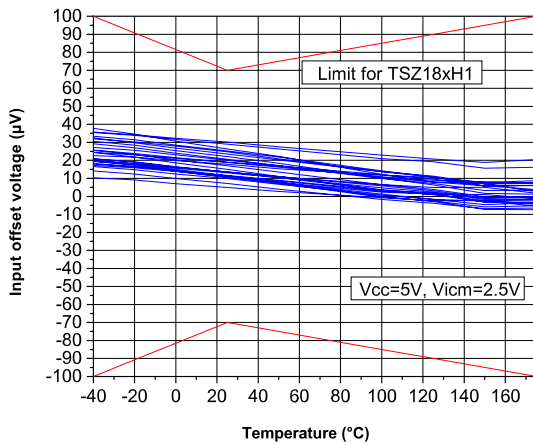


Figure 15. V_{OH} vs. supply voltage

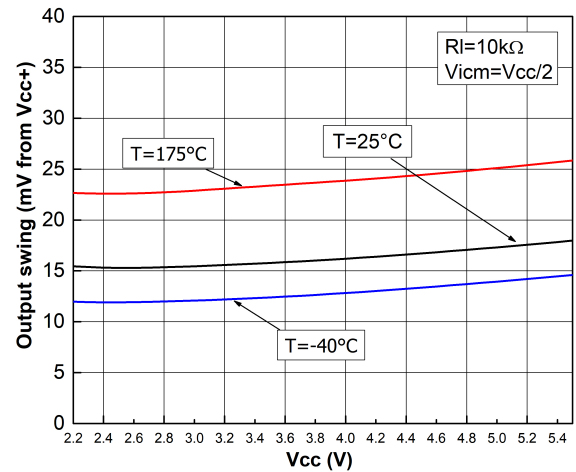


Figure 16. V_{OL} vs. supply voltage

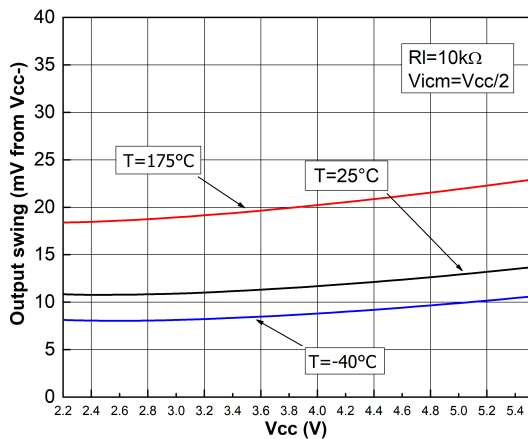


Figure 17. Output current vs. output voltage at $V_{CC} = 5\text{ V}$

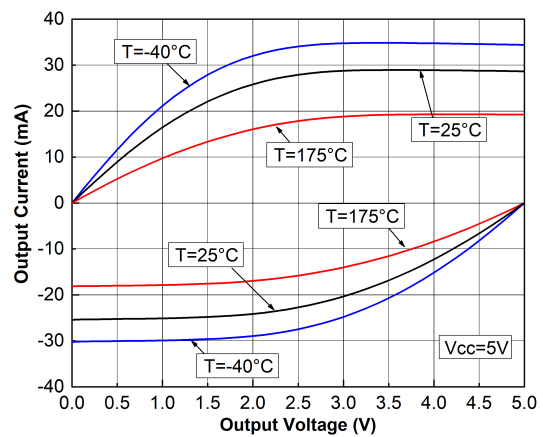


Figure 18. Output current vs. output voltage at $V_{CC} = 2.2\text{ V}$

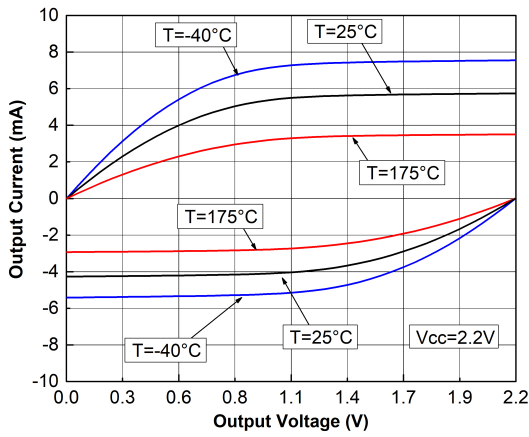


Figure 19. Input bias current vs. common-mode at $V_{CC} = 5\text{ V}$

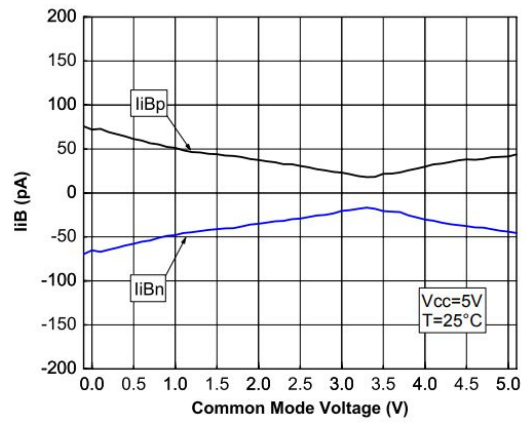


Figure 20. Input bias current vs. temp. at $V_{CC} = 5\text{ V}$

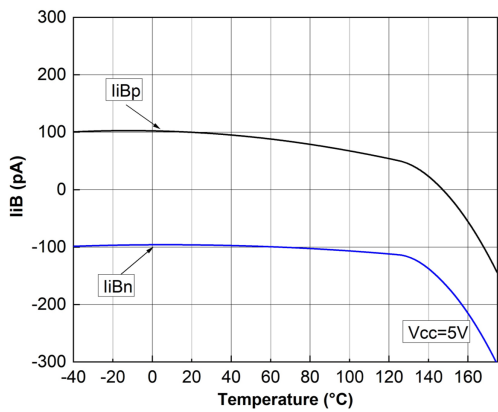


Figure 21. Output rail linearity

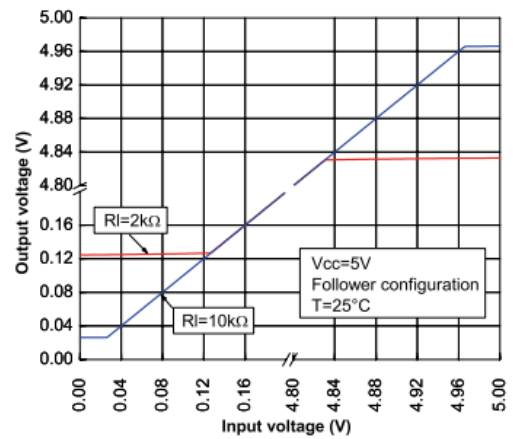


Figure 22. Bode diagram at $V_{CC} = 5\text{ V}$

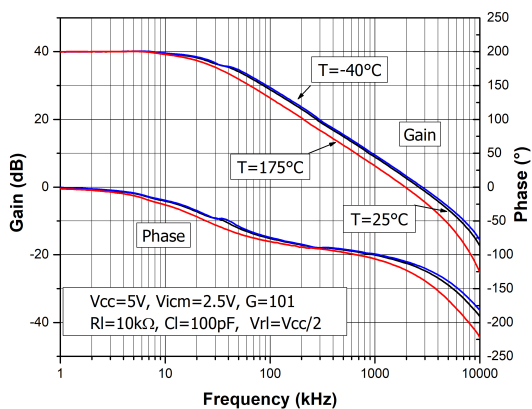


Figure 23. Bode diagram at $V_{CC} = 2.2\text{ V}$

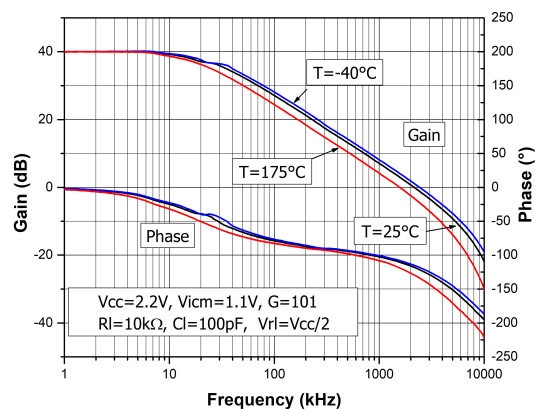


Figure 24. Bode diagram at $V_{CC} = 3.3\text{ V}$

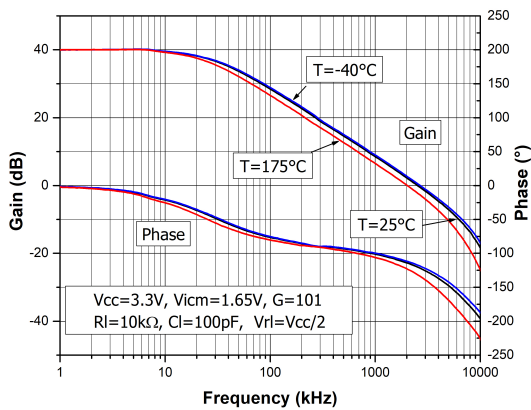


Figure 25. Open loop gain vs. frequency

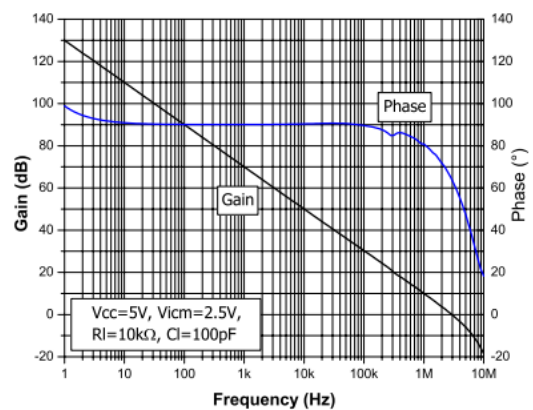


Figure 26. Positive slew rate vs. supply voltage

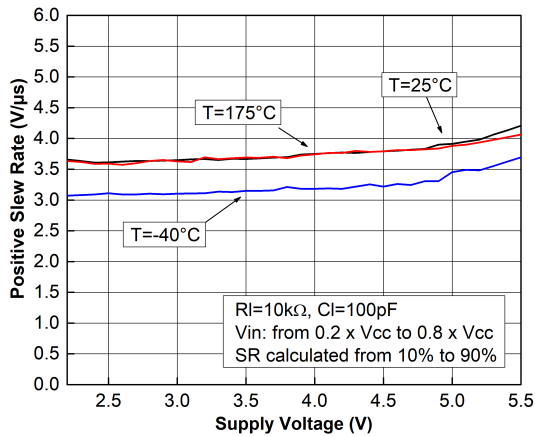


Figure 27. Negative slew rate vs. supply voltage

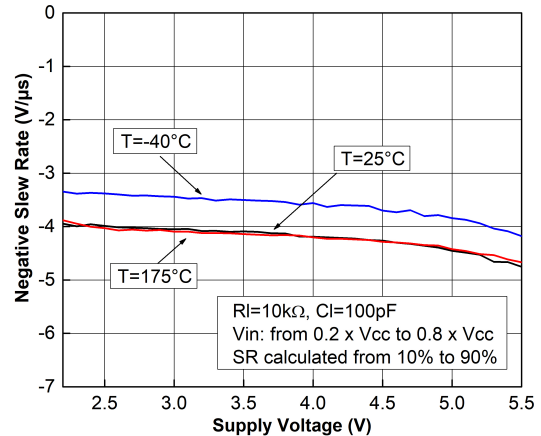


Figure 28. Noise 0.1 – 10 Hz vs. time

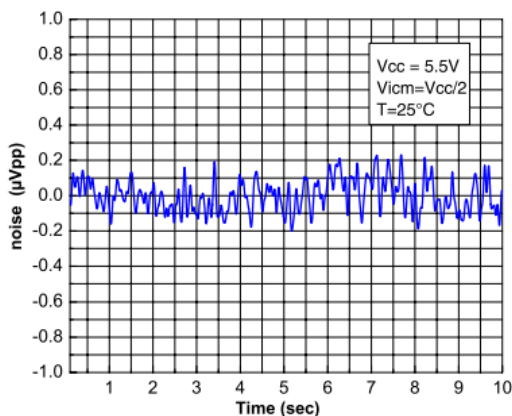


Figure 29. Noise vs. frequency

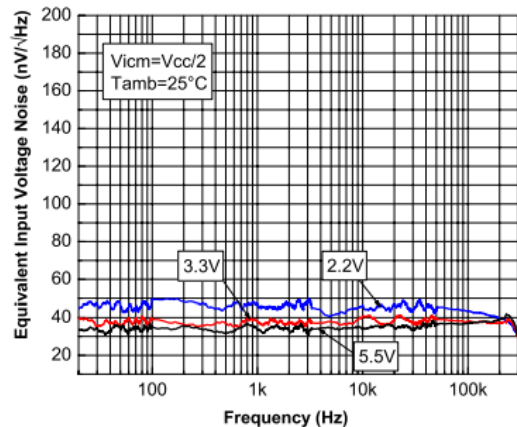


Figure 30. Output overshoot vs. load capacitance

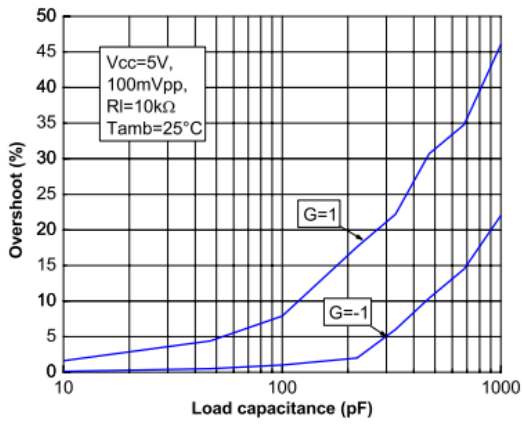


Figure 31. Small signal $V_{CC} = 5 V$

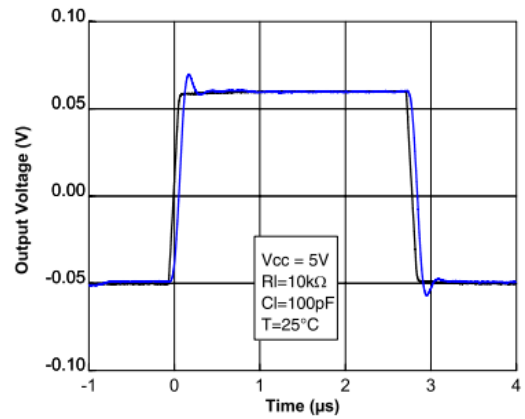


Figure 32. Small signal $V_{CC} = 2.2 V$

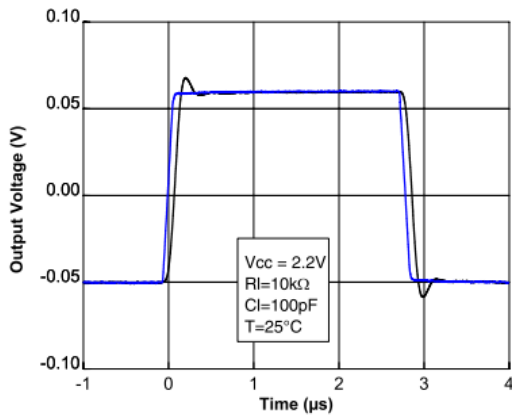


Figure 33. Large signal $V_{CC} = 5 V$

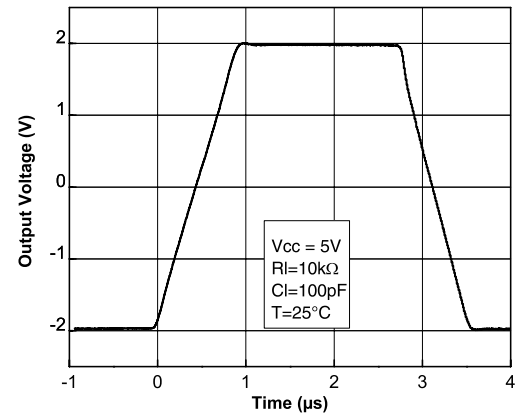


Figure 34. Large signal $V_{CC} = 2.2 V$

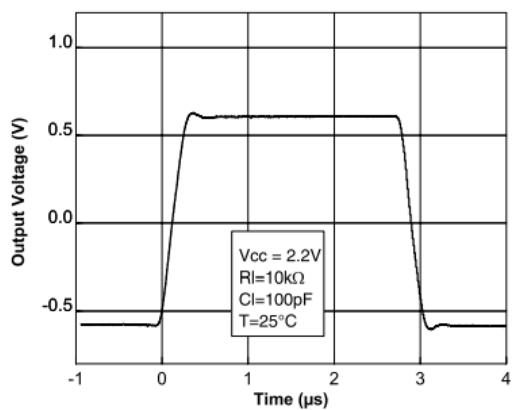


Figure 35. Negative overv. recovery $V_{CC} = 2.2 V$

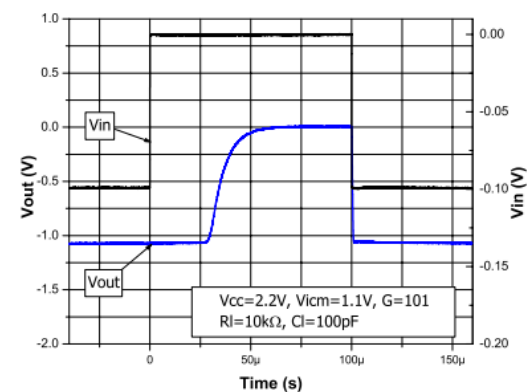


Figure 36. Positive overvoltage recovery $V_{CC} = 5\text{ V}$

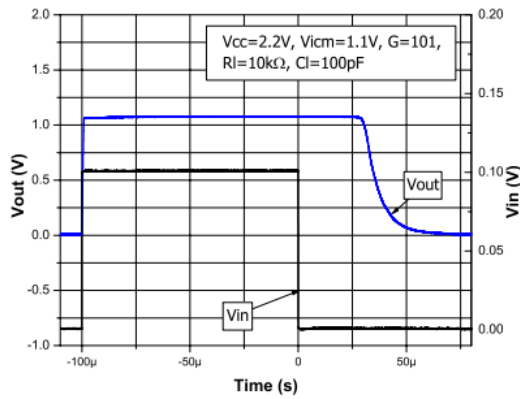


Figure 37. Output impedance vs. frequency

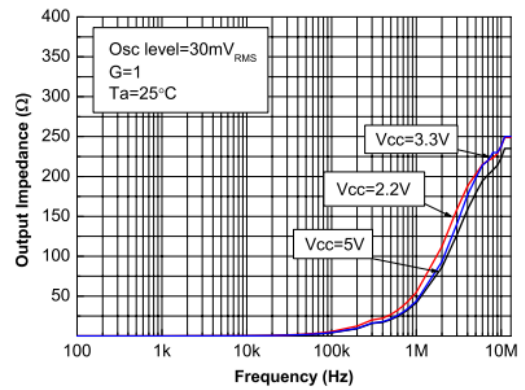


Figure 38. Settling time positive step (-2 V to 0 V)

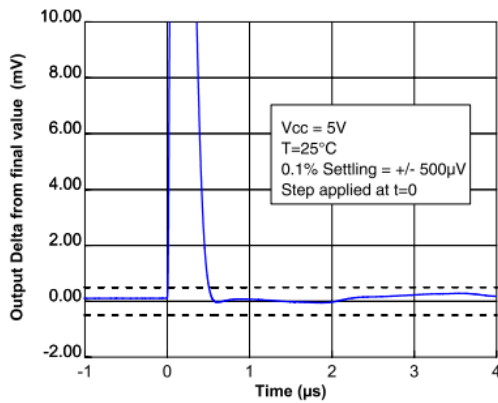


Figure 39. Settling time negative step (2 V to 0 V)

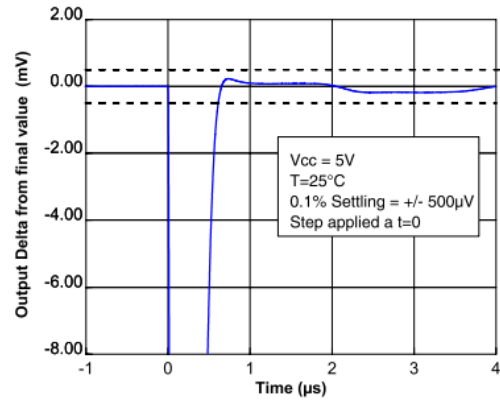


Figure 40. Settling time positive step (-0.8 V to 0 V)

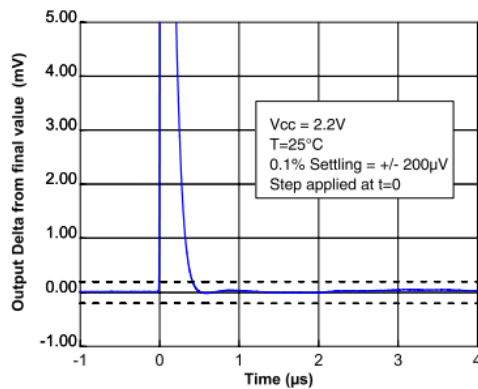


Figure 41. Settling time negative step (0.8 V to 0 V)

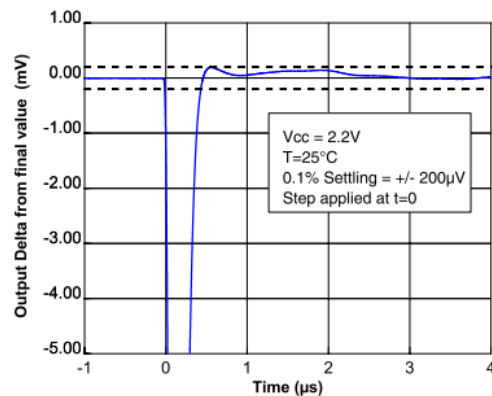


Figure 42. Maximum output voltage vs. frequency

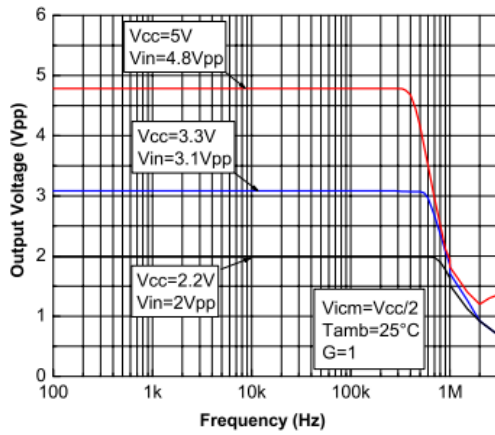


Figure 43. Crosstalk vs. frequency

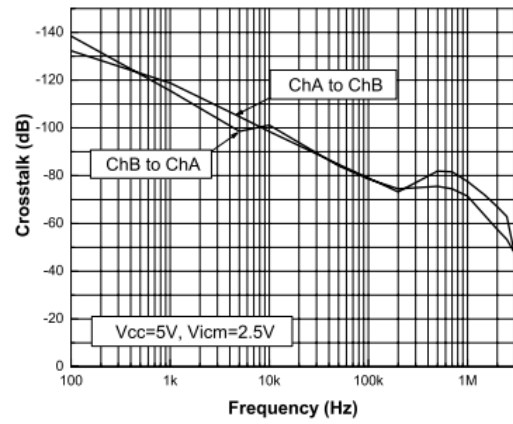
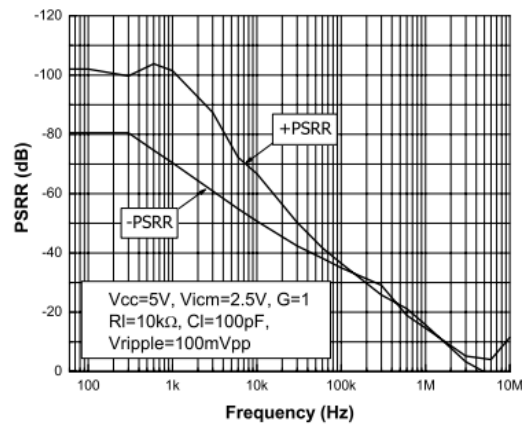
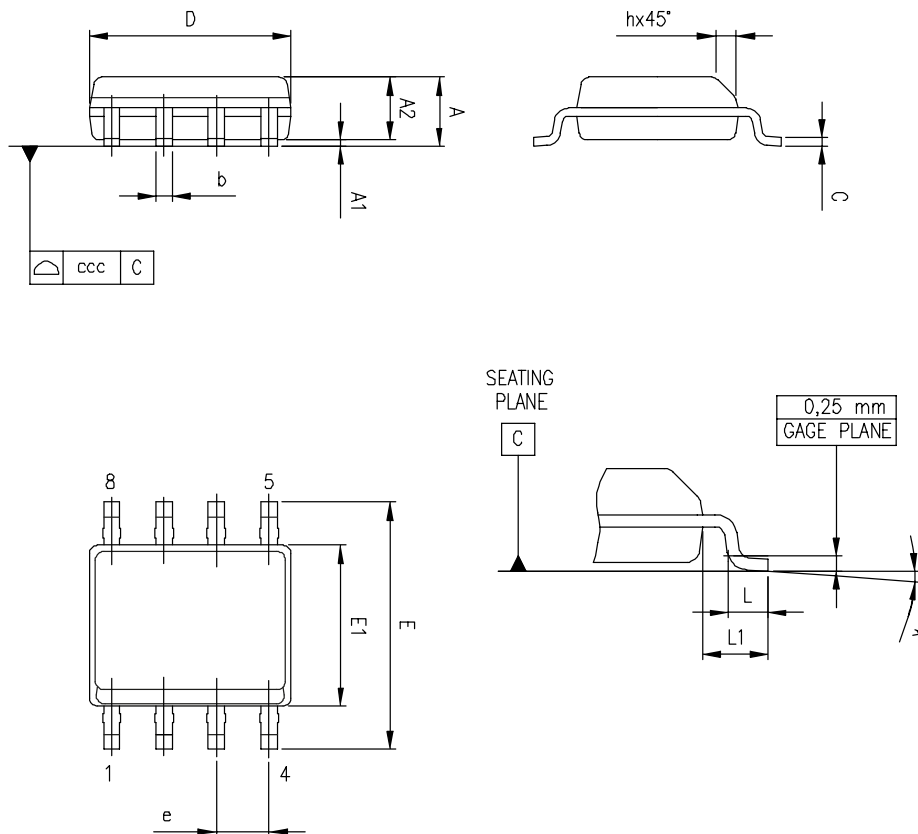


Figure 44. PSRR vs. frequency



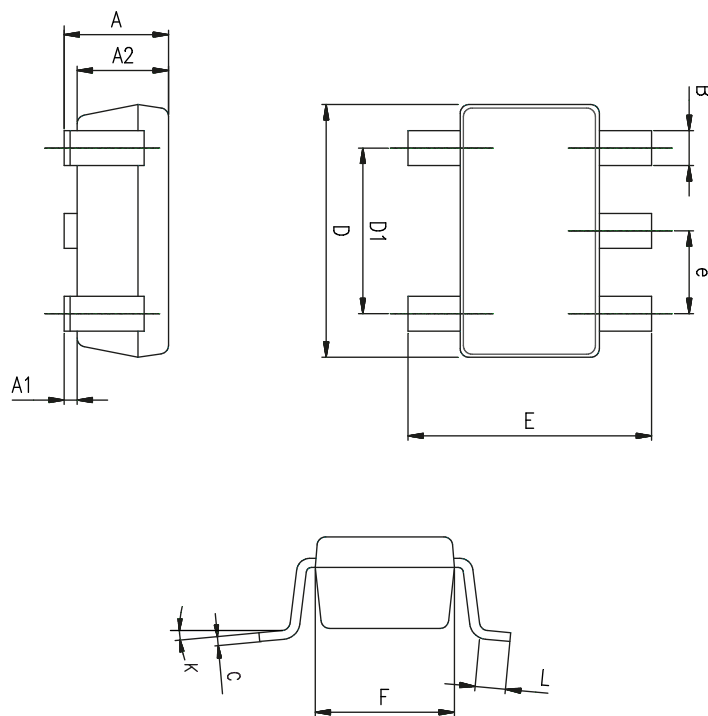
5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 SO8 package information
Figure 45. SO8 package outline

Table 6. SO8 mechanical data

| Dim. | mm | | | Inches | | |
|------|------|------|------|--------|-------|-------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | | | 1.75 | | | 0.069 |
| A1 | 0.1 | | 0.25 | 0.004 | | 0.01 |
| A2 | 1.25 | | | 0.049 | | |
| b | 0.28 | | 0.48 | 0.011 | | 0.019 |
| c | 0.17 | | 0.23 | 0.007 | | 0.01 |
| D | 4.8 | 4.9 | 5 | 0.189 | 0.193 | 0.197 |
| E | 5.8 | 6 | 6.2 | 0.228 | 0.236 | 0.244 |
| E1 | 3.8 | 3.9 | 4 | 0.15 | 0.154 | 0.157 |
| e | | 1.27 | | | 0.05 | |
| h | 0.25 | | 0.5 | 0.01 | | 0.02 |
| L | 0.4 | | 1.27 | 0.016 | | 0.05 |
| L1 | | 1.04 | | | 0.04 | |
| k | 0 | | 8 ° | 1 ° | | 8 ° |
| ccc | | | 0.1 | | | 0.004 |

5.2 SOT23-5 package information

Figure 46. SOT23-5 package outline

Table 7. SOT23-5 mechanical data

| Ref. | Dimensions | | | | | |
|------|-------------|------|------------|-----------|-------|------------|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.90 | 1.20 | 1.45 | 0.035 | 0.047 | 0.057 |
| A1 | | | 0.15 | | | 0.006 |
| A2 | 0.90 | 1.05 | 1.30 | 0.035 | 0.041 | 0.051 |
| B | 0.35 | 0.40 | 0.50 | 0.014 | 0.016 | 0.020 |
| C | 0.09 | 0.15 | 0.20 | 0.004 | 0.006 | 0.008 |
| D | 2.80 | 2.90 | 3.00 | 0.110 | 0.114 | 0.118 |
| D1 | | 1.90 | | | 0.075 | |
| e | | 0.95 | | | 0.037 | |
| E | 2.60 | 2.80 | 3.00 | 0.102 | 0.110 | 0.118 |
| F | 1.50 | 1.60 | 1.75 | 0.059 | 0.063 | 0.069 |
| L | 0.10 | 0.35 | 0.60 | 0.004 | 0.014 | 0.024 |
| K | 0 degrees | | 10 degrees | 0 degrees | | 10 degrees |

6 Ordering information

Table 8. Order code

| Order code | Package | Packaging | Marking |
|----------------------------|---------|-------------|---------|
| TSZ181H1YLT ⁽¹⁾ | SOT23-5 | Tape & Reel | K230 |
| TSZ182H1YDT ⁽¹⁾ | SO8 | Tape & Reel | Z182H1Y |

1. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.

Revision history

Table 9. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 01-Mar-2021 | 1 | Initial release. |
| 17-Jan-2023 | 2 | Added new TSZ181H1YLT part number in Table 8 . Order code and new SOT23-5 package information. Updated title, figure, features and description on the cover page. Updated Figure 1 , Figure 3 , Figure 4 , Figure 5 , Figure 6 , Figure 7 , Figure 8 , Figure 9 and Figure 14 . |

Contents

| | | |
|------------|--|-----------|
| 1 | Pin connections | 2 |
| 2 | Absolute maximum ratings and operating conditions | 3 |
| 3 | Electrical characteristics | 4 |
| 4 | Typical performance characteristics | 10 |
| 5 | Package information | 18 |
| 5.1 | SO8 package information | 19 |
| 5.2 | SOT23-5 package information | 20 |
| 6 | Ordering information | 21 |
| | Revision history | 22 |

List of tables

| | | |
|-----------------|--|----|
| Table 1. | Absolute maximum ratings | 3 |
| Table 2. | Operating conditions | 3 |
| Table 3. | Electrical characteristics at $V_{cc+} = 2.2\text{ V}$, $V_{cc-} = 0\text{ V}$, $V_{icm} = V_{cc}/2$, $T = 25\text{ }^{\circ}\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_{cc}/2$ (unless otherwise specified) | 4 |
| Table 4. | Electrical characteristics at $V_{cc+} = 3.3\text{ V}$, $V_{cc-} = 0\text{ V}$, $V_{icm} = V_{cc}/2$, $T = 25\text{ }^{\circ}\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_{cc}/2$ (unless otherwise specified) | 6 |
| Table 5. | Electrical characteristics at $V_{cc+} = 5\text{ V}$, $V_{cc-} = 0\text{ V}$, $V_{icm} = V_{cc}/2$, $T = 25\text{ }^{\circ}\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_{cc}/2$ (unless otherwise specified) | 8 |
| Table 6. | SO8 mechanical data | 19 |
| Table 7. | SOT23-5 mechanical data | 20 |
| Table 8. | Order code | 21 |
| Table 9. | Document revision history | 22 |

List of figures

| | | |
|-------------------|--|----|
| Figure 1. | Pin connections (top view) | 2 |
| Figure 2. | Supply current vs. supply voltage | 10 |
| Figure 3. | Input offset voltage distribution at $V_{CC} = 5\text{ V}$ | 10 |
| Figure 4. | Input offset voltage distribution at $V_{CC} = 3.3\text{ V}$ | 10 |
| Figure 5. | Input offset voltage distribution at $V_{CC} = 2.2\text{ V}$ | 10 |
| Figure 6. | Input offset voltage distribution at $V_{CC} = 5\text{ V}$, $T = 175\text{ }^{\circ}\text{C}$ | 11 |
| Figure 7. | Input offset voltage distribution at $V_{CC} = 5\text{ V}$, $T = -40\text{ }^{\circ}\text{C}$ | 11 |
| Figure 8. | Input offset voltage distribution at $V_{CC} = 2.2\text{ V}$, $T = 175\text{ }^{\circ}\text{C}$ | 11 |
| Figure 9. | Input offset voltage distribution at $V_{CC} = 2.2\text{ V}$, $T = -40\text{ }^{\circ}\text{C}$ | 11 |
| Figure 10. | Input offset voltage vs. supply voltage | 11 |
| Figure 11. | Input offset voltage vs. input common mode at $V_{CC} = 5.5\text{ V}$ | 11 |
| Figure 12. | Input offset voltage vs. input common mode at $V_{CC} = 3.3\text{ V}$ | 12 |
| Figure 13. | Input offset voltage vs. input common mode at $V_{CC} = 2.2\text{ V}$ | 12 |
| Figure 14. | Input offset voltage vs. temperature | 12 |
| Figure 15. | V_{OH} vs. supply voltage | 12 |
| Figure 16. | V_{OL} vs. supply voltage | 12 |
| Figure 17. | Output current vs. output voltage at $V_{CC} = 5\text{ V}$ | 12 |
| Figure 18. | Output current vs. output voltage at $V_{CC} = 2.2\text{ V}$ | 13 |
| Figure 19. | Input bias current vs. common-mode at $V_{CC} = 5\text{ V}$ | 13 |
| Figure 20. | Input bias current vs. temp. at $V_{CC} = 5\text{ V}$ | 13 |
| Figure 21. | Output rail linearity | 13 |
| Figure 22. | Bode diagram at $V_{CC} = 5\text{ V}$ | 13 |
| Figure 23. | Bode diagram at $V_{CC} = 2.2\text{ V}$ | 13 |
| Figure 24. | Bode diagram at $V_{CC} = 3.3\text{ V}$ | 14 |
| Figure 25. | Open loop gain vs. frequency | 14 |
| Figure 26. | Positive slew rate vs. supply voltage | 14 |
| Figure 27. | Negative slew rate vs. supply voltage | 14 |
| Figure 28. | Noise 0.1 – 10 Hz vs. time | 14 |
| Figure 29. | Noise vs. frequency | 14 |
| Figure 30. | Output overshoot vs. load capacitance | 15 |
| Figure 31. | Small signal $V_{CC} = 5\text{ V}$ | 15 |
| Figure 32. | Small signal $V_{CC} = 2.2\text{ V}$ | 15 |
| Figure 33. | Large signal $V_{CC} = 5\text{ V}$ | 15 |
| Figure 34. | Large signal $V_{CC} = 2.2\text{ V}$ | 15 |
| Figure 35. | Negative overv. recovery $V_{CC} = 2.2\text{ V}$ | 15 |
| Figure 36. | Positive overvoltage recovery $V_{CC} = 5\text{ V}$ | 16 |
| Figure 37. | Output impedance vs. frequency | 16 |
| Figure 38. | Settling time positive step (-2 V to 0 V) | 16 |
| Figure 39. | Settling time negative step (2 V to 0 V) | 16 |
| Figure 40. | Settling time positive step (-0.8 V to 0 V) | 16 |
| Figure 41. | Settling time negative step (0.8 V to 0 V) | 16 |
| Figure 42. | Maximum output voltage vs. frequency | 17 |
| Figure 43. | Crosstalk vs. frequency | 17 |
| Figure 44. | PSSR vs. frequency | 17 |
| Figure 45. | SO8 package outline | 19 |
| Figure 46. | SOT23-5 package outline | 20 |

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2023 STMicroelectronics – All rights reserved

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[STMicroelectronics:](#)

[TSZ182H1YDT](#) [TSZ181H1YLT](#)