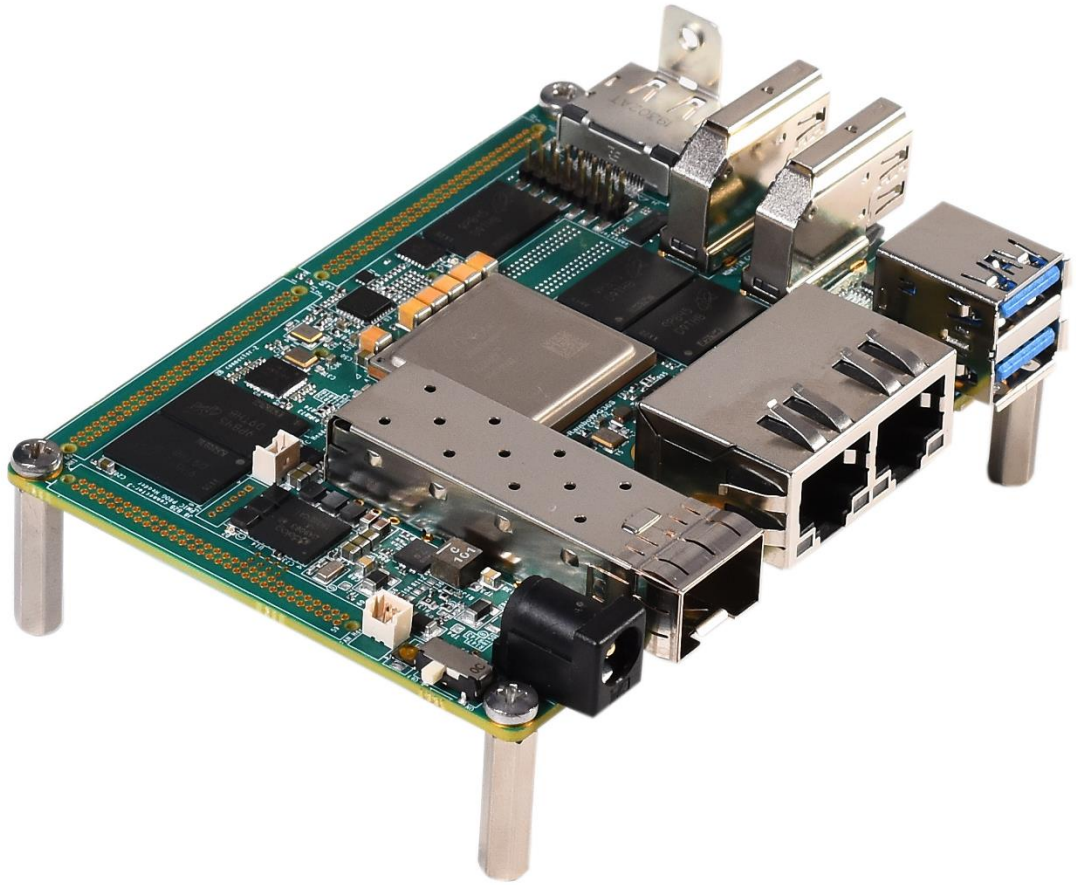
iW-RainboW-G36S
Zynq Ultrascale+ MPSoC SBC
Hardware User Guide



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Document Revision History

Document Number		iW-PRGGG-UM-01-R2.0-REL0.1-Hardware
Release	**Date**	**Description**
0.1	18th May 2021	Initial Draft Version
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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the Zynq Ultrascale+ MPSoC Single Board Computer based on the Xilinx Zynq Ultrascale+ MPSoC . This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the Zynq Ultrascale+ MPSoC SBC from a Hardware Systems perspective.

1.2 SBC Overview

The Zynq Ultrascale+ MPSoC SBC is an extension of Zynq Ultrascale+ MPSoC. Zynq Ultrascale+ MPSoC SBC has a form factor of 72mm x 100mm and provides the functional requirements for an embedded application. Three high speed ruggedized terminal strip connectors provide the interface to carry all the I/O signals from Zynq Ultrascale+ MPSoC.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ADC	Analog to Digital Converter
ARM	Advanced RISC Machine
BSP	Board Support Package
CAN	Controller Area Network
CPU	Central Processing Unit
DDR4 SDRAM	Double Data Rate fourth-generation Synchronous Dynamic Random Access Memory
FPGA	Field Programmable Gate Array
eMMC	Embedded Multimedia Card
GB	Giga Byte
Gbps	Gigabits per sec
GEM	Gigabit Ethernet Controller
GHz	Giga Hertz
GPIO	General Purpose Input Output
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
JTAG	Joint Test Action Group
Kbps	Kilobits per second
LVDS	Low Voltage Differential Signalling
MAC	Media Access Controller
MB	Mega Byte
Mbps	Megabits per sec
MHz	Mega Hertz

Acronyms	Abbreviations
NPTH	Non Plated Through hole
PCB	Printed Circuit Board
PMIC	Power Management Integrated IC
PTH	Plated Through hole
PL	Programmable Logic
PS	Processing System
RGMII	Reduced Gigabit Media Independent Interface
RTC	Real Time Clock
SBC	Single Board Computer
SD	Secure Digital
SDIO	Secure Digital Input Output
SoC	System On Chip
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
ULPI	UTMI+ Low Pin Interface
USB	Universal Serial Bus
USB OTG	USB On The Go
UTMI	USB2.0 Transceiver Macrocell Interface

1.4 Terminlogy Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
LVDS	Low Voltage Differential Signal
GBE	Gigabit Ethernet Media Dependent Interface differential pair signals
USB	Universal Serial Bus differential pair signals
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SBC.

1.5 References

- Zynq Ultrascale+ MPSoC Technical Reference Manual
- Zynq Ultrascale+ MPSoC Device Overview

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the Zynq Ultrascale+ MPSoC SBC features and Hardware architecture with high level block diagram. Also, this section provides detailed information about Board to Board connectors pin assignment and usage.

2.1 Zynq Ultrascale+ MPSoC SBC Block Diagram

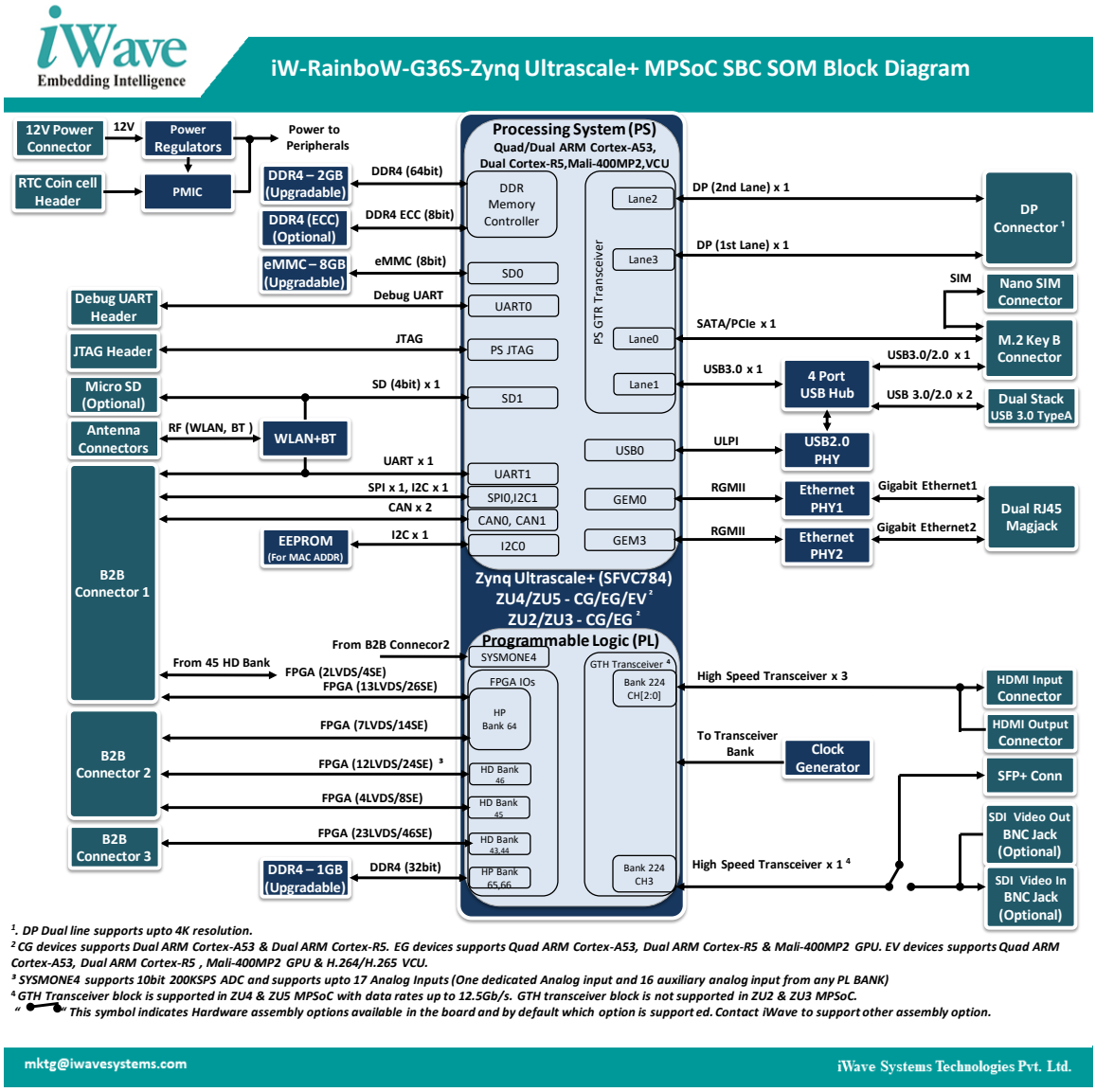

Figure 1: Zynq Ultrascale+ MPSoC SBC Block Diagram

2.1.1 Zynq Ultrascale+ MPSoC SBC Features

The Zynq Ultrascale+ MPSoC SBC supports the following features.

SoC

- Xilinx Zynq Ultrascale+ MPSoC
  - Compatible Zynq Ultrascale+ MPSoC Family (SFVC784) – ZU4EV, ZU5EV
    Programming Logic with up to 256K Logic cells and Processing System with integrated Quad-core ARM Cortex-A53 MPCore Application processor (up to 1.5GHz), Dual-core ARM Cortex-R5 MPCore Real Time Processor (up to 600MHz) and Mali™-400 MP2 Graphics Processor and H.264/H.265 Video Codec.
  - Compatible Zynq Ultrascale+ MPSoC Family (SFVC784) – ZU2EG, ZU3EG, ZU4EG, ZU5EG
    Programming Logic with up to 256K Logic cells and Processing System with integrated Quad-core ARM Cortex-A53 MPCore Application processor (up to 1.5GHz), Dual-core ARM Cortex-R5 MPCore Real Time Processor (up to 600MHz) and Mali™-400 MP2 Graphics Processor.
  - Compatible Zynq Ultrascale+ MPSoC Family (SFVC784) – ZU2CG, ZU3CG, ZU4CG, ZU5CG
    Programming Logic with up to 256K Logic cells and Processing System with integrated Dual-core ARM Cortex-A53 MPCore Application processor (up to 1.3GHz), Dual-core ARM Cortex-R5 MPCore Real Time Processor (up to 533MHz).

PMIC

- Dialog's DA9063 PMIC with RTC

Memory

- 2GB DDR4 SDRAM (64bit) for PS (Expandable)
- 1GB DDR4 SDRAM (32bit) for PL (Expandable)
- 8GB eMMC Flash (Expandable)
- EEPROM For MAC Address
- Micro SD Connector (Optional) [1]

Features from PS Block

- Dual 10/100/1000Mbps Ethernet through RJ45 Magjack
- WLAN & BT Module with Antenna connector [1,2]
- Debug UART Header

Features from PS-GTR Transceiver

- Display Port Connector (Dual Lane upto 4K@30)
- Dual USB3.0 Type A Jack
- M.2 Key B Connector with SATA, PCIex1 and USB3.0

Features from PL-GTH Transceiver [3]

- HDMI Input Connector (Upto 4K@60)
- HDMI Output Connector (Upto 4K@60)
- 10G SFP+ Connector [4]
- 3G/12G SDI Input through HD BNC Jack (Optional) [4]
- 3G/12G SDI Output through HD BNC Jack (Optional) [4]

Additional Features

- Clock Synthesizer/Generator
- JTAG Header
- FAN Header
- RTC Coin Cell Header
- Power On/OFF & Reset Switch

Board to Board Connector1 Interfaces (60pin)

From PS Block

- DATA UART1 x 1 Port [2]
- SPI x 1 Port
- I2C1 x 1 Port
- CAN x 2 Ports

From PL Block

- PL IOs - HP Bank64
  - Upto 13 LVDS IOs/26 Single ended (SE) IOs
    - Upto 3 GC Global Clock Input pins (LVDS/SE)
    - Upto 8 ADC Input pins (Differential/Single Ended)
    - Variable IO voltage support from 1.2V to 1.8V
- PL IOs - HD Bank45 [5]
  - Upto 4 Single ended (SE) IOs
    - Variable IO voltage support from 1.2V to 3.3V

Board to Board Connector2 Interfaces (60pin)

From PL Block

- PL IOs - HP Bank64
  - Upto 7 LVDS IOs/14 Single ended (SE) IOs
    - Upto 1 GC Global Clock Input pins (LVDS/SE)
    - Upto 5 ADC Input pins (Differential/Single Ended)
    - Variable IO voltage support from 1.2V to 1.8V
- PL IOs - HD Bank45 [5]
  - Upto 4 LVDS IOs/8 Single ended (SE) IOs
    - Upto 4 ADC Input pins (Differential/Single Ended)
    - Variable IO voltage support from 1.2V to 3.3V
- PL IOs - HD Bank46 [5]
  - Upto 12 LVDS IOs/24 Single ended (SE) IOs
    - Upto 4 GC Global Clock Input pins (LVDS/SE)
    - Upto 12 ADC Input pins (Differential/Single Ended)
    - Variable IO voltage support from 1.2V to 3.3V
- One dedicated ADC Input (Differential) from SYSMONE4

Board to Board Connector3 Interfaces (60pin)

From PL Block

- PL IOs - HD Bank43 [5]
  - Upto 11LVDS IOs/22 Single ended (SE) IOs
    - Upto 3 GC Global Clock Input pins (LVDS/SE)
    - Upto 11 ADC Input pins (Differential/Single Ended)
    - Variable IO voltage support from 1.2V to 3.3V
- PL IOs - HD Bank44 [5]
  - Upto 12 LVDS IOs/24 Single ended (SE) IOs
    - Upto 4 GC Global Clock Input pins (LVDS/SE)
    - Upto 8 ADC Input pins (Differential/Single Ended)
    - Variable IO voltage support from 1.2V to 3.3V

General Specification

- Power Supply : 12V, 5A Power Input Jack
- Form Factor : 72mm x 100mm

[1] In Zynq Ultrascale+ MPSoC SBC, SD1 signals from MPSoC is shared with WLAN module and MicroSD connector. So either WLAN or Micro SD connector can be supported. By default WLAN module is supported in SBC. Contact iWave to support Micro SD connector.

[2] In Zynq Ultrascale+ MPSoC SBC, UART1 signals from MPSoC is shared with Bluetooth and Board to Board connector1 So either Bluetooth or Board to Board connector1 UART can be supported. By default UART1 is supported in Bluetooth in SBC. Contact iWave to support UART1 on Board to Board Connector1.

[3] Important Note: Since PL-GTH Transceivers are not supported in ZU3 & ZU2 Zynq Ultrascale+MPSoC, these features from PL-GTH are not supported in ZU3 & ZU2 Zynq Ultrascale+MPSoC based SBC.

[4] In Zynq Ultrascale+ MPSoC SBC, GTH Transceiver Channel3 is shared with SFP+ and SDI In & Out. So either SFP+ or SDI IN & Out only can be supported. By default SFP+ is supported in SBC. Contact iWave to support SDI IN & Out.

[5] In ZCU2 & ZCU3 MPSoC devices, the PL Bank 43, 44, 45 & 46 is called as 44, 24, 25 & 26 respectively. Only the Bank Numbering is different and all other functionalities remain same.

2.2 Zynq Ultrascale+ MPSoC

Xilinx's SoC portfolio integrates the software programmability of a processor with the hardware programmability of an FPGA, providing unrivalled levels of system performance, flexibility, and scalability. Unlike traditional SoC processing solutions, the flexible programmable logic provides optimization and differentiation, allowing to add the peripherals and accelerators for a broad base of applications.

The Zynq Ultrascale+ MPSoC SBC is based on Xilinx Zynq Ultrascale+ MPSoC with SFVC784 package. Zynq Ultrascale+ MPSoC family integrates Processing system (PS) and Xilinx programmable logic (PL) in a single device. MPSoC's Processing system includes feature-rich Quad-core ARM Cortex-A53 MPCore up to 1.5 GHz of Application processor, Dual-core ARM Cortex-R5 MPCore up to 600MHz, Mali™-400 MP2 of Graphics Processor and H.264/H.265 Video Codec. The Block Diagram of Zynq Ultrascale+ MPSoC from Xilinx website is shown below for reference.

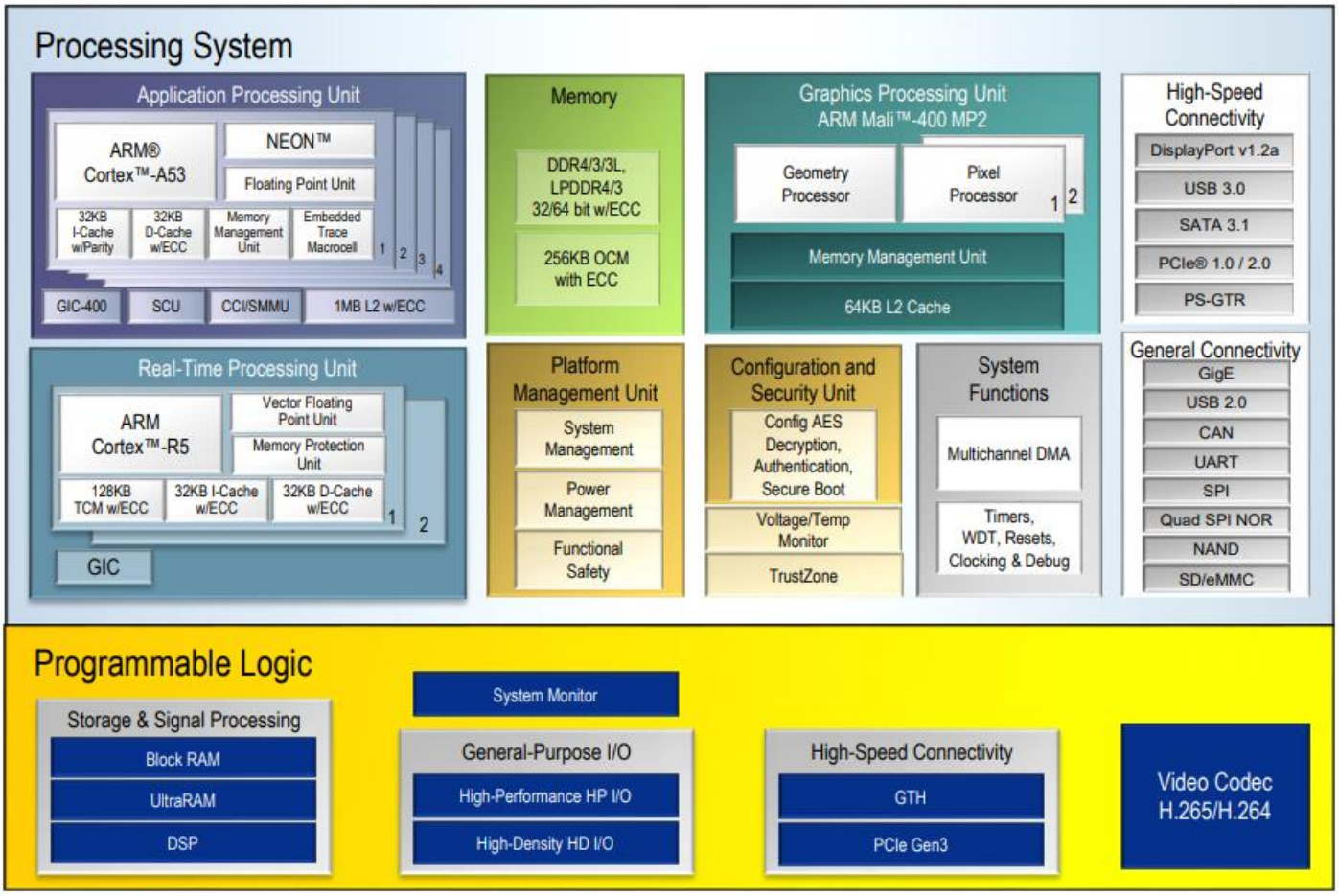

Figure 2: Zynq Ultrascale+ MPSoC CPU Simplified Block Diagram

Note: Please refer the latest Zynq Ultrascale+ MPSoC Datasheet & Technical Reference Manual for more details which may be revised from time to time.

The Zynq Ultrascale+ MPSoC SBC is compatible to ZU2CG, ZU3CG, ZU4CG, ZU5CG, ZU2EG, ZU3EG, ZU4EG, ZU5EG, ZU4EV and ZU5EV MPSoC devices and feature comparison between these devices are shown below.

	ZU2CG	ZU3CG	ZU4CG	ZU5CG	ZU2EG	ZU3EG	ZU4EG	ZU5EG	ZU4EV	ZU5EV
Application Processing Unit	Dual-core Arm Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point;32KB/32KB L1 Cache, 1MB L2 Cache				Quad-core Arm Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache				Quad-core Arm Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache	
Real-Time Processing Unit	Dual-core Arm Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM				Dual-core Arm Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM				Dual-core Arm Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM	
Embedded and External Memory	256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC				256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC				256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC	
General Connectivity	214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters				214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters				214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters	
High-Speed Connectivity	4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII				4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII				4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII	
Graphic Processing Unit	NA				Arm Mali™-400 MP2; 64KB L2 Cache				Arm Mali™-400 MP2; 64KB L2 Cache	
Video Codec	NA				NA				1	
System Logic Cells	1,03,320	1,54,350	1,92,150	2,56,200	1,03,320	1,54,350	1,92,150	2,56,200	1,92,150	2,56,200
CLB Flip-Flops	94,464	1,41,120	1,75,680	2,34,240	94,464	1,41,120	1,75,680	2,34,240	1,75,680	2,34,240
CLB LUTs	47,232	70,560	87,840	1,17,120	47,232	70,560	87,840	1,17,120	87,840	1,17,120
Distributed RAM (Mb)	1.2	1.8	2.6	3.5	1.2	1.8	2.6	3.5	2.6	3.5
Block RAM Blocks	150	216	128	144	150	216	128	144	128	144
Block RAM (Mb)	5.3	7.6	4.5	5.1	5.3	7.6	4.5	5.1	4.5	5.1
UltraRAM Blocks	0	0	48	64	0	0	48	64	48	64
UltraRAM (Mb)	0	0	13.5	18	0	0	13.5	18	13.5	18
DSP Slices	240	360	728	1,248	240	360	728	1,248	728	1,248
CMTs	3	3	4	4	3	3	4	4	4	4
Max. HP I/O	156	156	156	156	156	156	156	156	156	156
Max. HD I/O	96	96	96	96	96	96	96	96	96	96
System Monitor	2	2	2	2	2	2	2	2	2	2
GTH Transceiver 12.5Gb/s	0	0	4	4	0	0	4	4	4	4
Transceiver Fractional PLLs	0	0	8	8	0	0	8	8	8	8
PCIe Gen3 x16	0	0	2	2	0	0	2	2	2	2

Figure 3: Zynq Ultrascale+ MPSoC Devices Comparison

The Zynq Ultrascale+ MPSoC's PS has 78 dedicated I/O pins referred as MIO (Multiplexed I/O) for the PS peripheral interfaces. These 78 MIO pins are divided into three banks (PS BANK500, 501 & 502) and each bank includes 26 device pins. Since 78 MIO pins are not enough to support simultaneous use of all the peripherals supported by PS, there is option in MPSoC to route most of the IO peripheral interfaces to PL Bank I/O pins referred as EMIO (Extended MIO). Zynq Ultrascale+ MPSoC's PS Peripheral Pin mapping options between MIO & EMIO is shown below.

Peripheral Interface	MIO	EMIO
Quad-SPI NAND	Yes	No
USB2.0: 0,1	Yes: External PHY	No
SDIO 0,1	Yes	Yes
SPI: 0,1 I2C: 0,1 CAN: 0,1 GPIO	Yes CAN: External PHY GPIO: Up to 78 bits	Yes CAN: External PHY GPIO: Up to 96 bits
GigE: 0,1,2,3	RGMII v2.0: External PHY	Supports GMII, RGMII v2.0 (HSTL), RGMII v1.3, MII, SGMII, and 1000BASE-X in Programmable Logic
UART: 0,1	Simple UART: Only two pins (TX and RX)	Full UART (TX, RX, DTR, DCD, DSR, RI, RTS, and CTS) requires either: • Two Processing System (PS) pins (RX and TX) through MIO and six additional Programmable Logic (PL) pins, or • Eight Programmable Logic (PL) pins
Debug Trace Ports	Yes: Up to 16 trace bits	Yes: Up to 32 trace bits
Processor JTAG	Yes	Yes

The Zynq Ultrascale+ MPSoC's PL Banks are classified as high-performance (HP) banks or high-density (HD) banks. The HP Bank I/Os are optimized for highest performance operation organized in banks of 52pins. The HD Bank I/Os are reduced-feature I/Os organized in banks of 24pins.

In Zynq Ultrascale+ MPSoC PL, each bank supports four global clock (GC or HDGC) input pin pairs. GC pins have direct access to the global clock buffers, MMCMs and PLLs of the same Bank. HDGC pins are from HD I/O banks and have direct access only to the global clock buffers.

Also Zynq Ultrascale+ MPSoC supports one types of high speed transceivers namely GTH and PS-GTR. These transceivers are arranged in groups of four known as a transceiver Quad. GTH transceivers are from PL and PS-GTR transceivers are from PS.

2.2.1 MPSoC Power

The Zynq Ultrascale+ MPSoC SBC uses discrete power regulators along with DA9063 PMIC from Dialog Semiconductor for MPSoC power management. In SBC, PS low-power domain, PS full-power domain & PL power domain supply voltage (VCC_PSINTLP, VCC_PSINTFP, VCCINT) is fixed to 0.85V or 0.9V based on the speed grade of the MPSoC. Also all PS Bank (VCCO_PSIO) I/O voltage is fixed to 1.8V.

The I/O voltage of PL HP Banks (PL Bank 64) and PL HD Banks (PL Bank 43, 44, 45 & 46) which are connected to Board to Board Connectors are generated from PMIC LDO1 and LDO6, LDO3, LDO4, & LDO7 respectively. By default, HP Banks and HD Banks voltages are set to 1.2V and configurable through software after bootup

2.2.2 MPSoC Reset

The Zynq Ultrascale+ MPSoC SBC uses PMIC's Reset output (nRESET) for PS Power On Reset and connected to PS_POR_B pin of MPSoC. Also it supports warm reset input from Reset Switch (SW2) and connected to PS_SRST_B pin of MPSoC.

2.2.3 MPSoC Reference Clock

The Zynq Ultrascale+ MPSoC SBC supports on board clock oscillators for reference clock to different blocks of Zynq Ultrascale+ MPSoC. These reference clock details are mentioned in the below table.

Table 3: Zynq Ultrascale+ MPSoC SBC Reference Clock.

Sl. No	On-SBC Oscillator Frequency	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
1	33.33MHz	PS_REF_CLK / R16	1.8V, LVCMOS	33.33Mhz single ended reference clock for PS.
2	100MHz[1]	IO_L5P_HDGC_AD7P_43 / AE12	1.8V[2], LVCMOS	100Mhz single ended reference clock for PL. This is connected to PL Bank43 HDGC Global clock pin.
3	300MHz	IO_L13N_T2L_N1_GC_QBC_66 / D6 IO_L13P_T2L_N0_GC_QBC_66 / D7	1.8V, LVDS	LVDS reference clock for PL DDR4 SDRAM. This is connected to PL Bank66 Global clock pins.

[1] *Important Note: I/O voltage of PL Bank43 is software configurable. Since this oscillator supports 1.8V to 3.3V VCC only, this reference clock can be used only if the I/O voltage of PL Bank43 is set between 1.8V to 3.3V.*

[2] *Mentioned voltage level is based on after uboot bootup I/O voltage set to PL Bank43.*

2.2.4 MPSoC Configuration & Status

The Zynq Ultrascale+ MPSoC uses multi-stage boot process that supports both a non-secure and a secure boot. The PS is the master of the boot and configuration process. Upon reset, device executes code out of on-chip ROM and copies the first stage boot loader (FSBL) from the boot device to the on-chip RAM. The FSBL initiates the boot of the PS and can load and configure the PL or configuration of the PL can be deferred to a later stage.

The Zynq Ultrascale+ MPSoC SBC supports two LEDs for the MPSoC error status indication namely PS_ERROR_OUT and PS_ERROR_STATUS. LED D1 is for PS_ERROR_OUT and it is asserted for accidental loss of power, a hardware error, or an exception in the PMU. LED D7 is for PS_ERROR_STATUS and it indicates a secure lockdown state. Alternatively, it can be used by the PMU firmware to indicate system status.

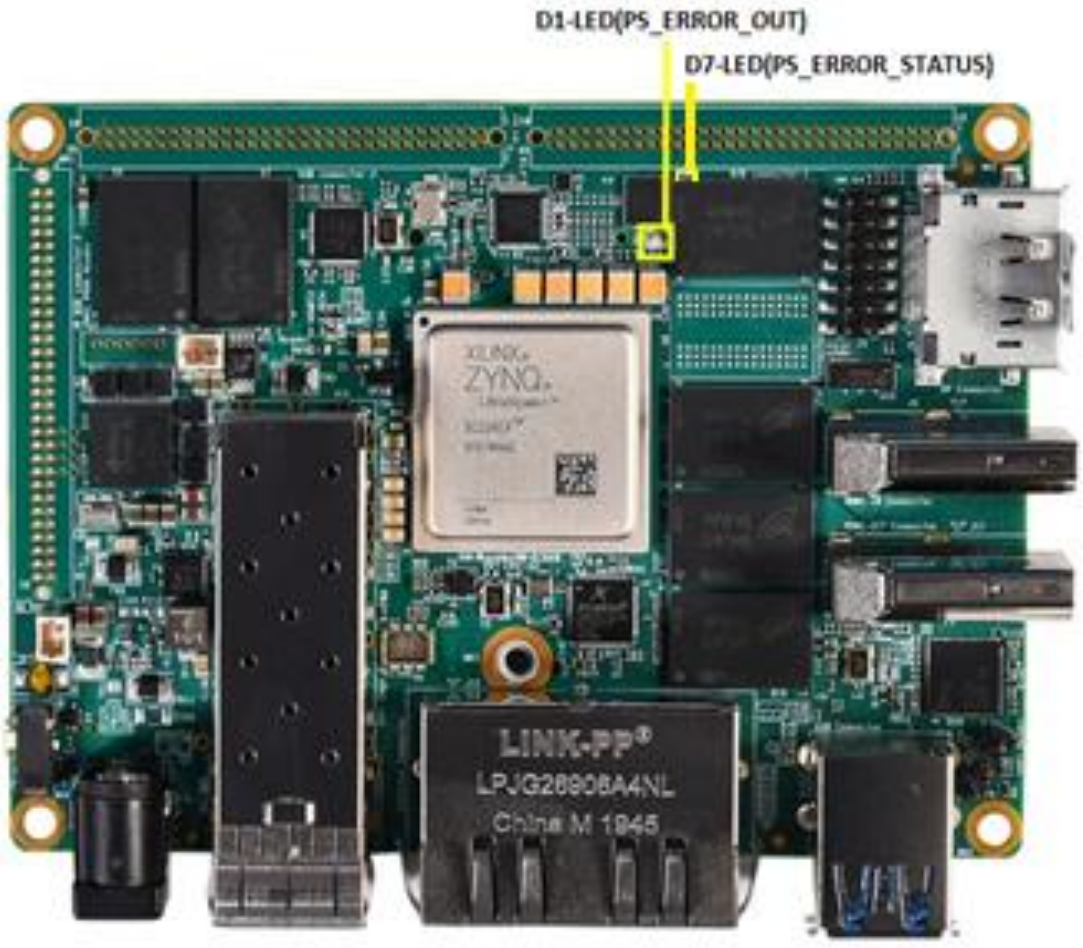

Figure 4: Error Status Indication LEDs

2.2.5 MPSoC Boot Mode

The Zynq Ultrascale+ MPSoC always boots from PS first and configures the PL through software. MPSoC can support eMMC, SD1, USB0 & JTAG as boot device and configurable through mode pins. Upon device reset, MPSoC mode pins are read to determine the primary boot device. By default, eMMC is supported as boot device in SBC.

2.2.6 MPSoC System Monitor/ADC

The Zynq Ultrascale+ MPSoC contain two System Monitor block (SYSMONE4), one in the PL (PL SYSMON) and another in the PS (PS SYSMON). It is used to enhance the overall safety, security and reliability of the system by monitoring the physical environment via on-chip power supply and temperature sensors.

The PL SYSMON uses 10-bit 200kSPS ADC to digitize the sensor/ADC inputs. It monitors the die temperature in the PL and several internal PL and PS power supply nodes. The PL SYSMON can also monitor up to 17 external analog channels which includes 16 auxiliary analog inputs and one VP_VN dedicated input. The external auxiliary inputs can be routed through any PL Bank. The ADC voltage reference is selectable between an internal reference and the external pins VREFP and VREFN. In Zynq Ultrascale+ MPSoC SBC, 1.25V external voltage reference is supported.

The PS SYSMON uses 10-bit 1MSPS ADC to digitize the sensor inputs. It is located in the PS LPD and monitors two temperature points & several internal fixed voltage nodes. The PS has two temperature sensors, one is physically located in the PS SYSMON near the RPU. The second, remote sensor is located in the FPD near the APU. The ADC always uses an internally generated voltage reference.

2.3 PMIC with RTC

The Zynq Ultrascale+ MPSoC SBC supports Dialog semiconductor DA9063 PMIC. The I2C0 module of Zynq Ultrascale+ MPSoC PS is used for PMIC interface through MIO pins with I2C address 0x5A. PMIC supports Six switching regulator,11 LDO regulator and upto 14 General purpose Input/Output pins.

PMIC's LDO1 is connected to I/O voltage of PL HP Banks (PL Bank 64) and by default set to 1.2V.The I/O voltage is configurable through software after bootup.

PMIC's LDO6 is connected to I/O voltage of PL HD Bank 43, LDO3 is connected to I/O voltage of PL HD Bank 44, LDO4 is connected to I/O voltage of PL HD Bank 45 & LDO7 is connected to I/O voltage of PL HD Bank 46 and by default set to 1.2V. The I/O voltage is configurable through software after bootup.

PMIC supports reset output and connected to Zynq Ultrascale+ MPSoC PS (PS_POR_B) for power on reset. Also PMIC supports IRQ output for events indication and connected to MPSoC's PS GPIO (PS_MIO2_500).

The PMIC supports Real Time Clock functionality through J6 connector for RTC backup power. The PMIC can support backup battery charging to charge Lithium-Manganese coin cell batteries and super capacitors if required.

2.4 Memory

2.4.1 DDR4 SDRAM for PS

The Zynq Ultrascale+ MPSoC SBC supports 64bit, 2GB DDR4 RAM memory for MPSoC's PS. Four 16 bit, 512MB DDR4 SDRAM ICs are used to support a total on board RAM memory of 2GB. These DDR4 devices operates at 1.2 voltage level. DDR4 memory is connected to the hard memory controller of the MPSoC PS. The RAM size can be expandable up to maximum of 8GB based on the availability of higher density 16bit DDR4 device.

*Note: Refer **ORDERING INFORMATION** section for exact RAM size used on the SBC based on the Product Part Number.*

2.4.2 DDR4 SDRAM for PL

The Zynq Ultrascale+ MPSoC SBC supports 32bit, 1GB DDR4 RAM memory for MPSoC's PL. Four 16 bit, 512MB DDR4 SDRAM IC is used to support RAM memory of 1GB for PL. This device operates at 1.2 voltage level. In Zynq Ultrascale+ MPSoC SBC, Bank65 & 66 is used for PL DDR4 interface. The RAM size can be expandable up to maximum of 32GB based on the availability of higher density 16bit DDR4 device.

The Zynq Ultrascale+ MPSoC SBC supports 300MHz LVDS Oscillator on board for PL DDR4 reference clock and connected to Bank64 D6 & D7 dedicated clock input pins through AC Coupling capacitors.

*Note: Refer **ORDERING INFORMATION** section for exact RAM size used on the SBC based on the Product Part Number.*

2.4.3 eMMC Flash

The Zynq Ultrascale+ MPSoC SBC supports 8GB eMMC Flash memory for Boot & Storage of Zynq Ultrascale+ MPSoC PS. This eMMC Flash memory is directly connected to the SD0 controller of the MPSOC's PS through MIO pins and operates at 1.8V Voltage level. This SD/SDIO controller supports eMMC4.51 standard with up to 8bit HS200 mode. The eMMC Flash size can be expandable up to maximum of 128GB based on the availability of higher density eMMC Flash device.

*Note: Refer **ORDERING INFORMATION** section for exact eMMC Flash size used on the SBC based on the Product Part Number.*

2.4.4 EEPROM

The Zynq Ultrascale+ MPSoC SBC supports 256kb EEPROM for MAC Address. The I2C0 module of Zynq Ultrascale+ MPSoC PS is used for EEPROM interface through MIO pins with I2C address 0x50. This device operates at 1.8 voltage level.

2.4.5 Micro SD Connector (Optional)

The Zynq Ultrascale+ MPSoC SBC optionaly supports MicroSD Connector through SD1 interface of Zynq Ultrascale+ MPSoC PS. This SD1 Signals from Zynq Ultrascale+ MPSoC PS is connected to Micro SD Connector (J24) through auto direction control memory card voltage level translator to support 1.8V and 3.3V supported cards. It supports up to 4-Bit data transfer with card detect.

The memory card voltage level translator's voltage selection is controlled through PS GPIO (PS_MIO43_501) pin from Zynq Ultrascale+ MPSoC PS. If PS_MIO43_501 is set to low, then 3.3V IO level is selected for SD1 signals to SD connector. If PS_MIO43_501 is set to high, then 1.8V IO level is selected for SD1 signals to SD connector.

2.5 Fearures from PS Block

2.5.1 Dual 10/100/1000Mbps Ethernet through RJ45 Magjack

The Zynq Ultrascale+ MPSoC SBC supports two 10/100/1000 Mbps Ethernet through Dual RJ45 MagJack (J15). The GEM0 and GEM3 RGMII interface of MPSoC is used for dual Ethernet support. The GEM0 & GEM3 MAC is integrated in the Zynq Ultrascale+ MPSoC PS and connected to the external individual Gigabit Ethernet PHY "AR8031" on SBC. Also both the Ethernet port supports Speed (Yellow) and Link/Activity (Green) LED indications on correponding RJ45 Magjack port. This Dual port RJ45 Magjack (J15) is physically located at the top of the board as shown below.

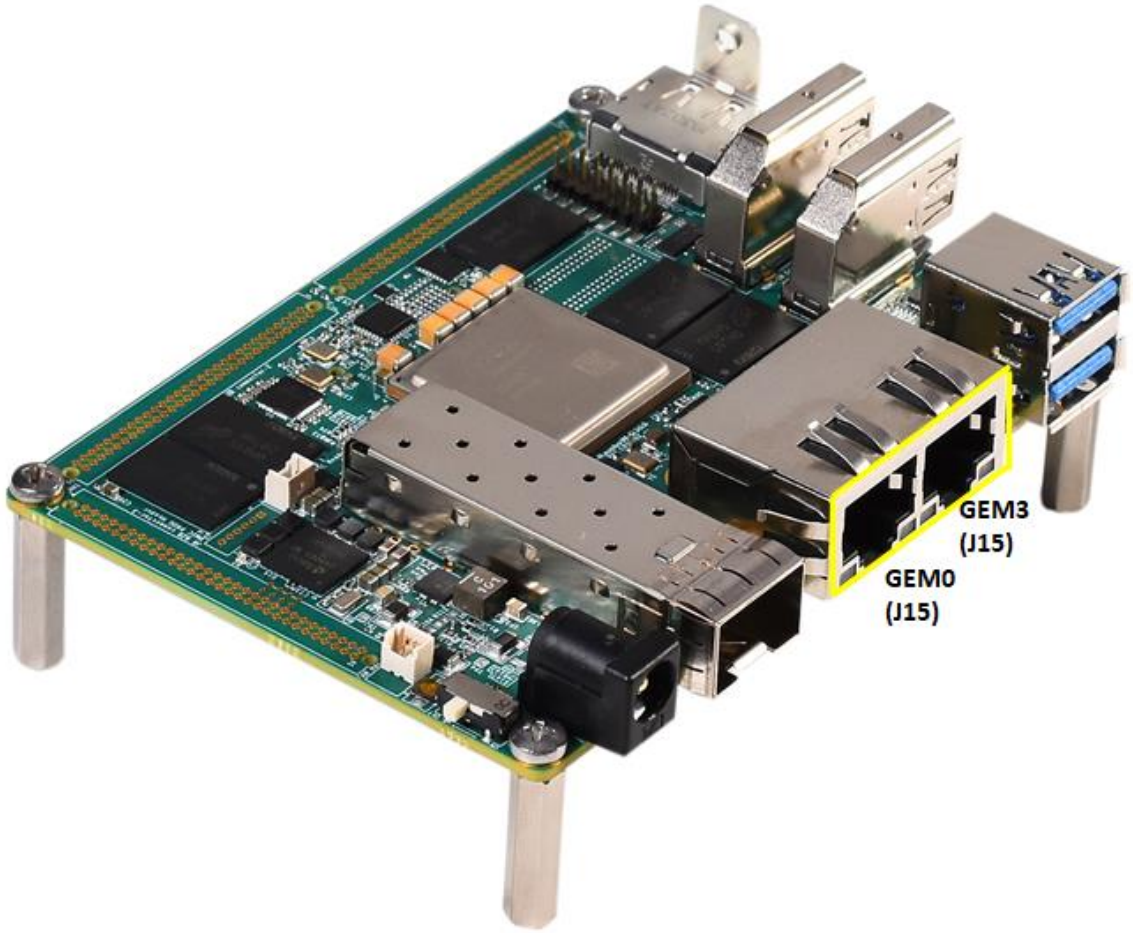

Figure 5: Dual Gigabit Ethernet Port

** Same MDC and MDIO control signals are shared to GEM0 & GEM3 external Gigabit Ethernet PHY.*

2.5.2 WLAN & BT Module with Antenna connector

The Zynq Ultrascale+ MPSoC SBC supports Muruta's "LBEE5HY1MW" based Wi-Fi & Bluetooth combo module for connectivity. This module is a very high-performance module based on Cypress CYW43455 combo chipset which supports WiFi IEEE 802.11a/b/g/n/ac + Bluetooth 5.0 BR/EDR/LE standard. The Zynq Ultrascale+ MPSoC SBC supports a 32.768 kHz clock oscillator for this module for sleep operation.

The LBEE5HY1MW Wi-Fi module supports single stream 1x1 IEEE 802.11 a/b/g/n/ac mode providing up to 390Mbps. The LBEE5HY1MW module features small form factor when integrating Power Amplifier (PA), Low Noise Amplifier (LNA), Transmit/Receive switch, Power Management. The Zynq Ultrascale+ MPSoC PS SD1 SDHC controller through MIO pins are used for Wi-Fi interface which supports 1-bit or 4-bit transfer mode at the clock range of 0-50 MHz and works at 1.8V IO level.

The LBEE5HY1MW Bluetooth supports Bluetooth 5.0 Basic Rate, Enhanced Rate & BLE. The Zynq Ultrascale+ MPSoC PS's UART1 interface thorugh MIO pins is used for Bluetooth interface.

Note: In Zynq Ultrascale+ MPSoC SBC, SD1 signals from MPSoC is shared with WLAN module and MicroSD connector. So either WLAN or Micro SD connector can be supported. By default WLAN module is supported in SBC. Contact iWave to support Micro SD connector.

Note: In Zynq Ultrascale+ MPSoC SBC, UART1 signals from MPSoC is shared with Bluetooth and Board to Board connector1 So either Bluetooth or Board to Board connector1 UART can be supported. By default UART1 is supported in Bluetooth in SBC. Contact iWave to support UART1 on Board to Board Connector1.

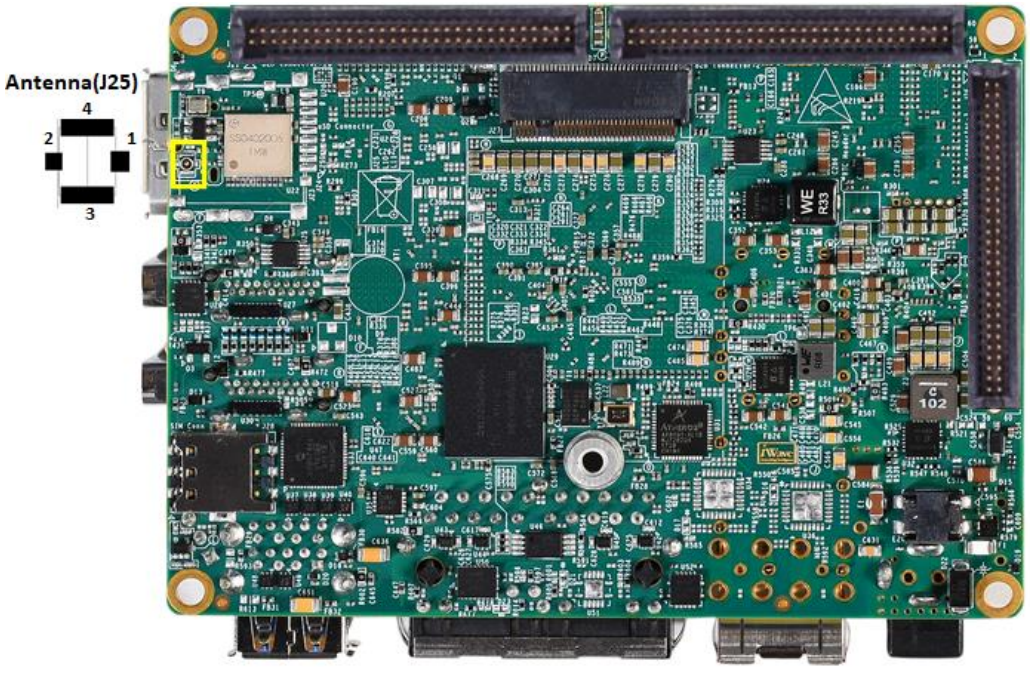

Figure 6: WLAN & BT with Antenna Connector

2.5.3 Debug UART Header

The Zynq Ultrascale+ MPSoC SBC supports debug interface through UART0 interface of Zynq Ultrascale+ MPSoC PS. This UART0 signals from Zynq Ultrascale+ MPSoC PS is connected to Debug UART Header(J14) through 1.8V to 3.3V Level Translator. This UART Header can be used for Debug purpose which is physically located at the top of the board as shown below.

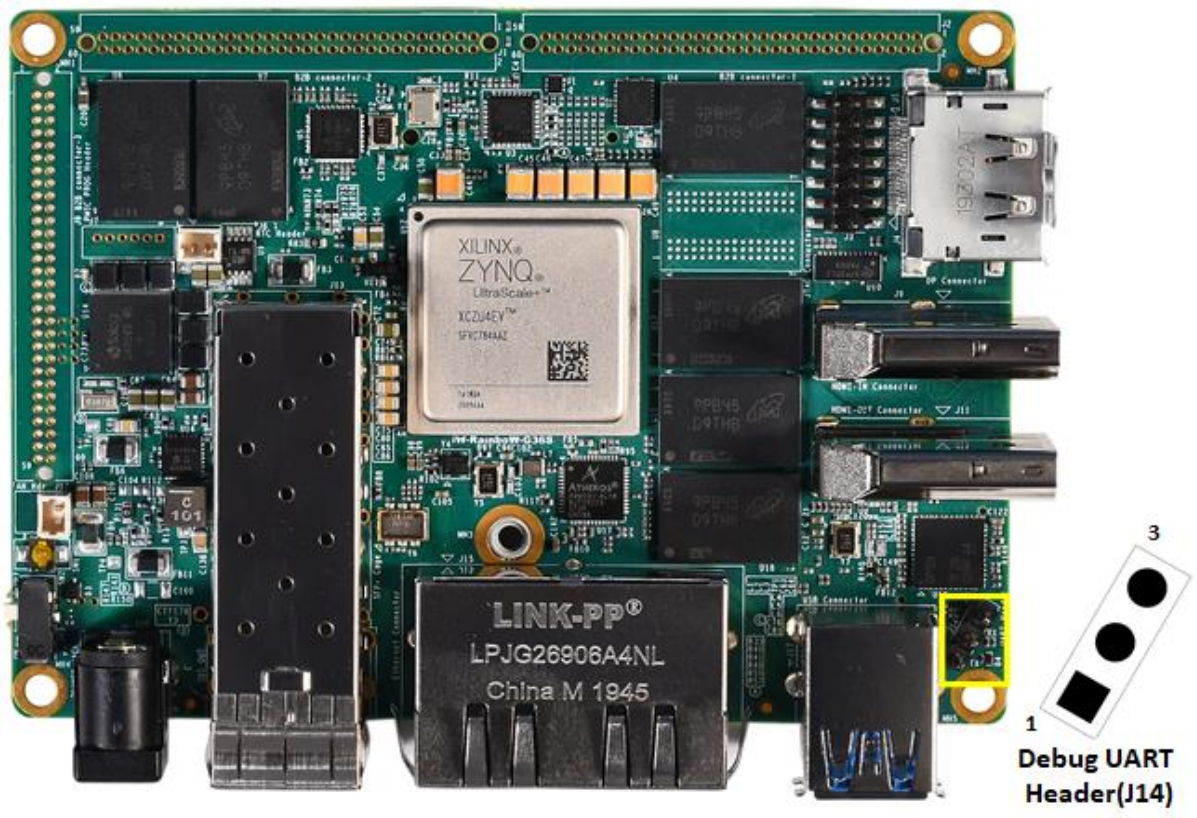

Figure 7: Debug UART Header

Table 4: Debug UART Header Pin Assignment

Pin No	Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
1	UART0_TX	PS_MIO07 _500	500	AH17	O, 3.3V LVCMOS	UART0 Transmit data line for Debug.
2	UART0_RX	PS_MIO06 _500	500	AF16	I, 3.3V LVCMOS	UART0 Receive data line for Debug.
3	GND	NA	NA	NA	Power	Ground.

2.6 Features from PS-GTR

The Zynq Ultrascale+ MPSoC supports four Multi-Gigabit PS-GTR transceivers with data rate from 1.25Gbps to 6.0Gbps. This PS-GTR transceiver lanes provide I/O path for MPSoC MAC controllers and their link partner outside.

The Zynq Ultrascale+ MPSoC SBC supports two PS GTR transceivers (Lane3 & Lane2) for Display Port Connector, one PS GTR transceiver (Lane1) for USB3.0 interface and another one PS GTR transceiver (Lane0) for SATA on M.2 Connector.

- 2 lanes of DisplayPort (TX only) at 1.62Gb/s, 2.7Gb/s, or 5.4Gb/s
- 1 lane of USB3.0 channels at 5.0Gb/s
- 1 lane of SATA channels at 1.5Gb/s, 3.0Gb/s, or 6.0Gb/s

2.6.1 Display Port Connector

The Zynq Ultrascale+ MPSoC SBC supports Display port connector through PS-GTR Lanes of Zynq Ultrascale+ MPSoC PS. PS-GTR Lane3 & Lane2 from Zynq Ultrascale+ MPSoC PS is connected to Display port connector to support dual lane display port. The Zynq Ultrascale+ MPSoC can support upto 4K@30 resolution.

The Display port connector supports AUX+ & AUX- signals from the PL Bank IOs. Also it supports Hot plug detect signal and connected to PL Bank IO. This Display Port connector (J5) is physically located at the top of the board as shown below.

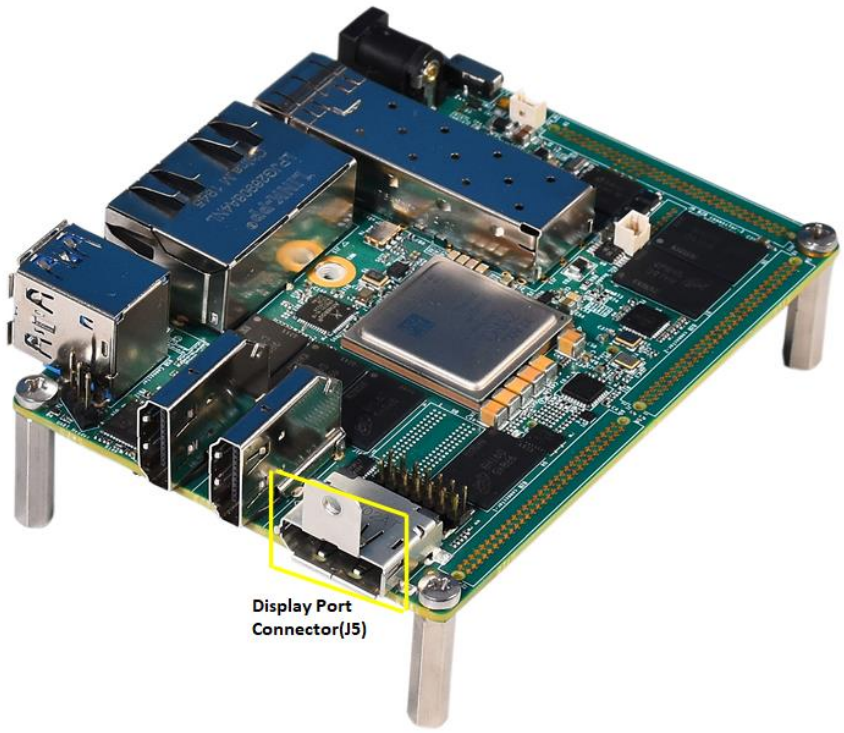

Figure 8: Display Port Connector

2.6.2 Dual USB3.0 Type A Jack

The Zynq Ultrascale+ MPSoC SBC support two Super Speed USB3.0 Host ports through dual stack USB 3.0 Type A connector. The PS-GTR Lane1 of Zynq Ultrascale+ MPSoC is used for USB3.0 interface through 4port USB3.0 HUB "USB5744" from Micro Chip. Two of the 4port HUB output is connected to USB dual stack typeA connector and third is connected to M.2 connector.

To support backward compatibility, USB 2.0 interface also supported through this HUB. The USB0 controller of Zynq Ultrascale+ MPSoC PS is used for USB 2.0 interface through on board ULPI transceiver "USB3320" from Microchip. So these USB 3.0 ports support all Super speed, high-speed, full-speed and low-speed transfers in host modes.

The VBUS power of this USB Type-A connector is connected through current limit power switch which can be used to switch On/Off the power based on the Host and also limits the current above 900mA in host mode. This dual stack USB Type-A connector (J17) is physically located at the top of the board as shown below.

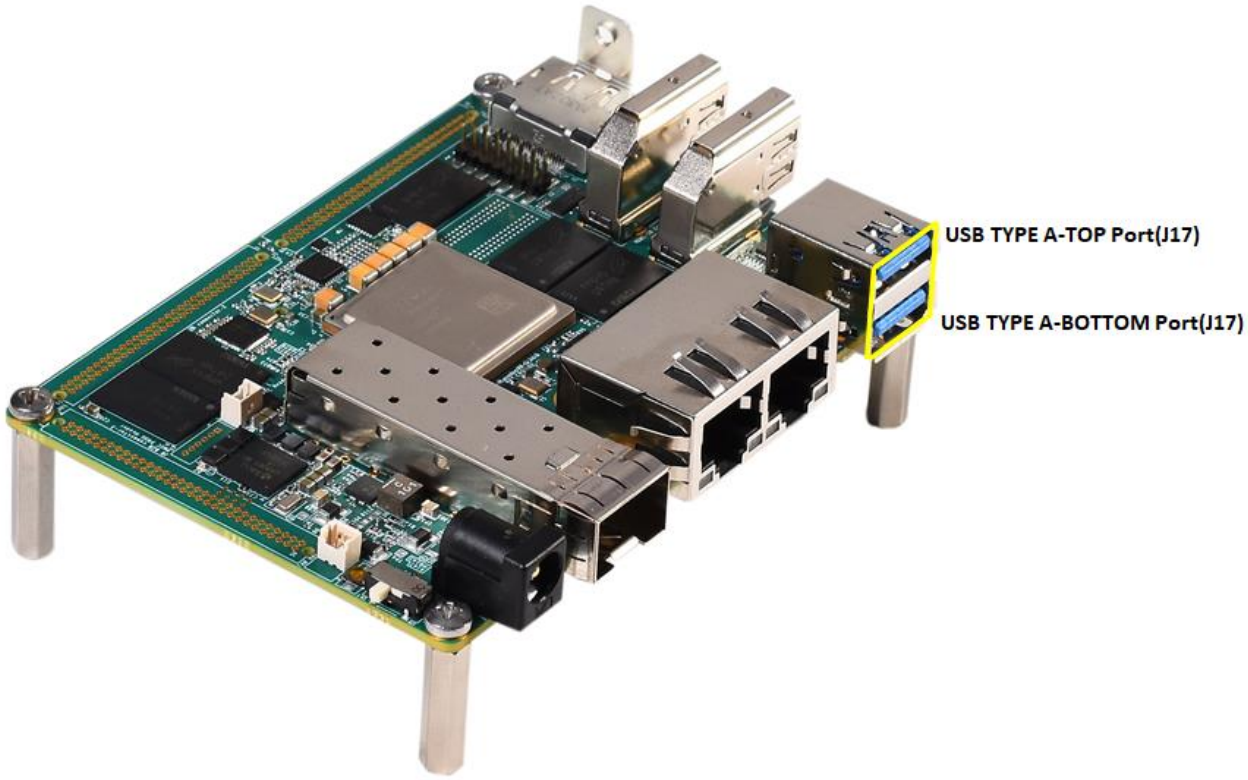

Figure 9: Dual Stack USB3.0 Type-A Jack

2.6.3 M.2 Key B Connector with SATA & USB3.0

The Zynq Ultrascale+ MPSoC SBC supports one SATA, PCIe and USB3.0 interface through M.2 (Key B) connector. PS-GTR0 Lane of Zynq Ultrascale+ MPSoC PS is used for SATA interface, USB3.0 and USB2.0 Signals are connected from USB3.0 HUB. MPSoC's SATA supports SATA Specification revision 3.1 with Gen1(1.5Gbps), Gen2(3Gbps) & Gen3(6Gbps) datarates. This M.2 connector (J27) is physically located at the bottom of the board as shown below.

** In Zynq Ultrascale+ MPSoC SBC, PS-GTR lane0 can be used for either SATA or PCIe Interface through M.2 Key-B Connector.*

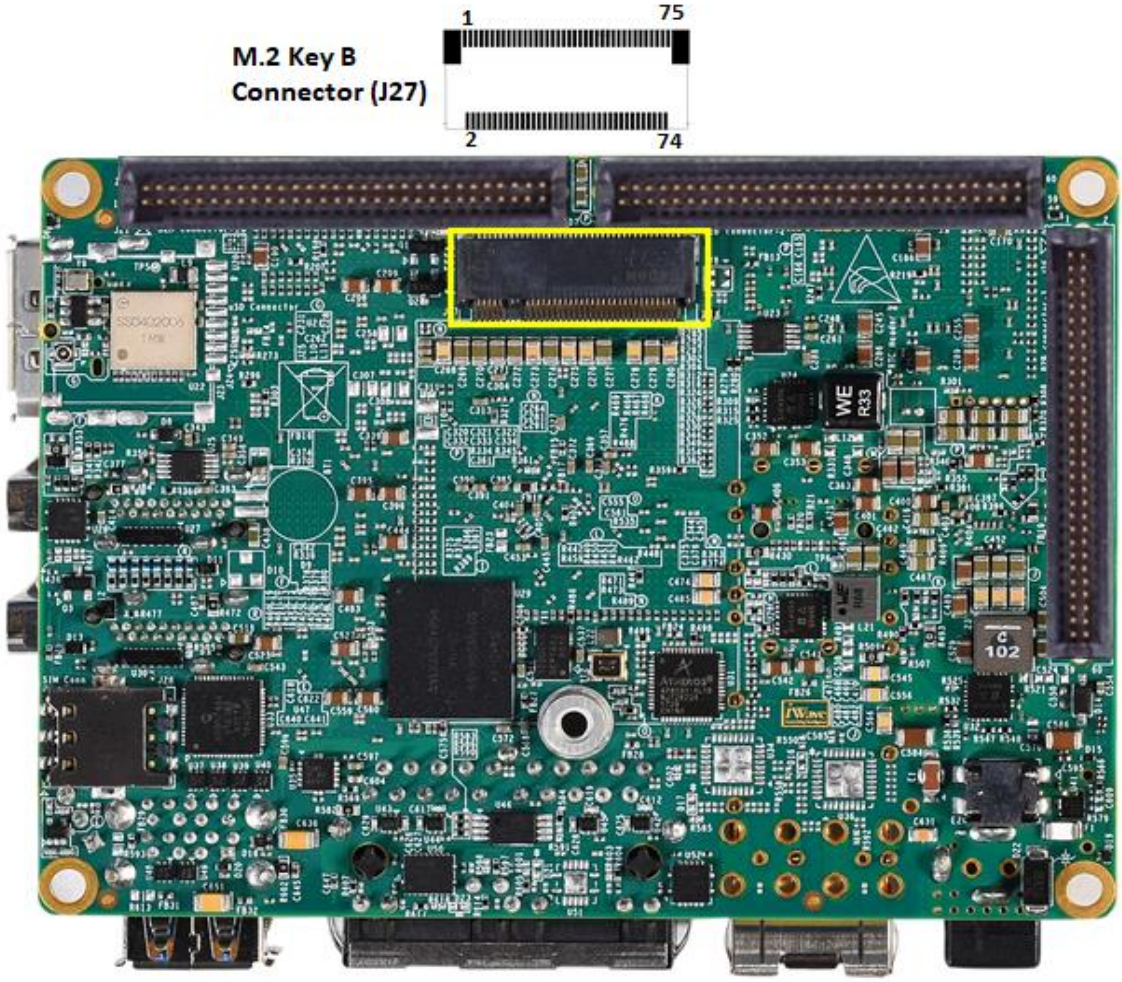

Figure 10: M.2 Key B Connector

Table 5: M.2 Connector Pin Assignment

Pin No	Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
1	CONFIG_3	NA	NA	NA	NA	M.2 Configuration Pin 3.
2	VCC_3V3	NA	NA	NA	O, 3.3V Power	Supply Voltage.
3	GND	NA	NA	NA	Power	Ground.
4	VCC_3V3	NA	NA	NA	O, 3.3V Power	Supply Voltage.
5	GND	NA	NA	NA	Power	Ground.
6	FULL_CARD_POWER_OFF#	NA	NA	NA	O, 3.3V CMOS/ 10K PU	FULL_CARD_POWER_OFF# This signal is configuring from PMIC GPIO13 (U14).
7	USB_D+	NA	NA	NA	IO, USB	USB2.0 Port3 USB data positive. This pin is connected from 17th pin of 4-Port USB HUB(U33).
8	W_DISABLE1#	NA	NA	NA	O, 3.3V CMOS/ 10K PU	M.2 Wireless Disable Signal This signal is configuring from PMIC GPIO2 (U14).
9	USB_D-	NA	NA	NA	IO, USB	USB2.0 Port3 USB data negative. This pin is connected from 18th pin of 4-Port USB HUB(U33).
10	GPIO9	NA	NA	NA	NA	NC.
11	GND	NA	NA	NA	Power	Ground
12	B1	NA	NA	NA	NA	NC.
13	B2	NA	NA	NA	NA	NC.
14	B3	NA	NA	NA	NA	NC.
15	B4	NA	NA	NA	NA	NC.
16	B5	NA	NA	NA	NA	NC.
17	B6	NA	NA	NA	NA	NC.
18	B7	NA	NA	NA	NA	NC.
19	B8	NA	NA	NA	NA	NC.
20	GPIO5	NA	NA	NA	NA	NC.
21	CONFIG_0	NA	NA	NA	NA	M.2 Configuration Pin 0.
22	GPIO6	NA	NA	NA	NA	NC.
23	GPIO11	NA	NA	NA	NA	NC.
24	GPIO7	NA	NA	NA	NA	NC.
25	DPR	NA	NA	NA	O, 1.8V CMOS	M.2 Dynamic Power Reduction Signal. This signal is configuring from PMIC GPIO1 (U14).
26	GPIO10	NA	NA	NA	NA	NC.
27	GND	NA	NA	NA	Power	Ground.
28	GPIO8	NA	NA	NA	NA	NC.

Pin No	Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
29	PERN1/USB3.1_RX-/SSIC_RX-	NA	NA	NA	I, DIFF	USB3.0 Port3 Receiver pair negative. This pin is connected to 23rd pin of 4-Port USB HUB(U33).
30	UIM-RESET	NA	NA	NA	O, SIM	SIM Card Reset Signal.
31	PERP1/USB3.1_RX+/SSIC_RX+	NA	NA	NA	I, DIFF	USB3.0 Port3 Receiver pair Positive. This pin is connected from 22nd pin of 4-Port USB HUB(U33).
32	UIM-CLK	NA	NA	NA	I, SIM	SIM Card Clock Signal.
33	GND	NA	NA	NA	Power	Ground.
34	UIM-DATA	NA	NA	NA	IO, SIM	SIM Card Data IO Signal.
35	PETN1/USB3.1-TX-/SSIC-TXN	NA	NA	NA	O, DIFF	USB3.0 Port3 Transmit pair negative. This pin is connected from 20th pin of 4-Port USB HUB(U33).
36	UIM-PWR	NA	NA	NA	O, SIM Power	SIM Card Power.
37	PETP1/USB3.1-TX+/SSIC-TXP	NA	NA	NA	O, DIFF	USB3.0 Port3 Transmit pair positive. This pin is connected from 19th pin of 4-Port USB HUB(U33).
38	DEVSLP	NA	NA	NA	NA	NC.
39	GND	NA	NA	NA	Power	Ground.
40	GPIO0	NA	NA	NA	NA	NC.
41	PERN0/SATA_B+	PS_MGTRRXP3_505	505	A25	I, DIFF	SATA Receiver pair Positive.
42	GPIO1	NA	NA	NA	NA	NC.
43	PERP0/SATA_B-	PS_MGTRRXN3_505	505	A26	I, DIFF	SATA Receiver pair negative.
44	GPIO2	NA	NA	NA	NA	NC.
45	GND	NA	NA	NA	Power	Ground.
46	GPIO3	NA	NA	NA	NA	NC.
47	PETN0/SATA_A-	PS_MGTRTXN3_505	505	B24	O, DIFF	SATA Transmit pair negative.
48	GPIO4	NA	NA	NA	NA	NC.
49	PETP0/SATA_A+	PS_MGTRTXP3_505	505	B23	O, DIFF	SATA Transmit pair Positive.
50	PERST#	PS_MIO1_500	500	AG16	O, 3.3V LVCMOS/ 10K PU	PCIe-PE-Reset. This pin is connected through level translator(U50).
51	GND	NA	NA	NA	Power	Ground.

Pin No	Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
52	CLKREQ#	NA	NA	NA	IO, 3.3V CMOS/ 10K PU	PCIe Clock Request. This signal is configuring from PMIC GPIO3 (U14).
53	REFCLKN	NA	NA	NA	O, DIFF	100 MHz PCIe Device negative Reference Clock. This pin is connected from 30th pin of clock synthesizer(OUT5b)
54	PEWAKE#	NA	NA	NA	O, 3.3V CMOS/ 10K PU	PCIe Wake. This signal is configuring from PMIC GPIO4 (U14).
55	REFCLKP	NA	NA	NA	O, DIFF	100 MHz PCIe Device Positive Reference Clock. This pin is connected from 31st pin of clock synthesizer(OUT5)
56	MFG_DATA	NA	NA	NA	NA	NC.
57	GND	NA	NA	NA	Power	Ground.
58	MFG_CLOCK	NA	NA	NA	NA	NC.
59	ANTCTL0	NA	NA	NA	NA	NC.
60	COEX3	NA	NA	NA	NA	NC.
61	ANTCTL1	NA	NA	NA	NA	NC.
62	COEX_TXD	NA	NA	NA	NA	NC.
63	ANTCTL2	NA	NA	NA	NA	NC.
64	COEX_RXD	NA	NA	NA	NA	NC.
65	ANTCTL3	NA	NA	NA	NA	NC.
66	SIM_DETECT	NA	NA	NA	NA	NC.
67	RESET#	GPIO_12(PS_ MIO12_500)	500	AC17	O, 1.8V LVCMOS/ 10K PU	Reset. Note: Same signal is sahred with USB 2.0 Phy Transceiver reset.
68	SUSCLK(32KHZ)	NA	NA	NA	NA	NC. *Note: Optionally 32.768KHz Oscillator is connected to this pin*
69	CONFIG_1	NA	NA	NA	NA	M.2 Configuration Pin 1.
70	VCC_3V3	NA	NA	NA	O, 3.3V Power	Supply Voltage.
71	GND	NA	NA	NA	Power	Ground.
72	VCC_3V3	NA	NA	NA	O, 3.3V Power	Supply Voltage.
73	GND	NA	NA	NA	Power	Ground.
74	VCC_3V3	NA	NA	NA	O, 3.3V Power	Supply Voltage.
75	CONFIG_2	NA	NA	NA	NA	M.2 Configuration Pin 2.

2.7 Features from PL-GTH

The Zynq Ultrascale+ MPSoC SBC, supports different high speed interfaces through 4 GTH Transceivers as mentioned below.

- HDMI IN (3 GTH Receiver)
- HDMI OUT (3 GTH Transmitter)
- SFP+ Connector (1 GTH Transceiver)
- 3G/12G SDI Video IN (1 GTH Transmitter) - Optional
- 3G/12G SDI Video OUT (1 GTH Receiver) Optional

Important Note: Since PL-GTH Transceivers are not supported in ZU3 & ZU2 Zynq Ultrascale+MPSoC, these features from PL-GTH are not supported in ZU3 & ZU2 Zynq Ultrascale+MPSoC based SBC.

Important Note: In Zynq Ultrascale+ MPSoC SBC, GTH Transceiver Channel3 is shared with SFP+ and SDI In & Out. So either SFP+ or SDI IN & Out only can be supported. By default SFP+ is supported in SBC. Contact iWave to support SDI IN & Out.

2.7.1 HDMI Input Connector

The Zynq Ultrascale+ MPSoC SBC supports one HDMI Input through HDMI TypeA connector (J9). The Zynq Ultrascale+ MPSoC's PL GTH Bank224 Channel0 to Channel2 receiver is directly connected from HDMI IN Connector. This HDMI In conector can support upto 4K@60 resolution. This HDMI IN connector (J9) is physically located at the top of the board as shown below.

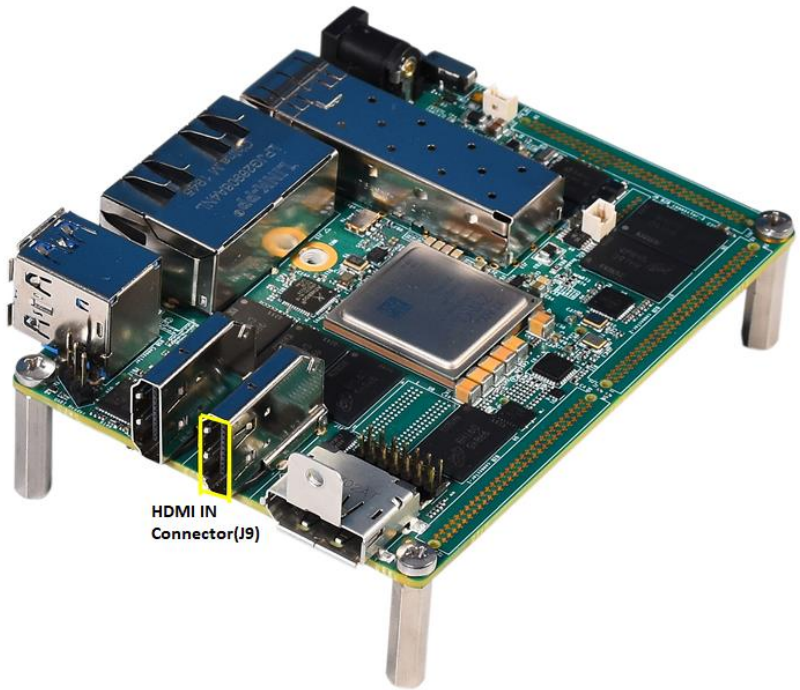

Figure 11: HDMI IN Connector

2.7.2 HDMI Output Connector

The Zynq Ultrascale+ MPSoC SBC supports one HDMI Output through HDMI TypeA connector (J11). The Zynq Ultrascale+ MPSoC's PL GTH Bank224 Channel0 to Channel2 transmitter is directly connected to HDMI Retimer chip (SN65DP159RGZR) and then connected to HDMI Out Connector for HDMI out. This HDMI Out connector can support upto 4K@60 resolution. This HDMI Out connector (J11) is physically located at the top of the board as shown below.

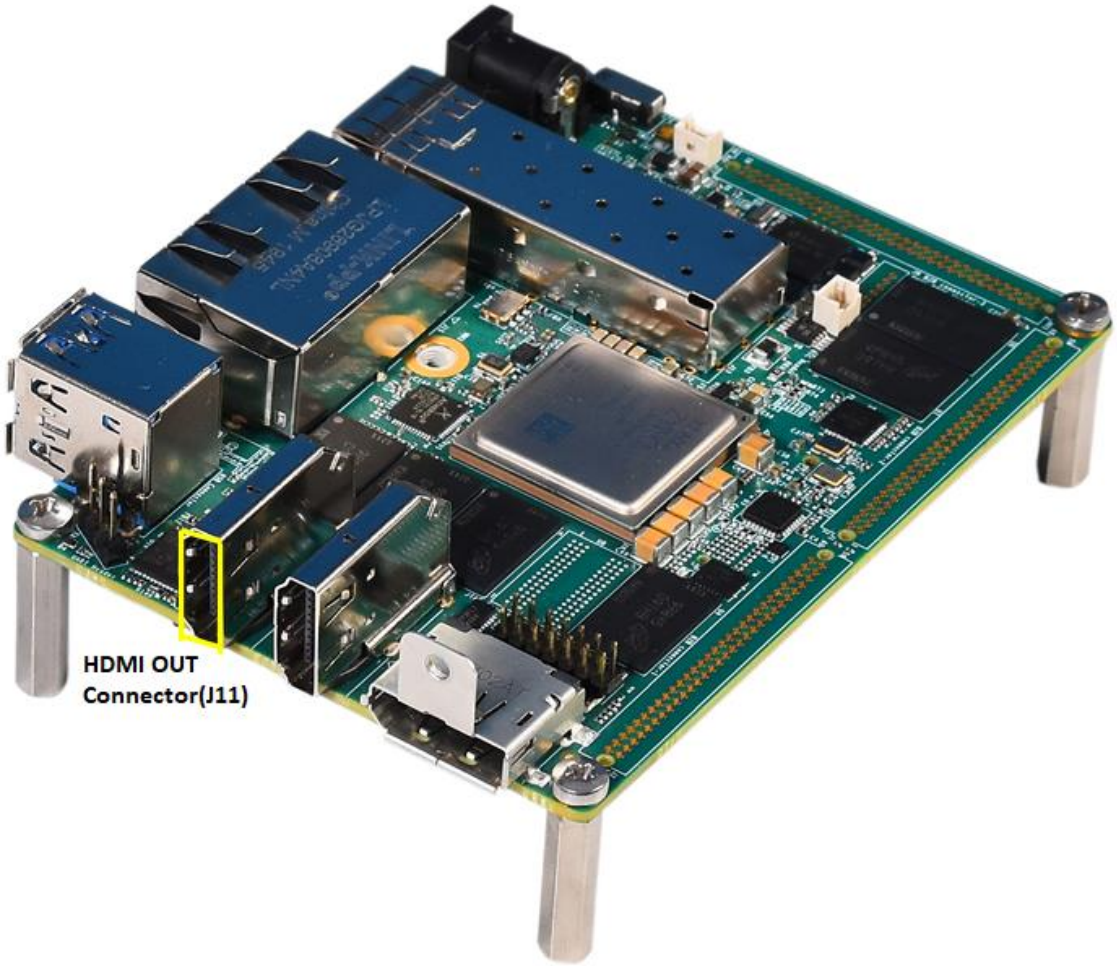

Figure 12: HDMI Out Connector

2.7.3 SFP+ Connector

The Zynq Ultrascale+ MPSoC SBC supports SFP+ Connector for 10G Ethernet support. The Zynq Ultrascale+ MPSoC's PL GTH Bank224 Channel3 is connected to SFP+ connector. Also PS I2C0 is connected to this connector for control and configuration. All other contorl signals of SFP+ connnector is connected from PMIC GPIOs. This SFP+ connector with dust case (J13) is physically located at the top of the board as shown below.

Important Note: In Zynq Ultrascale+ MPSoC SBC, GTH Transceiver Channel3 is shared with SFP+ and SDI In & Out. So either SFP+ or SDI IN & Out only can be supported. By default SFP+ is supported in SBC. Contact iWave to support SDI IN & Out.

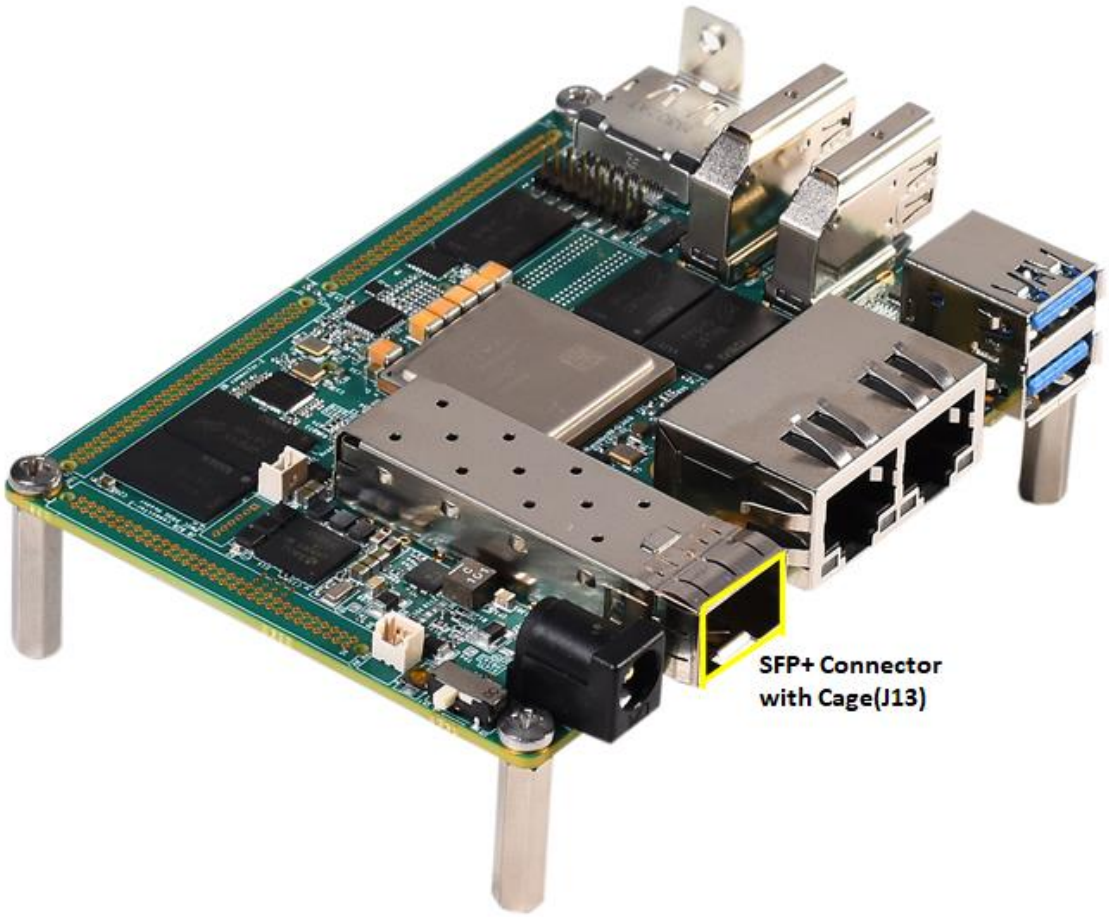

Figure 13: SFP+ Connector

Table 6: SFP+ Connector Pin Assignment

Pin No	Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
1	VEET1	NA	NA	NA	Power	Ground.
2	TFAULT	NA	NA	NA	I, LVTTL/ 4.7K PU	Module Transmitter Fault.
3	TDIS	NA	NA	NA	O, LVTTL/ 4.7K PD	Transmitter Disable.
4	SDA	PS_MIO11_500	500	AE17	IO, 3.3V CMOS	I2C Data.
5	SCL	PS_MIO10_500	500	AD17	O, 3.3V CMOS	I2C Clock.
6	MOD_ABS	NA	NA	NA	I, 3.3V CMOS/ 4.7K PU	Module Definition.
7	RS0	NA	NA	NA	O, 3.3V CMOS/ 4.7K PU	Rate select 0. This Pin is connected to PMIC GPIO7 for software control if required.
8	RX_LOS	NA	NA	NA	I, 3.3V CMOS/ 4.7K PU	Receiver loss of signal indication. This Pin is connected to PMIC GPIO10 for software control if required.
9	RS1	NA	NA	NA	O, 3.3V CMOS/ 4.7K PU	Rate select 1. This Pin is connected to PMIC GPIO09 for software control if required.
10	VEER1	NA	NA	NA	Power	Ground.
11	VEER2	NA	NA	NA	Power	Ground.
12	RD-	MGTHRXN3_224	224	P1	I, DIFF	SFP+ Receiver Data Negative.
13	RD+	MGTHRXP3_224	224	P2	I, DIFF	SFP+ Receiver Data Positive.
14	VEER3	NA	NA	NA	Power	Ground.
15	VCCR	NA	NA	NA	O, 3.3V Power	3.3V Receiver Supply Voltage.
16	VCCT	NA	NA	NA	O, 3.3V Power	3.3V Transmitter Supply Voltage.
17	VEET2	NA	NA	NA	Power	Ground.
18	TD+	MGTHTXP3_224	224	N4	O, DIFF	SFP+ Transmit Data Positive.
19	TD-	MGTHTXN3_224	224	N3	O, DIFF	SFP+ Transmit Data Negative.
20	VEET3	NA	NA	NA	Power	Ground.

2.7.4 3G/12G SDI IN (Optional)

The Zynq Ultrascale+ SBC supports one 3G/12G SDI Video IN interface through HD BNC connector (J20). The Video input signals from HD BNC Connector is directly connected to Adaptive Cable Equalizer chip and then connected to PL Bank224 Channel3 GTH receiver of Zynq Ultrascale+ MPSoC.

The Zynq Ultrascale+ MPSoC SBC supports Video Input Lock status LED (D17) for presence and absence of the Video Input signal on HD BNC connector (J20). This LED will glow when the Video Input signal is detected on HD BNC connector (J20). Also PS I2C0 is connected to Adaptive Cable Equalizer chip for control and configuration with I2C address 0x2D.

Important Note: In Zynq Ultrascale+ MPSoC SBC, GTH Transceiver Channel3 is shared with SFP+ and SDI In & Out. So either SFP+ or SDI IN & Out only can be supported. By default SFP+ is supported in SBC. Contact iWave to support SDI IN & Out.

2.7.5 3G/12G SDI Output (Optional)

The Zynq Ultrascale+ MPSoC SBC supports one 3G/12G SDI Video OUT interface through HD BNC connector (J19). Zynq Ultrascale+ MPSoC's PL Bank224 Channel3 GTH transmitter from Zynq Ultrascale+ MPSoC's is directly connected to Cable Driver chip and then connected to HD BNC Connector (J19) for Video out.

The Zynq Ultrascale+ MPSoC SBC supports Video Output Lock status LED (D16). This LED will glow when the video signal from MPSoC GTH transmitter is detected on Cable Driver chip. Also PS I2C0 is connected to Cable Driver chip for control and configuration with I2C address 0x30.

Important Note: In Zynq Ultrascale+ MPSoC SBC, GTH Transceiver Channel3 is shared with SFP+ and SDI In & Out. So either SFP+ or SDI IN & Out only can be supported. By default SFP+ is supported in SBC. Contact iWave to support SDI IN & Out.

2.8 Additional Features

2.8.1 Clock Synthesizers

The Zynq Ultrascale+ MPSoC SBC supports 6-output Clock Synthesizer "SI5332A-D-GM1" for on board clock distribution. This Clock Generator outputs are connected to PS-GTR, PL-GTH Transceiver Banks Reference Clock on Zynq Ultrascale+ MPSoC through 0.01uF AC coupling capacitors. An external 25MHz crystal is connected to this Clock Synthesizer for reference. This Clock Synthesizer supports from 5 MHz to 333.33 MHz clock output and configurable through PS I2C0.

Table 7: Clock Synthesier Output Clocks

Pin No	Pin Name	Signal Name	Programmed Frequency	Connected To
12	OUT0	PS_MGTREFCLK0P_505	125MHz	Zynq US+ MPSoC-U12.F23.
11	OUT0b	PS_MGTREFCLK0N_505		Zynq US+ MPSoC-U12.F24.
15	OUT1	PS_MGTREFCLK1P_505	100 MHz	Zynq US+ MPSoC-U12.E21.
14	OUT1b	PS_MGTREFCLK1N_505		Zynq US+ MPSoC-U12.E22.
19	OUT2	GTREFCLK0P_224	297 MHz	Zynq US+ MPSoC-U12.Y6.
18	OUT2b	GTREFCLK0N_224		Zynq US+ MPSoC-U12.Y5.
22	OUT3	GTREFCLK1P_224	148.5 MHz	Zynq US+ MPSoC-U12.V6.
21	OUT3b	GTREFCLK1N_224		Zynq US+ MPSoC-U12.V5.
27	OUT4	PS_MGTREFCLK3P_505	27 MHz	Zynq US+ MPSoC-U12.A21.
26	OUT4b	PS_MGTREFCLK3N_505		Zynq US+ MPSoC-U12.A22.
31	OUT5	M2_PCIE2_REFCLK_P	100 MHz	M.2 Key-B Connector-J27.55.
30	OUT5b	M2_PCIE2_REFCLK_N		M.2 Key-B Connector-J27.53.

Important Note: In Zynq Ultrascale+ MPSoC SBC, OUT3 & 3b from clock synthesizer is optionally connected to GTREFCLK1P & N_224 of Zynq Ultrascale+ MPSoC V6 & V5 . By default GTREFCLK1P & N_224 of V6 & V5 is connected from HDMI IN Connector(J9).

2.8.2 JTAG Header

The Zynq Ultrascale+ MPSoC SBC supports 14Pin JTAG Header (J3) for JTAG interface. JTAG Interface Signals from MPSoC's PS BANK503 is connected to this Header through 1.8V to 3.3V level translator. The Zynq Ultrascale+ MPSoC's PS and PL share a common set of JTAG pins and each have their own TAP controller which are chained together inside the Zynq Ultrascale MPSoC. These JTAG interface signals are at 3.3V Voltage level.

The JTAG Header (J3) is physically located on topside of the SBC as shown below. JTAG-HS2 Programming Cable can be directly connected to this JTAG Header.

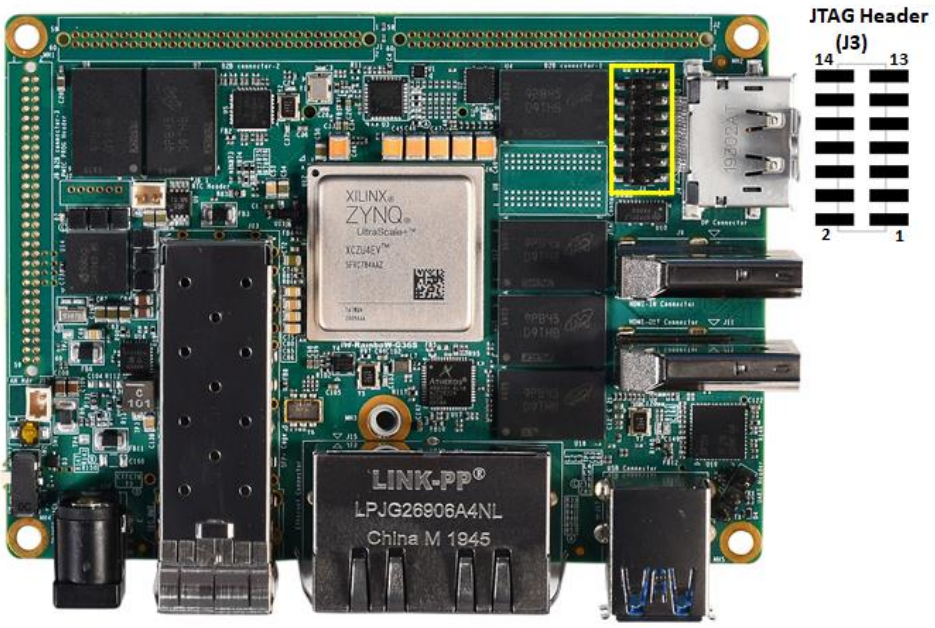

Figure 14: JTAG Header

Table 8: JTAG Header Pinout

Pin No	Pin Name	Signal Type/ Termination	Description
1	-	-	NC.
2	VCC_3V3	O, 3.3V Power	Supply Voltage.
3	GND	Power	Ground.
4	JTAG_TMS	I, 3.3V LVCMOS/ 49.9K PU	JTAG Test Mode Select.
5	GND	Power	Ground.
6	JTAG_TCK	I, 3.3V LVCMOS/ 49.9K PU	JTAG Test Clock.
7	GND	Power	Ground.
8	JTAG_TDO	O, 3.3V LVCMOS	JTAG Test Data Output.
9	GND	Power	Ground.
10	JTAG_TDI	I, 3.3V LVCMOS/ 49.9K PU	JTAG Test Data Input.
11	GND	Power	Ground.
12	-	-	NC.
13	GND	Power	Ground.
14	JTAG_RESETB	-	NC.

2.8.3 Fan Header

The Zynq Ultrascale+ MPSoC SBC supports a Fan Header (J12) to connect cooling Fan if required. The Fan Header (J12) is physically located on topside of the SBC as shown below.

Number of Pins - 2

Connector Part - 0530470210 from Molex

Mating Connector - 51021-0200 from Molex

Compatible Fan (Example) - AFB0505MB from Delta Electronics

Figure 15: Fan Header

Table 9: Fan Header Pinout

Pin No	Pin Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
1	VCC_5V	-	O, 5V Power	Supply Voltage.
2	GND	-	Power	Ground.

2.8.4 RTC Header

The Zynq Ultrascale+ MPSoC SBC supports Coin Cell Header to connect “2032” series 3V coin cell through external cable. This coin cell voltage is connected to Zynq Ultrascale+ MPSoC SBC for RTC back up voltage when VCC main power is off. This Coin Cell Header (J6) is physically located at the top of the board as shown below.

Figure 16: RTC Header

Table 10: RTC Header Pinout

Pin No	Pin Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
1	VRTC_3V0	-	O, 3V Power	Supply Voltage.
2	GND	-	Power	Ground.

2.8.5 Power On/OFF Switch

The Zynq Ultrascale+ MPSoC SBC has power ON/OFF switch (SW3) to control the Main power Input ON/OFF functionality. This power ON/OFF switch is physically located at the top of the board as shown below.

Figure 17: Power ON/OFF Switch

2.8.6 Reset Switch

The Zynq Ultrascale+ MPSoC SBC supports Push button switch (SW2) to reset the Zynq Ultrascale+ MPSoC CPU. Reset signal of Zynq Ultrascale+ MPSoC is directly connected from Reset Push button switch. This Reset Push button switch (SW2) is physically located at the top of the board as shown below.

Figure 18: Reset Switch

2.9 Board to Board Connector1

The Zynq Ultrascale+ MPSoC SBC supports three 60 pin high speed ruggedized terminal strip connectors, Three 60pin High performace High Density connector for interfaces expansion. All the effort is made in Zynq Ultrascale+ MPSoC SBC design to provide the maximum interfaces of Zynq Ultrascale+ MPSoC to SBC by adding these three Board to Board Connectors.

The Zynq Ultrascale+ MPSoC SBC Board to Board Connector1 pinout is provided in the below table and the interfaces which are available at Board to Board Connector1 are explained in the following sections. The Board to Board Connector1 (J21) is physically located on bottom side of the SBC as shown below.

Number of Pins - 60
Connector Part Number - TFC-130-11-L-D-A
Mating Connector - SFC-130-T1-L-D-A from Samtech
Staking Height - 7.75mm

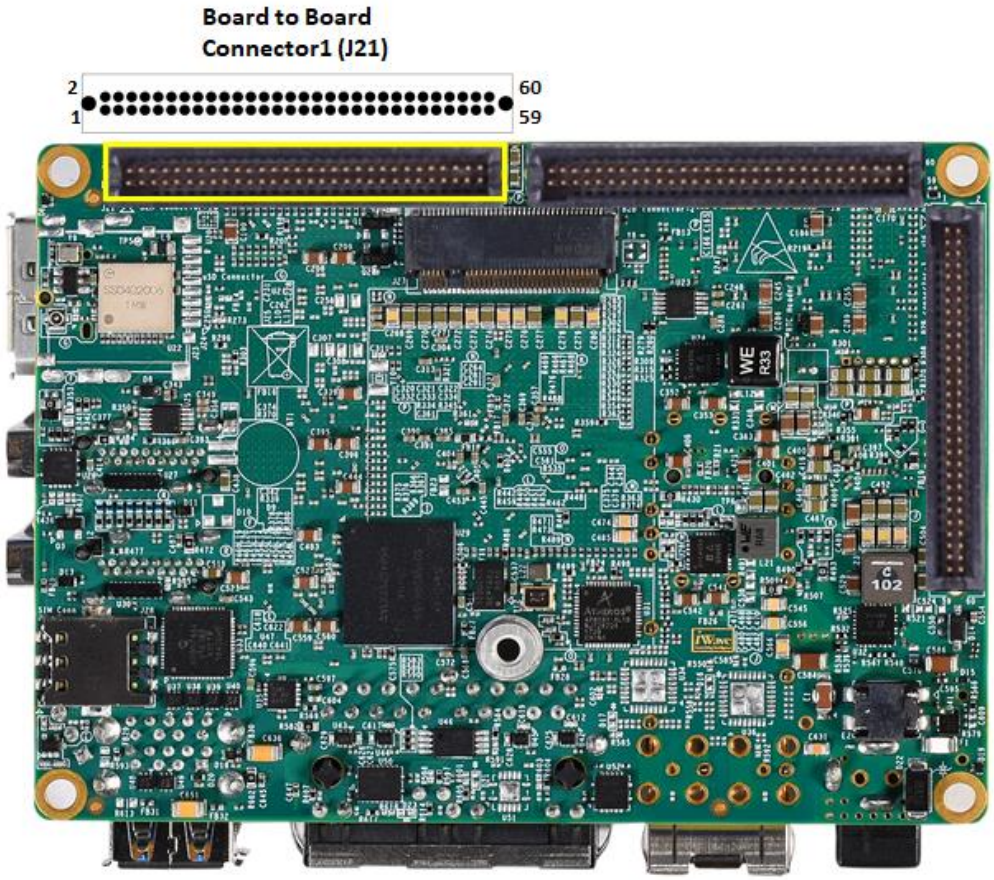

Figure 19: Board to Board Connector1

Table 11: Board to Board Connector1 Pinout

Signal Name	B2B-1 Pin	B2B-1 Pin	Signal Name
PL_AE5_LVDS64_L12P_GC	1	2	PL_C11_LVDS45_L9P
PL_AF5_LVDS64_L12N_GC	3	4	PL_B10_LVDS45_L9N
GND	5	6	PL_B11_LVDS45_L10P
PL_AF6_LVDS64_L11N_GC	7	8	PL_A10_LVDS45_L10N
PL_AF7_LVDS64_L11P_GC	9	10	NC
GND	11	12	NC
PL_AD5_LVDS64_L13P_GC	13	14	SPI0_MISO(PS_MIO4_500)
PL_AD4_LVDS64_L13N_GC	15	16	SPI0_MOSI(PS_MIO5_500)
GND	17	18	SPI0_SS0(PS_MIO3_500)
PL_AG5_LVDS64_L10N_QBC	19	20	SPI0_SCLK(PS_MIO0_500)
PL_AG6_LVDS64_L10P_QBC	21	22	I2C1_SCL(PS_MIO24_500)
GND	23	24	I2C1_SDA(PS_MIO25_500)
PL_AH7_LVDS64_L9N	25	26	GND
PL_AH8_LVDS64_L9P	27	28	CAN1_RX(PS_MIO41_501)
GND	29	30	CAN0_TX(PS_MIO39_501)
PL_AH9_LVDS64_L7N_QBC	31	32	CAN1_TX(PS_MIO40_501)
PL_AG9_LVDS64_L7P_QBC	33	34	CAN0_RX(PS_MIO38_501)
GND	35	36	GND
PL_AE8_LVDS64_L2N	37	38	PL_AG8_LVDS64_L8N
PL_AE9_LVDS64_L2P	39	40	PL_AF8_LVDS64_L8P
GND	41	42	GND
PL_AE7_LVDS64_L4N_DBC	43	44	PL_AD9_LVDS64_L1N_DBC
PL_AD7_LVDS64_L4P_DBC	45	46	PL_AC9_LVDS64_L1P_DBC
GND	47	48	GND
PL_AC8_LVDS64_L3N	49	50	PL_AC7_LVDS64_L5N
PL_AB8_LVDS64_L3P	51	52	PL_AB7_LVDS64_L5P
GND	53	54	GND
PL_AB6_LVDS64_L6P	55	56	GND
PL_AC6_LVDS64_L6N	57	58	VCC_5V
GND	59	60	VCC_1V8

2.9.1 PS Interfaces

The interfaces which are supported in Board to Board Connector1 from Zynq Ultrascale+ MPSoC's PS is explained in the following section.

2.9.1.1 SPI Interface

The Zynq Ultrascale+ MPSoC SBC supports one SPI interface with one chip select on Board to Board Connector1. The SPI0 controller of MPSoC's PS is used for SPI interface through MIO pins. It can function in master mode, slave mode or multi-master mode and supports full-duplex operation.

For more details on SPI Interface pinouts on Board to Board Connector1, refer the below table.

Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
14	SPI0_MISO(PS_MIO4_500)	PS_MIO4_500	500	AH16	IO, 1.8V LVCMOS	SPI Master input Slave output.
16	SPI0_MOSI(PS_MIO5_500)	PS_MIO5_500	500	AD16	IO, 1.8V LVCMOS	SPI Master output Slave input.
18	SPI0_SS0(PS_MIO3_500)	PS_MIO3_500	500	AH15	O, 1.8V LVCMOS	SPI chip select0.
20	SPI0_SCLK(PS_MIO0_500)	PS_MIO0_500	500	AG15	O, 1.8V LVCMOS	SPI clock.

2.9.1.2 CAN Interface

The Zynq Ultrascale+ MPSoC SBC supports two CAN interfaces on Board to Board Connector1. The CAN0 & CAN1 controller of MPSoC's PS is used for CAN interface through MIO pins. This CAN controller is compatible with the ISO 11898-1, CAN 2.0A, and CAN 2.0B standards. And it supports bit rates up to 1Mb/s.

For more details on CAN Interface pinouts on Board to Board Connector1, refer the below table.

Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
28	CAN1_RX(PS_MIO41_501)	PS_MIO41_501	501	J19	I, 1.8V LVCMOS	CAN1 Receive data.
32	CAN1_TX(PS_MIO40_501)	PS_MIO40_501	501	K18	O, 1.8V LVCMOS	CAN1 Transmit data.
30	CAN0_TX(PS_MIO39_501)	PS_MIO39_501	501	H19	O, 1.8V LVCMOS	CAN0 Transmit data.
34	CAN0_RX(PS_MIO38_501)	PS_MIO38_501	501	H19	I, 1.8V LVCMOS	CAN0 Receive data.

2.9.1.3 I2C Interface

The Zynq Ultrascale+ MPSoC SBC supports two I2C interfaces. One I2C0 interface is used for on Board Interfaces and another I2C1 interface is directly connected to Board to Board Connector1. The I2C1 module of MPSoC's PS is used for I2C interface through MIO pins and compatible with the standard NXP I2C bus protocol. It supports standard mode with data transfer rates up to 100kbps and Fast mode with data transfer rates up to 400kbps. It can function as a master or a slave in a multi-master design. The master can be programmed to use both normal (7-bit) addressing and extended (10-bit) addressing modes. Since flexible I2C standard allows multiple devices to be connected to the single bus in the Zynq Ultrascale+ MPSoC SBC.

For more details on I2C Interface pinouts on Board to Board Connector1, refer the below table.

Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
22	I2C1_SCL(PS_MIO24_500)	PS_MIO24_500	500	AB19	O, 1.8V OD/ 4.7K PU	I2C1 clock.
24	I2C1_SDA(PS_MIO25_500)	PS_MIO25_500	500	AB21	IO, 1.8V OD/ 4.7K PU	I2C1 data.

2.9.2 PL Interfaces

2.9.2.1 PL IOs – HP BANK64

The Zynq Ultrascale+ MPSoC SBC supports 13 LVDS IOs/26 Single Ended (SE) IOs on Board to Board Connector1 from MPSoC's PL High-Performace (HP) Bank64. Upon these 13 LVDS IOs/26 SE IOs, upto 3 HDGC Global Clock Inputs and upto 8 PLSYSMON auxiliary analog inputs are available.

The IO voltage of PL Bank64 is connected from LDO1 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 1.2V to 1.8V through software. While using as LVDS IOs or Single Ended IOs, make sure to set the PMIC LDO1 to output appropriate IO voltage for PL Bank64. By default, IO voltage of PL Bank64 is set as 1.2V and after U-boot bootup configured to 1.8V. For more details about supported IO standard, refer the Zynq Ultrascale+ MPSoC datasheet.

In the Zynq Ultrascale+ MPSoC SBC, PL Bank64 signals are routed as LVDS IOs to Board to Board Connector1. Even though PL Bank64 signals are routed as LVDS IOs, these pins can be used as SE IOs if required. The Board to Board Connector1 pins 1, 3, 7, 9, 13, and 15 are HDGC Global Clock Input capable pins of PL Bank64. Also Board to Board Connector1 pins 19, 21, 25, 27, 31, 33, 43, 45, 49, 51, 55, 57, 38, 40, 50, and 52 are PLSYSMON auxiliary analog Input capable pins of PL Bank64.

For more details on PL HP Bank64 pinouts on Board to Board Connector1, refer the below table.

B2B1 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
1	PL_AE5_LVDS64_L12P_GC	IO_L12P_T1U_N10_GC_64	64	AE5	IO, 1.8V LVDS	PL Bank64 IO12 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or Single ended I/O.
3	PL_AF5_LVDS64_L12N_GC	IO_L12N_T1U_N11_GC_64	64	AF5	IO, 1.8V LVDS	PL Bank64 IO12 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or Single ended I/O.
7	PL_AF6_LVDS64_L11N_GC	IO_L11N_T1U_N9_GC_64	64	AF6	IO, 1.8V LVDS	PL Bank64 IO11 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or Single ended I/O.
9	PL_AF7_LVDS64_L11P_GC	IO_L11P_T1U_N8_GC_64	64	AF7	IO, 1.8V LVDS	PL Bank64 IO12 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or Single ended I/O.
13	PL_AD5_LVDS64_L13P_GC	IO_L13P_T2L_N0_GC_QBC_64	64	AD5	IO, 1.8V LVDS	PL Bank64 IO13 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or Single ended I/O.

B2B1 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
15	PL_AD4_LVDS64_L13N_GC	IO_L13N_T2L_N1_GC_QBC_64	64	AD4	IO, 1.8V LVDS	PL Bank64 IO13 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or Single ended I/O.
19	PL_AG5_LVDS64_L10N_QBC	IO_L10N_T1U_N7_QBC_AD4N_64	64	AG5	IO, 1.8V LVDS	PL Bank64 IO10 differential negative. Same pin can be configured as PLSYSMON differential analog input4 Negative or Single ended I/O.
21	PL_AG6_LVDS64_L10P_QBC	IO_L10P_T1U_N6_QBC_AD4P_64	64	AG6	IO, 1.8V LVDS	PL Bank64 IO10 differential positive. Same pin can be configured as PLSYSMON differential analog input4 positive or Single ended I/O.
25	PL_AH7_LVDS64_L9N	IO_L9N_T1L_N5_AD12N_64	64	AH7	IO, 1.8V LVDS	PL Bank64 IO9 differential negative. Same pin can be configured as PLSYSMON differential analog input12 Negative or Single ended I/O.
27	PL_AH8_LVDS64_L9P	IO_L9P_T1L_N4_AD12P_64	64	AH8	IO, 1.8V LVDS	PL Bank64 IO9 differential positive. Same pin can be configured as PLSYSMON differential analog input12 positive or Single ended I/O.
31	PL_AH9_LVDS64_L7N_QBC	IO_L7N_T1L_N1_QBC_AD13N_64	64	AH9	IO, 1.8V LVDS	PL Bank64 IO7 differential negative. Same pin can be configured as PLSYSMON differential analog input13 Negative or Single ended I/O.

B2B1 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
33	PL_AG9_LVDS64_L7P_QBC	IO_L7P_T1L_N0_QBC_AD13P_64	64	AG9	IO, 1.8V LVDS	PL Bank64 IO7 differential positive. Same pin can be configured as PLSYSMON differential analog input13 positive or Single ended I/O.
37	PL_AE8_LVDS64_L2N	IO_L2N_T0L_N3_64	64	AE8	IO, 1.8V LVDS	PL Bank64 IO2 differential negative. Same pin can be configured as Single ended I/O.
39	PL_AE9_LVDS64_L2P	IO_L2P_T0L_N2_64	64	AE9	IO, 1.8V LVDS	PL Bank64 IO2 differential positive. Same pin can be configured as Single ended I/O.
43	PL_AE7_LVDS64_L4N_DBC	IO_L4N_T0U_N7_DBC_AD7N_64	64	AE7	IO, 1.8V LVDS	PL Bank64 IO4 differential negative. Same pin can be configured as PLSYSMON differential analog input7 Negative or Single ended I/O.
45	PL_AD7_LVDS64_L4P_DBC	IO_L4P_T0U_N6_DBC_AD7P_64	64	AD7	IO, 1.8V LVDS	PL Bank64 IO4 differential positive. Same pin can be configured as PLSYSMON differential analog input7 positive or Single ended I/O.
49	PL_AC8_LVDS64_L3N	IO_L3N_T0L_N5_AD15N_64	64	AC8	IO, 1.8V LVDS	PL Bank64 IO3 differential negative. Same pin can be configured as PLSYSMON differential analog input15 Negative or Single ended I/O.

B2B1 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
51	PL_AB8_LVDS64_L3P	IO_L3P_T0L_N4_AD15P_64	64	AB8	IO, 1.8V LVDS	PL Bank64 IO3 differential positive. Same pin can be configured as PLSYSMON differential analog input15 positive or Single ended I/O.
55	PL_AB6_LVDS64_L6P	IO_L6P_T0U_N10_AD6P_64	64	AB6	IO, 1.8V LVDS	PL Bank64 IO6 differential positive. Same pin can be configured as PLSYSMON differential analog input6 positive or Single ended I/O.
57	PL_AC6_LVDS64_L6N	IO_L6N_T0U_N11_AD6N_64	64	AC6	IO, 1.8V LVDS	PL Bank64 IO6 differential negative. Same pin can be configured as PLSYSMON differential analog input6 negative or Single ended I/O.
38	PL_AG8_LVDS64_L8N	IO_L8N_T1L_N3_AD5N_64	64	AG8	IO, 1.8V LVDS	PL Bank64 IO8 differential negative. Same pin can be configured as PLSYSMON differential analog input5 negative or Single ended I/O.
40	PL_AF8_LVDS64_L8P	IO_L8P_T1L_N2_AD5P_64	64	AF8	IO, 1.8V LVDS	PL Bank64 IO8 differential positive. Same pin can be configured as PLSYSMON differential analog input5 positive or Single ended I/O.
44	PL_AD9_LVDS64_L1N_DBC	IO_L1N_T0L_N1_DBC_64	64	AD9	IO, 1.8V LVDS	PL Bank64 IO1 differential negative. Same pin can be configured as Single ended I/O.

B2B1 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
46	PL_AC9_LVDS64_L1P_DBC	IO_L1P_T0L_N0_DBC_64	64	AC9	IO, 1.8V LVDS	PL Bank64 IO1 differential positive. Same pin can be configured as Single ended I/O.
50	PL_AC7_LVDS64_L5N	IO_L5N_T0U_N9_AD14N_64	64	AC7	IO, 1.8V LVDS	PL Bank64 IO5 differential negative. Same pin can be configured as PLSYSMON differential analog input14 negative or Single ended I/O.
52	PL_AB7_LVDS64_L5P	IO_L5P_T0U_N8_AD14P_64	64	AB7	IO, 1.8V LVDS	PL Bank64 IO5 differential positive. Same pin can be configured as PLSYSMON differential analog input14 positive or Single ended I/O.

2.9.2.2 PL IOs – HD BANK45

The Zynq Ultrascale+ MPSoC SBC supports 4 Single Ended (SE) IOs on Board to Board Connector1 from MPSoC's PL High-Density (HD) Bank45. Upon these 4 SE IOs are available. PL Bank45 signals are routed as Single Ended IOs to Board to Board Connector1.

The IO voltage of Bank45 is connected from LDO4 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 1.2V to 3.3V through software. While using as Single Ended IOs, make sure to set the PMIC LDO4 to output appropriate IO voltage for PL Bank45. By default, IO voltage of PL Bank45 is set as 1.2V and after U-boot bootup configured to 1.8V. For more details about supported IO standard, refer the Zynq Ultrascale+ MPSoC datasheet.

Note: In ZCU2 & ZCU3 MPSoC devices, the PL Bank 43, 44, 45 & 46 is called as 44, 24, 25 & 26 respectively. Only the Bank Numbering is different and all other functionalities remain same.

For more details on PL HD Bank45 pinouts on Board to Board Connector1, refer the below table.

B2B1 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
2	PL_C11_LVDS45_L9P	IO_L9P_AD11P_45	45	C11	IO, 1.8V LVCMOS	PL Bank45 IO9 Single ended I/O.
4	PL_B10_LVDS45_L9N	IO_L9N_AD11N_45	45	B10	IO, 1.8V LVCMOS	PL Bank45 IO9 Single ended I/O.
6	PL_B11_LVDS45_L10P	IO_L10P_AD10P_45	45	B11	IO, 1.8V LVCMOS	PL Bank45 IO10 Single ended I/O.
8	PL_A10_LVDS45_L10N	IO_L10N_AD10N_45	45	A10	IO, 1.8V LVCMOS	PL Bank45 IO10 Single ended I/O.

2.9.3 Power

In Zynq Ultrascale+ MPSoC SBC, 5V and 1.8V powers are fed to Board to Board Connector1. Also in Board to Board Connector1, Ground pins are distributed throughout the connector for better performance.

For more details on Power control & Ground pins on Board to Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Pin Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
58	VCC_5V	NA	O, 5V Power	5V Supply Voltage.
60	VCC_1V8	NA	O, 1.8V Power	1.8V Supply Voltage.
5, 11, 17, 23, 29, 35, 41, 47, 53, 59, 26, 36, 42, 48, 54, 56	GND	NA	Power	Ground.

2.10 Board to Board Connector2

The Zynq Ultrascale+ MPSoC SBC supports three 60 pin high speed ruggedized terminal strip connectors, Three 60pin High performance High Density connector for interfaces expansion. All the effort is made in Zynq Ultrascale+ MPSoC SBC design to provide the maximum interfaces of Zynq Ultrascale+ MPSoC to SBC by adding these three Board to Board Connectors.

The Zynq Ultrascale+ MPSoC SBC Board to Board Connector2 pinout is provided in the below table and the interfaces which are available at Board to Board Connector2 are explained in the following sections. The Board to Board Connector2 (J22) is physically located on bottom side of the SBC as shown below.

Number of Pins - 60
Connector Part Number - TFC-130-11-L-D-A
Mating Connector - SFC-130-T1-L-D-A from Samtech
Staking Height - 7.75mm

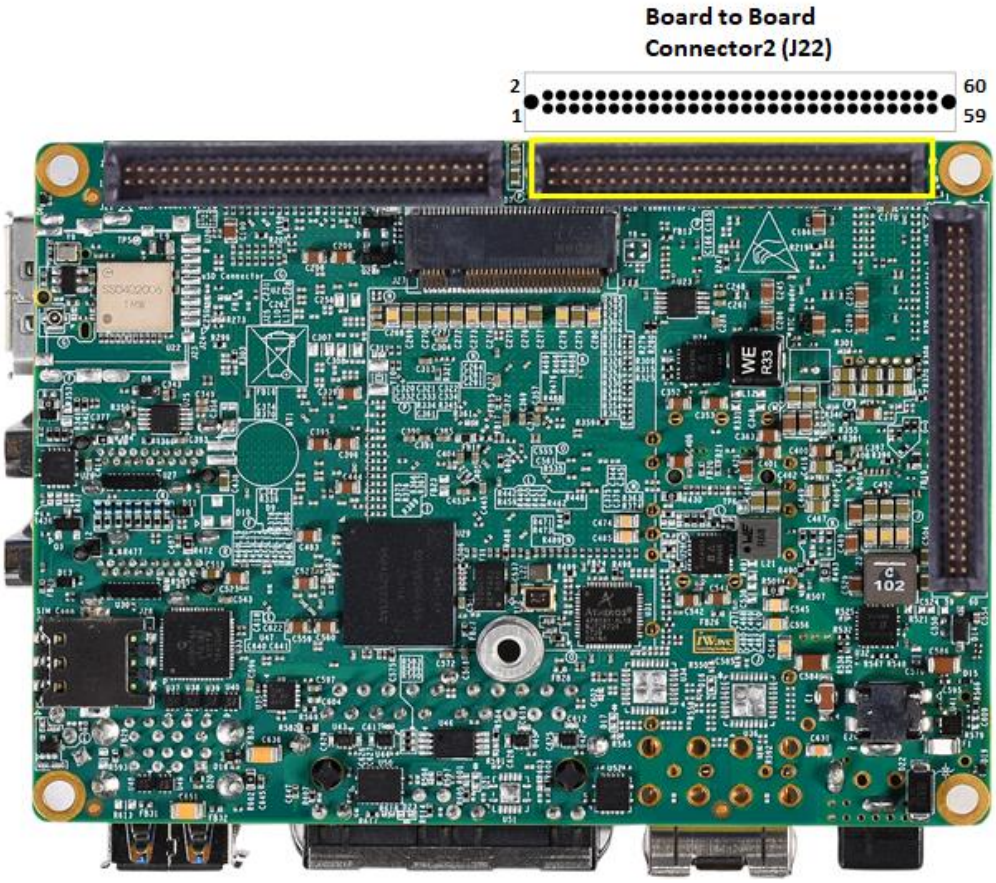

Figure 20: Board to Board Connector2

Table 12: Board to Board Connector2 Pinout

Signal	B2B-2 Pin	B2B-2 Pin	Signal
PL_AG4_LVDS64_L19P_DBC	1	2	PL_AH4_LVDS64_L19N_DBC
PL_AF1_LVDS64_L24P	3	4	PL_AG1_LVDS64_L24N
PL_AB4_LVDS64_L15P	5	6	PL_AB3_LVDS64_L15N
PL_AB2_LVDS64_L17P	7	8	PL_AC2_LVDS64_L17N
GND	9	10	GND
PL_AB1_LVDS64_L18P	11	12	PL_AC1_LVDS64_L18N
PL_AD2_LVDS64_L16P_QBC	13	14	PL_AD1_LVDS64_L16N_QBC
PL_AC4_LVDS64_L14P_GC	15	16	PL_AC3_LVDS64_L14N_GC
PL_K14_LVDS46_L11P	17	18	PL_J14_LVDS46_L11N
GND	19	20	GND
PL_L14_LVDS46_L12P	21	22	PL_L13_LVDS46_L12N
PL_G15_LVDS46_L9P	23	24	PL_G14_LVDS46_L9N
PL_B15_LVDS46_L1P	25	26	PL_A15_LVDS46_L1N
PL_D15_LVDS46_L5P_GC	27	28	PL_D14_LVDS46_L5N_GC
GND	29	30	GND
PL_C14_LVDS46_L4P	31	32	PL_C13_LVDS46_L4N
PL_B14_LVDS46_L2P	33	34	PL_A14_LVDS46_L2N
PL_B13_LVDS46_L3P	35	36	PL_A13_LVDS46_L3N
PL_E14_LVDS46_L6P_GC	37	38	PL_E13_LVDS46_L6N_GC
GND	39	40	GND
PL_F15_LVDS46_L8P_HDGC	41	42	PL_E15_LVDS46_L8N_HDGC
PL_G13_LVDS46_L7P_GC	43	44	PL_F13_LVDS46_L7N_GC
PL_H14_LVDS46_L10P	45	46	PL_H13_LVDS46_L10N
PL_H11_LVDS45_L3P	47	48	PL_G10_LVDS45_L3N
GND	49	50	GND
PL_J12_LVDS45_L4P	51	52	PL_H12_LVDS45_L4N
PL_J11_LVDS45_L1P	53	54	PL_J10_LVDS45_L1N
PL_K13_LVDS45_L2P	55	56	PL_K12_LVDS45_L2N
VCC_5V	57	58	SYSMON_VP
VCC_12V	59	60	SYSMON_VN

2.10.1 PL Interfaces

2.10.1.1 PL IOs – HP BANK64

The Zynq Ultrascale+ MPSoC SBC supports 7 LVDS IOs/14 Single Ended (SE) IOs on Board to Board Connector2 from MPSoC's PL High-Performance (HP) Bank64. Upon these 7 LVDS IOs/14 SE IOs, upto 1 HDGC Global Clock Inputs and upto 5 PLSYSMON auxiliary analog inputs are available.

The IO voltage of PL Bank64 is connected from LDO1 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 1.2V to 1.8V through software. While using as LVDS IOs or Single Ended IOs, make sure to set the PMIC LDO1 to output appropriate IO voltage for PL Bank64. By default, IO voltage of PL Bank64 is set as 1.2V and after U-boot bootup configured to 1.8V. For more details about supported IO standard, refer the Zynq Ultrascale+ MPSoC datasheet.

In the Zynq Ultrascale+ MPSoC SBC, PL Bank64 signals are routed as LVDS IOs to Board to Board Connector2. Even though PL Bank64 signals are routed as LVDS IOs, these pins can be used as SE IOs if required. The Board to Board Connector2 pins 15 and 16 are HDGC Global Clock Input capable pins of PL Bank64. Also Board to Board Connector2 pins 1, 2, 5, 6, 7, 8, 11, 12, 13, and 14 are PLSYSMON auxiliary analog Input capable pins of PL Bank64.

For more details on PL HP Bank64 pinouts on Board to Board Connector2, refer the below table.

B2B2 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
1	PL_AG4_LVDS64_L19P_DBC	IO_L19P_T3L_N0_DBC_AD9P_64	64	AG4	IO, 1.8V LVDS	PL Bank64 IO19 differential positive. Same pin can be configured as PLSYSMON differential analog input9 positive or Single ended I/O.
2	PL_AH4_LVDS64_L19N_DBC	IO_L19N_T3L_N1_DBC_AD9N_64	64	AH4	IO, 1.8V LVDS	PL Bank64 IO19 differential negative. Same pin can be configured as PLSYSMON differential analog input9 negative or Single ended I/O.
3	PL_AF1_LVDS64_L24P	IO_L24P_T3U_N10_64	64	AF1	IO, 1.8V LVDS	PL Bank64 IO24 differential positive. Same pin can be configured as Single ended I/O.

B2B2 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
4	PL_AG1_LVDS64_L24N	IO_L24N_T3U_N11_64	64	AG1	IO, 1.8V LVDS	PL Bank64 IO24 differential negative. Same pin can be configured as Single ended I/O.
5	PL_AB4_LVDS64_L15P	IO_L15P_T2L_N4_AD11P_64	64	AB4	IO, 1.8V LVDS	PL Bank64 IO15 differential positive. Same pin can be configured as PLSYSMON differential analog input11 positive or Single ended I/O.
6	PL_AB3_LVDS64_L15N	IO_L15N_T2L_N5_AD11N_64	64	AB3	IO, 1.8V LVDS	PL Bank64 IO15 differential negative. Same pin can be configured as PLSYSMON differential analog input11 negative or Single ended I/O.
7	PL_AB2_LVDS64_L17P	IO_L17P_T2U_N8_AD10P_64	64	AB2	IO, 1.8V LVDS	PL Bank64 IO17 differential positive. Same pin can be configured as PLSYSMON differential analog input10 positive or Single ended I/O.
8	PL_AC2_LVDS64_L17N	IO_L17N_T2U_N9_AD10N_64	64	AC2	IO, 1.8V LVDS	PL Bank64 IO17 differential negative. Same pin can be configured as PLSYSMON differential analog input10 negative or Single ended I/O.
11	PL_AB1_LVDS64_L18P	IO_L18P_T2U_N10_AD2P_64	64	AB1	IO, 1.8V LVDS	PL Bank64 IO18 differential positive. Same pin can be configured as PLSYSMON differential analog input2 positive or Single ended I/O.

B2B2 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
12	PL_AC1_LVDS64_L18N	IO_L18N_T2U_N11_AD2N_64	64	AC1	IO, 1.8V LVDS	PL Bank64 IO18 differential negative. Same pin can be configured as PLSYSMON differential analog input2 negative or Single ended I/O.
13	PL_AD2_LVDS64_L16P_QBC	IO_L16P_T2U_N6_QBC_AD3P_64	64	AD2	IO, 1.8V LVDS	PL Bank64 IO16 differential positive. Same pin can be configured as PLSYSMON differential analog input3 positive or Single ended I/O.
14	PL_AD1_LVDS64_L16N_QBC	IO_L16N_T2U_N7_QBC_AD3N_64	64	AD1	IO, 1.8V LVDS	PL Bank64 IO16 differential negative. Same pin can be configured as PLSYSMON differential analog input3 negative or Single ended I/O.
15	PL_AC4_LVDS64_L14P_GC	IO_L14P_T2L_N2_GC_64	64	AC4	IO, 1.8V LVDS	PL Bank64 IO14 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or Single ended I/O.
16	PL_AC3_LVDS64_L14N_GC	IO_L14N_T2L_N3_GC_64	64	AC3	IO, 1.8V LVDS	PL Bank64 IO14 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or Single ended I/O.

2.10.1.2 PL IOs –HD BANK45

The Zynq Ultrascale+ MPSoC SBC supports 4 LVDS IOs/8 Single Ended (SE) IOs on Board to Board Connector2 from MPSoC's PL High-Density (HD) Bank45. Upon these 4 LVDS IOs/8 SE IOs, upto 4 PLSYSMON auxiliary analog inputs are available.

The IO voltage of Bank45 is connected from LDO4 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 1.2V to 3.3V through software. While using as LVDS IOs or Single Ended IOs, make sure to set the PMIC LDO4 to output appropriate IO voltage for PL Bank45. By default, IO voltage of PL Bank45 is set as 1.2V and after U-boot bootup configured to 1.8V. For more details about supported IO standard, refer the Zynq Ultrascale+ MPSoC datasheet.

In the Zynq Ultrascale+ MPSoC SBC, PL Bank45 signals are routed as LVDS IOs to Board to Board Connector2. Even though PL Bank45 signals are routed as LVDS IOs, these pins can be used as SE IOs if required. The Board to Board Connector2 pins 47, 48, 51, 52, 53, 54, 55 and 56 are PLSYSMON auxiliary analog Input capable pins of PL Bank45.

Note: In ZCU2 & ZCU3 MPSoC devices, the PL Bank 43, 44, 45 & 46 is called as 44, 24, 25 & 26 respectively. Only the Bank Numbering is different and all other functionalities remain same.

For more details on PL HD Bank45 pinouts on Board to Board Connector2, refer the below table.

B2B2 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
47	PL_H11_LVDS45_L3P	IO_L3P_AD13P_45	45	H11	IO, 1.8V LVDS	PL Bank45 IO3 differential positive. Same pin can be configured as PLSYSMON differential analog input13 positive or Single ended I/O.
48	PL_G10_LVDS45_L3N	IO_L3N_AD13N_45	45	G10	IO, 1.8V LVDS	PL Bank45 IO3 differential negative. Same pin can be configured as PLSYSMON differential analog input13 negative or Single ended I/O.

B2B2 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
51	PL_J12_LVDS45_L4P	IO_L4P_AD12P_45	45	J12	IO, 1.8V LVDS	PL Bank45 IO4 differential positive. Same pin can be configured as PLSYSMON differential analog input12 positive or Single ended I/O.
52	PL_H12_LVDS45_L4N	IO_L4N_AD12N_45	45	H12	IO, 1.8V LVDS	PL Bank45 IO4 differential negative. Same pin can be configured as PLSYSMON differential analog input12 negative or Single ended I/O.
53	PL_J11_LVDS45_L1P	IO_L1P_AD15P_45	45	J11	IO, 1.8V LVDS	PL Bank45 IO1 differential positive. Same pin can be configured as PLSYSMON differential analog input15 positive or Single ended I/O.
54	PL_J10_LVDS45_L1N	IO_L1N_AD15N_45	45	J10	IO, 1.8V LVDS	PL Bank45 IO1 differential negative. Same pin can be configured as PLSYSMON differential analog input15 negative or Single ended I/O.
55	PL_K13_LVDS45_L2P	IO_L2P_AD14P_45	45	K13	IO, 1.8V LVDS	PL Bank45 IO2 differential positive. Same pin can be configured as PLSYSMON differential analog input14 positive or Single ended I/O.
56	PL_K12_LVDS45_L2N	IO_L2N_AD14N_45	45	K12	IO, 1.8V LVDS	PL Bank45 IO2 differential negative. Same pin can be configured as PLSYSMON differential analog input14 negative or Single ended I/O.

2.10.1.3 PL IOs –HD BANK46

The Zynq Ultrascale+ MPSoC SBC supports 12 LVDS IOs/24 Single Ended (SE) IOs on Board to Board Connector2 from MPSoC's PL High-Density (HD) Bank46. Upon these 12 LVDS IOs/24 SE IOs, upto 4 HDGC Global Clock Inputs and upto 12 PLSYSMON auxiliary analog inputs are available.

The IO voltage of Bank46 is connected from LDO7 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 1.2V to 3.3V through software. While using as LVDS IOs or Single Ended IOs, make sure to set the PMIC LDO7 to output appropriate IO voltage for PL Bank46. By default, IO voltage of PL Bank46 is set as 1.2V and after U-boot bootup configured to 1.8V. For more details about supported IO standard, refer the Zynq Ultrascale+ MPSoC datasheet.

In the Zynq Ultrascale+ MPSoC SBC, PL Bank46 signals are routed as LVDS IOs to Board to Board Connector2. Even though PL Bank46 signals are routed as LVDS IOs, these pins can be used as SE IOs if required. The Board to Board Connector2 pins 27, 28, 37, 38, 41, 42, 43 and 44 are HDGC Global Clock Input capable pins of PL Bank46. Also Board to Board Connector2 pins 17, 18, 21, 22, 23, 24, 25, 26, 27, 28, 31, 32, 33, 34, 35, 36, 37, 38, 41, 42, 43, 44, 45 and 46 are PLSYSMON auxiliary analog Input capable pins of PL Bank46.

Note: In ZCU2 & ZCU3 MPSoC devices, the PL Bank 43, 44, 45 & 46 is called as 44, 24, 25 & 26 respectively. Only the Bank Numbering is different and all other functionalities remain same.

For more details on PL HD Bank46 pinouts on Board to Board Connector2, refer the below table.

B2B2 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
17	PL_K14_LVDS46_L11P	IO_L11P_AD1P_46	46	K14	IO, 1.8V LVDS	PL Bank46 IO11 differential positive. Same pin can be configured as PLSYSMON differential analog input1 positive or Single ended I/O.
18	PL_J14_LVDS46_L11N	IO_L11N_AD1N_46	46	J14	IO, 1.8V LVDS	PL Bank46 IO11 differential negative. Same pin can be configured as PLSYSMON differential analog input1 negative or Single ended I/O.

B2B2 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
21	PL_L14_LVDS46_ L12P	IO_L12P_AD0P_46	46	L14	IO, 1.8V LVDS	PL Bank46 IO12 differential positive. Same pin can be configured as PLSYSMON differential analog input0 positive or Single ended I/O.
22	PL_L13_LVDS46_ L12N	IO_L12N_AD0N_46	46	L13	IO, 1.8V LVDS	PL Bank46 IO12 differential negative. Same pin can be configured as PLSYSMON differential analog input0 negative or Single ended I/O.
23	PL_G15_LVDS46_ L9P	IO_L9P_AD3P_46	46	G15	IO, 1.8V LVDS	PL Bank46 IO9 differential positive. Same pin can be configured as PLSYSMON differential analog input3 positive or Single ended I/O.
24	PL_G14_LVDS46_ L9N	IO_L9N_AD3N_46	46	G14	IO, 1.8V LVDS	PL Bank46 IO9 differential negative. Same pin can be configured as PLSYSMON differential analog input3 negative or Single ended I/O.
25	PL_B15_LVDS46_ L1P	IO_L1P_AD11P_46	46	B15	IO, 1.8V LVDS	PL Bank46 IO1 differential positive. Same pin can be configured as PLSYSMON differential analog input11 positive or Single ended I/O.
26	PL_A15_LVDS46_ L1N	IO_L1N_AD11N_46	46	A15	IO, 1.8V LVDS	PL Bank46 IO1 differential negative. Same pin can be configured as PLSYSMON differential analog input11 negative or Single ended I/O.

B2B2 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
27	PL_D15_LVDS46_L5P_GC	IO_L5P_HDGC_AD7P_46	46	D15	IO, 1.8V LVDS	PL Bank46 IO5 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or PLSYSMON differential analog input7 positive or Single ended I/O.
28	PL_D14_LVDS46_L5N_GC	IO_L5N_HDGC_AD7N_46	46	D14	IO, 1.8V LVDS	PL Bank46 IO5 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or PLSYSMON differential analog input7 negative or Single ended I/O.
31	PL_C14_LVDS46_L4P	IO_L4P_AD8P_46	46	C14	IO, 1.8V LVDS	PL Bank46 IO4 differential positive. Same pin can be configured as PLSYSMON differential analog input8 positive or Single ended I/O.
32	PL_C13_LVDS46_L4N	IO_L4N_AD8N_46	46	C13	IO, 1.8V LVDS	PL Bank46 IO4 differential negative. Same pin can be configured as PLSYSMON differential analog input8 negative or Single ended I/O.
33	PL_B14_LVDS46_L2P	IO_L2P_AD10P_46	46	B14	IO, 1.8V LVDS	PL Bank46 IO2 differential positive. Same pin can be configured as PLSYSMON differential analog input10 positive or Single ended I/O.

B2B2 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
34	PL_A14_LVDS46_L2N	IO_L2N_AD10N_46	46	A14	IO, 1.8V LVDS	PL Bank46 IO2 differential negative. Same pin can be configured as PLSYSMON differential analog input10 negative or Single ended I/O.
35	PL_B13_LVDS46_L3P	IO_L3P_AD9P_46	46	B13	IO, 1.8V LVDS	PL Bank46 IO3 differential positive. Same pin can be configured as PLSYSMON differential analog input9 positive or Single ended I/O.
36	PL_A13_LVDS46_L3N	IO_L3N_AD9N_46	46	A13	IO, 1.8V LVDS	PL Bank46 IO3 differential negative. Same pin can be configured as PLSYSMON differential analog input9 negative or Single ended I/O.
37	PL_E14_LVDS46_L6P_GC	IO_L6P_HDGC_AD6P_46	46	E14	IO, 1.8V LVDS	PL Bank46 IO6 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or PLSYSMON differential analog input6 positive or Single ended I/O.
38	PL_E13_LVDS46_L6N_GC	IO_L6N_HDGC_AD6N_46	46	E13	IO, 1.8V LVDS	PL Bank46 IO6 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or PLSYSMON differential analog input6 negative or Single ended I/O.

B2B2 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
41	PL_F15_LVDS46_L8P_HDGC	IO_L8P_HDGC_AD4P_46	46	F15	IO, 1.8V LVDS	PL Bank46 IO8 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or PLSYSMON differential analog input4 positive or Single ended I/O.
42	PL_E15_LVDS46_L8N_HDGC	IO_L8N_HDGC_AD4N_46	46	E15	IO, 1.8V LVDS	PL Bank46 IO8 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or PLSYSMON differential analog input4 negative or Single ended I/O.
43	PL_G13_LVDS46_L7P_GC	IO_L7P_HDGC_AD5P_46	46	G13	IO, 1.8V LVDS	PL Bank46 IO7 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or PLSYSMON differential analog input5 positive or Single ended I/O.
44	PL_F13_LVDS46_L7N_GC	IO_L7N_HDGC_AD5N_46	46	F13	IO, 1.8V LVDS	PL Bank46 IO7 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or PLSYSMON differential analog input5 negative or Single ended I/O.

B2B2 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
45	PL_H14_LVDS46_ L10P	IO_L10P_AD2P_46	46	H14	IO, 1.8V LVDS	PL Bank46 IO10 differential positive. Same pin can be configured as PLSYSMON differential analog input2 positive or Single ended I/O.
46	PL_H13_LVDS46_ L10N	IO_L10N_AD2N_46	46	H13	IO, 1.8V LVDS	PL Bank46 IO10 differential negative. Same pin can be configured as PLSYSMON differential analog input2 negative or Single ended I/O.

2.10.2 Power

In Zynq Ultrascale+ MPSoC SBC, 5V and 12V powers are fed to Board to Board Connector2. Also in Board to Board Connector2, Ground pins are distributed throughout the connector for better performance.

For more details on Power control & Ground pins on Board to Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Pin Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
57	VCC_5V	NA	O, 5V Power	5V Supply Voltage.
59	VCC_12V	NA	O, 12V Power	12V Supply Voltage.
9, 19, 29, 39, 49, 10, 20, 30, 40, 50	GND	NA	Power	Ground.

2.11 Board to Board Connector3

The Zynq Ultrascale+ MPSoC SBC supports three 60 pin high speed ruggedized terminal strip connectors, Three 60pin High performance High Density connector for interfaces expansion. All the effort is made in Zynq Ultrascale+ MPSoC SBC design to provide the maximum interfaces of Zynq Ultrascale+ MPSoC to SBC by adding these three Board to Board Connectors.

The Zynq Ultrascale+ MPSoC SBC Board to Board Connector3 pinout is provided in the below table and the interfaces which are available at Board to Board Connector3 are explained in the following sections. The Board to Board Connector3 (J26) is physically located on bottom side of the SBC as shown below.

Number of Pins - 60
Connector Part Number - TFC-130-11-L-D-A
Mating Connector - SFC-130-T1-L-D-A from Samtech
Staking Height - 7.75mm

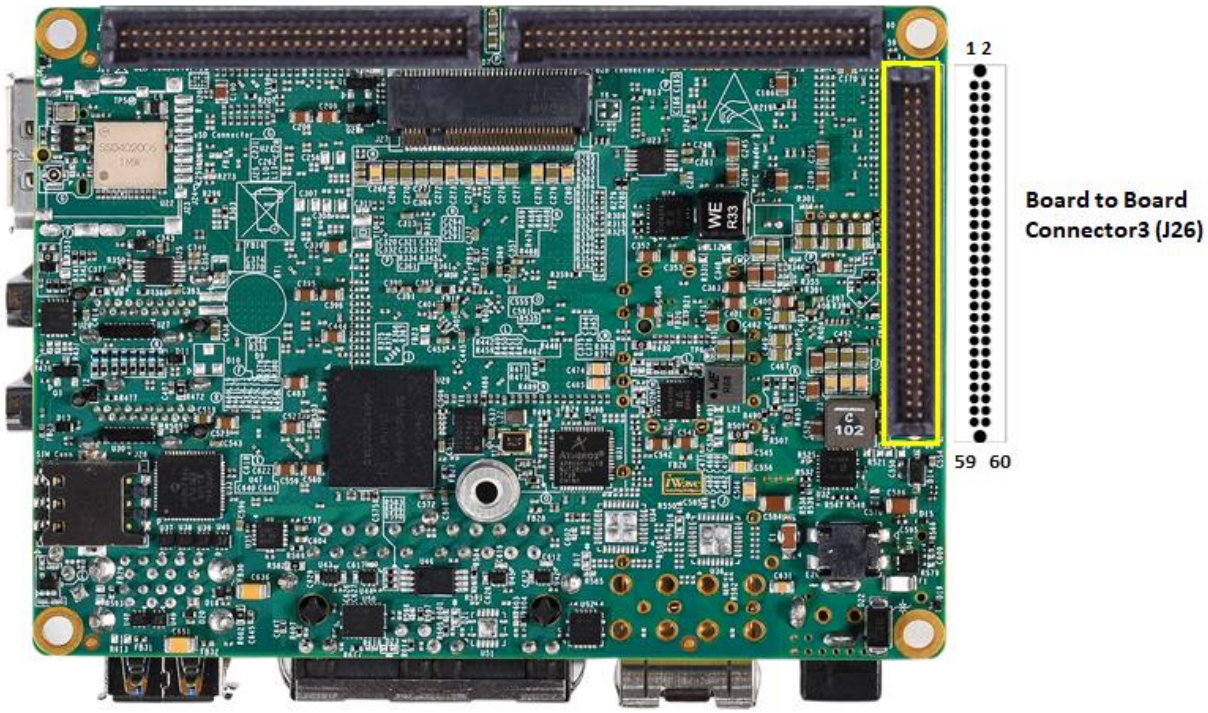

Figure 21: Board to Board Connector3

Table 13: Board to Board Connector3 Pinout

Signal	B2B-3 Pin	B2B-3 Pin	Signal
PL_AE13_LVDS44_L4P	1	2	PL_AF13_LVDS44_L4N
PL_AE15_LVDS44_L1P	3	4	PL_AE14_LVDS44_L1N
PL_AD15_LVDS44_L5P_HDGC	5	6	PL_AD14_LVDS44_L5N_HDGC
PL_AB15_LVDS44_L8P_HDGC	7	8	PL_AB14_LVDS44_L8N_HDGC
GND	9	10	GND
PL_AC14_LVDS44_L6P_HDGC	11	12	PL_AC13_LVDS44_L6N_HDGC
PL_Y14_LVDS44_L10P	13	14	PL_Y13_LVDS44_L10N
PL_W14_LVDS44_L9P	15	16	PL_W13_LVDS44_L9N
PL_AA13_LVDS44_L7P_HDGC	17	18	PL_AB13_LVDS44_L7N_HDGC
GND	19	20	GND
PL_W12_LVDS44_L11P	21	22	PL_W11_LVDS44_L11N
PL_Y12_LVDS44_L12P	23	24	PL_AA12_LVDS44_L12N
PL_AG14_LVDS44_L2P	25	26	PL_AH14_LVDS44_L2N
GND	27	28	GND
PL_AG13_LVDS44_L3P	29	30	PL_AH13_LVDS44_L3N
PL_W10_LVDS43_L10P	31	32	PL_Y10_LVDS43_L10N
PL_Y9_LVDS43_L11P	33	34	PL_AA8_LVDS43_L11N
PL_AA11_LVDS43_L9P	35	36	PL_AA10_LVDS43_L9N
GND	37	38	GND
PL_AB10_LVDS43_L12P	39	40	PL_AB9_LVDS43_L12N
PL_AB11_LVDS43_L8P_HDGC	41	42	PL_AC11_LVDS43_L8N_HDGC
PL_AD11_LVDS43_L7P_HDGC	43	44	PL_AD10_LVDS43_L7N_HDGC
GND	45	46	GND
PL_AE10_LVDS43_L4P	47	48	PL_AF10_LVDS43_L4N
PL_AF11_LVDS43_L2P	49	50	PL_AG11_LVDS43_L2N
PL_AG10_LVDS43_L1P	51	52	PL_AH10_LVDS43_L1N
PL_AC12_LVDS43_L6P_HDGC	53	54	PL_AD12_LVDS43_L6N_HDGC
GND	55	56	GND
VCC_5V	57	58	PL_AH12_LVDS43_L3P
VCC_12V	59	60	PL_AH11_LVDS43_L3N

2.11.1 PL Interfaces

2.11.1.1 PL IOs –HD BANK43

The Zynq Ultrascale+ MPSoC SBC supports 11 LVDS IOs/22 Single Ended (SE) IOs on Board to Board Connector3 from MPSoC's PL High-Density (HD) Bank43. Upon these 11 LVDS IOs/22 SE IOs, upto 3 HDGC Global Clock Inputs and upto 11 PLSYSMON auxiliary analog inputs are available.

The IO voltage of Bank43 is connected from LDO6 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 1.2V to 3.3V through software. While using as LVDS IOs or Single Ended IOs, make sure to set the PMIC LDO6 to output appropriate IO voltage for PL Bank43. By default, IO voltage of PL Bank43 is set as 1.2V and after U-boot bootup configured to 1.8V. For more details about supported IO standard, refer the Zynq Ultrascale+ MPSoC datasheet.

In the Zynq Ultrascale+ MPSoC SBC, PL Bank43 signals are routed as LVDS IOs to Board to Board Connector3. Even though PL Bank43 signals are routed as LVDS IOs, these pins can be used as SE IOs if required. The Board to Board Connector3 pins 41, 42, 43, 44, 53 and 54 are HDGC Global Clock Input capable pins of PL Bank43. Also Board to Board Connector3 pins 31, 32, 33, 34, 35, 36, 39, 40, 41, 42, 43, 44, 47, 48, 49, 50, 51, 52, 53, 54, 58, and 60 are PLSYSMON auxiliary analog Input capable pins of PL Bank43.

Note: In ZCU2 & ZCU3 MPSoC devices, the PL Bank 43, 44, 45 & 46 is called as 44, 24, 25 & 26 respectively. Only the Bank Numbering is different and all other functionalities remain same.

For more details on PL HD Bank43 pinouts on Board to Board Connector3, refer the below table.

B2B3 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
31	PL_W10_LVDS43_L10P	IO_L10P_AD2P_43	43	W10	IO, 1.8V LVDS	PL Bank43 IO10 differential positive. Same pin can be configured as PLSYSMON differential analog input2 positive or Single ended I/O.
32	PL_Y10_LVDS43_L10N	IO_L10N_AD2N_43	43	Y10	IO, 1.8V LVDS	PL Bank43 IO10 differential negative. Same pin can be configured as PLSYSMON differential analog input2 negative or Single ended I/O.

B2B3 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
33	PL_Y9_LVDS43_L11P	IO_L11P_AD1P_43	43	Y9	IO, 1.8V LVDS	PL Bank43 IO11 differential positive. Same pin can be configured as PLSYSMON differential analog input1 positive or Single ended I/O.
34	PL_AA8_LVDS43_L11N	IO_L11N_AD1N_43	43	AA8	IO, 1.8V LVDS	PL Bank43 IO11 differential negative. Same pin can be configured as PLSYSMON differential analog input1 negative or Single ended I/O.
35	PL_AA11_LVDS43_L9P	IO_L9P_AD3P_43	43	AA11	IO, 1.8V LVDS	PL Bank43 IO9 differential positive. Same pin can be configured as PLSYSMON differential analog input3 positive or Single ended I/O.
36	PL_AA10_LVDS43_L9N	IO_L9N_AD3N_43	43	AA10	IO, 1.8V LVDS	PL Bank43 IO9 differential negative. Same pin can be configured as PLSYSMON differential analog input3 negative or Single ended I/O.
39	PL_AB10_LVDS43_L12P	IO_L12P_AD0P_43	43	AB10	IO, 1.8V LVDS	PL Bank43 IO12 differential positive. Same pin can be configured as PLSYSMON differential analog input0 positive or Single ended I/O.
40	PL_AB9_LVDS43_L12N	IO_L12N_AD0N_43	43	AB9	IO, 1.8V LVDS	PL Bank43 IO12 differential negative. Same pin can be configured as PLSYSMON differential analog input0 negative or Single ended I/O.

B2B3 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
41	PL_AB11_LVDS43_L8P_HDGC	IO_L8P_HDGC_AD4P_43	43	AB11	IO, 1.8V LVDS	PL Bank43 IO8 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or PLSYSMON differential analog input4 positive or Single ended I/O.
42	PL_AC11_LVDS43_L8N_HDGC	IO_L8N_HDGC_AD4N_43	43	AC11	IO, 1.8V LVDS	PL Bank43 IO8 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or PLSYSMON differential analog input4 negative or Single ended I/O.
43	PL_AD11_LVDS43_L7P_HDGC	IO_L7P_HDGC_AD5P_43	43	AD11	IO, 1.8V LVDS	PL Bank43 IO7 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or PLSYSMON differential analog input5 positive or Single ended I/O.
44	PL_AD10_LVDS43_L7N_HDGC	IO_L7N_HDGC_AD5N_43	43	AD10	IO, 1.8V LVDS	PL Bank43 IO7 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or PLSYSMON differential analog input5 negative or Single ended I/O.

B2B3 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
47	PL_AE10_LVDS43_L4P	IO_L4P_AD8P_43	43	AE10	IO, 1.8V LVDS	PL Bank43 IO4 differential positive. Same pin can be configured as PLSYSMON differential analog input8 positive or Single ended I/O.
48	PL_AF10_LVDS43_L4N	IO_L4N_AD8N_43	43	AF10	IO, 1.8V LVDS	PL Bank43 IO4 differential negative. Same pin can be configured as PLSYSMON differential analog input8 negative or Single ended I/O.
49	PL_AF11_LVDS43_L2P	IO_L2P_AD10P_43	43	AF11	IO, 1.8V LVDS	PL Bank43 IO2 differential positive. Same pin can be configured as PLSYSMON differential analog input10 positive or Single ended I/O.
50	PL_AG11_LVDS43_L2N	IO_L2N_AD10N_43	43	AG11	IO, 1.8V LVDS	PL Bank43 IO2 differential negative. Same pin can be configured as PLSYSMON differential analog input10 negative or Single ended I/O.
51	PL_AG10_LVDS43_L1P	IO_L1P_AD11P_43	43	AG10	IO, 1.8V LVDS	PL Bank43 IO1 differential positive. Same pin can be configured as PLSYSMON differential analog input11 positive or Single ended I/O.
52	PL_AH10_LVDS43_L1N	IO_L1N_AD11N_43	43	AH10	IO, 1.8V LVDS	PL Bank43 IO1 differential negative. Same pin can be configured as PLSYSMON differential analog input11 negative or Single ended I/O.

B2B3 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
53	PL_AC12_LVDS43_L6P_HDGC	IO_L6P_HDGC_AD6P_43	43	AC12	IO, 1.8V LVDS	PL Bank43 IO6 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or PLSYSMON differential analog input6 positive or Single ended I/O.
54	PL_AD12_LVDS43_L6N_HDGC	IO_L6N_HDGC_AD6N_43	43	AD12	IO, 1.8V LVDS	PL Bank43 IO6 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or PLSYSMON differential analog input6 negative or Single ended I/O.
58	PL_AH12_LVDS43_L3P	IO_L3P_AD9P_43	43	AH12	IO, 1.8V LVDS	PL Bank43 IO3 differential positive. Same pin can be configured as PLSYSMON differential analog input9 positive or Single ended I/O.
60	PL_AH11_LVDS43_L3N	IO_L3N_AD9N_43	43	AH11	IO, 1.8V LVDS	PL Bank43 IO3 differential negative. Same pin can be configured as PLSYSMON differential analog input9 negative or Single ended I/O.

2.11.1.2 PL IOs –HD BANK44

The Zynq Ultrascale+ MPSoC SBC supports 12 LVDS IOs/24 Single Ended (SE) IOs on Board to Board Connector3 from MPSoC's PL High-Density (HD) Bank44. Upon these 12 LVDS IOs/24 SE IOs, upto 4 HDGC Global Clock Inputs and upto 8 PLSYSMON auxiliary analog inputs are available.

The IO voltage of Bank44 is connected from LDO3 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 1.2V to 3.3V through software. While using as LVDS IOs or Single Ended IOs, make sure to set the PMIC LDO3 to output appropriate IO voltage for PL Bank44. By default, IO voltage of PL Bank44 is set as 1.2V and after U-boot bootup configured to 1.8V. For more details about supported IO standard, refer the Zynq Ultrascale+ MPSoC datasheet.

In the Zynq Ultrascale+ MPSoC SBC, PL Bank44 signals are routed as LVDS IOs to Board to Board Connector3. Even though PL Bank44 signals are routed as LVDS IOs, these pins can be used as SE IOs if required. The Board to Board Connector3 pins 5, 6, 7, 8, 11, 12, 17, and 18 are HDGC Global Clock Input capable pins of PL Bank44. Also Board to Board Connector3 pins 1, 2, 3, 4, 13, 14, 15, 16, 21, 22, 23, 24, 25, 26, 29 and 30 are PLSYSMON auxiliary analog Input capable pins of PL Bank44.

Note: In ZCU2 & ZCU3 MPSoC devices, the PL Bank 43, 44, 45 & 46 is called as 44, 24, 25 & 26 respectively. Only the Bank Numbering is different and all other functionalities remain same.

For more details on PL HD Bank44 pinouts on Board to Board Connector3, refer the below table.

B2B3 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
1	PL_AE13_LVDS44_L4P	IO_L4P_AD12P_44	44	AE13	IO, 1.8V LVDS	PL Bank44 IO4 differential positive. Same pin can be configured as PLSYSMON differential analog input12 positive or Single ended I/O.
2	PL_AF13_LVDS44_L4N	IO_L4N_AD12N_44	44	AF13	IO, 1.8V LVDS	PL Bank44 IO4 differential negative. Same pin can be configured as PLSYSMON differential analog input12 negative or Single ended I/O.

B2B3 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
3	PL_AE15_LVDS44_L1P	IO_L1P_AD15P_44	44	AE15	IO, 1.8V LVDS	PL Bank44 IO1 differential positive. Same pin can be configured as PLSYSMON differential analog input15 positive or Single ended I/O.
4	PL_AE14_LVDS44_L1N	IO_L1N_AD15N_44	44	AE14	IO, 1.8V LVDS	PL Bank44 IO1 differential negative. Same pin can be configured as PLSYSMON differential analog input15 negative or Single ended I/O.
5	PL_AD15_LVDS44_L5P_HDGC	IO_L5P_HDGC_44	44	AD15	IO, 1.8V LVDS	PL Bank44 IO5 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or Single ended I/O.
6	PL_AD14_LVDS44_L5N_HDGC	IO_L5N_HDGC_44	44	AD14	IO, 1.8V LVDS	PL Bank44 IO5 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or Single ended I/O.
7	PL_AB15_LVDS44_L8P_HDGC	IO_L8P_HDGC_44	44	AB15	IO, 1.8V LVDS	PL Bank44 IO8 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or Single ended I/O.
8	PL_AB14_LVDS44_L8N_HDGC	IO_L8N_HDGC_44	44	AB14	IO, 1.8V LVDS	PL Bank44 IO8 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or Single ended I/O.

B2B3 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
11	PL_AC14_LVDS44_L6P_HDGC	IO_L6P_HDGC_44	44	AC14	IO, 1.8V LVDS	PL Bank44 IO6 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or Single ended I/O.
12	PL_AC13_LVDS44_L6N_HDGC	IO_L6N_HDGC_44	44	AC13	IO, 1.8V LVDS	PL Bank44 IO6 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or Single ended I/O.
13	PL_Y14_LVDS44_L10P	IO_L10P_AD10P_44	44	Y14	IO, 1.8V LVDS	PL Bank44 IO10 differential positive. Same pin can be configured as PLSYSMON differential analog input10 positive or Single ended I/O.
14	PL_Y13_LVDS44_L10N	IO_L10N_AD10N_44	44	Y13	IO, 1.8V LVDS	PL Bank44 IO10 differential negative. Same pin can be configured as PLSYSMON differential analog input10 negative or Single ended I/O.
15	PL_W14_LVDS44_L9P	IO_L9P_AD11P_44	44	W14	IO, 1.8V LVDS	PL Bank44 IO9 differential positive. Same pin can be configured as PLSYSMON differential analog input11 positive or Single ended I/O.
16	PL_W13_LVDS44_L9N	IO_L9N_AD11N_44	44	W13	IO, 1.8V LVDS	PL Bank44 IO9 differential negative. Same pin can be configured as PLSYSMON differential analog input11 negative or Single ended I/O.

B2B3 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
17	PL_AA13_LVDS44_L7P_HDGC	IO_L7P_HDGC_44	44	AA13	IO, 1.8V LVDS	PL Bank44 IO7 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or Single ended I/O.
18	PL_AB13_LVDS44_L7N_HDGC	IO_L7N_HDGC_44	44	AB13	IO, 1.8V LVDS	PL Bank44 IO7 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or Single ended I/O.
21	PL_W12_LVDS44_L11P	IO_L11P_AD9P_44	44	W12	IO, 1.8V LVDS	PL Bank44 IO11 differential positive. Same pin can be configured as PLSYSMON differential analog input9 positive or Single ended I/O.
22	PL_W11_LVDS44_L11N	IO_L11N_AD9N_44	44	W11	IO, 1.8V LVDS	PL Bank44 IO11 differential negative. Same pin can be configured as PLSYSMON differential analog input9 negative or Single ended I/O.
23	PL_Y12_LVDS44_L12P	IO_L12P_AD8P_44	44	Y12	IO, 1.8V LVDS	PL Bank44 IO12 differential positive. Same pin can be configured as PLSYSMON differential analog input8 positive or Single ended I/O.
24	PL_AA12_LVDS44_L12N	IO_L12N_AD8N_44	44	AA12	IO, 1.8V LVDS	PL Bank44 IO12 differential negative. Same pin can be configured as PLSYSMON differential analog input8 negative or Single ended I/O.

B2B3 Pin No	Signal Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
25	PL_AG14_LVDS44_L2P	IO_L2P_AD14P_44	44	AG14	IO, 1.8V LVDS	PL Bank44 IO2 differential positive. Same pin can be configured as PLSYSMON differential analog input14 positive or Single ended I/O.
26	PL_AH14_LVDS44_L2N	IO_L2N_AD14N_44	44	AH14	IO, 1.8V LVDS	PL Bank44 IO2 differential negative. Same pin can be configured as PLSYSMON differential analog input14 negative or Single ended I/O.
29	PL_AG13_LVDS44_L3P	IO_L3P_AD13P_44	44	AG13	IO, 1.8V LVDS	PL Bank44 IO3 differential positive. Same pin can be configured as PLSYSMON differential analog input13 positive or Single ended I/O.
30	PL_AH13_LVDS44_L3N	IO_L3N_AD13N_44	44	AH13	IO, 1.8V LVDS	PL Bank44 IO3 differential negative. Same pin can be configured as PLSYSMON differential analog input13 negative or Single ended I/O.

2.11.2 Power

In Zynq Ultrascale+ MPSoC SBC, 5V and 12V powers are fed to Board to Board Connector3. Also in Board to Board Connector3, Ground pins are distributed throughout the connector for better performance.

For more details on Power control & Ground pins on Board to Board Connector3, refer the below table.

B2B-2 Pin No	B2B Connector3 Pin Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
57	VCC	NA	O, 5V Power	5V Supply Voltage.
59	VCC	NA	O, 12V Power	12V Supply Voltage.
9, 19, 27, 37, 45, 55, 10, 20, 28, 38, 46, 56,	GND	NA	Power	Ground.

2.12 Zynq Ultrascale+ MPSoC PS Pin Multiplexing on Board to Board Connectors

The Zynq Ultrascale+ MPSoC PS IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement. Also most of MPSoC PS IO pins can be configured as GPIO if required. The below table provides the details of PS pin connections on Zynq Ultrascale+ MPSoC SBC with selected pin function (highlighted) and available alternate functions. This table has been prepared by referring PS I/O configuration in Xilinx Vivado Design Suite. To know the complete available alternate functions, refer the PS I/O configuration in the latest Vivado Design Suite

Table 14: PS IOMUX on Zynq Ultrascale+ MPSoC SBC

Interface/ Function	B2B Connector Pin Number	Zynq Ultrascale+ MPSoC Pin Name	GPIO	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13
On SBC Features from MPSoC PS																
eMMC FLASH	NA	PS_MIO13_500	GPIO13	NFC_CE	eMMC_DATA0	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TDI	SPI0_SS2	-	-	UART1_RX	-
	NA	PS_MIO14_500	GPIO14	NFC_CLE	eMMC _DATA1	-	CAN0_RX	-	I2C0_SCL	-	PJTAG_TDO	SPI0_SS1	-	UART0_RX	-	-
	NA	PS_MIO15_500	GPIO15	NFC_ALE	eMMC_DATA2	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TMS	SPI0_SS0	-	UART0_TX	-	-
	NA	PS_MIO16_500	GPIO16	NFC_DATA0	eMMC _DATA3	-	-	CAN1_TX	-	I2C1_SCL	-	SPI0_MISO	-	-	UART1_TX	-
	NA	PS_MIO17_500	GPIO17	NFC_DATA1	eMMC _DATA4	-	-	CAN1_RX	-	I2C1_SDA	-	SPI0_MIOSI	-	-	UART1_RX	-
	NA	PS_MIO18_500	GPIO18	NFC_DATA2	eMMC _DATA5	-	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_SCLK	UART0_RX	-	-
	NA	PS_MIO19_500	GPIO19	NFC_DATA3	eMMC _DATA6	-	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_SS2	UART0_TX	-	-
	NA	PS_MIO20_500	GPIO20	NFC_DATA4	eMMC _DATA7	-	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_SS1	-	UART1_TX	-
	NA	PS_MIO21_500	GPIO21	NFC_DATA5	eMMC _CMD	-	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_SS0	-	UART1_RX	-
	NA	PS_MIO22_500	GPIO22	NFC_WE_B	eMMC _CLK	-	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_MISO	UART0_RX	-	-
	NA	PS_MIO23_500	GPIO23	NFC_DATA6	eMMC_Reset	-	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_MIOSI	UART0_TX	-	-
GEM0	NA	PS_MIO26_501	GPIO26	GEM0_TX_CLK	-	-	CAN0_RX	-	I2C0_SCL	-	PJTAG_TCK	SPI0_SCLK	-	UART0_RX	-	-
	NA	PS_MIO27_501	GPIO27	GEM0_TXD0	-	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TDI	SPI0_SS2	-	UART0_TX	-	-
	NA	PS_MIO28_501	GPIO28	GEM0_TXD1	-	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TDO	SPI0_SS1	-	-	UART1_TX	-
	NA	PS_MIO29_501	GPIO29	GEM0_TXD2	-	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TMS	SPI0_SS0	-	-	UART1_RX	-
	NA	PS_MIO30_501	GPIO30	GEM0_TXD3	-	-	CAN0_RX	-	I2C0_SCL	-	-	SPI0_MISO	-	UART0_RX	-	-
	NA	PS_MIO31_501	GPIO31	GEM0_TX_CTL	-	-	CAN0_TX	-	I2C0_SDA	-	-	SPI0_MIOSI	-	UART0_TX	-	-
	NA	PS_MIO32_501	GPIO32	GEM0_RX_CLK	-	-	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_SCLK	-	UART1_TX	-
	NA	PS_MIO33_501	GPIO33	GEM0_RXD0	-	-	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_SS2	-	UART1_RX	-
	NA	PS_MIO34_501	GPIO34	GEM0_RXD1	-	-	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_SS1	UART0_RX	-	-
	NA	PS_MIO35_501	GPIO35	GEM0_RXD2	-	-	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_SS0	UART0_TX	-	-
	NA	PS_MIO36_501	GPIO36	GEM0_RXD3	-	-	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_MISO	-	UART1_TX	-
	NA	PS_MIO37_501	GPIO37	GEM0_RX_CTL	-	-	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_MIOSI	-	UART1_RX	-
	NA	PS_MIO76_502	GPIO76	GEM0_MDC	-	SD1_CLK	-	CAN1_TX	-	I2C1_SCL	-	-	-	-	-	-
	NA	PS_MIO77_502	GPIO77	GEM0_MDIO	-	SD1_CD	-	CAN1_RX	-	I2C1_SDA	-	-	-	-	-	-
	NA	PS_MIO12_500	GPIO12	-	-	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TCK	SPI0_SCLK	-	-	UART1_TX	-
	NA	PS_MIO42_501	GPIO42	GEM1_TXD3	eMMC _DATA1	-	CAN0_RX	-	I2C0_SCL	-	-	SPI0_MISO	-	UART0_RX	-	-
USB2.0	NA	PS_MIO52_502	GPIO52	GEM2_TX_CLK	-	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TCK	SPI0_SCLK	-	-	UART1_TX	USB0_CLK
	NA	PS_MIO53_502	GPIO53	GEM2_TXD0	-	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TDI	SPI0_SS2	-	-	UART1_RX	USB0_DIR
	NA	PS_MIO54_502	GPIO54	GEM2_TXD1	-	-	CAN0_RX	-	I2C0_SCL	-	PJTAG_TDO	SPI0_SS1	-	UART0_RX	-	USB0_DATA2
	NA	PS_MIO55_502	GPIO55	GEM2_TXD2	-	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TMS	SPI0_SS0	-	UART0_TX	-	USB0_NXT
	NA	PS_MIO56_502	GPIO56	GEM2_TXD3	-	-	-	CAN1_TX	-	I2C1_SCL	-	SPI0_MISO	-		UART1_TX	USB0_DATA0
	NA	PS_MIO57_502	GPIO57	GEM2_TX_CTL	-	-	-	CAN1_RX	-	I2C1_SDA	-	SPI0_MIOSI	-		UART1_RX	USB0_DATA1
	NA	PS_MIO58_502	GPIO58	GEM2_RX_CLK	-	-	CAN0_RX	-	I2C0_SCL	-	PJTAG_TCK	-	SPI1_SCLK	UART0_RX	-	USB0_STP
	NA	PS_MIO59_502	GPIO59	GEM2_RXD0	-	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TDI	-	SPI1_SS2	UART0_TX	-	USB0_DATA3
	NA	PS_MIO60_502	GPIO60	GEM2_RXD1	-	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TDO	-	SPI1_SS1	-	UART1_TX	USB0_DATA4
	NA	PS_MIO61_502	GPIO61	GEM2_RXD2	-	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TMS	-	SPI1_SS0	-	UART1_RX	USB0_DATA5
	NA	PS_MIO62_502	GPIO62	GEM2_RXD3	-	-	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_MISO	UART0_RX	-	USB0_DATA6
	NA	PS_MIO63_502	GPIO63	GEM2_RX_CTL	-	-	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_MIOSI	UART0_TX	-	USB0_DATA7

Interface/ Function	B2B Connector Pin Number	Zynq Ultrascale+ MPSoC Pin Name	GPIO	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13
On SBC Features from MPSoC PS																
Interface/ Function	B2B Connector Pin Number	Zynq Ultrascale+ MPSoC Pin Name	GPIO	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13
Board to Board Connector1 Interfaces from MPSoC PS																
GEM3	NA	PS_MIO64_502	GPIO64	GEM3_TX_CLK	eMMC _CLK	-	-	CAN1_TX	-	I2C1_SCL	-	SPI0_SCLK	-	-	UART1_TX	USB1_CLK
	NA	PS_MIO65_502	GPIO65	GEM3_TXD0	-	-	-	CAN1_RX	-	I2C1_SDA	-	SPI0_SS2	-	-	UART1_RX	USB1_DIR
	NA	PS_MIO66_502	GPIO66	GEM3_TXD1	eMMC _CMD	-	CAN0_RX	-	I2C0_SCL	-	-	SPI0_SS1	-	UART0_RX	-	USB1_DATA2
	NA	PS_MIO67_502	GPIO67	GEM3_TXD2	eMMC_DATA0	-	CAN0_TX	-	I2C0_SDA	-	-	SPI0_SS0	-	UART0_TX	-	USB1_NXT
	NA	PS_MIO68_502	GPIO68	GEM3_TXD3	eMMC _DATA1	-	-	CAN1_TX	-	I2C1_SCL	-	SPI0_MISO	-	-	UART1_TX	USB1_DATA0
	NA	PS_MIO69_502	GPIO69	GEM3_TX_CTL	eMMC_DATA2	SD1_WP	-	CAN1_RX	-	I2C1_SDA	-	SPI0_MIOSI	-	-	UART1_RX	USB1_DATA1
	NA	PS_MIO70_502	GPIO70	GEM3_RX_CLK	eMMC _DATA3	SD1_PWR	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_SCLK	UART0_RX	-	USB1_STP
	NA	PS_MIO71_502	GPIO71	GEM3_RXD0	eMMC _DATA4	SD1_DATA0	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_SS2	UART0_TX	-	USB1_DATA3
	NA	PS_MIO72_502	GPIO72	GEM3_RXD1	eMMC _DATA5	SD1_DATA1	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_SS1	-	UART1_TX	USB1_DATA4
	NA	PS_MIO73_502	GPIO73	GEM3_RXD2	eMMC _DATA6	SD1_DATA2	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_SS0	-	UART1_RX	USB1_DATA5
	NA	PS_MIO74_502	GPIO74	GEM3_RXD3	eMMC _DATA7	SD1_DATA3	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_MISO	UART0_RX	-	USB1_DATA6
	NA	PS_MIO75_502	GPIO75	GEM3_RX_CTL	eMMC_Reset	SD1_CMD	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_MIOSI	UART0_TX	-	USB1_DATA7
SD1(4-Bit)	NA	PS_MIO44_501	GPIO44	GEM1_RX_CLK	eMMC _DATA3	SD1_WP	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_SCLK	-	UART1_TX	-
	NA	PS_MIO45_501	GPIO45	GEM1_RXD0	eMMC _DATA4	SD1_CD	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_SS2	-	UART1_RX	-
	NA	PS_MIO43_501	GPIO43	GEM1_TX_CTL	eMMC_DATA2	SD1_PWR	CAN0_TX	-	I2C0_SDA	-	-	SPI0_MIOSI	-	UART0_TX	-	-
	NA	PS_MIO46_501	GPIO46	GEM1_RXD1	eMMC _DATA5	SD1_DATA0	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_SS1	UART0_RX	-	-
	NA	PS_MIO47_501	GPIO47	GEM1_RXD2	eMMC _DATA6	SD1_DATA1	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_SS0	UART0_TX	-	-
	NA	PS_MIO48_501	GPIO48	GEM1_RXD3	eMMC _DATA7	SD1_DATA2	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_MISO	-	UART1_TX	-
	NA	PS_MIO49_501	GPIO49	GEM1_RX_CTL	eMMC_Reset	SD1_DATA3	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_MIOSI	-	UART1_RX	-
	NA	PS_MIO50_501	GPIO50	GEM1_MDC	-	SD1_CMD	CAN0_RX	-	I2C0_SCL	-	-	-	-	UART0_RX	-	-
	NA	PS_MIO51_501	GPIO51	GEM1_MDIO	-	SD1_CLK	CAN0_TX	-	I2C0_SDA	-	-	-	-	UART0_TX	-	-
Debug UART (UART0)	NA	PS_MIO07_500	GPIO7				CAN0_TX		I2C0_SDA				SPI1_SS2		UART0_TX	
	NA	PS_MIO06_500	GPIO6				CAN0_RX		I2C0_SCL				SPI1_SCLK		UART0_RX	
UART1	NA	PS_MIO08_500	GPIO8	-	-	-	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_SS1	-	UART1_TX	-
	NA	PS_MIO09_500	GPIO9	-	-	-	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_SS0	-	UART1_RX	-
I2C0	NA	PS_MIO11_500	GPIO11	-	-	-	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_MIOSI	UART0_TX	-	-
	NA	PS_MIO10_500	GPIO10	NFC_RB_N	-	-	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_MISO	UART0_RX	-	-
I2C1	NA	PS_MIO25_500	GPIO25	NFC_RE_N	-	-	-	CAN1_RX	-	I2C1_SDA	-	-	-	-	UART1_RX	-
	NA	PS_MIO24_500	GPIO24	NFC_DATA7	-	-	-	CAN1_TX	-	I2C1_SCL	-	-	-	-	UART1_TX	-
GPIO	NA	PS_MIO1_500	GPIO1	QSPI_MISO	-	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TDI	SPI0_SS2	-	-	UART1_RX	-
JTAG		PS_JTAG_TDI	-	PS_JTAG_TDI	-	-	-	-	-	-	-	-	-	-	-	-
		PS_JTAG_TMS	-	PS_JTAG_TMS	-	-	-	-	-	-	-	-	-	-	-	-
		PS_JTAG_TCK	-	PS_JTAG_TCK	-	-	-	-	-	-	-	-	-	-	-	-
		PS_JTAG_TDO	-	PS_JTAG_TDO	-	-	-	-	-	-	-	-	-	-	-	-
Board to Board Connector1 Interfaces from MPSoC PS																
SPI0		PS_MIO0_500	GPIO0	QSPI_SCLK	-	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TCK	SPI0_SCLK	-	-	UART1_TX	-
		PS_MIO3_500	GPIO3	QSPI_SS0	-	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TMS	SPI0_SS0	-	UAR`T0_TX	-	-
		PS_MIO4_500	GPIO4	-	-	-	-	CAN1_TX	-	I2C1_SCL	-	SPI0_MISO	-	-	UART1_TX	-
		PS_MIO5_500	GPIO5	-	-	-	-	CAN1_RX	-	I2C1_SDA	-	SPI0_MOSI	-	-	UART1_RX	-
CAN0		PS_MIO38_501	GPIO38	GEM1_TX_CLK	eMMC _CLK	-	CAN0_RX	-	I2C0_SCL	-	PJTAG_TCK	SPI0_SCLK	-	UART0_RX	-	-
		PS_MIO39_501	GPIO39	GEM1_TXD0	-	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TDI	SPI0_SS2	-	UART0_TX	-	-
CAN1		PS_MIO40_501	GPIO40	GEM1_TXD1	eMMC _CMD	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TDO	SPI0_SS1	-	-	UART1_TX	-
		PS_MIO41_501	GPIO41	GEM1_TXD2	eMMC_DATA0	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TMS	SPI0_SS0	-	-	UART1_RX	-

3. TECHNICAL SPECIFICATION

This section provides detailed information about the Zynq Ultrascale+ MPSoC SBC technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Power Input Requirement

The Zynq Ultrasclae+ MPSoC SBC is designed to work with 12V external power and uses on board voltage regulators for internal power management. 12V power input from an external power supply is connected to the Zynq Ultrascale+ MPSoC SBC through Power Jack (J18). This connector is physically placed at the top of the board as shown below.

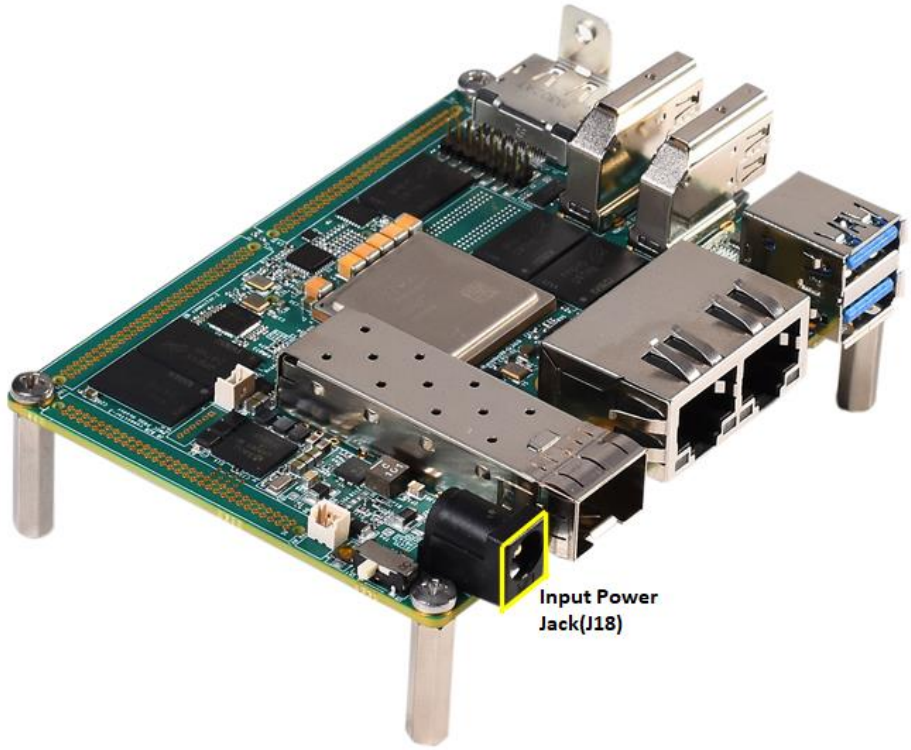

Figure 22: Input Power Jack

The below table provides the Power Input Requirement of Zynq Ultrascale+ MPSoC SBC .

Table 15: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_12V	11.75V	12V	12.25V	±50mV.

3.2 Power Output Specification

The Zynq Ultrasclae+ MPSoC SBC shares different on-board power to Board to Board Connector 1, 2, and 3 for its Add-On Module power.

Table 16: Power Output Specification

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Output Current
To Board to Board Connector1					
1	VCC_5V	4.85V	5V	5.15V	500mA.
2	VCC_1V8	1.75	1.8	1.85	500mA.
To Board to Board Connector2					
1	VCC_12V	11.75V	12V	12.25V	500mA.
2	VCC_5V	4.85V	5V	5.15V	500mA.
To Board to Board Connector3					
1	VCC_12V	11.75V	12V	12.25V	500mA.
2	VCC_5V	4.85V	5V	5.15V	500mA.

3.2.1 Power Consumption

Table 17: Power Consumption[1]

Task/Status	Power Rail	Current Drawn/Power Consumption
TBD	TBD	TBD

3.3 Environmental Characteristics

3.3.1 Temperature Specification

The below table provides the Environment specification of Zynq Ultrascale+ MPSoC SBC.

Table 18: Temperature Specification

Parameters	Min	Max
Operating temperature range - Industrial[1]	-40°C	85°C
Operating temperature range - Extended[1]	0°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

3.3.2 RoHS2 Compliance

iWave's Zynq Ultrascale+ MPSoC SBC is designed by using RoHS2 compliant components and manufactured on lead free production process.

3.3.3 Electrostatic Discharge

iWave's Zynq Ultrascale+ MPSoC SBC is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SBC except at an electrostatic free workstation.

3.3.4 Heat Sink

For any highly integrated SBC, thermal design is very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management technique Heat sink must be used. Always remember that, if you use more effective thermal solution, you will get more performance out of the CPU.

3.4 MechanicalCharacteristics

3.4.1 Zynq Ultrascale+ MPSoC SBC Mechanical Dimensions

Zynq Ultrascale+ MPSoC SBC PCB size is 72mm x 100 mm x 1.6mm. SBC mechanical dimension is shown below. Measured dimensions are all in MM.

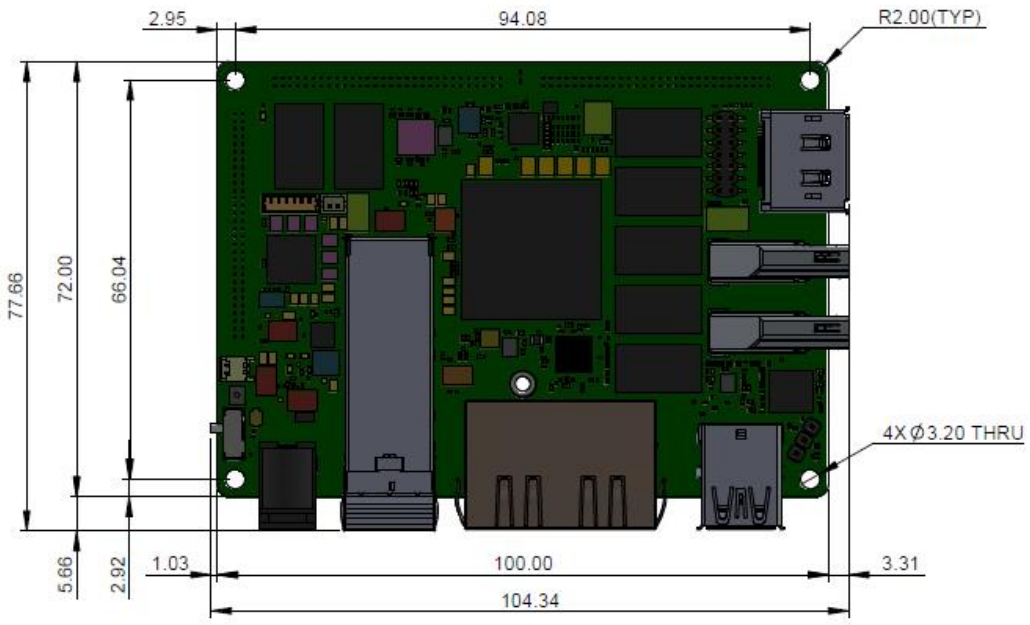

Figure 23: Mechanical dimension of Zynq Ultrascale+ MPSoC SBC - Top View

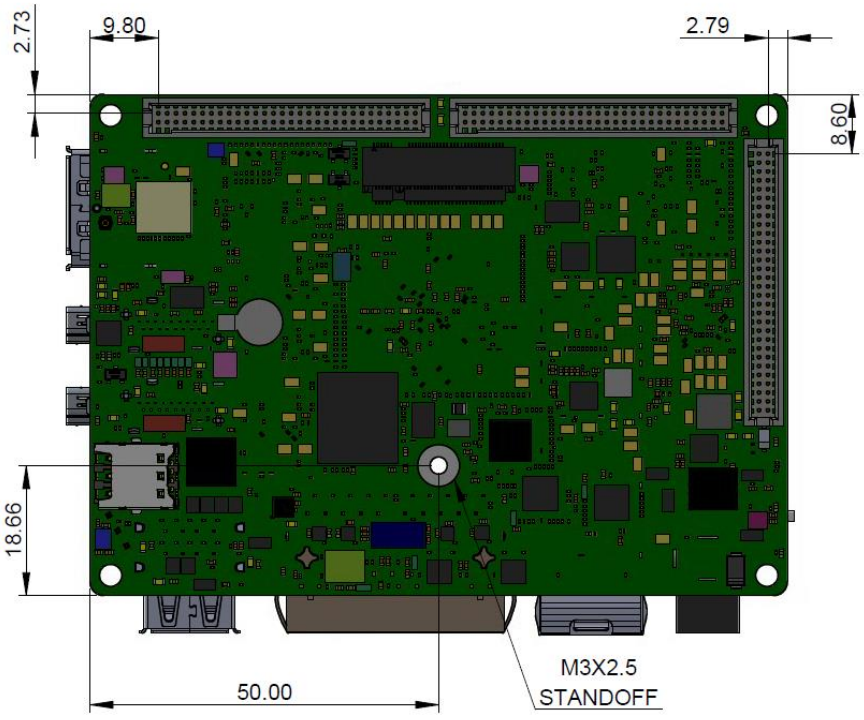

Figure 24: Mechanical dimension of Zynq Ultrascale+ MPSoC SBC - Bottom View

Zynq Ultrascale+ MPSoC SBC PCB thickness is 1.60±0.1mm, top side maximum height component is HDMI IN & Out Connectors J11 & J9 (16.40mm) followed by USB Type-A connector J17 (16.20mm) and bottom side maximum height component is Board to Board connectors J21, J22, J26 (7.37mm) followed by Inductor L12 (4.05mm). Please refer the below figure which gives height details of the Zynq Ultrascale+ MPSoC SBC.

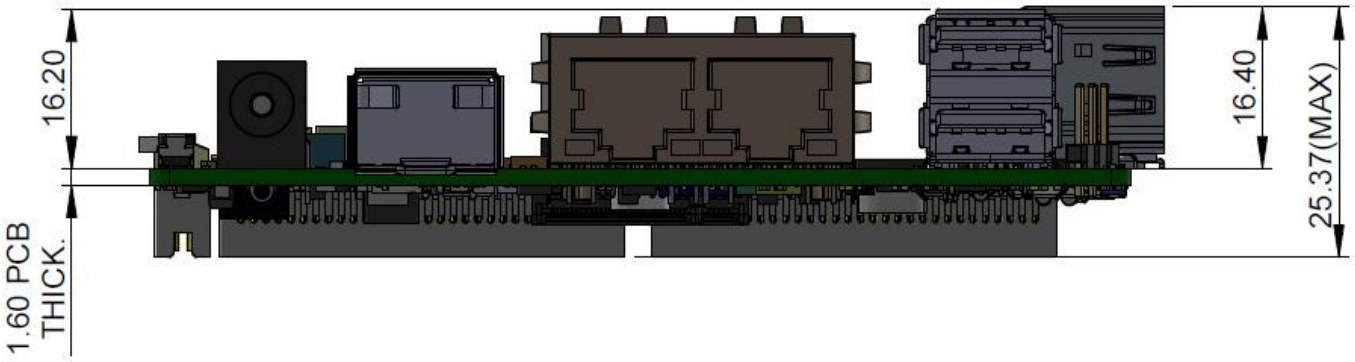

Figure 25: Mechanical dimension of Zynq Ultrascale+ MPSoC SBC - Side View

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different Zynq Ultrascale+ MPSoC SBC variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SBC configurations. Also if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 19: Orderable Product Part Numbers

Product Part Number	Description	Temperature
ZU5EV MPSoC based SBC		
iW-G36S-5EV1-4E002G-E008G-BEE	ZU5EV (-1) MPSOC(XCZU5EV-1SFVC784E), 2GB PS DDR4, 1GB PL DDR4, 8GB EMMC, HDMI In/Out, SFP+ and Wi-Fi – Boot code	Extended
iW-G36S-5EV1-4E002G-E008G-BEF	ZU5EV (-1) MPSOC(XCZU5EV-1SFVC784E), 2GB PS DDR4, 1GB PL DDR4, 8GB EMMC, HDMI In/Out, SDI and Wi-Fi – Boot code	Extended
iW-G36S-5EV1-4E002G-E008G-BEG	ZU5EV (-1) MPSOC(XCZU5EV-1SFVC784E), 2GB PS DDR4, 1GB PL DDR4, 8GB EMMC, HDMI In/Out, SFP+ – Boot code	Extended
iW-G36S-5EV1-4E002G-E008G-BEH	ZU5EV (-1) MPSOC(XCZU5EV-1SFVC784E), 2GB PS DDR4, 1GB PL DDR4, 8GB EMMC, HDMI In/Out, SDI – Boot code	Extended
iW-G36S-5EV1-4E002G-E008G-BIE	ZU5EV (-1) MPSOC(XCZU5EV-1SFVC784I), 2GB PS DDR4, 1GB PL DDR4, 8GB EMMC, HDMI In/Out, SFP+ and Wi-Fi – Boot code	Industrial
iW-G36S-5EV1-4E002G-E008G-BIF	ZU5EV (-1) MPSOC(XCZU5EV-1SFVC784I), 2GB PS DDR4, 1GB PL DDR4, 8GB EMMC, HDMI In/Out, SDI and Wi-Fi – Boot code	Industrial
iW-G36S-5EV1-4E002G-E008G-BIG	ZU5EV (-1) MPSOC(XCZU5EV-1SFVC784I), 2GB PS DDR4, 1GB PL DDR4, 8GB EMMC, HDMI In/Out, SFP+ – Boot code	Industrial
iW-G36S-5EV1-4E002G-E008G-BIH	ZU5EV (-1) MPSOC(XCZU5EV-1SFVC784I), 2GB PS DDR4, 1GB PL DDR4, 8GB EMMC, HDMI In/Out, SDI – Boot code	Industrial
ZU4EV MPSoC based SBC		
iW-G36S-4EV1-4E002G-E008G-BEE	ZU4EV (-1) MPSOC(XCZU4EV-1SFVC784E), 2GB PS DDR4, 1GB PL DDR4, 8GB EMMC, HDMI In/Out, SFP+ and Wi-Fi – Boot code	Extended

Product Part Number	Description	Temperature
iW-G36S-4EV1-4E002G-E008G-BEF	ZU4EV (-1) MPSOC(XCZU4EV-1SFVC784E), 2GB PS DDR4, 1GB PL DDR4, 8GB EMMC, HDMI In/Out, SDI and Wi-Fi – Boot code	Extended
iW-G36S-4EV1-4E002G-E008G-BEG	ZU4EV (-1) MPSOC(XCZU4EV-1SFVC784E), 2GB PS DDR4, 1GB PL DDR4, 8GB EMMC, HDMI In/Out, SFP+ – Boot code	Extended
iW-G36S-4EV1-4E002G-E008G-BEH	ZU4EV (-1) MPSOC(XCZU4EV-1SFVC784E), 2GB PS DDR4, 1GB PL DDR4, 8GB EMMC, HDMI In/Out, SDI – Boot code	Extended
iW-G36S-4EV1-4E002G-E008G-BIE	ZU4EV (-1) MPSOC(XCZU4EV-1SFVC784I), 2GB PS DDR4, 1GB PL DDR4, 8GB EMMC, HDMI In/Out, SFP+ and Wi-Fi – Boot code	Industrial
iW-G36S-4EV1-4E002G-E008G-BIF	ZU4EV (-1) MPSOC(XCZU4EV-1SFVC784I), 2GB PS DDR4, 1GB PL DDR4, 8GB EMMC, HDMI In/Out, SDI and Wi-Fi – Boot code	Industrial
iW-G36S-4EV1-4E002G-E008G-BIG	ZU4EV (-1) MPSOC(XCZU4EV-1SFVC784I), 2GB PS DDR4, 1GB PL DDR4, 8GB EMMC, HDMI In/Out, SFP+ – Boot code	Industrial
iW-G36S-4EV1-4E002G-E008G-BIH	ZU4EV (-1) MPSOC(XCZU4EV-1SFVC784I), 2GB PS DDR4, 1GB PL DDR4, 8GB EMMC, HDMI In/Out, SDI – Boot code	Industrial
ZU3EG MPSoC based SBC		
iW-G36S-3EG1-4E002G-E008G-BEE	ZU3EG (-1) MPSOC(XCZU3EG-1SFVC784E), 2GB PS DDR4, 8GB EMMC and Wi-Fi – Boot code	Extended
iW-G36S-3EG1-4E002G-E008G-BEF	ZU3EG (-1) MPSOC(XCZU3EG-1SFVC784E), 2GB PS DDR4, 8GB EMMC – Boot code	Extended
iW-G36S-3EG1-4E002G-E008G-BIE	ZU3EG (-1) MPSOC(XCZU3EG-1SFVC784I), 2GB PS DDR4, 8GB EMMC and Wi-Fi – Boot code	Industrial
iW-G36S-3EG1-4E002G-E008G-BIF	ZU3EG (-1) MPSOC(XCZU3EG-1SFVC784I), 2GB PS DDR4, 8GB EMMC – Boot code	Industrial
ZU2CG MPSoC based SBC		
iW-G36S-2CG1-4E002G-E008G-BEE	ZU2CG (-1) MPSOC(XCZU2CG-1SFVC784E), 2GB PS DDR4, 8GB EMMC and Wi-Fi – Boot code	Extended
iW-G36S-2CG1-4E002G-E008G-BEF	ZU2CG (-1) MPSOC(XCZU2CG-1SFVC784E), 2GB PS DDR4, 8GB EMMC – Boot code	Extended
iW-G36S-2CG1-4E002G-E008G-BIE	ZU2CG (-1) MPSOC(XCZU2CG-1SFVC784I), 2GB PS DDR4, 8GB EMMC and Wi-Fi – Boot code	Industrial

Product Part Number	Description	Temperature
iW-G36S-2CG1-4E002G-E008G-BIF	ZU2CG (-1) MPSOC(XCZU2CG-1SFVC784I), 2GB PS DDR4, 8GB EMMC – Boot code	Industrial


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