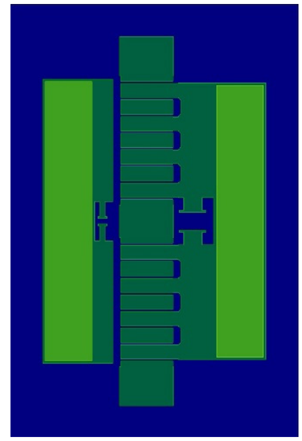
TGF2933

DC – 25 GHz, 28 V, 7 W GaN RF Transistor

Product Overview

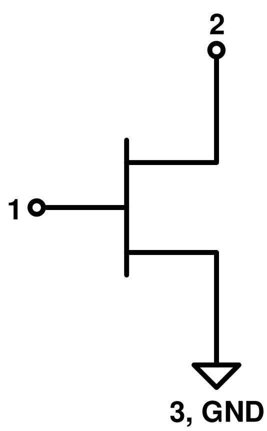
The Qorvo TGF2933 is a 7 W (P_{3dB}) discrete GaN on SiC HEMT which operates from DC to 25 GHz and 28 V supply. The device is constructed with Qorvo's proven QGaN15 process. The device can support pulsed, CW, and linear operations.

Lead-free and ROHS compliant



0.833 x 0.551 x 0.100 mm

Functional Block Diagram



Key Features

- Frequency: DC to 25 GHz
- Output Power (P_{3dB})[1]: 7.2 W
- Linear Gain[1]: 15 dB
- Typical PAE_{3dB}[1]: 57%
- Typical Noise Figure[1]: 1.3dB
- Operating Voltage: 28 V
- CW and Pulse capable
- Non-linear & Noise Models available

Note 1: @ 10 GHz

Applications

- Defense and Aerospace
- Broadband wireless
- Low noise amplifier

Ordering info

Part No.	ECCN	Description
TGF2933	EAR99	DC–25 GHz, 28 V, 7 W GaN RF Transistor

Absolute Maximum Ratings[1]

Parameter	Rating	Units
Breakdown Voltage, BV_{DG}	+60	V
Gate Voltage Range, V_G	-7 to +1.5	V
Drain Current, I_{D_MAX}	2	A
Gate Current Range, I_G	See page 20.	mA
Power Dissipation, CW, P_{DISS}	9.9	W
RF Input Power, CW, 10 GHz, T = 25 °C	+30	dBm
Channel Temperature, T_{CH}	275	°C
Mounting Temperature (30 Seconds)	320	°C
Storage Temperature	–65 to +150	°C

Notes:
1. Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions[1]

Parameter	Min	Typ	Max	Units
Operating Temp. Range	–40	+25	+85	°C
Drain Voltage Range, V_D	+12	+20	+29.5	V
Drain Bias Current, I_{DQ}	40	80	160	mA
Drain Current, I_D	–	500	–	mA
Gate Voltage, V_G[3]	–	–2.8	–	V
Channel Temperature (T_{CH})	–	–	250	°C
Power Dissipation, CW (P_D)[2]	–	–	8.9	W

Notes:
1. Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions.
2. Package base at 85 °C
3. To be adjusted to desired I_{DQ}

Model Load Pull Performance – Power Tuned[1]

Parameter	Typical Values								Units
Frequency, F	3		6		10		18		GHz
Drain Voltage, V_D	20	28	20	28	20	28	20	28	V
Drain Bias Current, I_{DQ}	80	80	80	80	80	80	80	80	mA
Output Power at 3dB compression, P_{3dB}	37.7	38.8	37.7	39.0	37.5	38.6	37.6	37.9	dBm
Power Added Efficiency at 3dB compression, PAE_{3dB}	60.4	57.1	60.3	58.0	59.2	50.5	48.6	51.2	%
Gain at 3dB compression, G_{3dB}	22.1	21.3	15.5	16.3	11.7	11.9	6.5	9.0	dB
Load Reflection Coefficient (2), Γ_L	0.36∠146°	0.22∠117°	0.50∠143°	0.50∠121°	0.72∠146°	0.64∠141°	0.85∠159°	0.89∠153°	--

Notes:
1. CW, bondwires not included
2. Characteristic Impedance, Zo = 50 Ω.

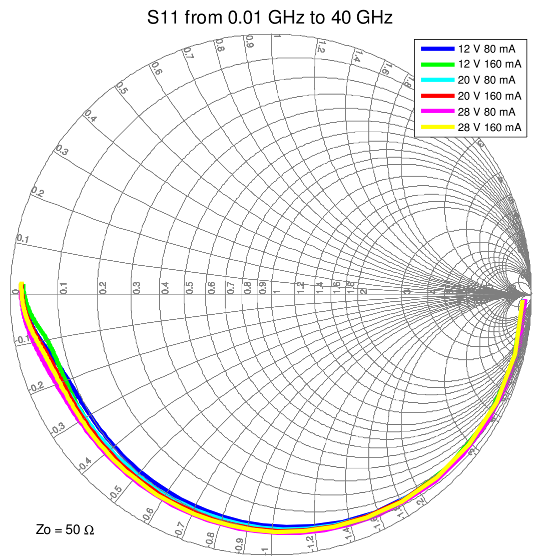
Model Load Pull Performance – Efficiency Tuned[1]

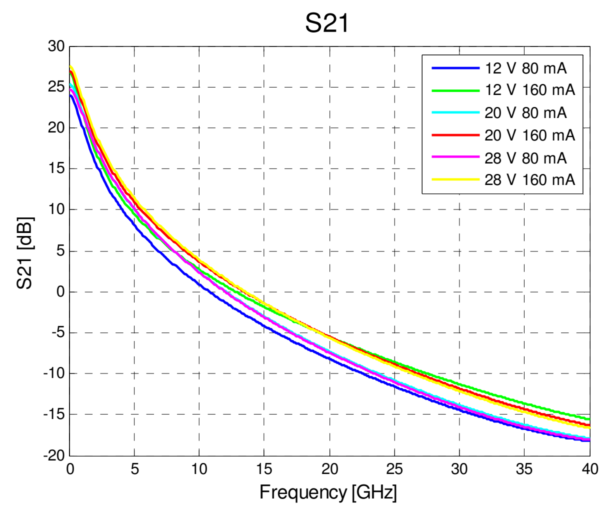
Parameter	Typical Values								Units
Frequency, F	3		6		10		18		GHz
Drain Voltage, V_D	20	28	20	28	20	28	20	28	V
Drain Bias Current, I_{DQ}	80	80	80	80	80	80	80	80	mA
Output Power at 3dB compression, P_{3dB}	37.0	38.1	36.6	38.6	36.2	38.5	37.6	37.9	dBm
Power Added Efficiency at 3dB compression, PAE_{3dB}	64.6	60.8	63.6	60.6	59.7	57.0	48.6	51.2	%
Gain at 3dB compression, G_{3dB}	23.0	22.8	16.3	16.9	12.0	12.6	6.5	9.0	dB
Load Reflection Coefficient (2), Γ_L	0.45∠117°	0.40∠90°	0.64∠129°	0.58∠121°	0.78∠140°	0.78∠140°	0.85∠159°	0.89∠153°	--

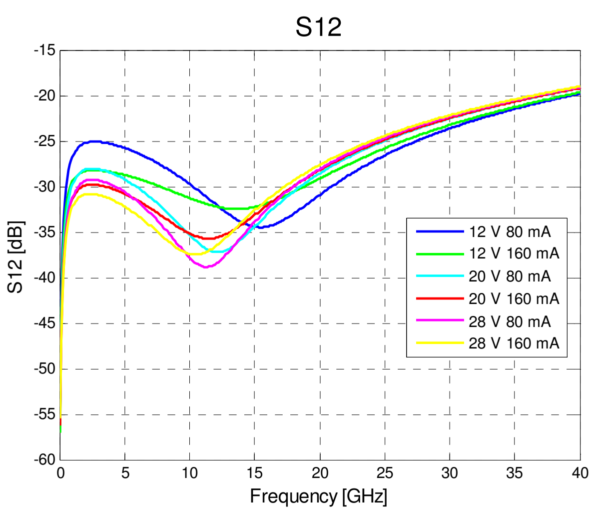
Notes:
1. CW, bondwires not included
2. Characteristic Impedance, Zo = 50 Ω.

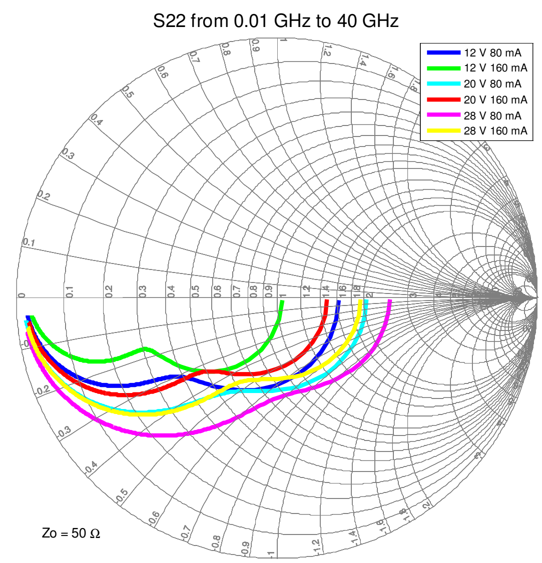
Model S-parameters[1]

Notes:
1. Bondwires are not included. T = 25 °C.



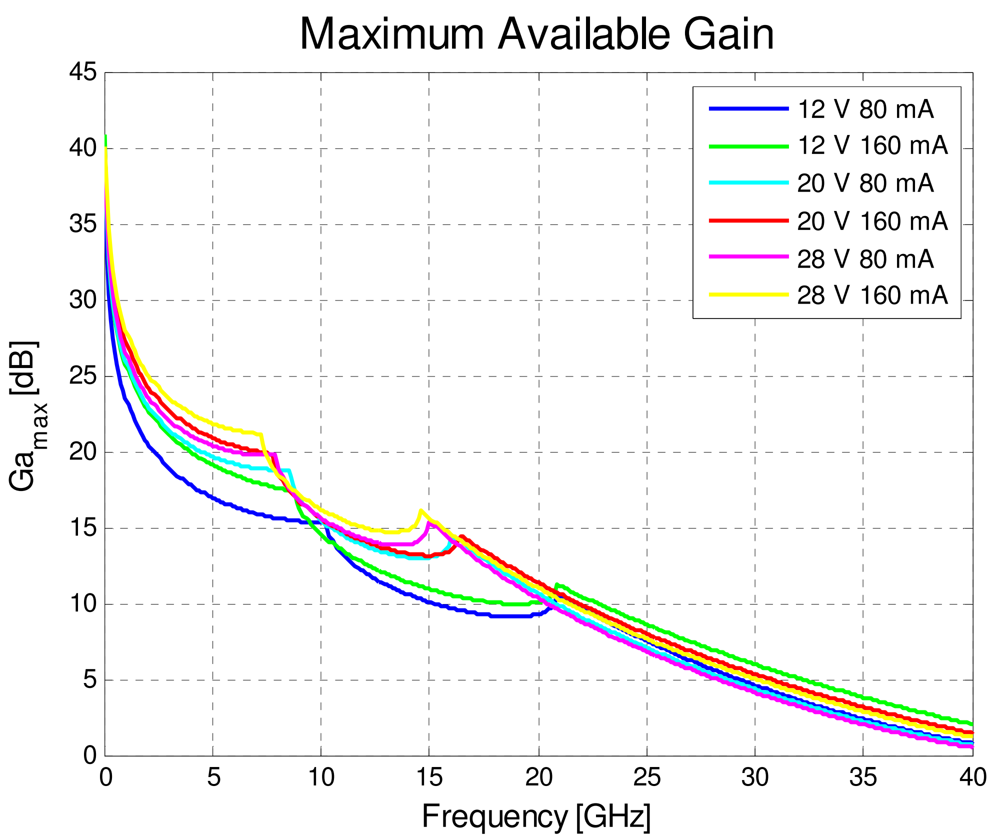






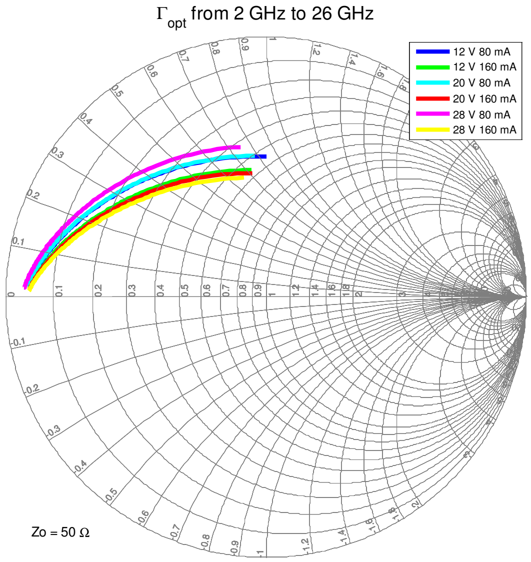
Model Maximum Available Gain[1]

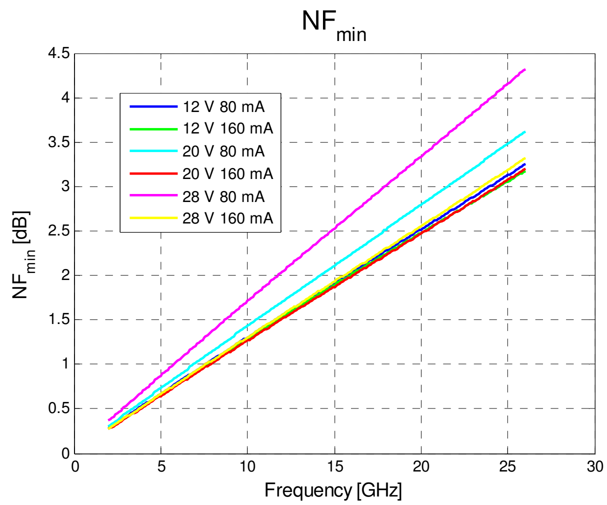
Notes:
1. Bondwires are not included. T = 25 °C.

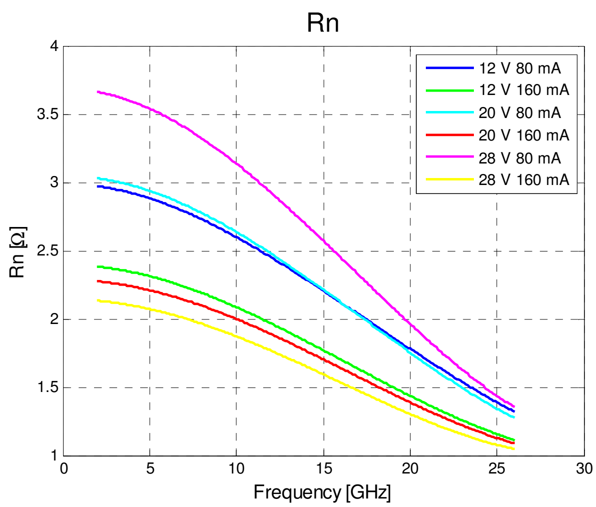


Model Noise[1]

Notes:
1. Bondwires are not included. T = 25 °C.

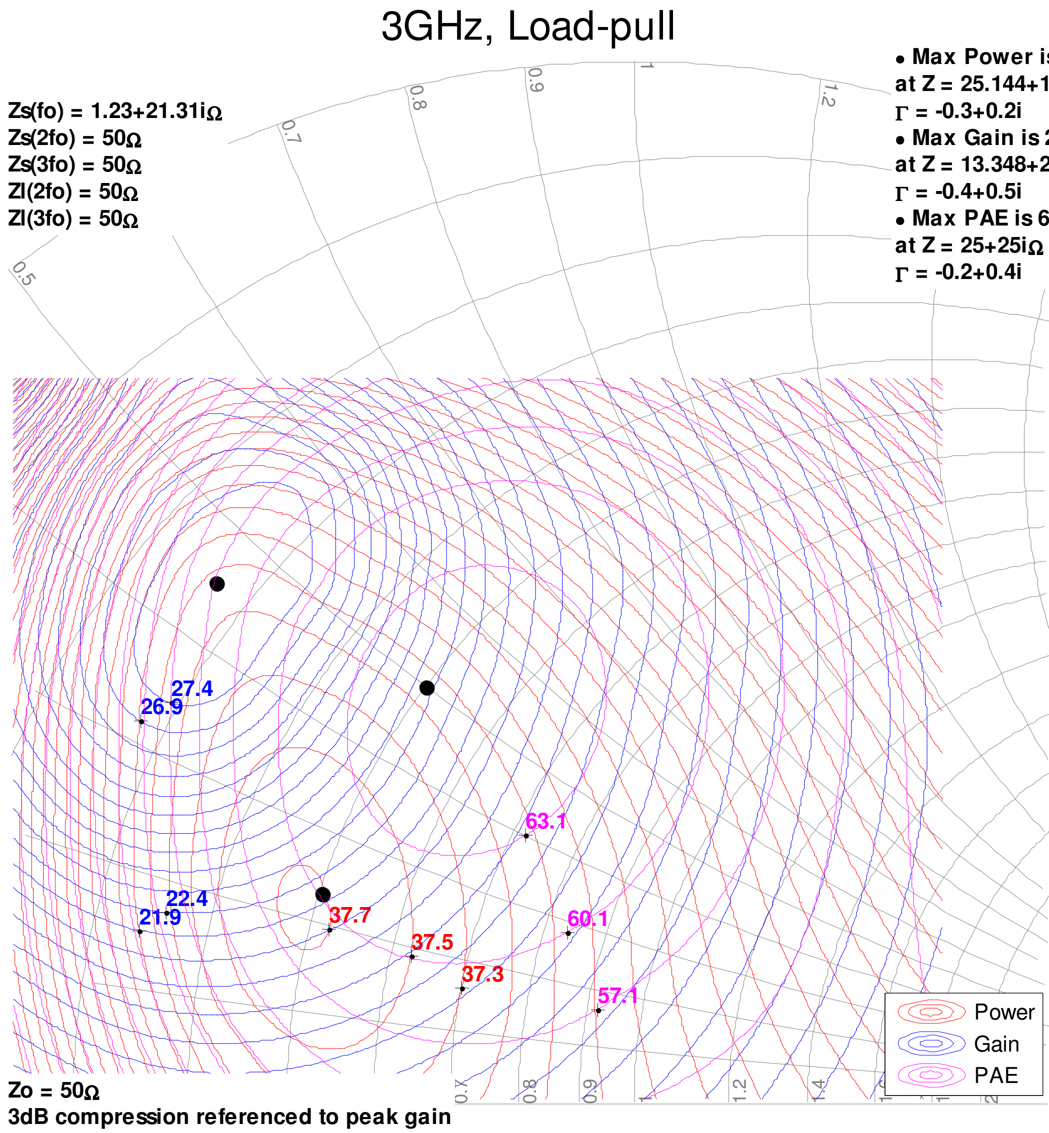






Model Load-Pull Smith Charts[1, 2]

Notes:
1. Test Conditions: V_D = 20 V, I_{DQ} = 80 mA, CW, Bondwires not included
2. See page 22 for load pull reference planes where the performance was simulated.



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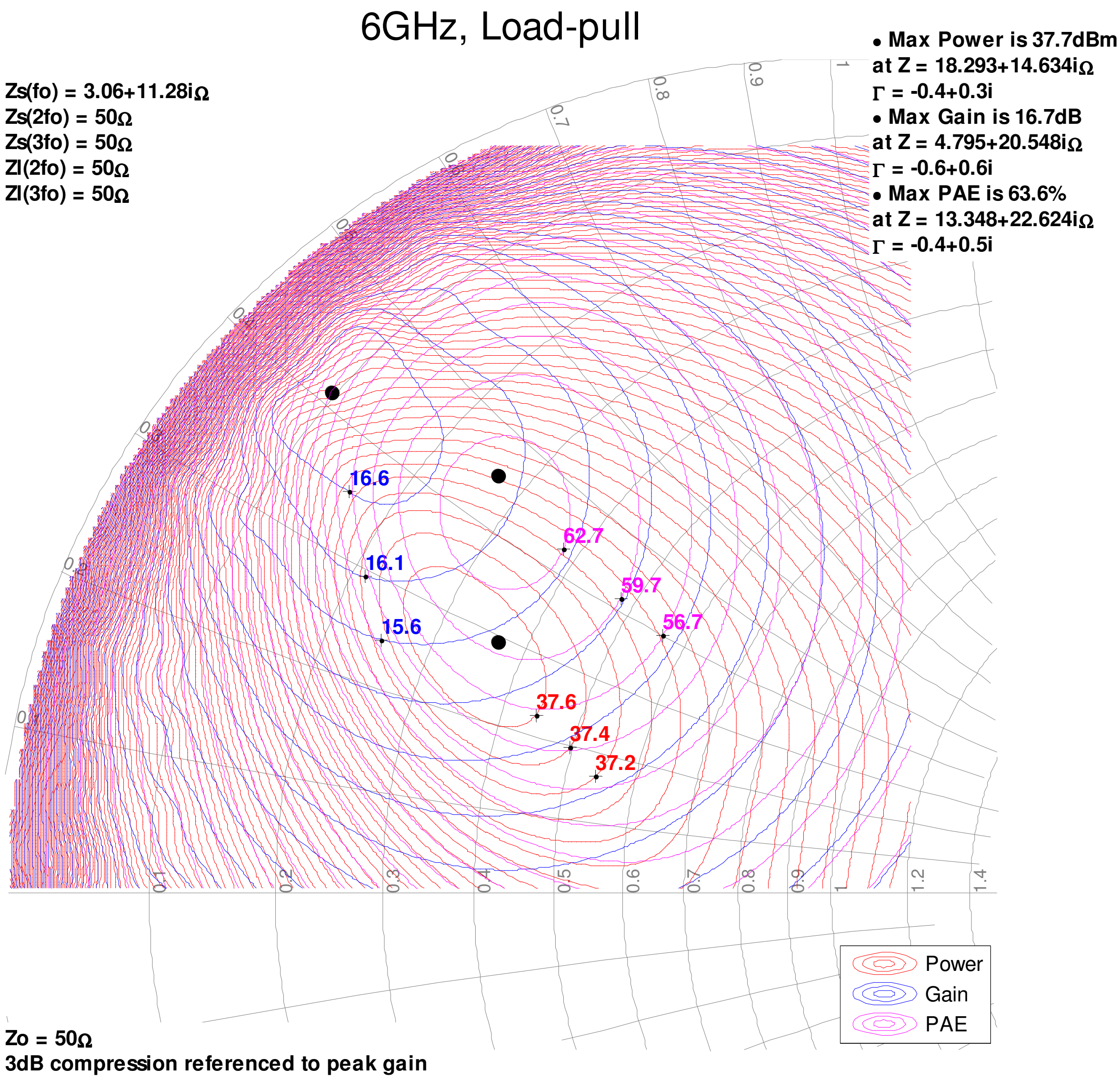

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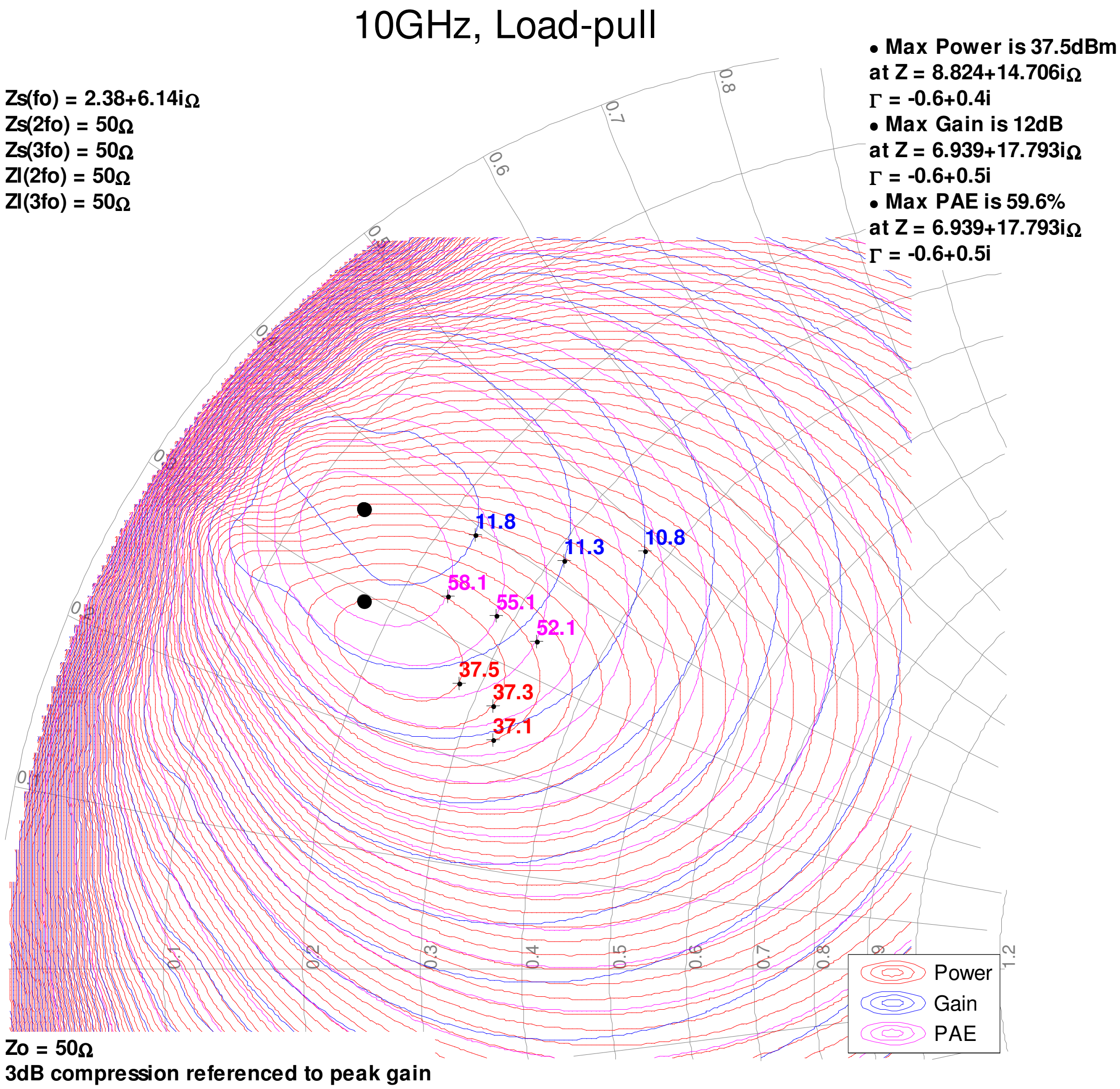

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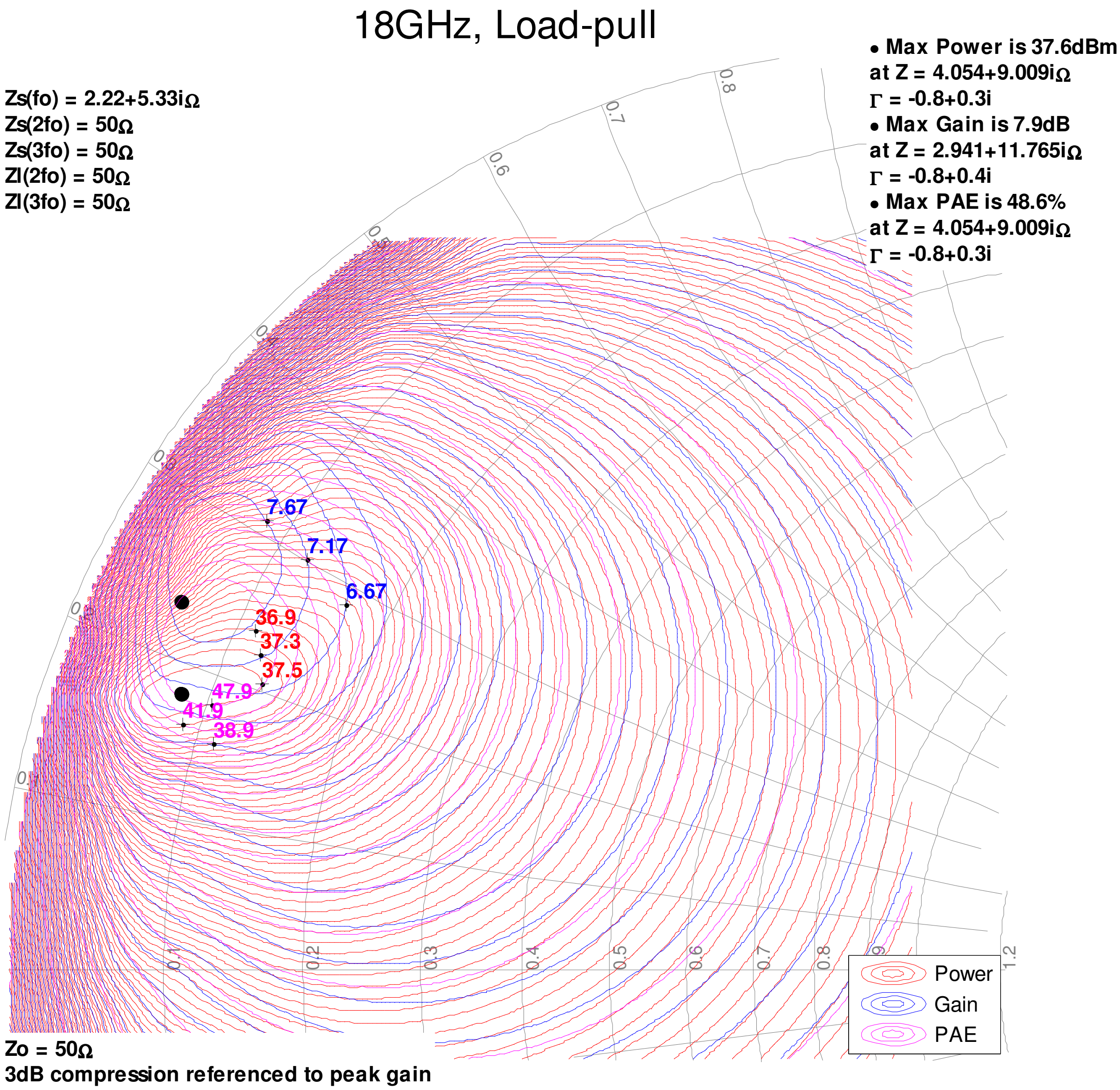
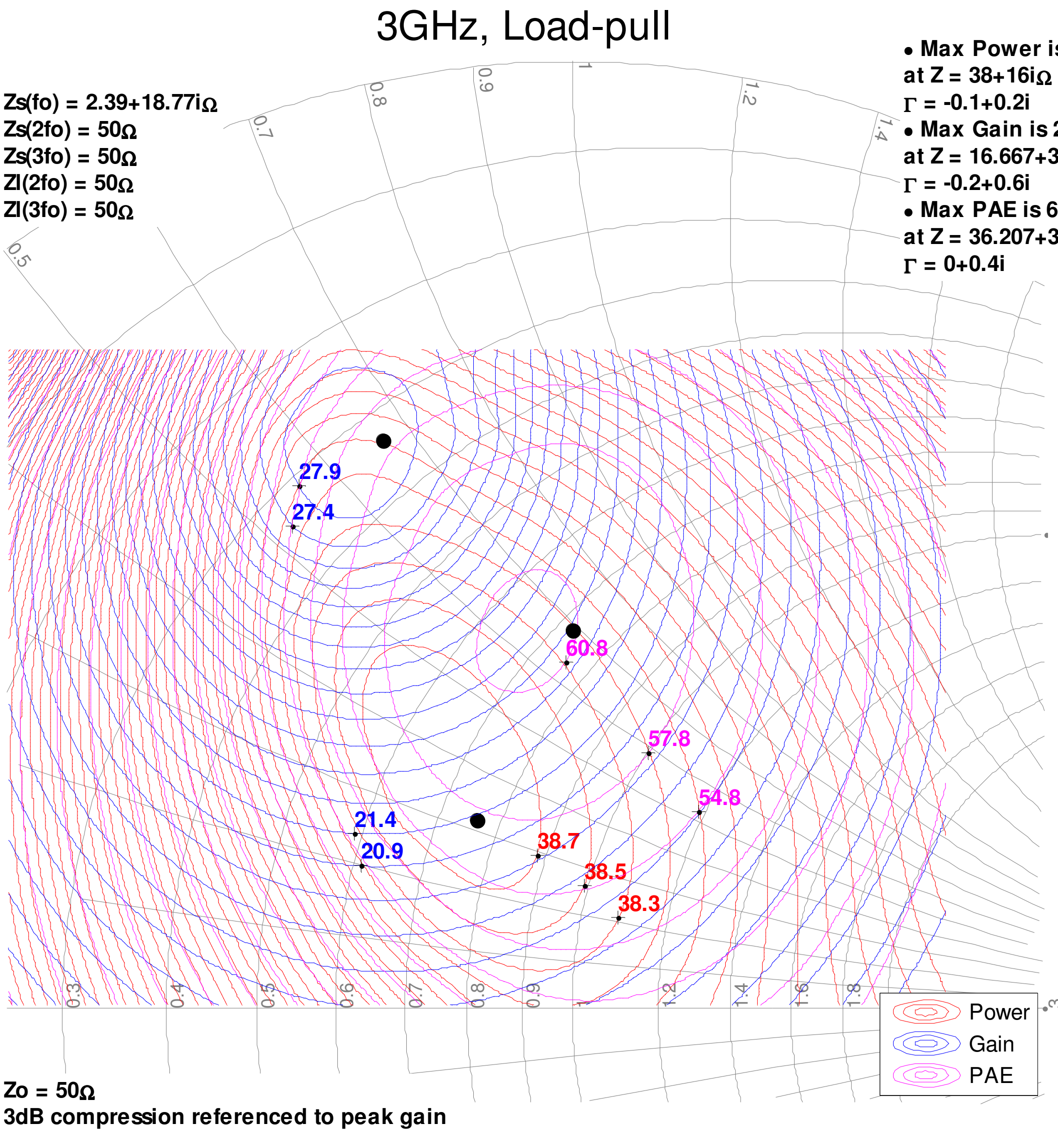


Model Load-Pull Smith Charts[1, 2]

Notes:
1. Test Conditions: V_D = 28 V, I_{DQ} = 80 mA, CW, Bondwires not included
2. See page 22 for load pull reference planes where the performance was simulated.



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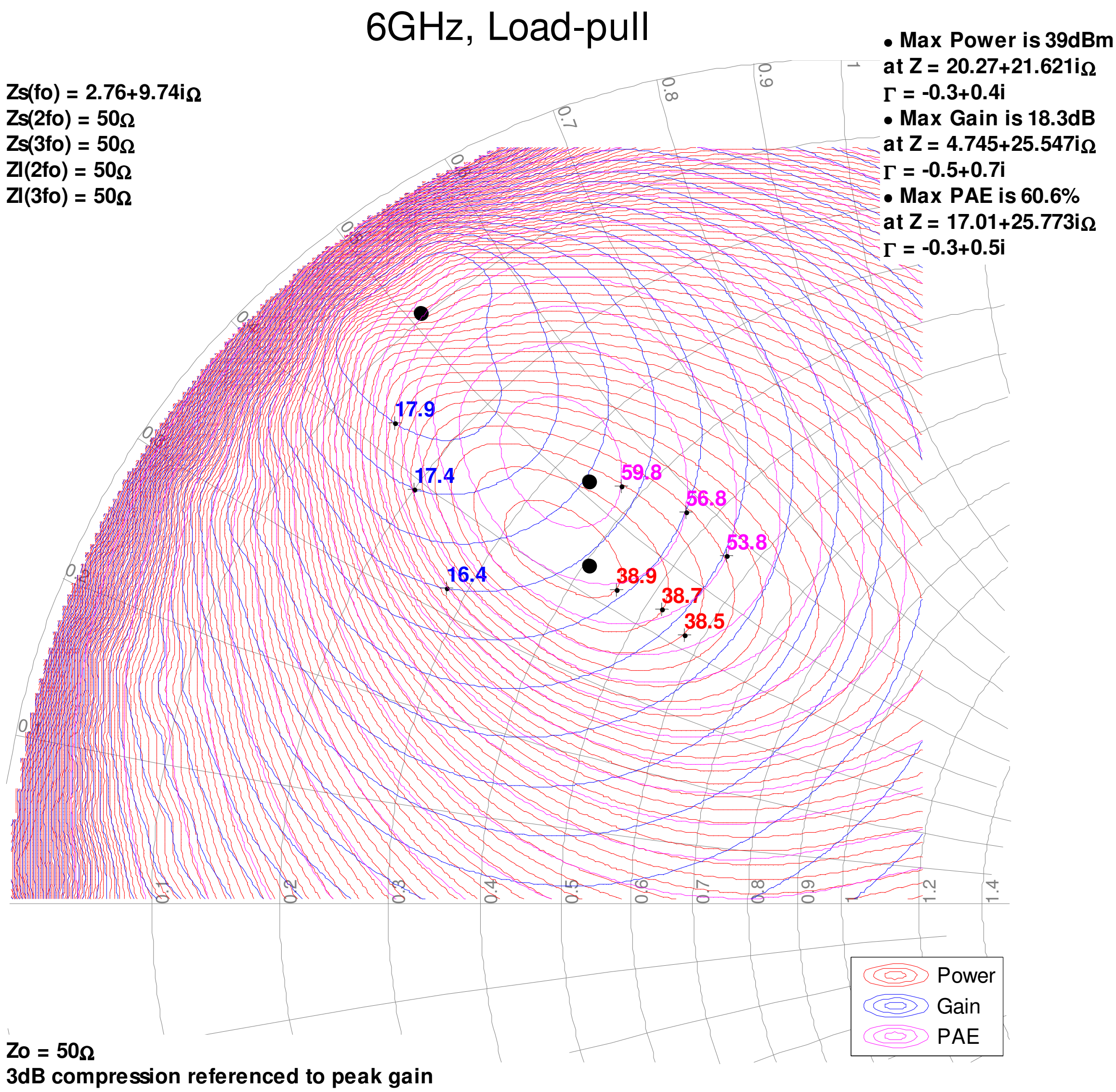

Model Load-Pull Smith Charts[1, 2]

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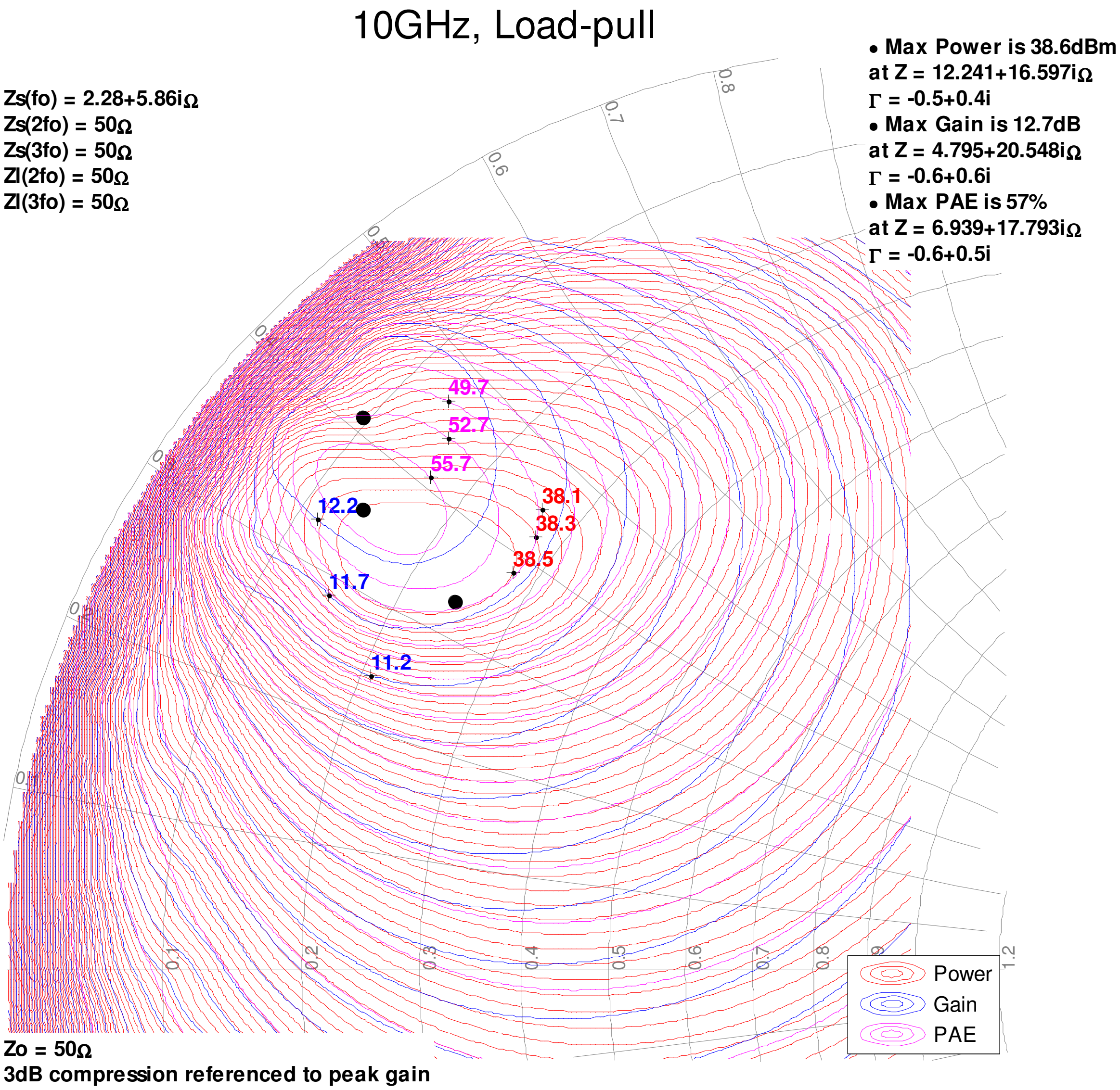

Model Load-Pull Smith Charts[1, 2]

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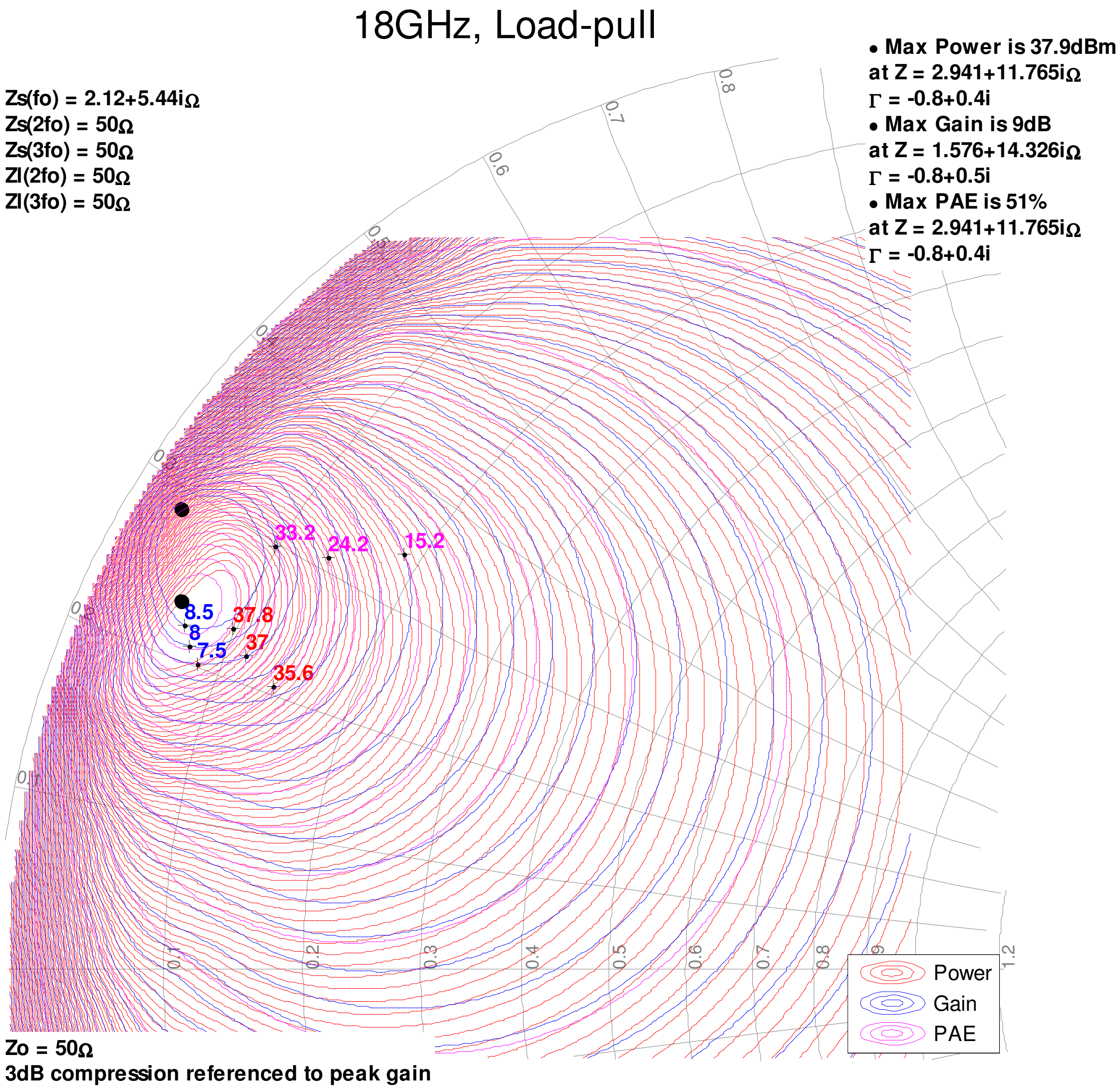
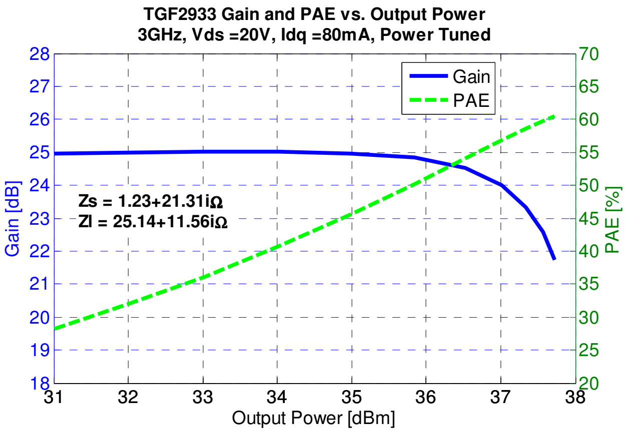
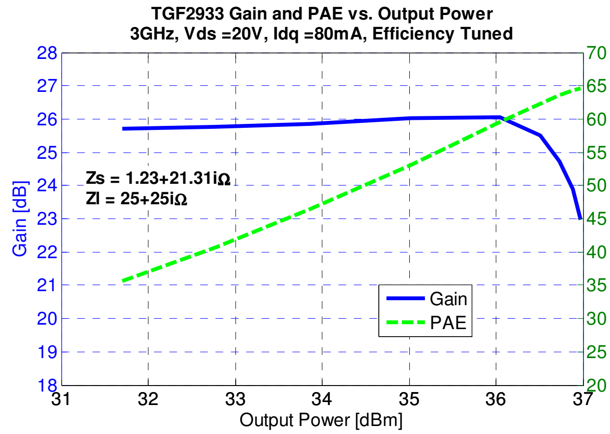
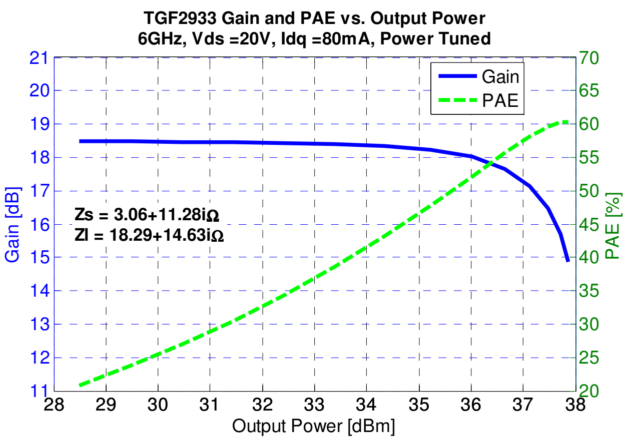


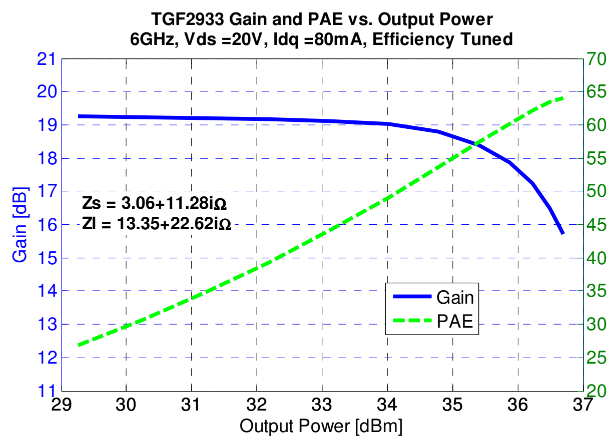
Typical Model Performance – Load-Pull Drive-up[1, 2]

Notes:
1. CW, Bondwires not included
2. See page 22 for load-pull and source-pull reference planes where the performance was measured.



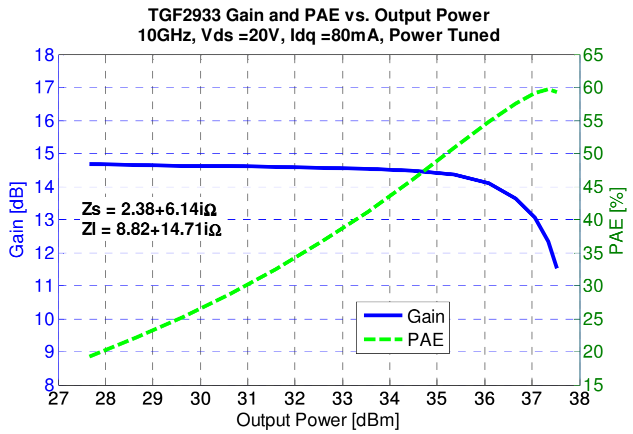


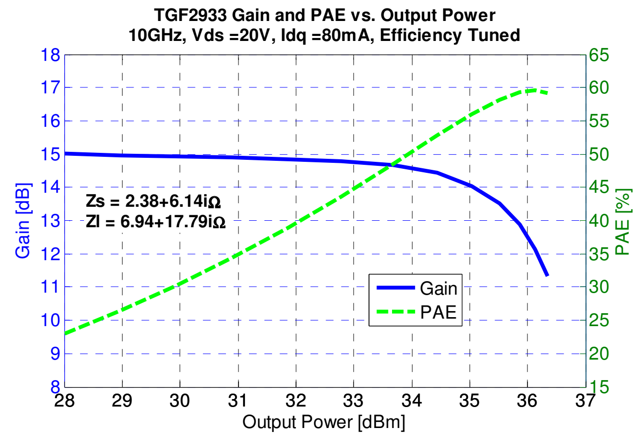


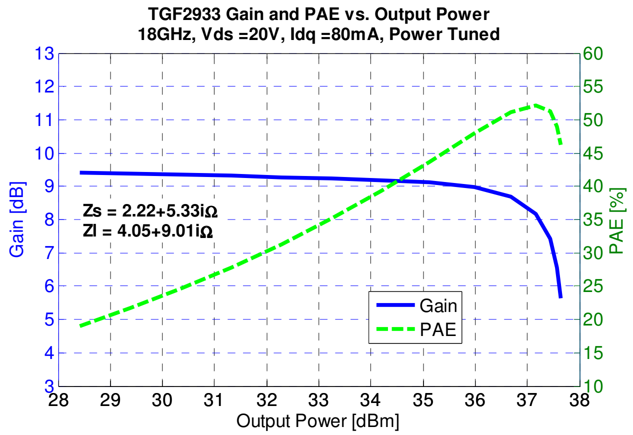


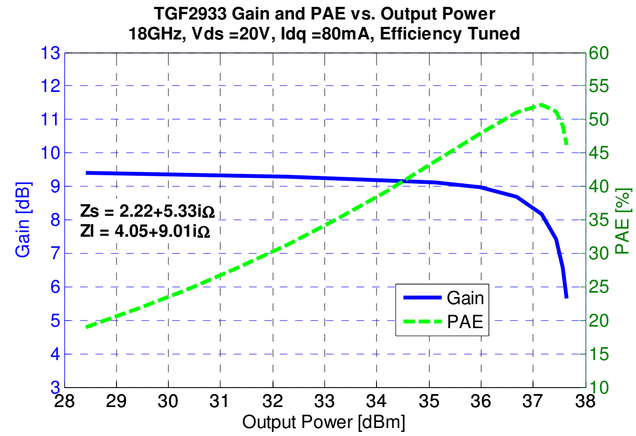
Typical Model Performance – Load-Pull Drive-up[1, 2]

Notes:
1. CW, Bondwires not included
2. See page 22 for load-pull and source-pull reference planes where the performance was measured.



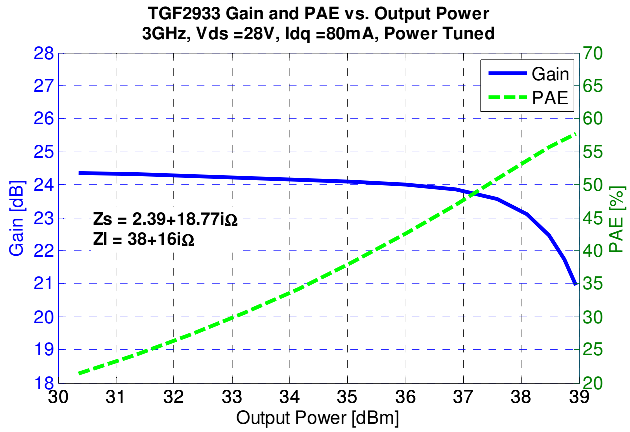


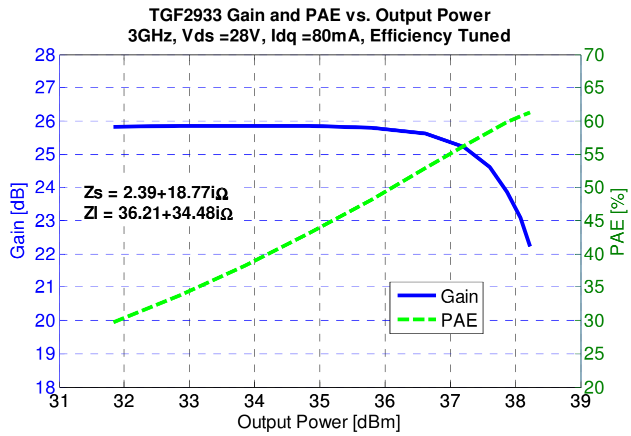


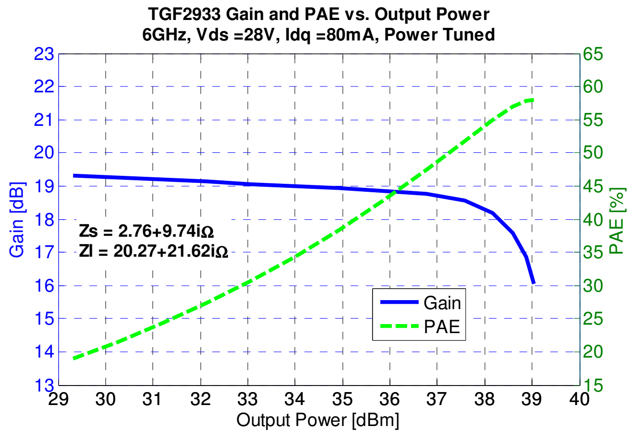


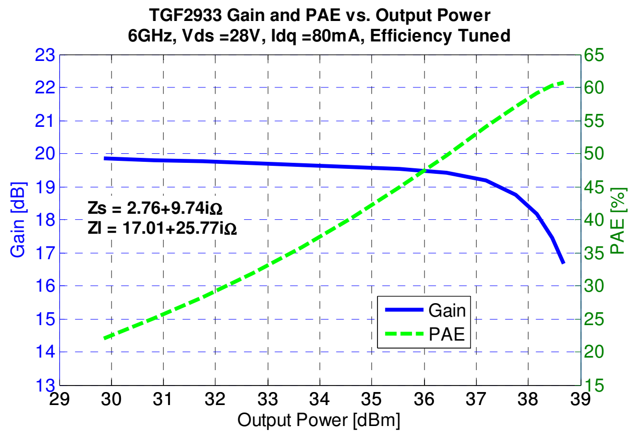
Typical Model Performance – Load-Pull Drive-up[1, 2]

Notes:
1. CW, Bondwires not included
2. See page 22 for load-pull and source-pull reference planes where the performance was measured.



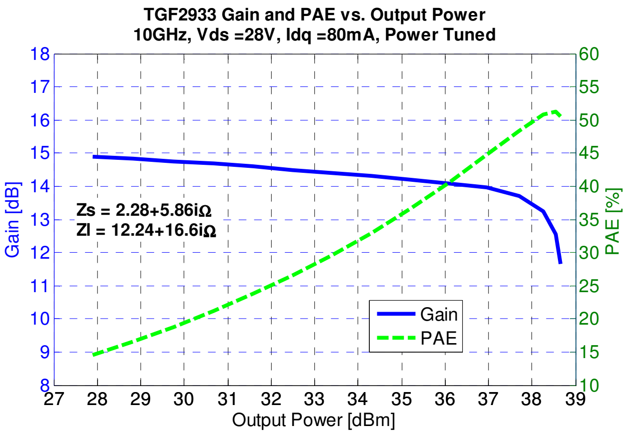


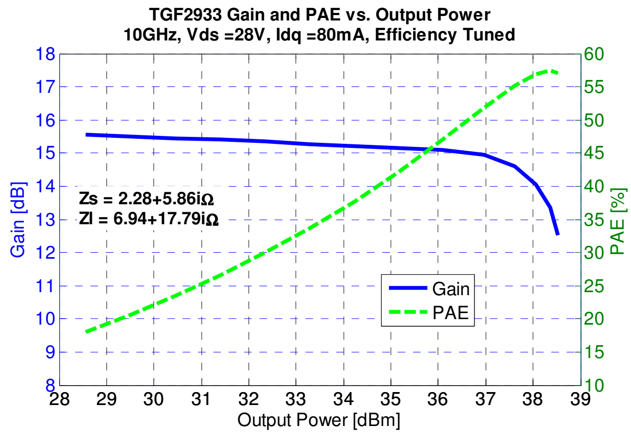


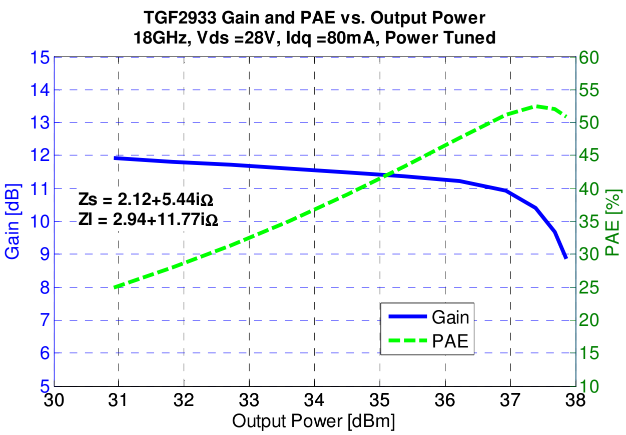


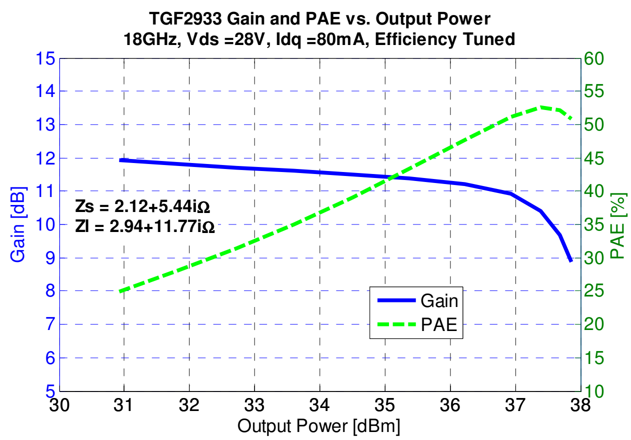
Typical Model Performance – Load-Pull Drive-up[1, 2]

Notes:
1. CW, Bondwires not included
2. See page 22 for load-pull and source-pull reference planes where the performance was measured.

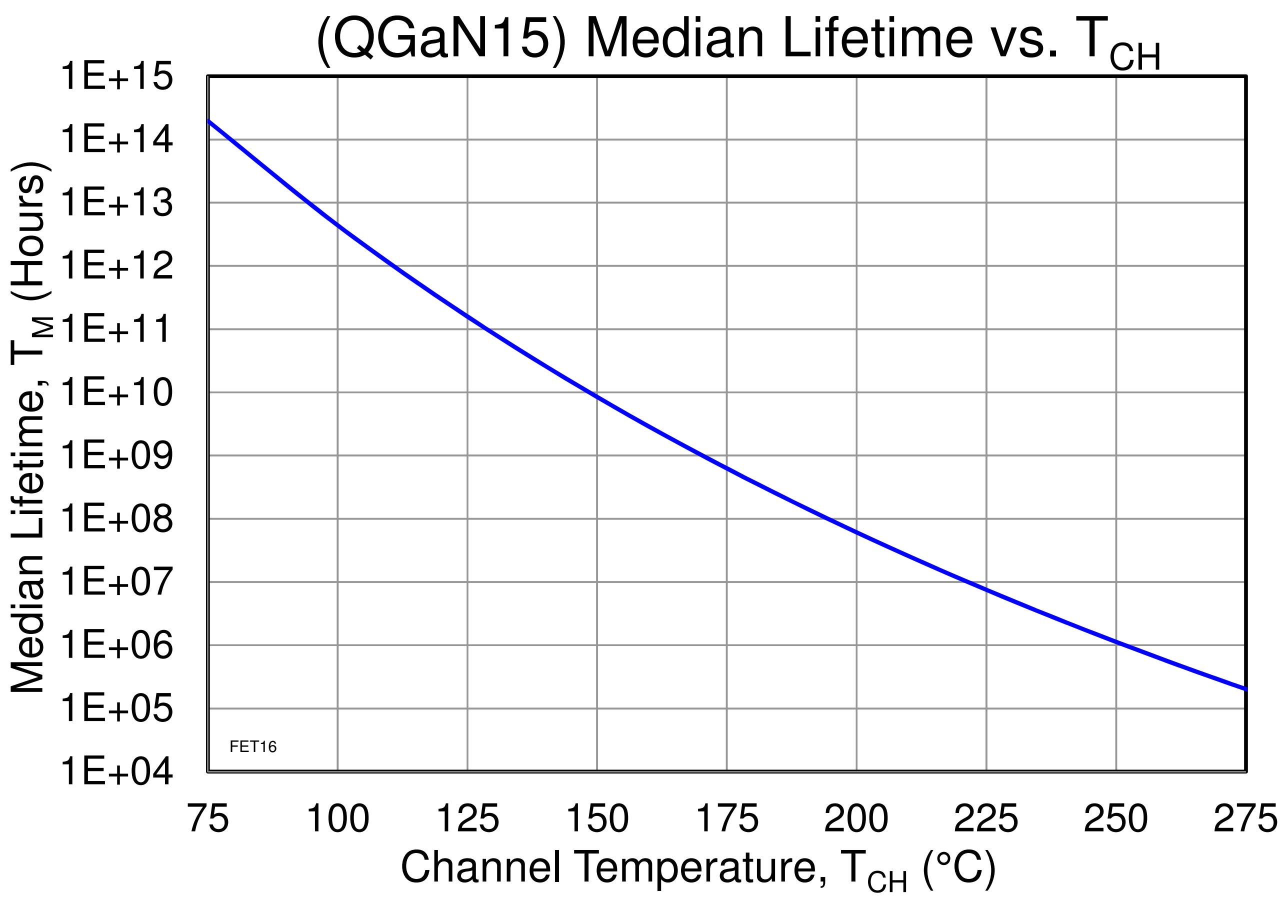






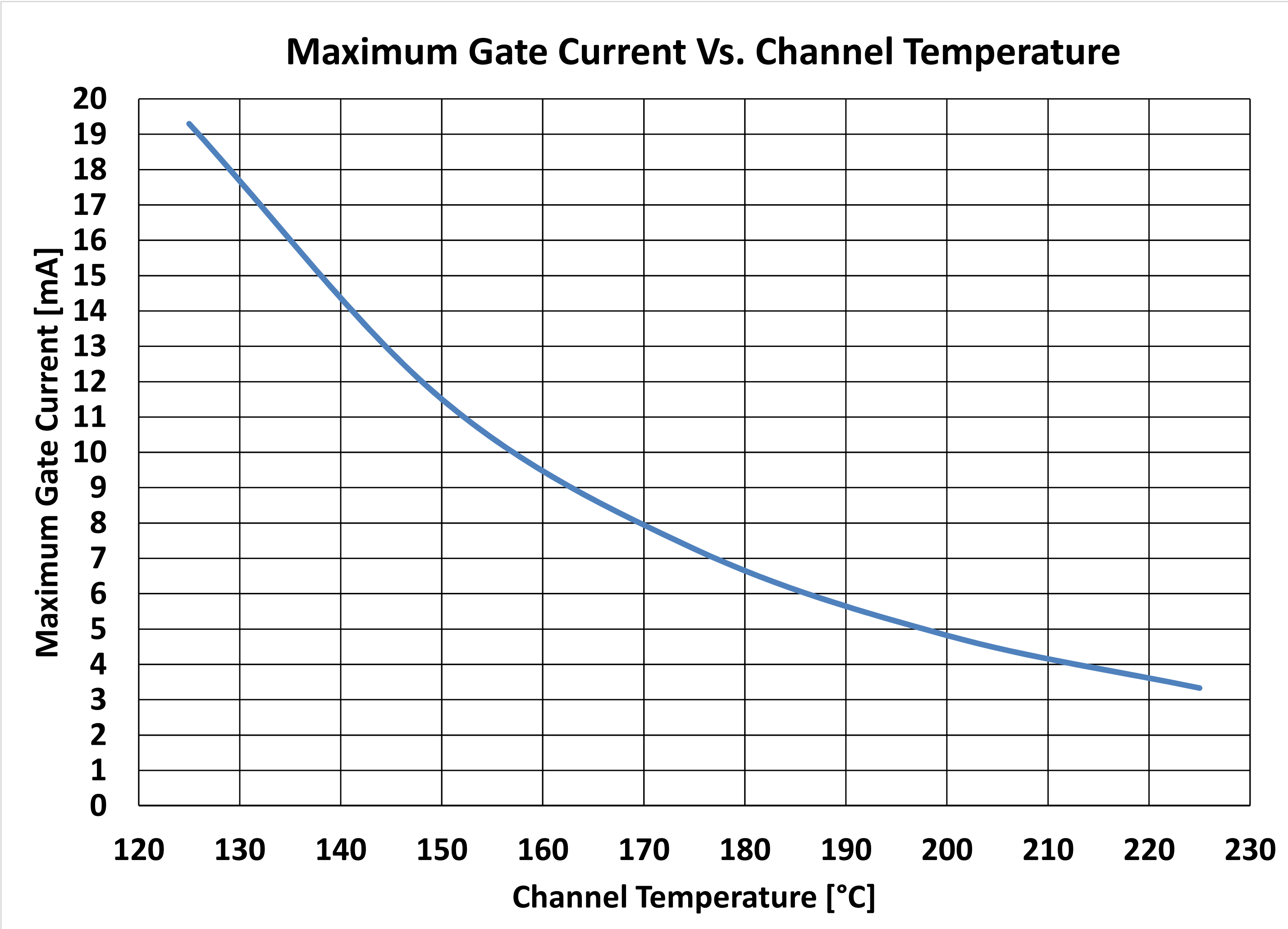


Median Lifetime[1]



Notes:
1. Test Conditions: V_D = +28 V; Failure Criteria = 10 % reduction in I_{D_MAX} during DC Life Testing

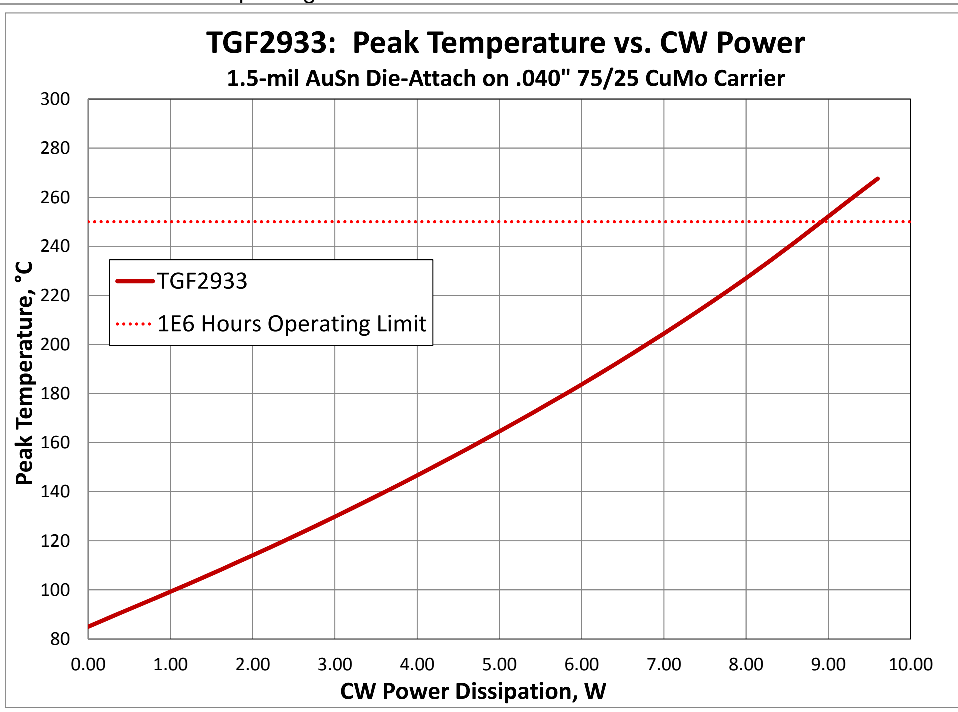
Maximum Gate Current



Thermal and Reliability Information

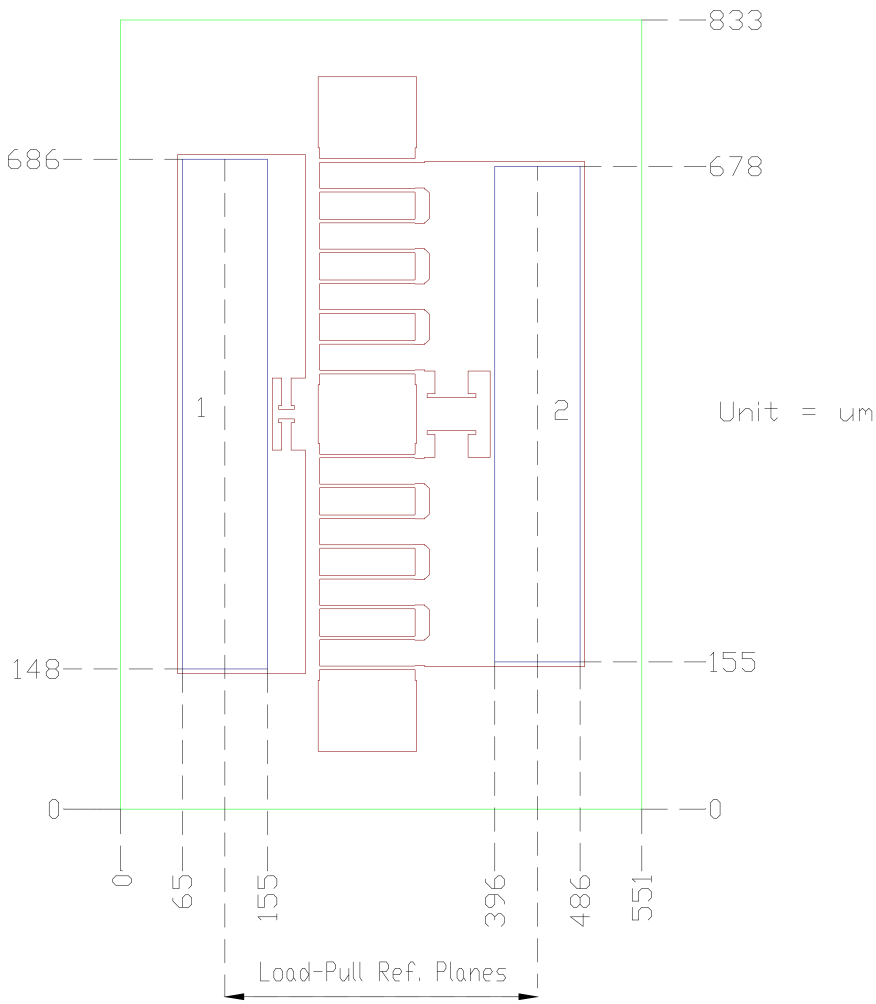
Parameter	Test Conditions	Value	Units
Thermal Resistance, θ_{JC} [(1)]	CW $T_{baseplate}$ = +85 °C P_{DISS} = 1.6 W	14.4	°C/W
Channel Temperature, T_{CH}		108	°C
Median Lifetime, T_M		1.4E12	Hrs
Thermal Resistance, θ_{JC} [(1)]	CW $T_{baseplate}$ = +85 °C P_{DISS} = 3.2 W	15.0	°C/W
Channel Temperature, T_{CH}		133	°C
Median Lifetime, T_M		6.0E10	Hrs
Thermal Resistance, θ_{JC} [(1)]	CW $T_{baseplate}$ = +85 °C P_{DISS} = 4.8 W	15.8	°C/W
Channel Temperature, T_{CH}		161	°C
Median Lifetime, T_M		2.6E9	Hrs
Thermal Resistance, θ_{JC} [(1)]	CW $T_{baseplate}$ = +85 °C P_{DISS} = 6.4 W	16.7	°C/W
Channel Temperature, T_{CH}		192	°C
Median Lifetime, T_M		1.2E8	Hrs
Thermal Resistance, θ_{JC} [(1)]	CW $T_{baseplate}$ = +85 °C P_{DISS} = 8 W	17.8	°C/W
Channel Temperature, T_{CH}		227	°C
Median Lifetime, T_M		6.4E6	Hrs
Thermal Resistance, θ_{JC} [(1)]	CW $T_{baseplate}$ = +85 °C P_{DISS} = 9.6 W	19.1	°C/W
Channel Temperature, T_{CH}		268	°C
Median Lifetime, T_M		3.2E5	Hrs

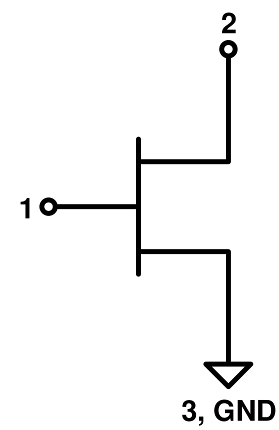
Notes:
1. Thermal resistance measured at back of package.



Pin Configuration and Description[1]

Notes: 1. Die size tolerance is ± 0.015 mm.





Pin Description

Pin	Symbol	Description	Dimension
1	RF IN / V_G	Gate	0.538 x 0.090 mm
2	RF OUT / V_D	Drain	0.523 x 0.090 mm
3	Source	Source / Ground / Backside of die	0.833 x 0.551 mm

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment (i.e. epoxy) not recommended.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300°C to 3-4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Ball bonding is the preferred interconnect technique, except where noted on the assembly diagram.
- Force, time, and ultrasonics are critical bonding parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Disclaimer

GaN/SiC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Bias-up Procedure	Bias-down Procedure
1. Set V_G to -4 V. 2. Set I_D limit to 100 mA. 3. Slowly adjust V_G until I_D reaches 80 mA. 4. Set I_D limit to 500 mA. 5. Apply RF signal.	1. Turn off RF signal. 2. Turn off V_D and wait 1 second to allow drain capacitor discharge. 3. Turn of V_G.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	N/A	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	N/A	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	N/A	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260 °C max. reflow temp.) and tin/lead (245 °C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: NiPdAu

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Qorvo:

Web: www.Qorvo.com　　**Tel:** +1.972.994.8465
Email: info-sales@qorvo.com　　**Fax:** +1.972.994.8504

For technical questions and application information: **Email:** info-products@qorvo.com

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