



## SNx4LVC541A Octal Buffers/Drivers With 3-State Outputs

### 1 Features

- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 5.1 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $>2$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- $I_{off}$  Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

### 2 Applications

- Servers
- PCs and Notebooks
- Network Switches
- Wearable Health and Wellness Devices
- Telecom Infrastructures
- Electronic Points of Sale

### 3 Description

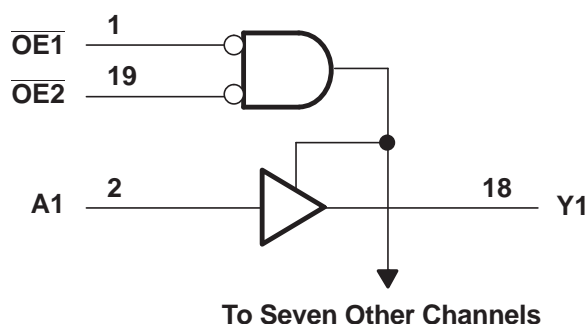
The SN54LVC541A octal buffer/driver is designed for 2.7-V to 3.6-V  $V_{CC}$  operation, and the SN74LVC541A octal buffer/driver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

**Device Information<sup>(1)</sup>**

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC541A	SSOP (20)	7.20 mm × 5.30 mm
	TVSOP (20)	5.00 mm × 4.40 mm
	VQFN (20)	4.50 mm × 3.50 mm
	SOIC (20)	12.80 mm × 7.50 mm
	TSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### 4 Simplified Schematic



## Table of Contents

<b>1 Features</b>	<b>1</b>	<b>9 Detailed Description</b>	<b>10</b>
<b>2 Applications</b>	<b>1</b>	9.1 Overview	10
<b>3 Description</b>	<b>1</b>	9.2 Functional Block Diagram	10
<b>4 Simplified Schematic</b>	<b>1</b>	9.3 Feature Description	10
<b>5 Revision History</b>	<b>2</b>	9.4 Device Functional Modes	10
<b>6 Pin Configuration and Functions</b>	<b>3</b>	<b>10 Application and Implementation</b>	<b>11</b>
<b>7 Specifications</b>	<b>4</b>	10.1 Application Information	11
7.1 Absolute Maximum Ratings	4	10.2 Typical Application	11
7.2 Handling Ratings	4	<b>11 Power Supply Recommendations</b>	<b>12</b>
7.3 Recommended Operating Conditions	5	<b>12 Layout</b>	<b>12</b>
7.4 Thermal Information	5	12.1 Layout Guidelines	12
7.5 Electrical Characteristics—DC Limit Changes	6	12.2 Layout Example	12
7.6 Switching Characteristics—AC Limit Changes	7	<b>13 Device and Documentation Support</b>	<b>13</b>
7.7 Switching Characteristics, SN74LVC541A –40°C to 85°C	7	13.1 Related Links	13
7.8 Switching Characteristics, SN74LVC541A –40°C to 125°C	7	13.2 Trademarks	13
7.9 Operating Characteristics	7	13.3 Electrostatic Discharge Caution	13
7.10 Typical Characteristics	8	13.4 Glossary	13
<b>8 Parameter Measurement Information</b>	<b>9</b>	<b>14 Mechanical, Packaging, and Orderable Information</b>	<b>13</b>

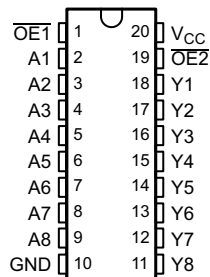
## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

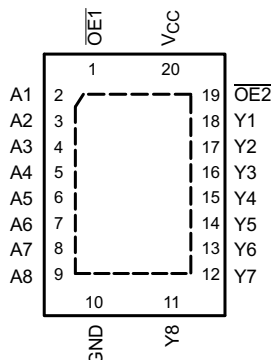
Changes from Revision M (May 2005) to Revision N	Page
• Updated document to new TI data sheet format	1
• Removed Ordering Information table	1
• Updated $I_{off}$ Feature bullet	1
• Updated Features to include Military Disclaimer	1
• Added Applications	1
• Added Device Information table	1
• Added Handling Ratings table	4
• Changed MAX operating free-air temperature from 85°C to 125°C for SN74LVC541A	5
• Updated Thermal Information table	5
• Added –40°C TO 125°C temperature range to Electrical Characteristics table for SN74LVC541A	6
• Added Switching Characteristics table –40°C TO 125°C temperature range for SN74LVC541A	7
• Added Typical Characteristics	8

## 6 Pin Configuration and Functions

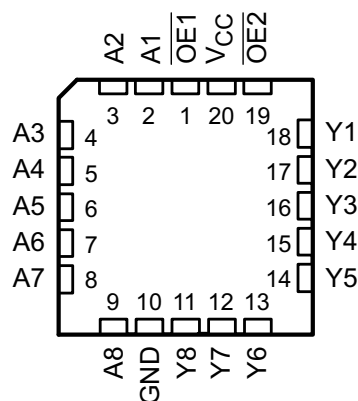
**SN54LVC541A . . . J OR W PACKAGE**  
**SN74LVC541A . . . DB, DGV, DW, NS,**  
**OR PW PACKAGE**  
(TOP VIEW)



**SN74LVC541A . . . RGY PACKAGE**  
(TOP VIEW)



**SN54LVC541A . . . FK PACKAGE**  
(TOP VIEW)



### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$\overline{OE1}$	I	Output enable
2	A1	I	A1 input
3	A2	I	A2 input
4	A3	I	A3 input
5	A4	I	A4 input
6	A5	I	A5 input
7	A6	I	A6 input
8	A7	I	A7 input
9	A8	I	A8 input
10	GND	—	Ground pin
11	Y8	O	Y8 output
12	Y7	O	Y7 output
13	Y6	O	Y6 output
14	Y5	O	Y5 output
15	Y4	O	Y4 output
16	Y3	O	Y3 output
17	Y2	O	Y2 output
18	Y1	O	Y1 output
19	$\overline{OE2}$	I	Output enable
20	VCC	—	Power pin

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	–0.5	6.5	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	–0.5	6.5	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	–0.5	6.5	V
V <sub>O</sub>	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	–0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		–50 mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		–50 mA
I <sub>O</sub>	Continuous output current		±50	mA
	Continuous current through V <sub>CC</sub> or GND		±100	mA

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the *Recommended Operating Conditions* table.

### 7.2 Handling Ratings

			MIN	MAX	UNIT
T <sub>stg</sub>	Storage temperature range		−65	150	°C
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	0	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			SN54LVC541A		SN74LVC541A		UNIT
			MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V			0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V			1.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V	2		2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V			0.35 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V			0.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V		0.8	0.8		
V <sub>I</sub>	Input voltage		0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	High or low state	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
		3-state	0	5.5	0	5.5	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V				–4	mA
		V <sub>CC</sub> = 2.3 V				–8	
		V <sub>CC</sub> = 2.7 V		–12		–12	
		V <sub>CC</sub> = 3 V		–24		–24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V				4	mA
		V <sub>CC</sub> = 2.3 V				8	
		V <sub>CC</sub> = 2.7 V		12		12	
		V <sub>CC</sub> = 3 V		24		24	
T <sub>A</sub>	Operating free-air temperature		–55	125	–40	125	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

### 7.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC <sup>(1)</sup>		SN74LVC541A					UNIT
		DB	DGV	DW	NS	PW	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	112.1	128.9	99.4	90.3	100.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	73.6	43.8	66.9	56.6	35.2	
R <sub>θJB</sub>	Junction-to-board thermal resistance	67.3	70.4	66.9	57.8	51.8	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	33.3	3.2	33.8	28.7	2.2	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	66.9	69.7	66.5	57.4	51.2	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, literature number [SPRA953](#).

**SN54LVC541A, SN74LVC541A**

SCAS298N – JANUARY 1993 – REVISED JUNE 2014

[www.ti.com](http://www.ti.com)

## 7.5 Electrical Characteristics—DC Limit Changes

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	–55°C TO 125°C			–40°C TO 85°C			–40°C TO 125°C			UNIT	
			SN54LVC541A			SN74LVC541A			SN74LVC541A				
			MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX		
V <sub>OH</sub>	I <sub>OH</sub> = –100 μA	1.65 V to 3.6 V	V <sub>CC</sub> – 0.2			V <sub>CC</sub> – 0.2			V <sub>CC</sub> – 0.3			V	
		2.7 V to 3.6 V											
	I <sub>OH</sub> = –4 mA	1.65 V	1.20			1.20							
	I <sub>OH</sub> = –8 mA	2.3 V	1.7			1.7							
	I <sub>OH</sub> = –12 mA	2.7 V	2.2	2.2			2.2						
		3 V	2.4	2.4			2.4						
	I <sub>OH</sub> = –24 mA	3 V	2.2	2.2			2.2						
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V	0.2			0.2			0.3			V	
		2.7 V to 3.6 V											
	I <sub>OL</sub> = 4 mA	1.65 V	0.45			0.45							
	I <sub>OL</sub> = 8 mA	2.3 V	0.7			0.7							
	I <sub>OL</sub> = 12 mA	2.7 V	0.4			0.4							
	I <sub>OL</sub> = 24 mA	3 V	0.55			0.55							
I <sub>I</sub>	V <sub>I</sub> = 0 to 5.5 V	3.6 V	±5			±5			±5			μA	
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0				±10			±10			μA	
I <sub>OZ</sub>	V <sub>O</sub> = 0 to 5.5 V	3.6 V	±15			±10			±10			μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	I <sub>O</sub> = 0	3.6 V	10			10			10			μA
	3.6 V ≤ V <sub>I</sub> ≤ 5.5 V <sup>(2)</sup>			10			10						
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V	500			500			500			μA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	4			4			4			pF	
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	5.5			5.5			5.5			pF	

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This applies in the disabled state only.

## 7.6 Switching Characteristics—AC Limit Changes

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC541A				UNIT
			V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y		5.6	1	5.1	ns
t <sub>en</sub>	$\overline{\text{OE}}$	Y		7.5	1	7	ns
t <sub>dis</sub>	$\overline{\text{OE}}$	Y		7.7	1	7	ns

## 7.7 Switching Characteristics, SN74LVC541A –40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC541A								UNIT
			−40°C TO 85°C								
			V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	1	15.7	1	7.8	1	5.6	1.5	5.1	ns
t <sub>en</sub>	$\overline{\text{OE}}$	Y	1	17.5	1	10.5	1	7.5	1.5	7	ns
t <sub>dis</sub>	$\overline{\text{OE}}$	Y	1	16.5	1	9	1	7.7	1.5	7	ns
t <sub>sk(o)</sub>										1	ns

## 7.8 Switching Characteristics, SN74LVC541A –40°C to 125°C

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

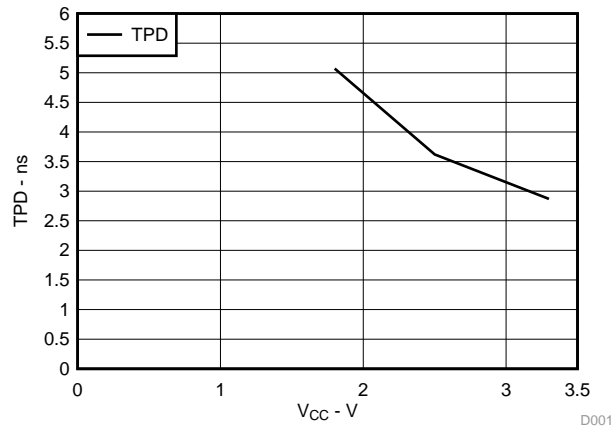
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC541A								UNIT
			−40°C TO 125°C								
			V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	1	16.3	1	8.3	1	6.1	1	5.6	ns
t <sub>en</sub>	$\overline{\text{OE}}$	Y	1	18.5	1	11.1	1	8	1	7.5	ns
t <sub>dis</sub>	$\overline{\text{OE}}$	Y	1	17.3	1	9.7	1	8.2	1	7.5	ns
t <sub>sk(o)</sub>										1.5	ns

## 7.9 Operating Characteristics

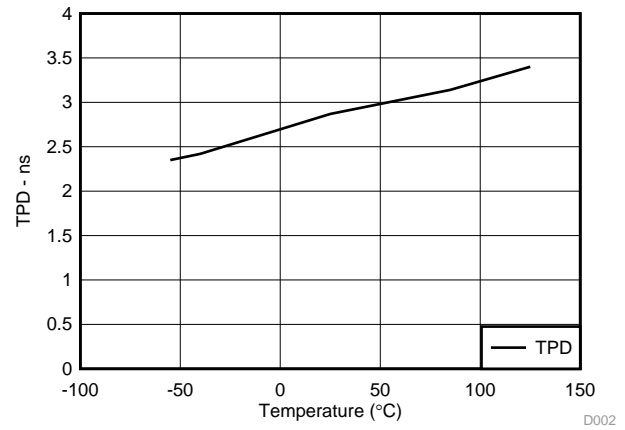
T<sub>A</sub> = 25°C

PARAMETER			TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
				TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz	65	58	33	pF
		Outputs disabled		2	2	2	

## 7.10 Typical Characteristics



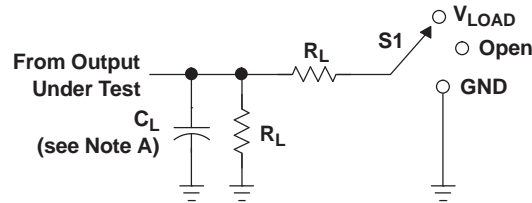
**Figure 1. SN74LVC541A TPD Across V<sub>CC</sub> at 25°C**



**Figure 2. SN74LVC541A TPD Across Temperature at 3.3 V**



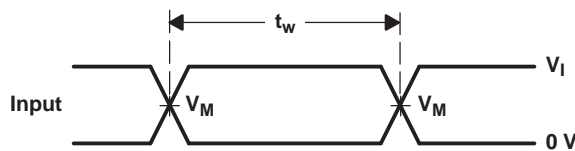
## 8 Parameter Measurement Information



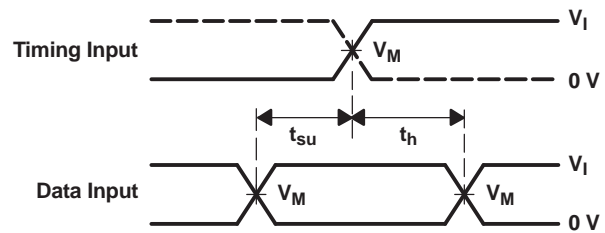
**LOAD CIRCUIT**

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

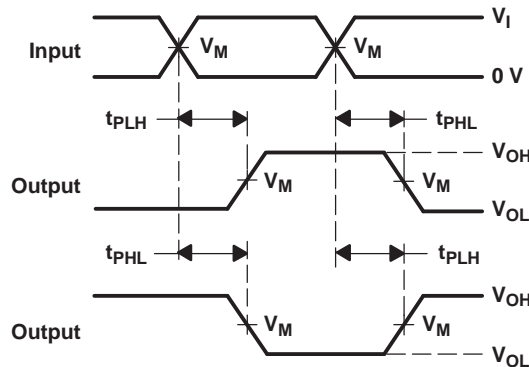
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



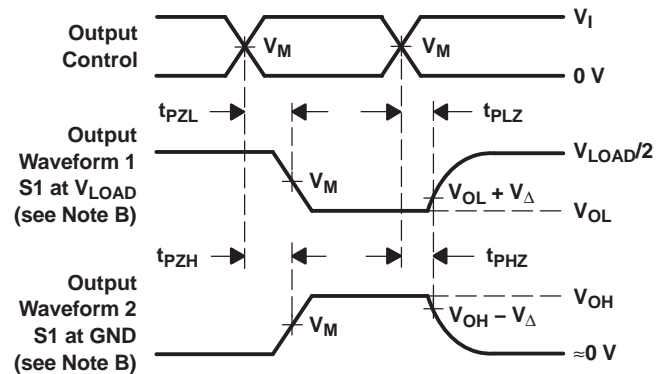
**VOLTAGE WAVEFORMS  
PULSE DURATION**



**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING**

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**

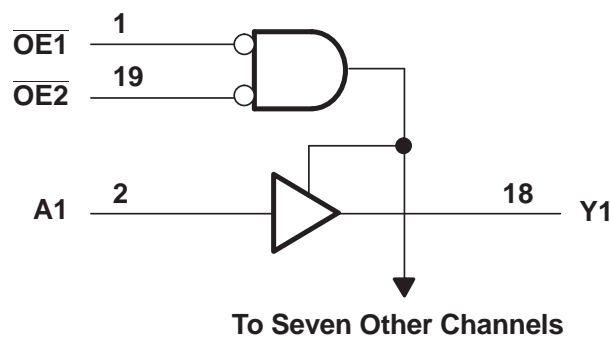
## 9 Detailed Description

### 9.1 Overview

The 'LVC541A devices are ideal for driving bus lines or buffering memory address registers.

These devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout. The 3-state control gate is a 2-input AND gate with active-low inputs so that, if either output enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all eight outputs are in the high-impedance state. Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment. These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

- Wide operating voltage range
  - Operates from 1.65 V to 3.6 V
- Allows down voltage translation
  - Inputs accept voltages to 5.5 V
- $I_{off}$  feature
  - Allows voltages on the inputs and outputs when  $V_{CC}$  is 0 V

### 9.4 Device Functional Modes

**Table 1. Function Table**

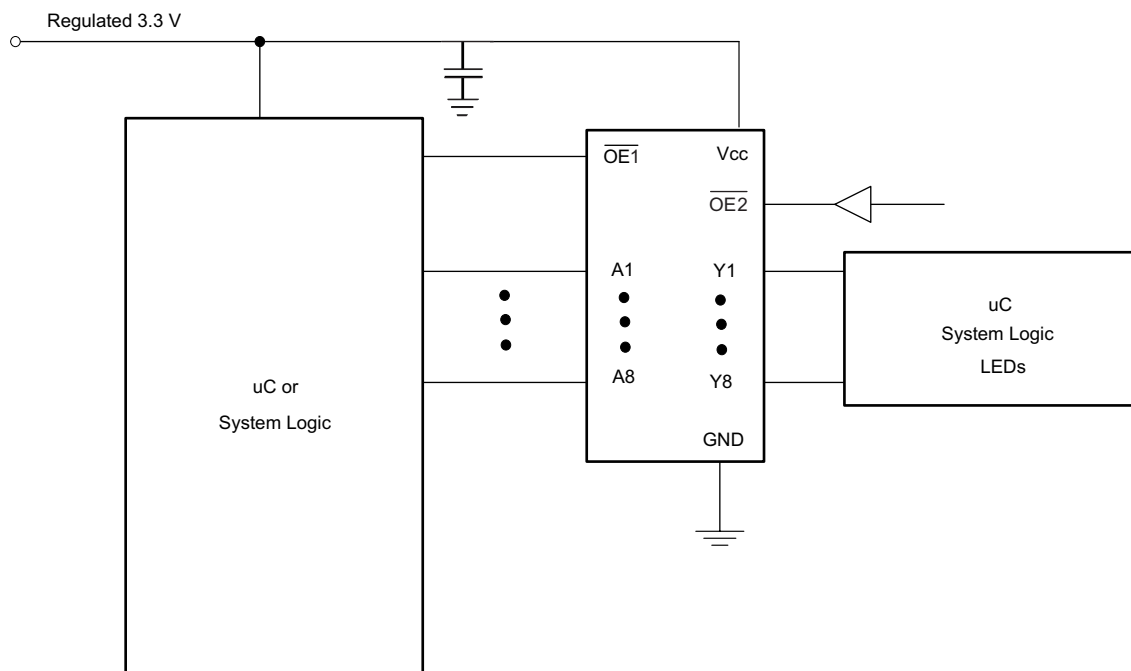
INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

## 10 Application and Implementation

### 10.1 Application Information

The SN74LVC541A is a high-drive CMOS device that can be used for a multitude of bus-interface type applications where the data needs to be retained or latched. It can produce 24 mA of drive current at 3.3 V. Therefore, this device is ideal for driving multiple outputs and for high-speed applications up to 100 Mhz. The inputs are 5.5 V tolerant allowing the device to translate down to  $V_{CC}$ .

### 10.2 Typical Application



**Figure 4. Typical Application Diagram**

#### 10.2.1 Design Requirements

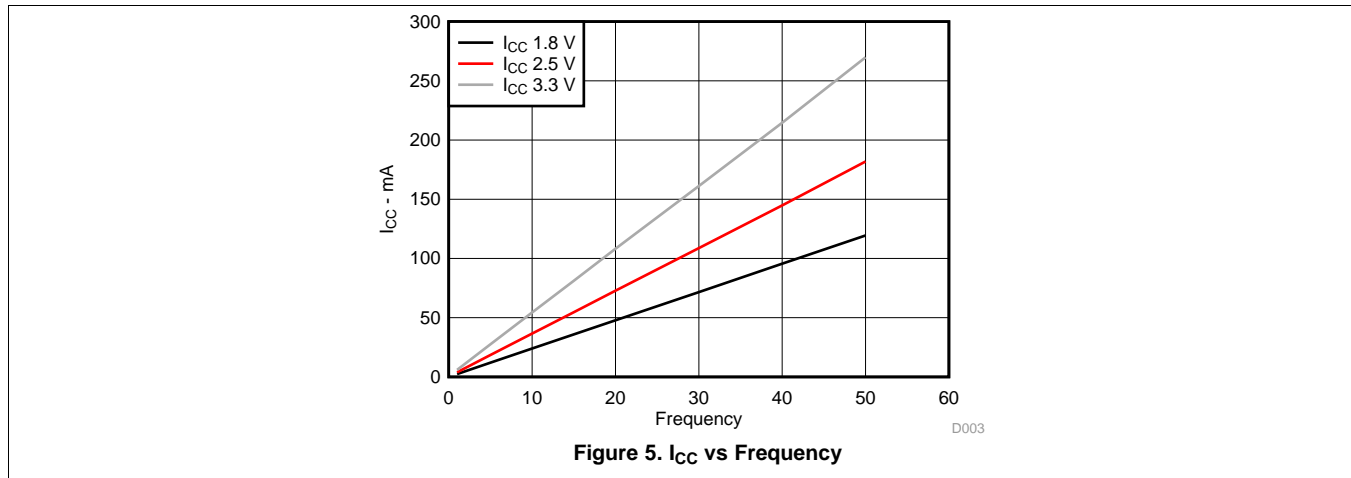
This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

#### 10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
  - Rise time and fall time specs: See  $(\Delta t/\Delta V)$  in the [Recommended Operating Conditions](#) table.
  - Specified high and low levels: See  $(V_{IH}$  and  $V_{IL})$  in the [Recommended Operating Conditions](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$ .
2. Recommend Output Conditions
  - Load currents should not exceed 25 mA per output and 50 mA total for the part.
  - Outputs should not be pulled above  $V_{CC}$ .

## Typical Application (continued)

### 10.2.3 Application Curves



## 11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{f}$  is recommended; if there are multiple  $V_{CC}$  pins, then 0.01  $\mu\text{f}$  or 0.022  $\mu\text{f}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{f}$  and a 1  $\mu\text{f}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

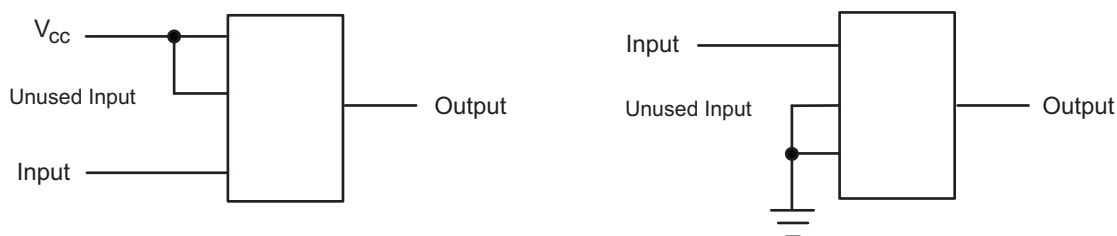
## 12 Layout

### 12.1 Layout Guidelines

When using multiple bit logic devices inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Figure 6](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$  whichever make more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

### 12.2 Layout Example



**Figure 6. Layout Diagram**

## 13 Device and Documentation Support

### 13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LVC541A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
SN74LVC541A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 13.2 Trademarks

All trademarks are the property of their respective owners.

### 13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9759501Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9759501Q2A SNJ54LVC 541AFK	<a href="#">Samples</a>
5962-9759501QRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9759501QR A SNJ54LVC541AJ	<a href="#">Samples</a>
5962-9759501QSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9759501QS A SNJ54LVC541AW	<a href="#">Samples</a>
SN74LVC541ADBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A	<a href="#">Samples</a>
SN74LVC541ADBRG4	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A	<a href="#">Samples</a>
SN74LVC541ADGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A	<a href="#">Samples</a>
SN74LVC541ADGVRE4	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A	<a href="#">Samples</a>
SN74LVC541ADGVRG4	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A	<a href="#">Samples</a>
SN74LVC541ADW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC541A	<a href="#">Samples</a>
SN74LVC541ADWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC541A	<a href="#">Samples</a>
SN74LVC541ADWRE4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC541A	<a href="#">Samples</a>
SN74LVC541ANSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC541A	<a href="#">Samples</a>
SN74LVC541APW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A	<a href="#">Samples</a>
SN74LVC541APWG4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A	<a href="#">Samples</a>
SN74LVC541APWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	LC541A	<a href="#">Samples</a>
SN74LVC541APWRE4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A	<a href="#">Samples</a>
SN74LVC541APWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC541APWT	ACTIVE	TSSOP	PW	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A	<a href="#">Samples</a>
SN74LVC541ARGYR	ACTIVE	VQFN	RGY	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC541A	<a href="#">Samples</a>
SN74LVC541ARGYRG4	ACTIVE	VQFN	RGY	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC541A	<a href="#">Samples</a>
SNJ54LVC541AFK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9759501Q2A SNJ54LVC 541AFK	<a href="#">Samples</a>
SNJ54LVC541AJ	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9759501QR A SNJ54LVC541AJ	<a href="#">Samples</a>
SNJ54LVC541AW	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9759501QS A SNJ54LVC541AW	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LVC541A, SN74LVC541A :**

- Catalog : [SN74LVC541A](#)
- Automotive : [SN74LVC541A-Q1](#), [SN74LVC541A-Q1](#)
- Enhanced Product : [SN74LVC541A-EP](#), [SN74LVC541A-EP](#)
- Military : [SN54LVC541A](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications



**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC541ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVC541ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC541ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LVC541ANSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LVC541APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVC541APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVC541APWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVC541APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVC541ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC541ADBR	SSOP	DB	20	2000	853.0	449.0	35.0
SN74LVC541ADGVR	TVSOP	DGV	20	2000	853.0	449.0	35.0
SN74LVC541ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LVC541ANSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LVC541APWR	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74LVC541APWR	TSSOP	PW	20	2000	853.0	449.0	35.0
SN74LVC541APWRG4	TSSOP	PW	20	2000	367.0	367.0	38.0
SN74LVC541APWT	TSSOP	PW	20	250	853.0	449.0	35.0
SN74LVC541ARGYR	VQFN	RGY	20	3000	853.0	449.0	35.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9759501Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
SN74LVC541ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVC541APW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LVC541APWG4	PW	TSSOP	20	70	530	10.2	3600	3.5
SNJ54LVC541AFK	FK	LCCC	20	1	506.98	12.06	2030	NA



4220724/A 05/2016

## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

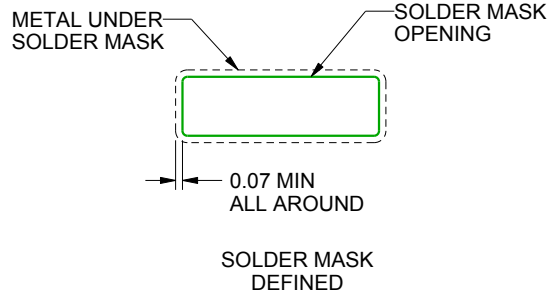
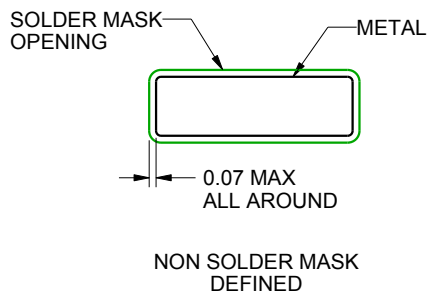
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



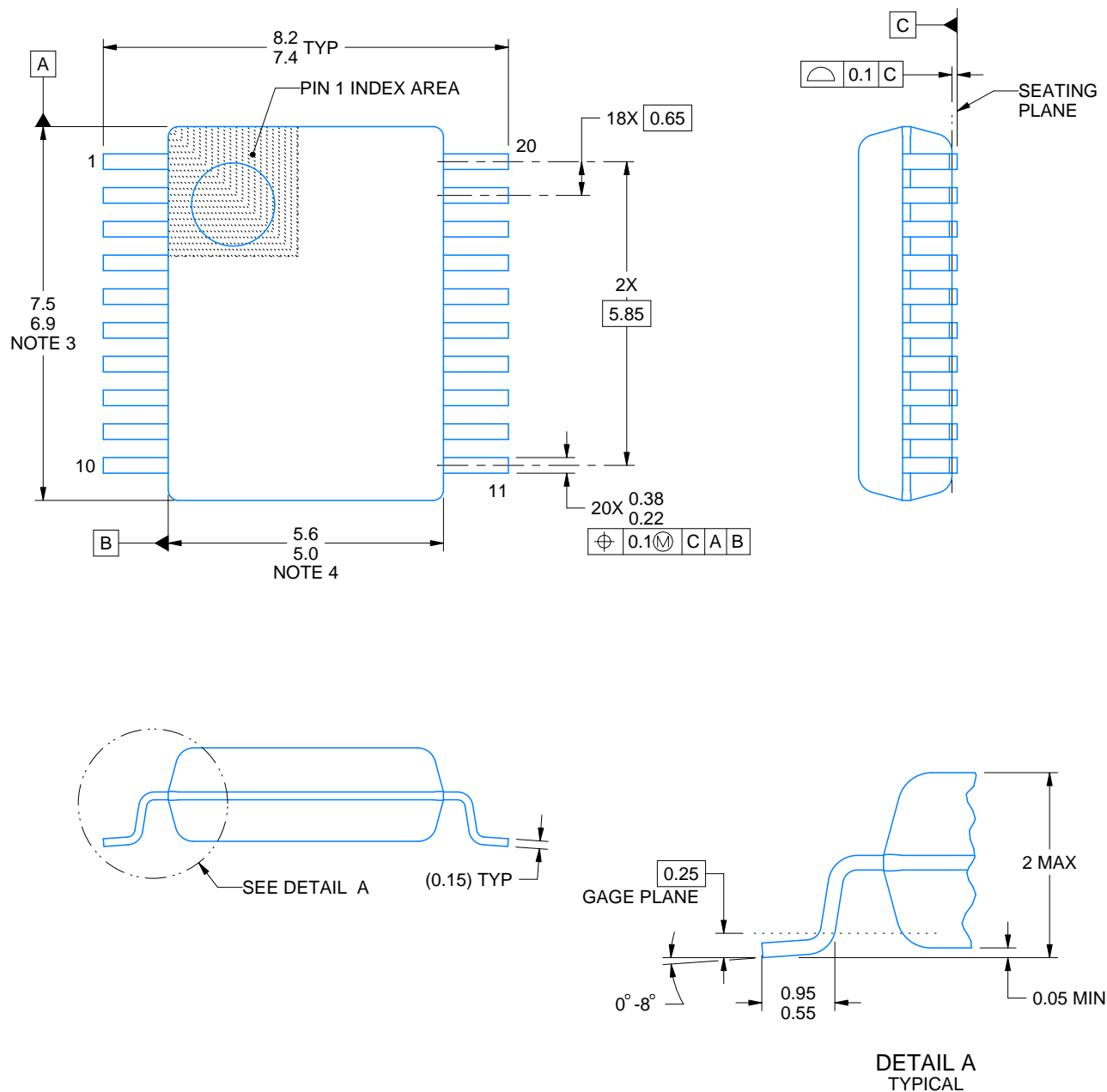
4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004



## SSOP - 2 mm max height

## SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



# EXAMPLE BOARD LAYOUT

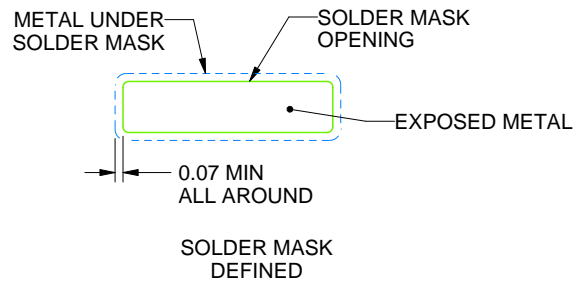
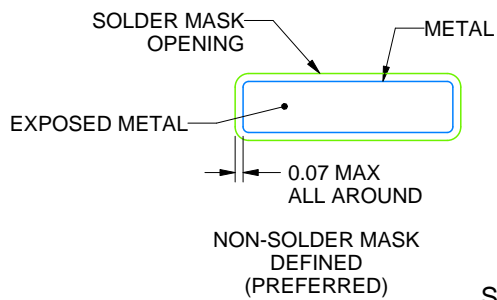
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

## GENERIC PACKAGE VIEW

**RGY 20**

**VQFN - 1 mm max height**

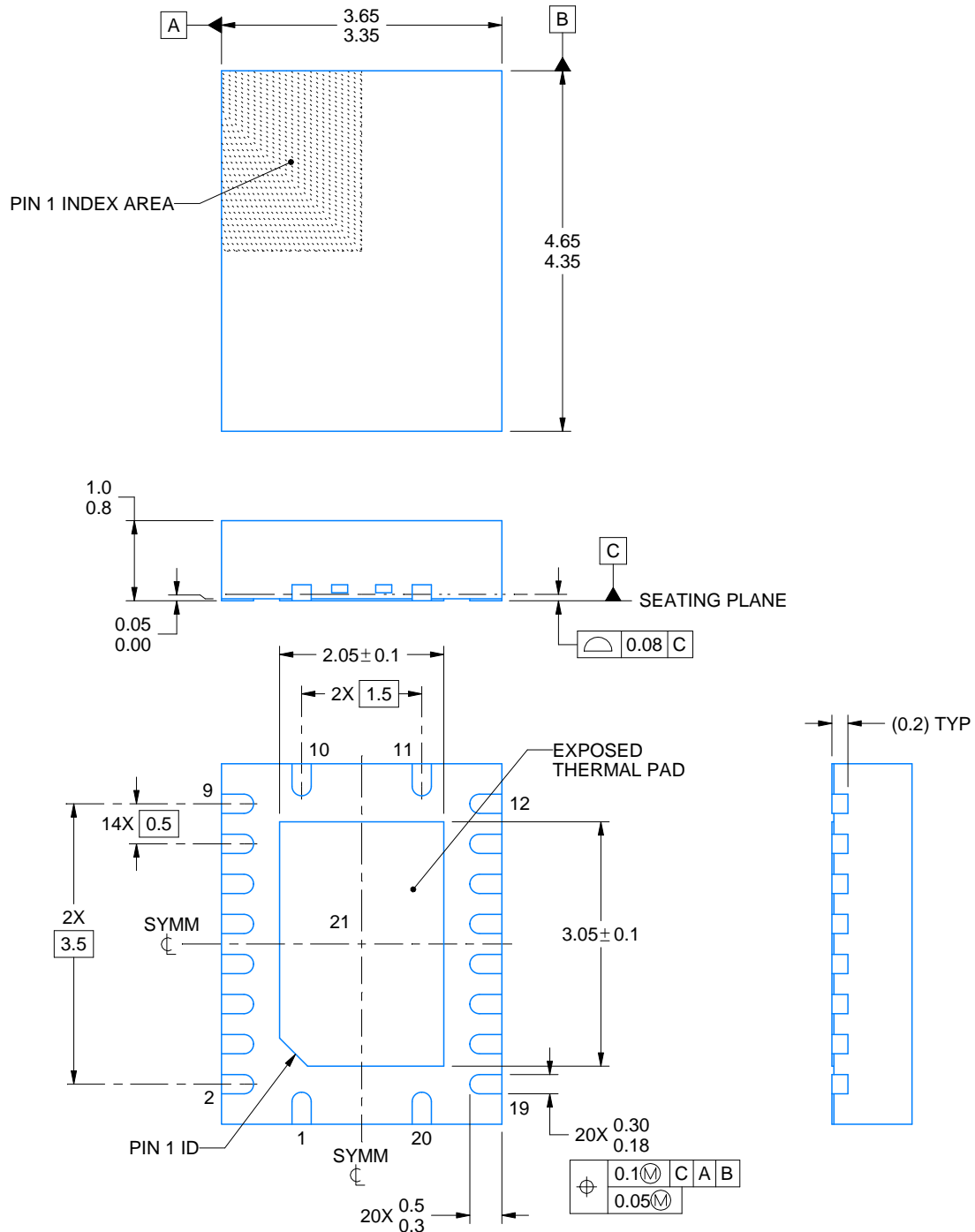
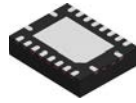
3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225264/A



4225320/A 09/2019

## NOTES:

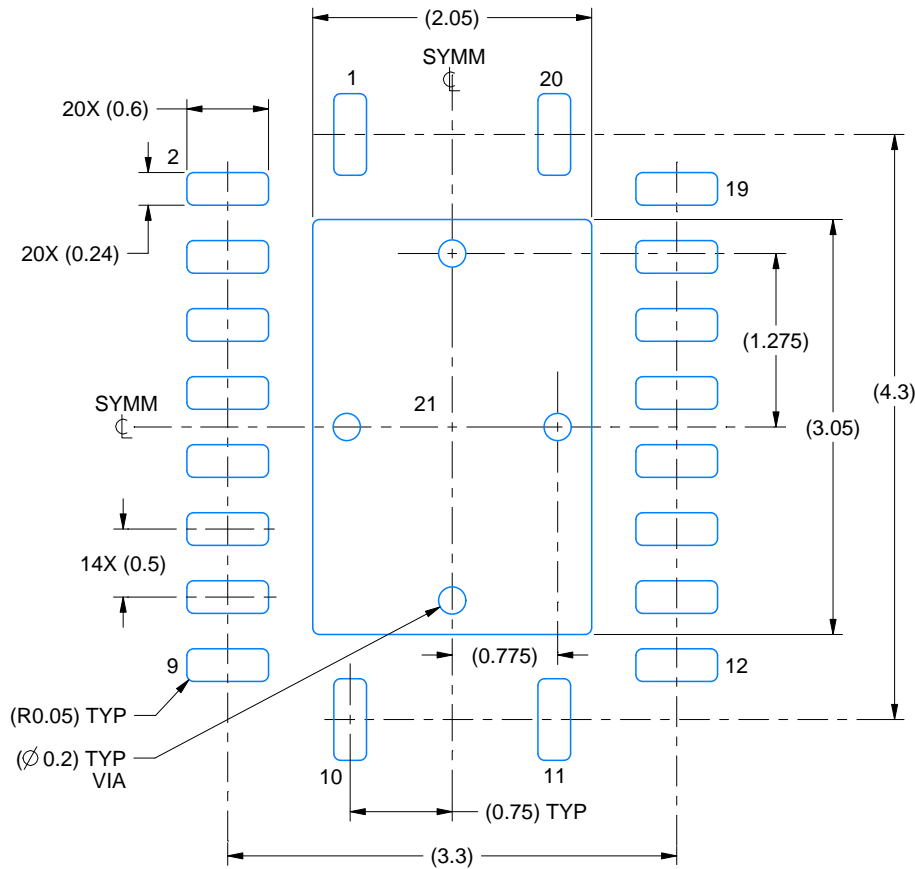
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

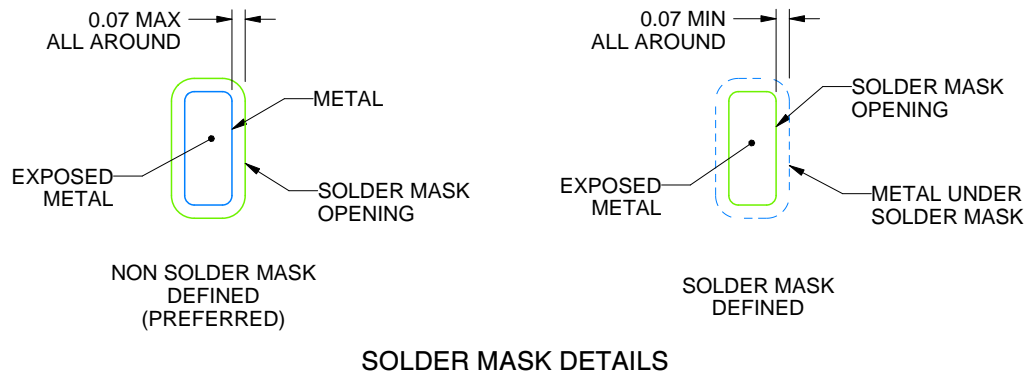
RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



4225320/A 09/2019

NOTES: (continued)

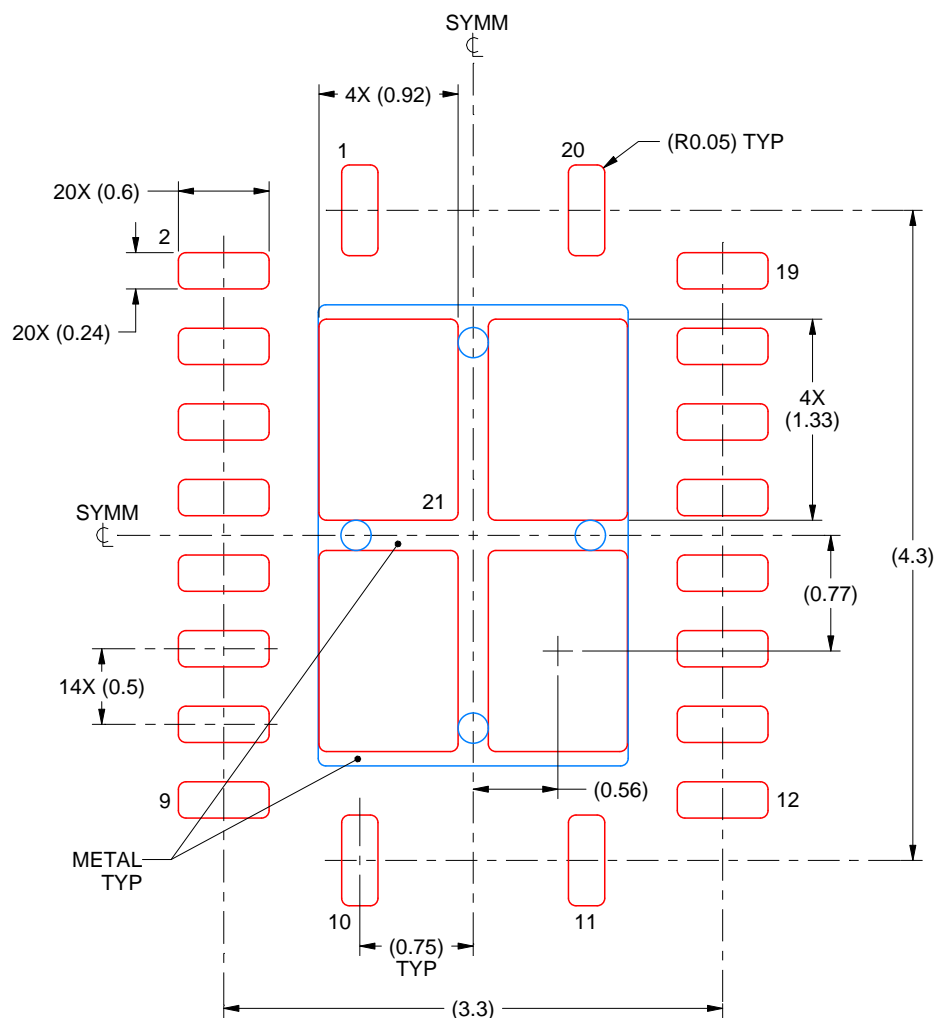
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



**RGY0020A**

### VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
**BASED ON 0.125 mm THICK STENCIL**

EXPOSED PAD 21  
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



## NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20



4220206/A 02/2017

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated