

NLSV8T244

8-Bit Dual-Supply Non-Inverting Level Translator

The NLSV8T244 is a 8-bit configurable dual-supply voltage level translator. The input A_n and output B_n ports are designed to track two different power supply rails, V_{CCA} and V_{CCB} respectively. Both supply rails are configurable from 0.9 V to 4.5 V allowing universal low-voltage translation from the input A_n to the output B_n port.

Features

- Wide V_{CCA} and V_{CCB} Operating Range: 0.9 V to 4.5 V
- High-Speed w/ Balanced Propagation Delay
- Inputs and Outputs have OVT Protection to 4.5 V
- Non-preferential V_{CCA} and V_{CCB} Sequencing
- Outputs at 3-State until Active V_{CC} is Reached
- Power-Off Protection
- Outputs Switch to 3-State with V_{CCB} at GND
- Ultra-Small Packaging: 4.0 mm x 2.0 mm UDFN20
- This is a Pb-Free Device

Typical Applications

- Mobile Phones, PDAs, Other Portable Devices

Important Information

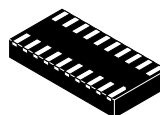
- ESD Protection for All Pins:
HBM (Human Body Model) > 6000 V



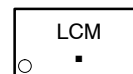
ON Semiconductor®

<http://onsemi.com>

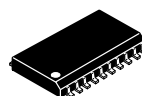
MARKING DIAGRAMS



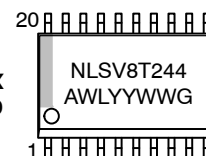
UQFN20
MU SUFFIX
CASE 517AK



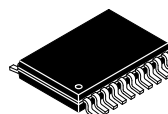
LC = Specific Device Code
M = Date Code
▪ = Pb-Free Package



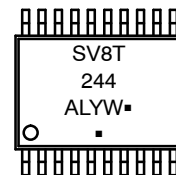
SOIC-20
DW SUFFIX
CASE 751D



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package



TSSOP-20
DT SUFFIX
CASE 948E



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

NLSV8T244

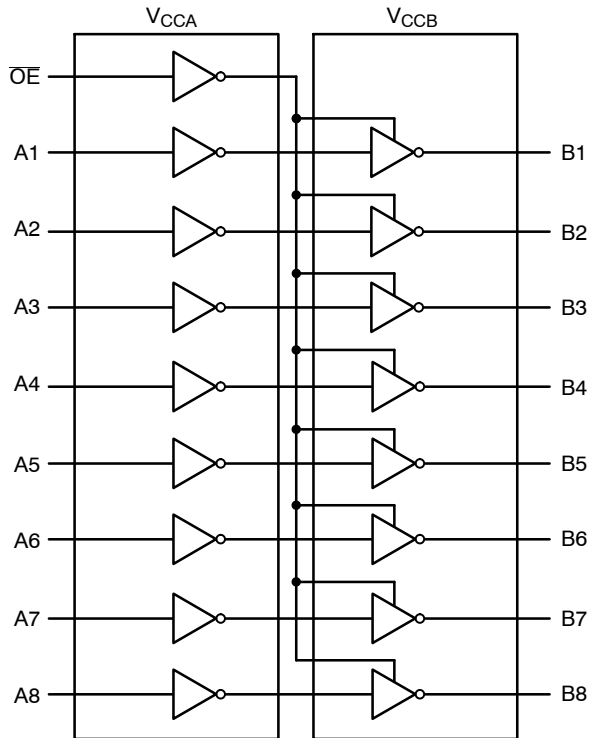


Figure 1. Logic Diagram

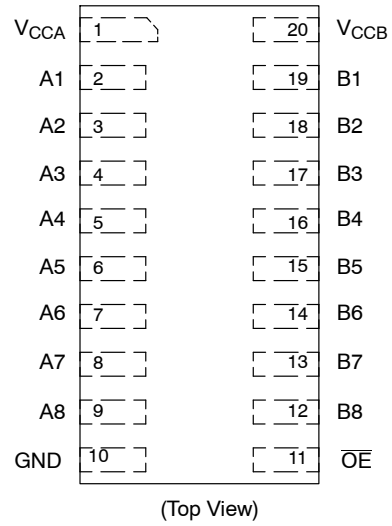


Figure 2. Pin Assignment

TRUTH TABLE

| Inputs | | Outputs |
|-----------------|-------|---------|
| \overline{OE} | A_n | B_n |
| L | L | L |
| L | H | H |
| H | X | 3-State |

PIN ASSIGNMENT

| PIN | FUNCTION |
|-----------------|-----------------------------|
| V_{CCA} | Input Port DC Power Supply |
| V_{CCB} | Output Port DC Power Supply |
| GND | Ground |
| A_n | Input Port |
| B_n | Output Port |
| \overline{OE} | Output Enable |

NLSV8T244

MAXIMUM RATINGS

| Symbol | Rating | Value | Condition | Unit |
|--------------------|--------------------------------------|--------------|-------------------------|-------------|
| V_{CCA}, V_{CCB} | DC Supply Voltage | -0.5 to +5.5 | | V |
| V_I | DC Input Voltage A_n | -0.5 to +5.5 | | V |
| V_C | Control Input \overline{OE} | -0.5 to +5.5 | | V |
| V_O | DC Output Voltage (Power Down) B_n | -0.5 to +5.5 | $V_{CCA} = V_{CCB} = 0$ | V |
| | (Active Mode) B_n | -0.5 to +5.5 | | V |
| | (Tri-State Mode) B_n | -0.5 to +5.5 | | V |
| I_{IK} | DC Input Diode Current | -20 | $V_I < GND$ | mA |
| I_{OK} | DC Output Diode Current | -50 | $V_O < GND$ | mA |
| I_O | DC Output Source/Sink Current | ± 50 | | mA |
| I_{CCA}, I_{CCB} | DC Supply Current Per Supply Pin | ± 100 | | mA |
| I_{GND} | DC Ground Current per Ground Pin | ± 100 | | mA |
| T_{STG} | Storage Temperature | -65 to +150 | | $^{\circ}C$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|-----------------------|---|-----|-----------|-------------|
| V_{CCA}, V_{CCB} | Positive DC Supply Voltage | 0.9 | 4.5 | V |
| V_I | Bus Input Voltage | GND | 4.5 | V |
| V_C | Control Input \overline{OE} | GND | 4.5 | V |
| V_{IO} | Bus Output Voltage (Power Down Mode) B_n | GND | 4.5 | V |
| | (Active Mode) B_n | GND | V_{CCB} | V |
| | (Tri-State Mode) B_n | GND | 4.5 | V |
| T_A | Operating Temperature Range | -40 | +85 | $^{\circ}C$ |
| $\Delta t / \Delta V$ | Input Transition Rise or Rate V_I , from 30% to 70% of V_{CC} ; $V_{CC} = 3.3 V \pm 0.3 V$ | 0 | 10 | nS |

NLSV8T244

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | V _{CCA} (V) | V _{CCB} (V) | -40°C to +85°C | | Unit |
|---|---|--|----------------------|----------------------|-------------------------|-------------------------|------|
| | | | | | Min | Max | |
| V _{IH} | Input HIGH Voltage (An, OE) | | 3.6 – 4.5 | 0.9 – 4.5 | 2.2 | – | V |
| | | | 2.7 – 3.6 | | 2.0 | – | |
| | | | 2.3 – 2.7 | | 1.6 | – | |
| | | | 1.4 – 2.3 | | 0.65 * V _{CCA} | – | |
| | | | 0.9 – 1.4 | | 0.9 * V _{CCA} | – | |
| V _{IL} | Input LOW Voltage (An, OE) | | 3.6 – 4.5 | 0.9 – 4.5 | – | 0.8 | V |
| | | | 2.7 – 3.6 | | – | 0.8 | |
| | | | 2.3 – 2.7 | | – | 0.7 | |
| | | | 1.4 – 2.3 | | – | 0.35 * V _{CCA} | |
| | | | 0.9 – 1.4 | | – | 0.1 * V _{CCA} | |
| V _{OH} | Output HIGH Voltage | I _{OH} = -100 μA; V _I = V _{IH} | 0.9 – 4.5 | 0.9 – 4.5 | V _{CCB} - 0.2 | – | V |
| | | I _{OH} = -0.5 mA; V _I = V _{IH} | 0.9 | 0.9 | 0.75 * V _{CCB} | – | |
| | | I _{OH} = -2 mA; V _I = V _{IH} | 1.4 | 1.4 | 1.05 | – | |
| | | I _{OH} = -6 mA; V _I = V _{IH} | 1.65 | 1.65 | 1.25 | – | |
| | | | 2.3 | 2.3 | 2.0 | – | |
| | | I _{OH} = -12 mA; V _I = V _{IH} | 2.3 | 2.3 | 1.8 | – | |
| | | | 2.7 | 2.7 | 2.2 | – | |
| | | I _{OH} = -18 mA; V _I = V _{IH} | 2.3 | 2.3 | 1.7 | – | |
| 3.0 | 3.0 | | 2.4 | – | | | |
| V _{OL} | Output LOW Voltage | I _{OL} = 100 μA; V _I = V _{IL} | 0.9 – 4.5 | 0.9 – 4.5 | – | 0.2 | V |
| | | I _{OL} = 0.5 mA; V _I = V _{IL} | 1.1 | 1.1 | – | 0.3 | |
| | | I _{OL} = 2 mA; V _I = V _{IL} | 1.4 | 1.4 | – | 0.35 | |
| | | I _{OL} = 6 mA; V _I = V _{IL} | 1.65 | 1.65 | – | 0.3 | |
| | | | 2.3 | 2.3 | – | 0.4 | |
| | | I _{OL} = 12 mA; V _I = V _{IL} | 2.7 | 2.7 | – | 0.4 | |
| | | | 2.3 | 2.3 | – | 0.6 | |
| | | 3.0 | 3.0 | – | 0.45 | | |
| I _{OL} = 24 mA; V _I = V _{IL} | 3.0 | 3.0 | – | 0.6 | | | |
| I _I | Input Leakage Current | V _I = V _{CCA} or GND | 0.9 – 4.5 | 0.9 – 4.5 | -1.0 | 1.0 | μA |
| I _{OFF} | Power-Off Leakage Current | OE = 0 V | 0 0.9 – 4.5 | 0.9 – 4.5 0 | -1.0 -1.0 | 1.0 1.0 | μA |
| I _{CCA} | Quiescent Supply Current | V _I = V _{CCA} or GND; I _O = 0, V _{CCA} = V _{CCB} | 0.9 – 4.5 | 0.9 – 4.5 | – | 2.0 | μA |
| I _{CCB} | Quiescent Supply Current | V _I = V _{CCA} or GND; I _O = 0, V _{CCA} = V _{CCB} | 0.9 – 4.5 | 0.9 – 4.5 | – | 2.0 | μA |
| I _{CCA} + I _{CCB} | Quiescent Supply Current | V _I = V _{CCA} or GND; I _O = 0, V _{CCA} = V _{CCB} | 0.9 – 4.5 | 0.9 – 4.5 | – | 4.0 | μA |
| ΔI _{CCA} | Increase in I _{CC} per Input Voltage, Other Inputs at V _{CCA} or GND | V _I = V _{CCA} - 0.6 V; V _I = V _{CCA} or GND | 4.5 | 4.5 | – | 10 | μA |
| | | | 3.6 | 3.6 | – | 5.0 | |
| ΔI _{CCB} | Increase in I _{CC} per Input Voltage, Other Inputs at V _{CCA} or GND | V _I = V _{CCA} - 0.6 V; V _I = V _{CCA} or GND | 4.5 | 4.5 | – | 10 | μA |
| | | | 3.6 | 3.6 | – | 5.0 | |
| I _{OZ} | I/O Tri-State Output Leakage Current | T _A = 25°C, OE = 0 V | 0.9 – 4.5 | 0.9 – 4.5 | -1.0 | 1.0 | μA |

NLSV8T244

TOTAL STATIC POWER CONSUMPTION ($I_{CCA} + I_{CCB}$)

| V_{CCA} (V) | -40°C to +85°C | | | | | | | | | | Unit |
|---------------|----------------|-------|-----|-------|-----|-------|-----|-------|-----|-------|---------|
| | V_{CCB} (V) | | | | | | | | | | |
| | 4.5 | | 3.3 | | 2.8 | | 1.8 | | 0.9 | | |
| | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| 4.5 | | 2 | | 2 | | 2 | | 2 | | < 1.5 | μ A |
| 3.3 | | 2 | | 2 | | 2 | | 2 | | < 1.5 | μ A |
| 2.8 | | < 2 | | < 1 | | < 1 | | < 0.5 | | < 0.5 | μ A |
| 1.8 | | < 1 | | < 1 | | < 0.5 | | < 0.5 | | < 0.5 | μ A |
| 0.9 | | < 0.5 | | < 0.5 | | < 0.5 | | < 0.5 | | < 0.5 | μ A |

NOTE: Connect ground before applying supply voltage V_{CCA} or V_{CCB} . This device is designed with the feature that the power-up sequence of V_{CCA} and V_{CCB} will not damage the IC.

AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | V_{CCA} (V) | -40°C to +85°C | | | | | | | | | | Unit |
|--|---|---------------|----------------|------|-----|------|-----|------|-----|------|-----|------|------|
| | | | V_{CCB} (V) | | | | | | | | | | |
| | | | 4.5 | | 3.3 | | 2.8 | | 1.8 | | 1.2 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{PLH} , t_{PHL} (Note 1) | Propagation Delay, A_n to B_n | 4.5 | | 1.6 | | 1.8 | | 2.0 | | 2.1 | | 2.3 | nS |
| | | 3.3 | | 1.7 | | 1.9 | | 2.1 | | 2.3 | | 2.6 | |
| | | 2.8 | | 1.9 | | 2.1 | | 2.3 | | 2.5 | | 2.8 | |
| | | 1.8 | | 2.1 | | 2.4 | | 2.5 | | 2.7 | | 3.0 | |
| | | 1.2 | | 2.4 | | 2.7 | | 2.8 | | 3.0 | | 3.3 | |
| t_{PZH} , t_{PZL} (Note 1) | Output Enable, \overline{OE} to B_n | 4.5 | | 2.6 | | 3.8 | | 4.0 | | 4.1 | | 4.3 | nS |
| | | 3.3 | | 3.7 | | 3.9 | | 4.1 | | 4.3 | | 4.6 | |
| | | 2.5 | | 3.9 | | 4.1 | | 4.3 | | 4.5 | | 4.8 | |
| | | 1.8 | | 4.1 | | 4.4 | | 4.5 | | 4.7 | | 5.0 | |
| | | 1.2 | | 4.4 | | 4.7 | | 4.8 | | 5.0 | | 5.3 | |
| t_{PHZ} , t_{PLZ} (Note 1) | Output Disable, \overline{OE} to B_n | 4.5 | | 2.6 | | 3.8 | | 4.0 | | 4.1 | | 4.3 | nS |
| | | 3.3 | | 3.7 | | 3.9 | | 4.1 | | 4.3 | | 4.6 | |
| | | 2.5 | | 3.9 | | 4.1 | | 4.3 | | 4.5 | | 4.8 | |
| | | 1.8 | | 4.1 | | 4.4 | | 4.5 | | 4.7 | | 5.0 | |
| | | 1.2 | | 4.4 | | 4.7 | | 4.8 | | 5.0 | | 5.3 | |
| t_{OSHL} , t_{OSLH} (Note 1) | Output to Output Skew, Time | 4.5 | | 0.15 | | 0.15 | | 0.15 | | 0.15 | | 0.15 | nS |
| | | 3.3 | | 0.15 | | 0.15 | | 0.15 | | 0.15 | | 0.15 | |
| | | 2.5 | | 0.15 | | 0.15 | | 0.15 | | 0.15 | | 0.15 | |
| | | 1.8 | | 0.15 | | 0.15 | | 0.15 | | 0.15 | | 0.15 | |
| | | 1.2 | | 0.15 | | 0.15 | | 0.15 | | 0.15 | | 0.15 | |

1. Propagation delays defined per Figure 3.

CAPACITANCE

| Symbol | Parameter | Test Conditions | Typ (Note 2) | Unit |
|-----------|-------------------------------|--|--------------|------|
| C_{IN} | Control Pin Input Capacitance | $V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or $V_{CCA/B}$ | 3.5 | pF |
| $C_{I/O}$ | I/O Pin Input Capacitance | $V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or $V_{CCA/B}$ | 5.0 | pF |
| C_{PD} | Power Dissipation Capacitance | $V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or V_{CCA} , $f = 10$ MHz | 20 | pF |

2. Typical values are at $T_A = +25^\circ\text{C}$.

3. C_{PD} is defined as the value of the IC's equivalent capacitance from which the operating current can be calculated from:
 $I_{CC(\text{operating})} \cong C_{PD} \times V_{CC} \times f_{IN} \times N_{SW}$ where $I_{CC} = I_{CCA} + I_{CCB}$ and N_{SW} = total number of outputs switching.

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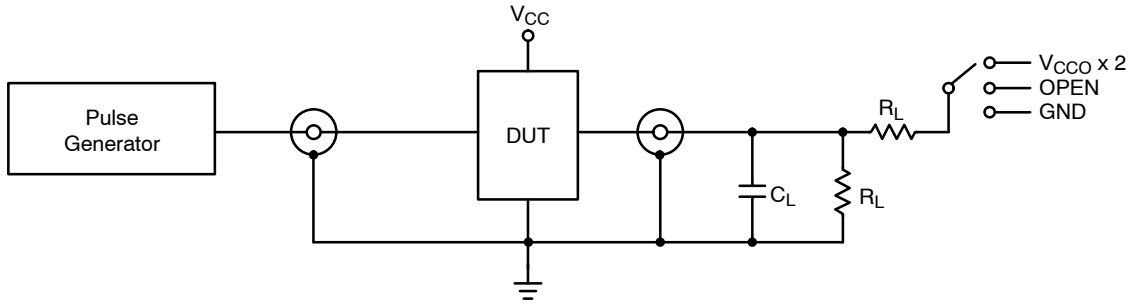
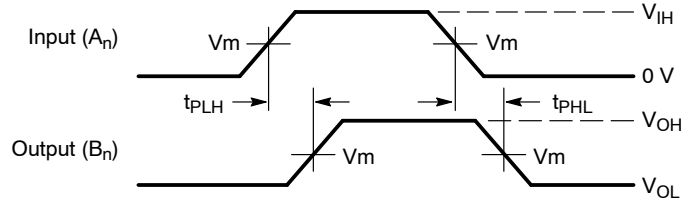


Figure 3. AC (Propagation Delay) Test Circuit

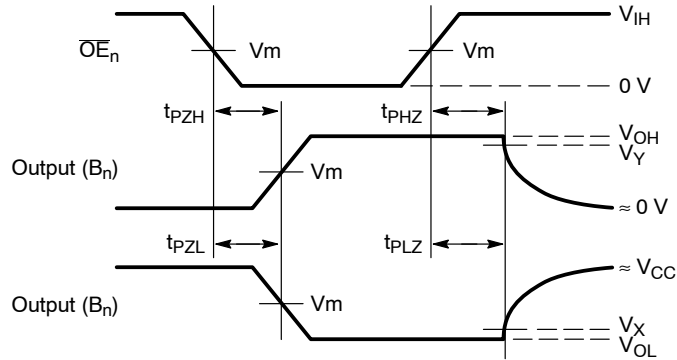
| Test | Switch |
|-----------------------|--------------------|
| t_{PLH} , t_{PHL} | OPEN |
| t_{PLZ} , t_{PZL} | $V_{CC0} \times 2$ |
| t_{PHZ} , t_{PZH} | GND |

$C_L = 15 \text{ pF}$ or equivalent (includes probe and jig capacitance)
 $R_L = 2 \text{ k}\Omega$ or equivalent
 Z_{OUT} of pulse generator = 50Ω



Waveform 1 - Propagation Delays

$t_R = t_F = 2.0 \text{ ns}$, 10% to 90%; $f = 1 \text{ MHz}$; $t_W = 500 \text{ ns}$



Waveform 2 - Output Enable and Disable Times

$t_R = t_F = 2.0 \text{ ns}$, 10% to 90%; $f = 1 \text{ MHz}$; $t_W = 500 \text{ ns}$

Figure 4. AC (Propagation Delay) Test Circuit Waveforms

| Symbol | V_{CC} | | | | |
|----------|---------------------|---------------------|---------------------|---------------------|---------------------|
| | 3.0 V – 4.5 V | 2.3 V – 2.7 V | 1.65 V – 1.95 V | 1.4 V – 1.6 V | 0.9 V – 1.3 V |
| V_{mA} | $V_{CCA}/2$ | $V_{CCA}/2$ | $V_{CCA}/2$ | $V_{CCA}/2$ | $V_{CCA}/2$ |
| V_{mB} | $V_{CCB}/2$ | $V_{CCB}/2$ | $V_{CCB}/2$ | $V_{CCB}/2$ | $V_{CCB}/2$ |
| V_X | $V_{OL} \times 0.1$ | $V_{OL} \times 0.1$ | $V_{OL} \times 0.1$ | $V_{OL} \times 0.1$ | $V_{OL} \times 0.1$ |
| V_Y | $V_{OH} \times 0.9$ | $V_{OH} \times 0.9$ | $V_{OH} \times 0.9$ | $V_{OH} \times 0.9$ | $V_{OH} \times 0.9$ |

NLSV8T244

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|----------------|-----------------------|-----------------------|
| NLSV8T244MUTAG | UQFN20 (Pb-Free) | 3000 / Tape & Reel |
| NLSV8T244DTR2G | TSSOP-20 (Pb-Free) | 2500 / Tape & Reel |
| NLSV8T244DWR2G | SOIC-20 (Pb-Free) | 1000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

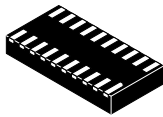
PACKAGE DIMENSIONS

ON Semiconductor®

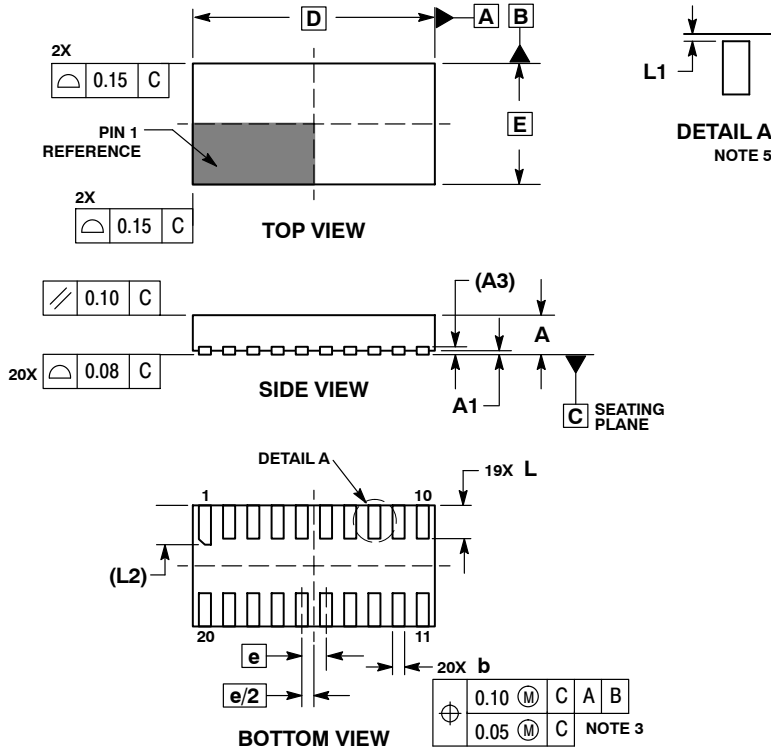


UDFN20 4x2, 0.4P
CASE 517AK-01
ISSUE O

DATE 14 NOV 2006



SCALE 4:1

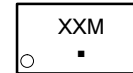


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH MAY NOT EXCEED 0.03 ONTO BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.45 | 0.55 |
| A1 | 0.00 | 0.05 |
| A3 | 0.13 REF | |
| b | 0.15 | 0.25 |
| D | 4.00 BSC | |
| E | 2.00 BSC | |
| e | 0.40 BSC | |
| L | 0.50 | 0.60 |
| L1 | 0.00 | 0.03 |
| L2 | 0.60 | 0.70 |

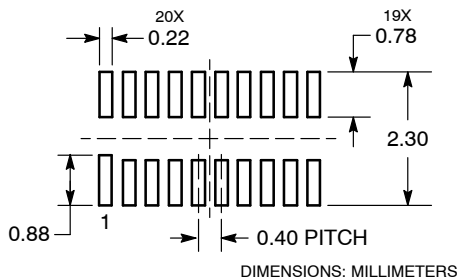
GENERIC MARKING DIAGRAM*



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

MOUNTING FOOTPRINT
SOLDERMASK DEFINED

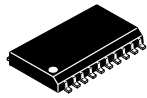


| | | |
|-------------------------|---------------------------|--|
| DOCUMENT NUMBER: | 98AON23419D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | UDFN20 4 X 2, 0.4P | PAGE 1 OF 1 |

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015

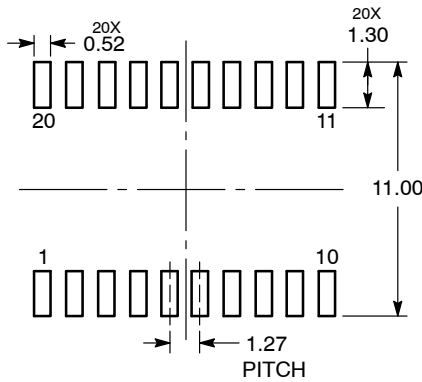


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

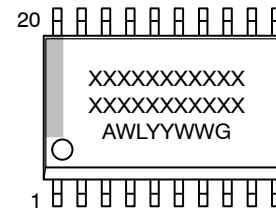
RECOMMENDED
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

| | | |
|------------------|-------------|--|
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| DESCRIPTION: | SOIC-20 WB | PAGE 1 OF 1 |

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



TSSOP-20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

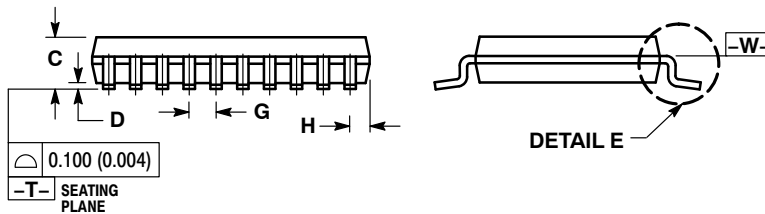
SCALE 2:1



NOTES:

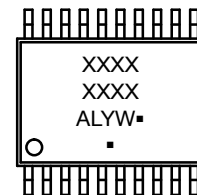
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |



SOLDERING FOOTPRINT

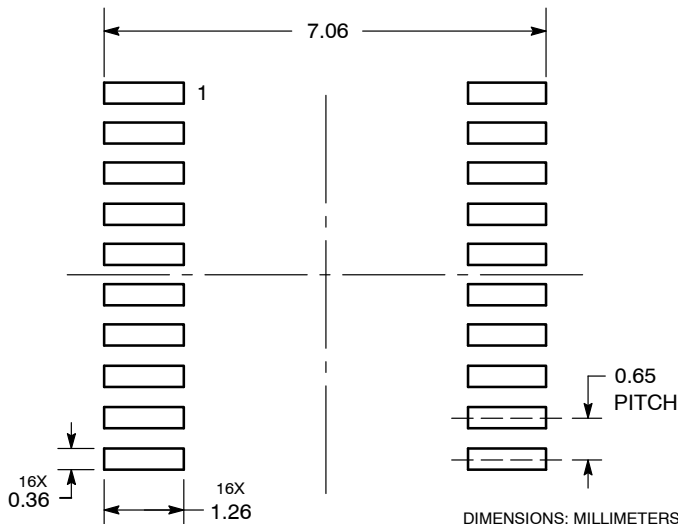
GENERIC MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.



DIMENSIONS: MILLIMETERS

| | | |
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