

# TL431A, B Series, NCV431A, B Series, SCV431A



ON Semiconductor®

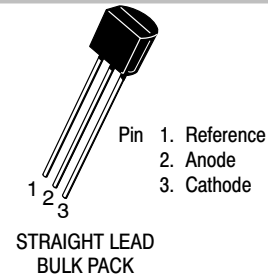
[www.onsemi.com](http://www.onsemi.com)

## Programmable Precision References

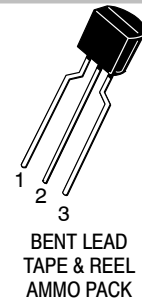
The TL431A, B integrated circuits are three-terminal programmable shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient zener which is programmable from  $V_{ref}$  to 36 V with two external resistors. These devices exhibit a wide operating current range of 1.0 mA to 100 mA with a typical dynamic impedance of 0.22  $\Omega$ . The characteristics of these references make them excellent replacements for zener diodes in many applications such as digital voltmeters, power supplies, and op amp circuitry. The 2.5 V reference makes it convenient to obtain a stable reference from 5.0 V logic supplies, and since the TL431A, B operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

### Features

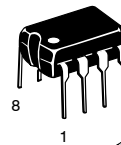
- Programmable Output Voltage to 36 V
- Voltage Reference Tolerance:  $\pm 0.4\%$ , Typ @ 25°C (TL431B)
- Low Dynamic Output Impedance, 0.22  $\Omega$  Typical
- Sink Current Capability of 1.0 mA to 100 mA
- Equivalent Full-Range Temperature Coefficient of 50 ppm/°C Typical
- Temperature Compensated for Operation over Full Rated Operating Temperature Range
- Low Output Noise Voltage
- NCV/SCV Prefixes for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



TO-92  
LP SUFFIX  
CASE 29-11



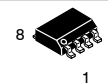
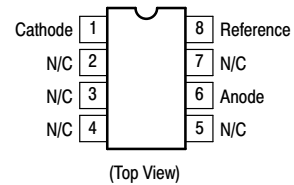
TO-92  
LPRA, LPRE, LPRM,  
LPRP SUFFIX  
CASE 29-11



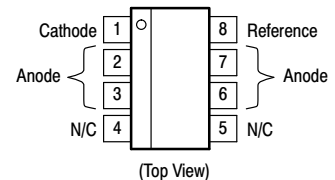
PDIP-8  
P SUFFIX  
CASE 626



Micro8™  
DM SUFFIX  
CASE 846A



SOIC-8  
D SUFFIX  
CASE 751



This is an internally modified SOIC-8 package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification increases power dissipation capability when appropriately mounted on a printed circuit board. This modified package conforms to all external dimensions of the standard SOIC-8 package.

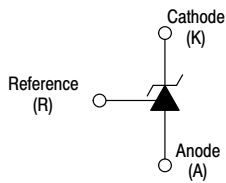
### ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

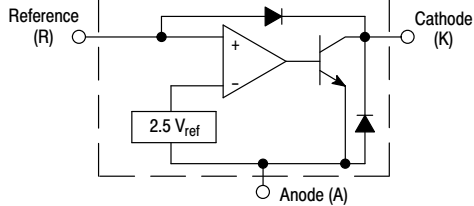
### DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 14 of this data sheet.

# TL431A, B Series, NCV431A, B Series, SCV431A

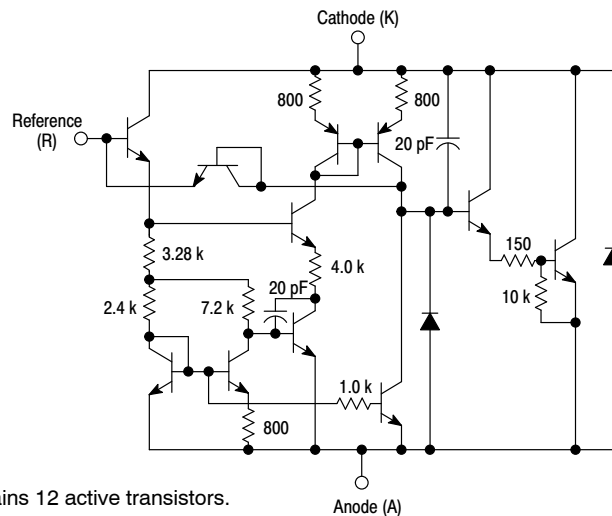


**Figure 1. Symbol**



**Figure 2. Representative Block Diagram**

This device contains 12 active transistors.



**Figure 3. Representative Schematic Diagram**

Component values are nominal

**MAXIMUM RATINGS** (Full operating ambient temperature range applies, unless otherwise noted.)

Rating	Symbol	Value	Unit
Cathode to Anode Voltage	$V_{KA}$	37	V
Cathode Current Range, Continuous	$I_K$	-100 to +150	mA
Reference Input Current Range, Continuous	$I_{ref}$	-0.05 to +10	mA
Operating Junction Temperature	$T_J$	150	°C
Operating Ambient Temperature Range	$T_A$		°C
TL431I, TL431AI, TL431BI		-40 to +85	
TL431C, TL431AC, TL431BC		0 to +70	
NCV431AI, NCV431B, TL431BV, SCV431AI		-40 to +125	
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C Ambient Temperature	$P_D$		W
D, LP Suffix Plastic Package		0.70	
P Suffix Plastic Package		1.10	
DM Suffix Plastic Package		0.52	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C Case Temperature	$P_D$		W
D, LP Suffix Plastic Package		1.5	
P Suffix Plastic Package		3.0	
ESD Rating (Note 1)			V
Human Body Model per JEDEC JESD22-A114F	HBM	>2000	
Machine Model per JEDEC JESD22-A115C	MM	>200	
Charged Device Model per JEDEC JESD22-C101E	CDM	>500	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device contains latch-up protection and exceeds  $\pm 100$  mA per JEDEC standard JESD78.

**RECOMMENDED OPERATING CONDITIONS**

Condition	Symbol	Min	Max	Unit
Cathode to Anode Voltage	$V_{KA}$	$V_{ref}$	36	V
Cathode Current	$I_K$	1.0	100	mA

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# TL431A, B Series, NCV431A, B Series, SCV431A

## THERMAL CHARACTERISTICS

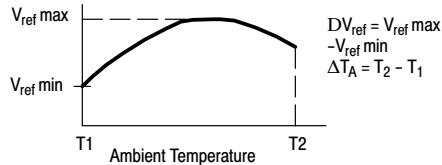
Characteristic	Symbol	D, LP Suffix Package	P Suffix Package	DM Suffix Package	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	178	114	240	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	83	41	-	$^{\circ}\text{C}/\text{W}$

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^{\circ}\text{C}$ , unless otherwise noted.)

Characteristic	Symbol	TL431I			TL431C			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Input Voltage (Figure 1) $V_{KA} = V_{ref}$ , $I_K = 10 \text{ mA}$ $T_A = 25^{\circ}\text{C}$ $T_A = T_{low}$ to $T_{high}$ (Note 2)	$V_{ref}$	2.44 2.41	2.495 -	2.55 2.58	2.44 2.423	2.495 -	2.55 2.567	V
Reference Input Voltage Deviation Over Temperature Range (Figure 1, Notes 3, 4) $V_{KA} = V_{ref}$ , $I_K = 10 \text{ mA}$	$\Delta V_{ref}$	-	7.0	30	-	3.0	17	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage $I_K = 10 \text{ mA}$ (Figure 2), $\Delta V_{KA} = 10 \text{ V}$ to $V_{ref}$ $\Delta V_{KA} = 36 \text{ V}$ to $10 \text{ V}$	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	- -	-1.4 -1.0	-2.7 -2.0	- -	-1.4 -1.0	-2.7 -2.0	mV/V
Reference Input Current (Figure 2) $I_K = 10 \text{ mA}$ , $R_1 = 10 \text{ k}$ , $R_2 = \infty$ $T_A = 25^{\circ}\text{C}$ $T_A = T_{low}$ to $T_{high}$ (Note 2)	$I_{ref}$	- -	1.8 -	4.0 6.5	- -	1.8 -	4.0 5.2	$\mu\text{A}$
Reference Input Current Deviation Over Temperature Range (Figure 2, Note 3) $I_K = 10 \text{ mA}$ , $R_1 = 10 \text{ k}$ , $R_2 = \infty$	$\Delta I_{ref}$	-	0.8	2.5	-	0.4	1.2	$\mu\text{A}$
Minimum Cathode Current For Regulation $V_{KA} = V_{ref}$ (Figure 1)	$I_{min}$	-	0.5	1.0	-	0.5	1.0	mA
Off-State Cathode Current (Figure 3) $V_{KA} = 36 \text{ V}$ , $V_{ref} = 0 \text{ V}$	$I_{off}$	-	20	1000	-	20	1000	nA
Dynamic Impedance (Figure 1, Note 5) $V_{KA} = V_{ref}$ , $\Delta I_K = 1.0 \text{ mA}$ to $100 \text{ mA}$ , $f \leq 1.0 \text{ kHz}$	$ Z_{KA} $	-	0.22	0.5	-	0.22	0.5	$\Omega$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- $T_{low} = -40^{\circ}\text{C}$  for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431AIDM, TL431IDM, TL431BIDM;  
 $= 0^{\circ}\text{C}$  for TL431ACP, TL431ACLP, TL431CP, TL431CLP, TL431CD, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM  
 $T_{high} = +85^{\circ}\text{C}$  for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431IDM, TL431AIDM, TL431BIDM  
 $= +70^{\circ}\text{C}$  for TL431ACP, TL431ACLP, TL431CP, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM
- Guaranteed by design.
- The deviation parameter  $\Delta V_{ref}$  is defined as the difference between the maximum and minimum values obtained over the full operating ambient temperature range that applies.



The average temperature coefficient of the reference input voltage,  $\alpha V_{ref}$  is defined as:

$$V_{ref} \frac{\text{ppm}}{^{\circ}\text{C}} = \frac{\left( \frac{\Delta V_{ref}}{V_{ref} @ 25^{\circ}\text{C}} \right) \times 10^6}{\Delta T_A} = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A (V_{ref} @ 25^{\circ}\text{C})}$$

$\alpha V_{ref}$  can be positive or negative depending on whether  $V_{ref} \text{ Min}$  or  $V_{ref} \text{ Max}$  occurs at the lower ambient temperature. (Refer to Figure 6.)

Example :  $\Delta V_{ref} = 8.0 \text{ mV}$  and slope is positive,

$$V_{ref} @ 25^{\circ}\text{C} = 2.495 \text{ V}, \Delta T_A = 70^{\circ}\text{C}$$

$$\alpha V_{ref} = \frac{0.008 \times 10^6}{70 (2.495)} = 45.8 \text{ ppm}/^{\circ}\text{C}$$

- The dynamic impedance  $Z_{KA}$  is defined as:  $|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_K}$ . When the device is programmed with two external resistors,  $R_1$  and  $R_2$ ,

(refer to Figure 2) the total dynamic impedance of the circuit is defined as:  $|Z_{KA}'| \approx |Z_{KA}| \left( 1 + \frac{R_1}{R_2} \right)$

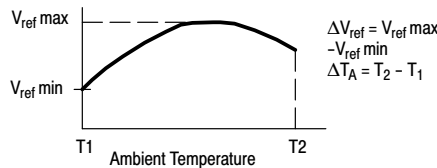
# TL431A, B Series, NCV431A, B Series, SCV431A

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C, unless otherwise noted.)

Characteristic	Symbol	TL431AI / NCV431AI/ SCV431AI			TL431AC			TL431BC / TL431BI / TL431BV / NCV431BV			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Input Voltage (Figure 1) V <sub>KA</sub> = V <sub>ref</sub> , I <sub>K</sub> = 10 mA T <sub>A</sub> = 25°C T <sub>A</sub> = T <sub>low</sub> to T <sub>high</sub> (Note 6)	V <sub>ref</sub>	2.47 2.44	2.495 –	2.52 2.55	2.47 2.453	2.495 –	2.52 2.537	2.485 2.475	2.495 2.495	2.505 2.515	V
Reference Input Voltage Deviation Over Temperature Range (Figure 1, Notes 7, 8) V <sub>KA</sub> = V <sub>ref</sub> , I <sub>K</sub> = 10 mA	ΔV <sub>ref</sub>	–	7.0	30	–	3.0	17	–	3.0	17	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage I <sub>K</sub> = 10 mA (Figure 2), ΔV <sub>KA</sub> = 10 V to V <sub>ref</sub> ΔV <sub>KA</sub> = 36 V to 10 V	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	–	–1.4 –1.0	–2.7 –2.0	–	–1.4 –1.0	–2.7 –2.0	–	–1.4 –1.0	–2.7 –2.0	mV/V
Reference Input Current (Figure 2) I <sub>K</sub> = 10 mA, R1 = 10 k, R2 = ∞ T <sub>A</sub> = 25°C T <sub>A</sub> = T <sub>low</sub> to T <sub>high</sub> (Note 6)	I <sub>ref</sub>	–	1.8 –	4.0 6.5	–	1.8 –	4.0 5.2	–	1.1 –	2.0 4.0	μA
Reference Input Current Deviation Over Temperature Range (Figure 2, Note 7) I <sub>K</sub> = 10 mA, R1 = 10 k, R2 = ∞	ΔI <sub>ref</sub>	–	0.8	2.5	–	0.4	1.2	–	0.8	2.5	μA
Minimum Cathode Current For Regulation V <sub>KA</sub> = V <sub>ref</sub> (Figure 1)	I <sub>min</sub>	–	0.5	1.0	–	0.5	1.0	–	0.5	1.0	mA
Off-State Cathode Current (Figure 3) V <sub>KA</sub> = 36 V, V <sub>ref</sub> = 0 V	I <sub>off</sub>	–	20	1000	–	20	1000	–	0.23	500	nA
Dynamic Impedance (Figure 1, Note 9) V <sub>KA</sub> = V <sub>ref</sub> , ΔI <sub>K</sub> = 1.0 mA to 100 mA f ≤ 1.0 kHz	Z <sub>KA</sub>	–	0.22	0.5	–	0.22	0.5	–	0.14	0.3	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. T<sub>low</sub> = –40°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431BV, TL431AIDM, TL431IDM, TL431BIDM, NCV431AIDMR2G, NCV431AIDR2G, NCV431BVDR2G, SCV431AIDMR2G  
 = 0°C for TL431ACP, TL431ACLP, TL431CP, TL431CLP, TL431CD, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM, SCV431AIDMR2G  
 T<sub>high</sub> = +85°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431IDM, TL431AIDM, TL431BIDM  
 = +70°C for TL431ACP, TL431ACLP, TL431CP, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM  
 = +125°C TL431BV, NCV431AIDMR2G, NCV431AIDR2G, NCV431BVDR2G, NCV431BVDR2G, SCV431AIDMR2G
7. Guaranteed by design.
8. The deviation parameter ΔV<sub>ref</sub> is defined as the difference between the maximum and minimum values obtained over the full operating ambient temperature range that applies.



The average temperature coefficient of the reference input voltage, αV<sub>ref</sub> is defined as:

$$V_{ref} \frac{\text{ppm}}{^{\circ}\text{C}} = \left( \frac{\Delta V_{ref}}{V_{ref} @ 25^{\circ}\text{C}} \right) \times 10^6 = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A (V_{ref} @ 25^{\circ}\text{C})}$$

αV<sub>ref</sub> can be positive or negative depending on whether V<sub>ref</sub> Min or V<sub>ref</sub> Max occurs at the lower ambient temperature. (Refer to Figure 6.)

Example : ΔV<sub>ref</sub> = 8.0 mV and slope is positive,

$$V_{ref} @ 25^{\circ}\text{C} = 2.495 \text{ V}, \Delta T_A = 70^{\circ}\text{C}$$

$$\alpha V_{ref} = \frac{0.008 \times 10^6}{70 (2.495)} = 45.8 \text{ ppm}/^{\circ}\text{C}$$

9. The dynamic impedance Z<sub>KA</sub> is defined as  $|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_K}$  When the device is programmed with two external resistors, R1 and R2, (refer

to Figure 2) the total dynamic impedance of the circuit is defined as:  $|Z_{KA}'| \approx |Z_{KA}| \left( 1 + \frac{R1}{R2} \right)$

10. NCV431AIDMR2G, NCV431AIDR2G, NCV431BVDR2G, NCV431BVDR2G, SCV431AIDMR2G T<sub>low</sub> = –40°C, T<sub>high</sub> = +125°C.  
 NCV prefix is for automotive and other applications requiring unique site and control change requirements.

# TL431A, B Series, NCV431A, B Series, SCV431A

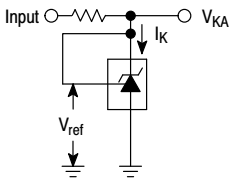


Figure 1. Test Circuit for  $V_{KA} = V_{ref}$

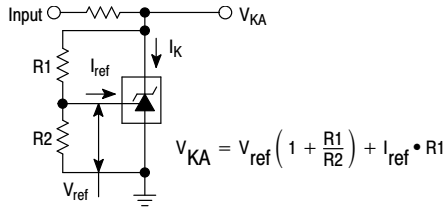


Figure 2. Test Circuit for  $V_{KA} > V_{ref}$

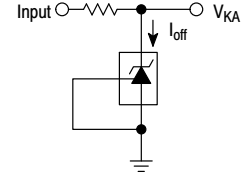


Figure 3. Test Circuit for  $I_{off}$

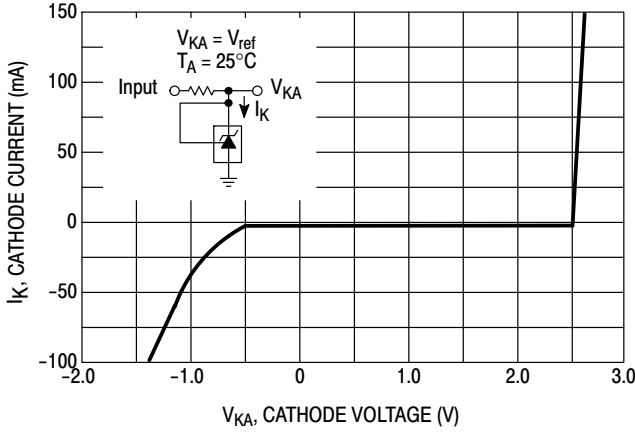


Figure 4. Cathode Current versus Cathode Voltage

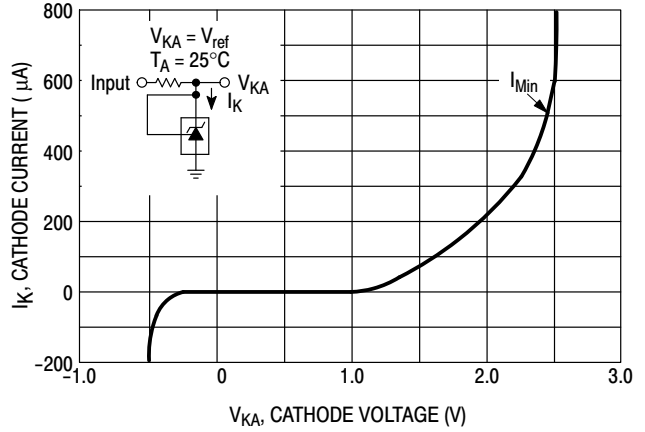


Figure 5. Cathode Current versus Cathode Voltage

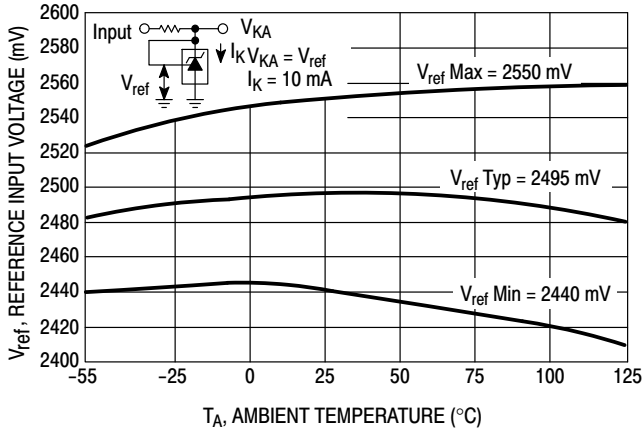


Figure 6. Reference Input Voltage versus Ambient Temperature

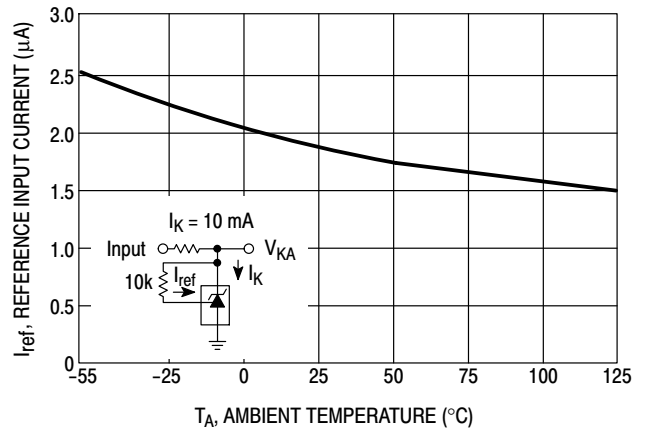
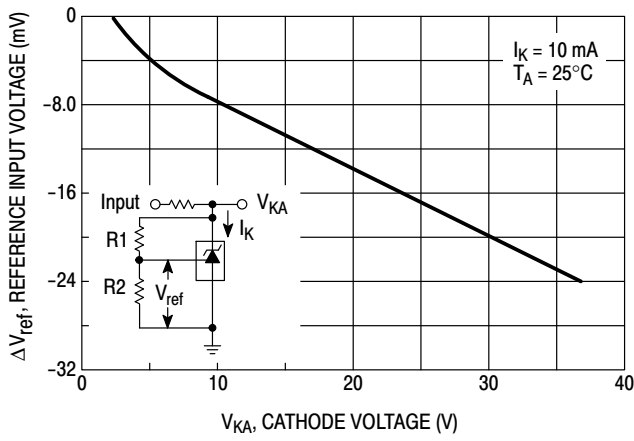
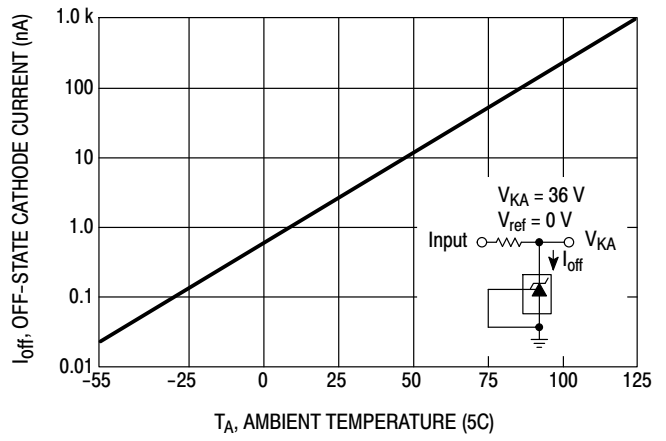


Figure 7. Reference Input Current versus Ambient Temperature

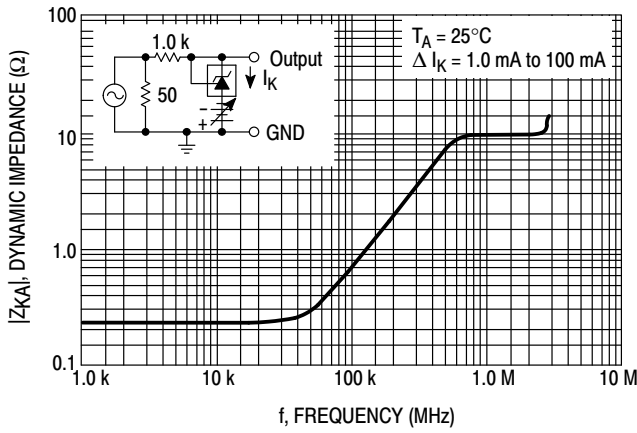
# TL431A, B Series, NCV431A, B Series, SCV431A



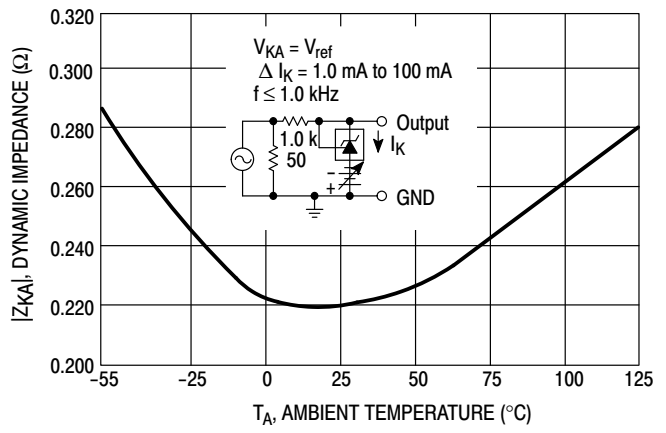
**Figure 8. Change in Reference Input Voltage versus Cathode Voltage**



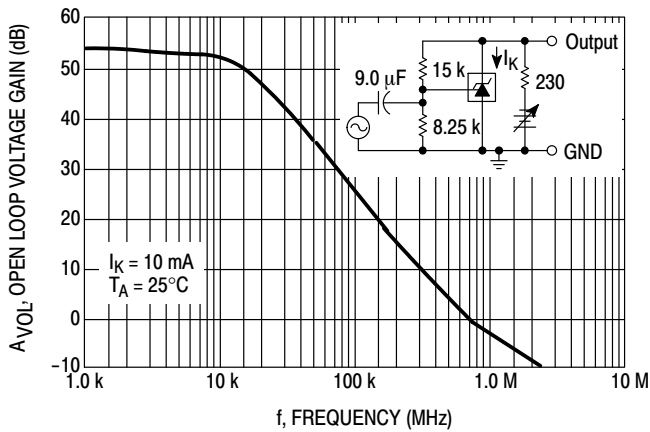
**Figure 9. Off-State Cathode Current versus Ambient Temperature**



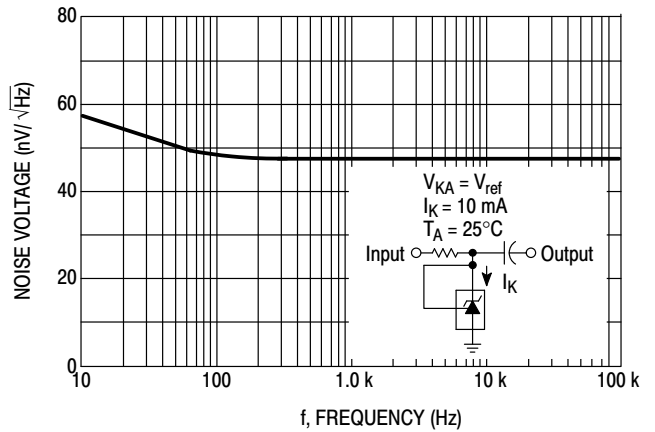
**Figure 10. Dynamic Impedance versus Frequency**



**Figure 11. Dynamic Impedance versus Ambient Temperature**



**Figure 12. Open-Loop Voltage Gain versus Frequency**



**Figure 13. Spectral Noise Density**

# TL431A, B Series, NCV431A, B Series, SCV431A

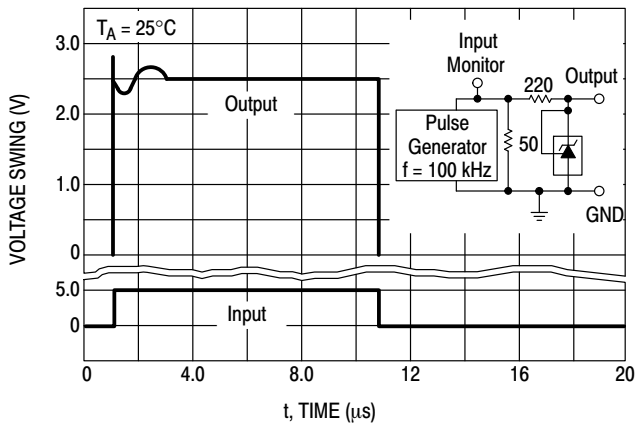


Figure 14. Pulse Response

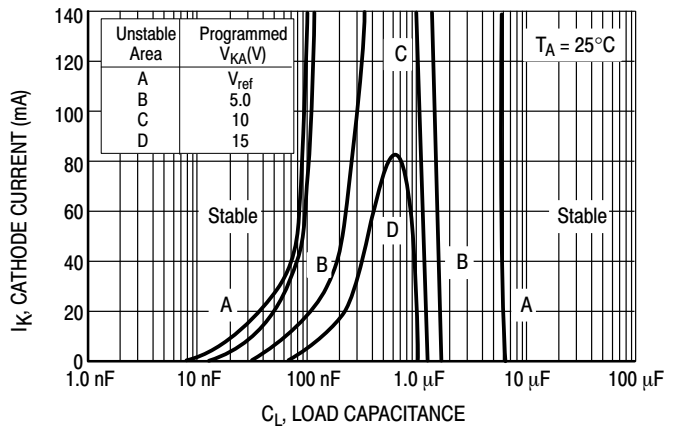


Figure 15. Stability Boundary Conditions

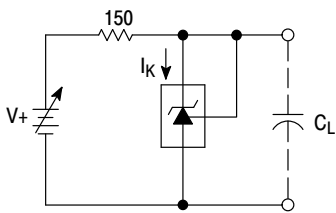


Figure 16. Test Circuit For Curve A of Stability Boundary Conditions

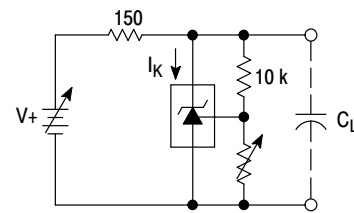


Figure 17. Test Circuit For Curves B, C, and D of Stability Boundary Conditions

## TYPICAL APPLICATIONS

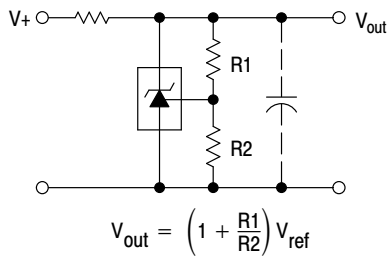


Figure 18. Shunt Regulator

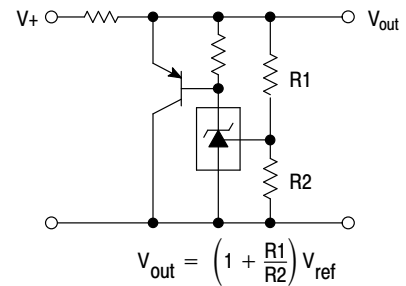


Figure 19. High Current Shunt Regulator

TL431A, B Series, NCV431A, B Series, SCV431A

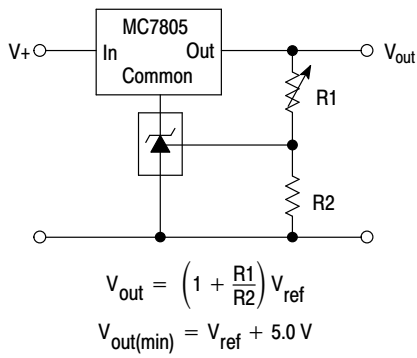


Figure 20. Output Control for a Three-Terminal Fixed Regulator

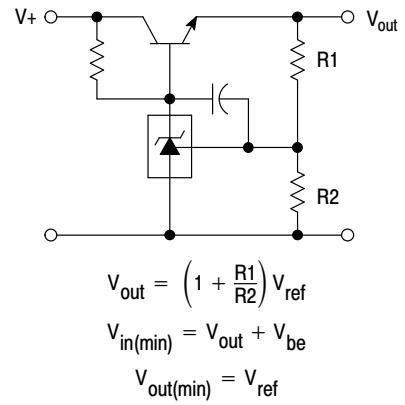


Figure 21. Series Pass Regulator

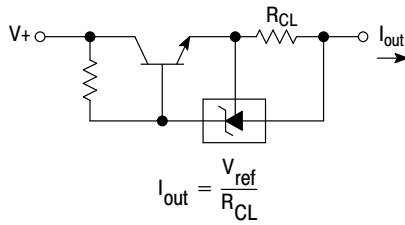


Figure 22. Constant Current Source

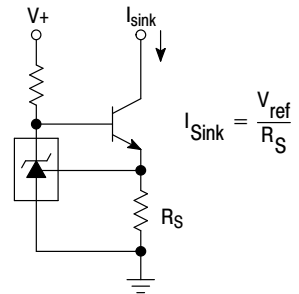


Figure 23. Constant Current Sink

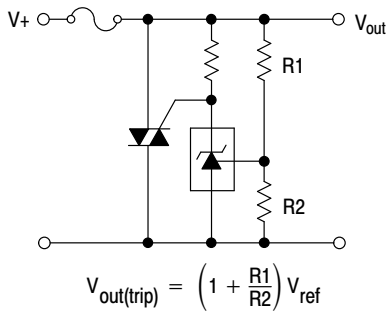


Figure 24. TRIAC Crowbar

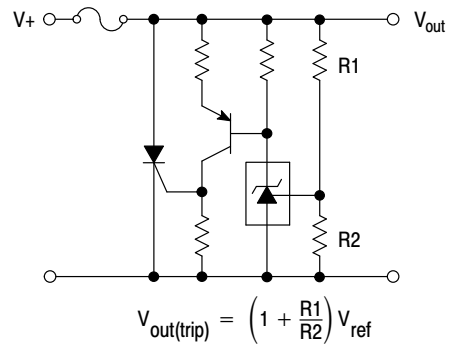
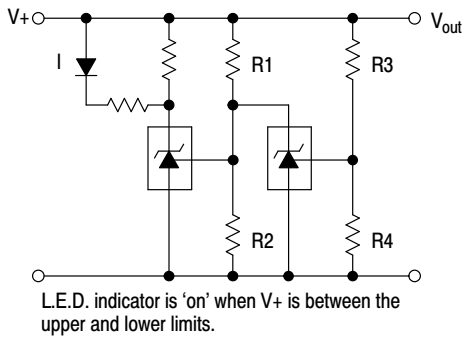


Figure 25. SRC Crowbar



TL431A, B Series, NCV431A, B Series, SCV431A



$$\text{Lower Limit} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

$$\text{Upper Limit} = \left(1 + \frac{R3}{R4}\right) V_{ref}$$

Figure 26. Voltage Monitor

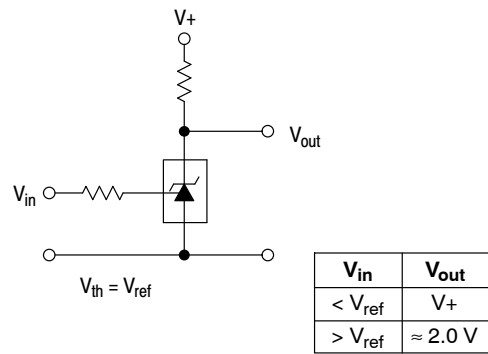


Figure 27. Single-Supply Comparator with Temperature-Compensated Threshold

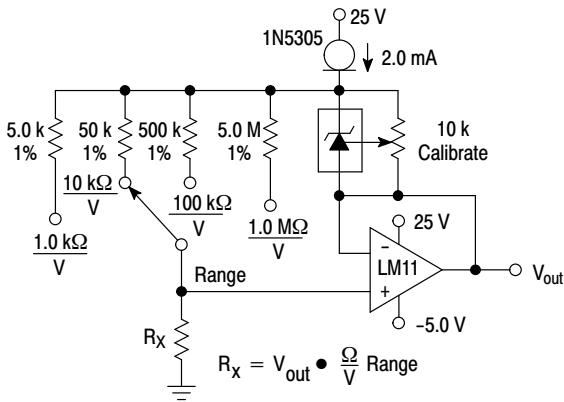


Figure 28. Linear Ohmmeter

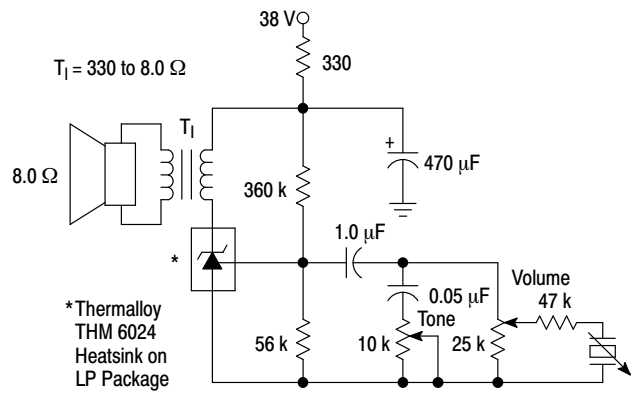


Figure 29. Simple 400 mW Phono Amplifier

# TL431A, B Series, NCV431A, B Series, SCV431A

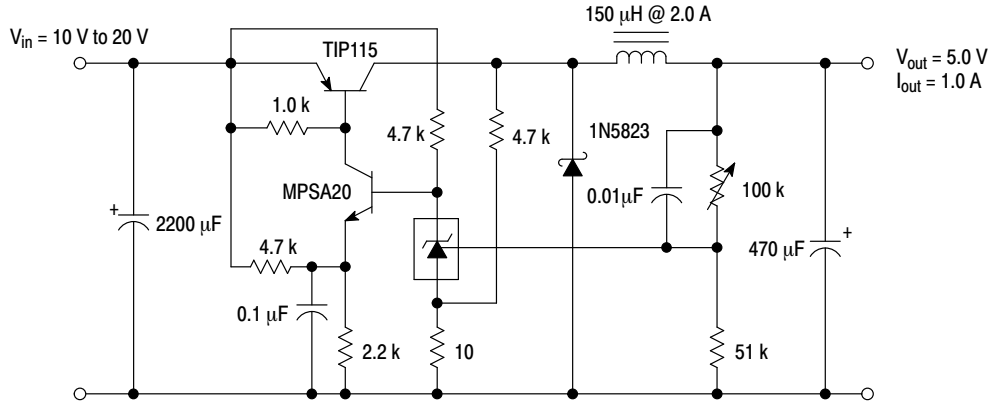


Figure 30. High Efficiency Step-Down Switching Converter

Test	Conditions	Results
Line Regulation	$V_{in} = 10\text{ V to } 20\text{ V}$ , $I_o = 1.0\text{ A}$	53 mV (1.1%)
Load Regulation	$V_{in} = 15\text{ V}$ , $I_o = 0\text{ A to } 1.0\text{ A}$	25 mV (0.5%)
Output Ripple	$V_{in} = 10\text{ V}$ , $I_o = 1.0\text{ A}$	50 mVpp P.A.R.D.
Output Ripple	$V_{in} = 20\text{ V}$ , $I_o = 1.0\text{ A}$	100 mVpp P.A.R.D.
Efficiency	$V_{in} = 15\text{ V}$ , $I_o = 1.0\text{ A}$	82%

APPLICATIONS INFORMATION

The TL431 is a programmable precision reference which is used in a variety of ways. It serves as a reference voltage in circuits where a non-standard reference voltage is needed. Other uses include feedback control for driving an optocoupler in power supplies, voltage monitor, constant current source, constant current sink and series pass regulator. In each of these applications, it is critical to maintain stability of the device at various operating currents and load capacitances. In some cases the circuit designer can estimate the stabilization capacitance from the stability boundary conditions curve provided in Figure 15. However, these typical curves only provide stability information at specific cathode voltages and at a specific load condition. Additional information is needed to determine the capacitance needed to optimize phase margin or allow for process variation.

A simplified model of the TL431 is shown in Figure 31. When tested for stability boundaries, the load resistance is 150 Ω. The model reference input consists of an input transistor and a dc emitter resistance connected to the device anode. A dependent current source, G<sub>m</sub>, develops a current whose amplitude is determined by the difference between the 1.78 V internal reference voltage source and the input transistor emitter voltage. A portion of G<sub>m</sub> flows through compensation capacitance, C<sub>p2</sub>. The voltage across C<sub>p2</sub> drives the output dependent current source, G<sub>o</sub>, which is connected across the device cathode and anode.

Model component values are:

$$V_{ref} = 1.78 \text{ V}$$

$$G_m = 0.3 + 2.7 \exp(-I_C/26 \text{ mA})$$

where I<sub>C</sub> is the device cathode current and G<sub>m</sub> is in mhos

$$G_o = 1.25 (V_{cp2}) \mu\text{mhos.}$$

Resistor and capacitor typical values are shown on the model. Process tolerances are ±20% for resistors, ±10% for capacitors, and ±40% for transconductances.

An examination of the device model reveals the location of circuit poles and zeroes:

$$P1 = \frac{1}{2\pi R_{GM} C_{P1}} = \frac{1}{2\pi * 1.0 \text{ M} * 20 \text{ pF}} = 7.96 \text{ kHz}$$

$$P2 = \frac{1}{2\pi R_{P2} C_{P2}} = \frac{1}{2\pi * 10 \text{ M} * 0.265 \text{ pF}} = 60 \text{ kHz}$$

$$Z1 = \frac{1}{2\pi R_{Z1} C_{P1}} = \frac{1}{2\pi * 15.9 \text{ k} * 20 \text{ pF}} = 500 \text{ kHz}$$

In addition, there is an external circuit pole defined by the load:

$$P_L = \frac{1}{2\pi R_L C_L}$$

Also, the transfer dc voltage gain of the TL431 is:

$$G = G_M R_{GM} G_o R_L$$

Example 1:

I<sub>C</sub> = 10 mA, R<sub>L</sub> = 230 Ω, C<sub>L</sub> = 0. Define the transfer gain.

The DC gain is:

$$G = G_M R_{GM} G_o R_L = (2.138)(1.0 \text{ M})(1.25 \mu)(230) = 615 = 56 \text{ dB}$$

$$\text{Loop gain} = G \frac{8.25 \text{ k}}{8.25 \text{ k} + 15 \text{ k}} = 218 = 47 \text{ dB}$$

The resulting transfer function Bode plot is shown in Figure 32. The asymptotic plot may be expressed as the following equation:

$$A_v = 615 \frac{\left(1 + \frac{jf}{500 \text{ kHz}}\right)}{\left(1 + \frac{jf}{8.0 \text{ kHz}}\right)\left(1 + \frac{jf}{60 \text{ kHz}}\right)}$$

The Bode plot shows a unity gain crossover frequency of approximately 600 kHz. The phase margin, calculated from the equation, would be 55.9 degrees. This model matches the Open-Loop Bode Plot of Figure 12. The total loop would have a unity gain frequency of about 300 kHz with a phase margin of about 44 degrees.

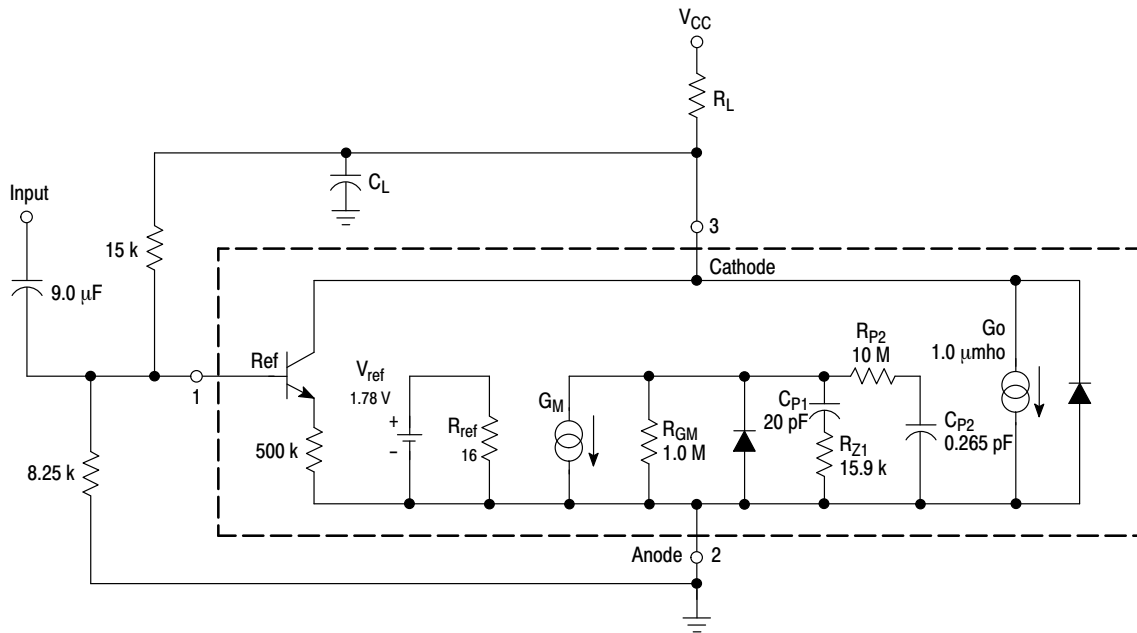


Figure 31. Simplified TL431 Device Model

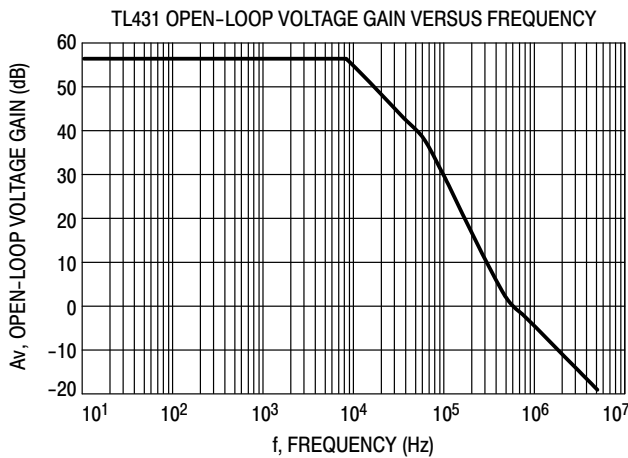


Figure 32. Example 1 Circuit Open Loop Gain Plot

Example 2.

$I_C = 7.5 \text{ mA}$ ,  $R_L = 2.2 \text{ k}\Omega$ ,  $C_L = 0.01 \text{ }\mu\text{F}$ . Cathode tied to reference input pin. An examination of the data sheet stability boundary curve (Figure 15) shows that this value of load capacitance and cathode current is on the boundary. Define the transfer gain.

The DC gain is:

$$G = G_M R_{GM} G_o R_L =$$

$$(2.323)(1.0 \text{ M})(1.25 \text{ }\mu)(2200) = 6389 = 76 \text{ dB}$$

The resulting open loop Bode plot is shown in Figure 33. The asymptotic plot may be expressed as the following equation:

$$A_v = 615 \frac{\left(1 + \frac{jf}{500 \text{ kHz}}\right)}{\left(1 + \frac{jf}{8.0 \text{ kHz}}\right)\left(1 + \frac{jf}{60 \text{ kHz}}\right)\left(1 + \frac{jf}{7.2 \text{ kHz}}\right)}$$

Note that the transfer function now has an extra pole formed by the load capacitance and load resistance.

Note that the crossover frequency in this case is about 250 kHz, having a phase margin of about -46 degrees. Therefore, instability of this circuit is likely.

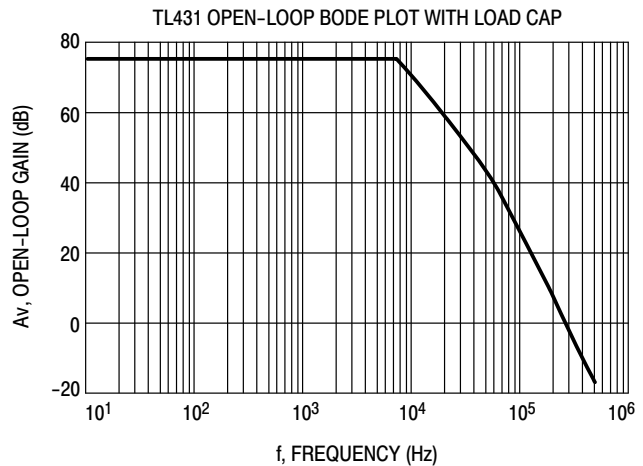


Figure 33. Example 2 Circuit Open Loop Gain Plot

With three poles, this system is unstable. The only hope for stabilizing this circuit is to add a zero. However, that can only be done by adding a series resistance to the output capacitance, which will reduce its effectiveness as a noise filter. Therefore, practically, in reference voltage applications, the best solution appears to be to use a smaller value of capacitance in low noise applications or a very large value to provide noise filtering and a dominant pole rolloff of the system.

# TL431A, B Series, NCV431A, B Series, SCV431A

## ORDERING INFORMATION

Device	Marking Code	Operating Temperature Range	Package Code	Shipping Information†	Tolerance	
TL431ACDG	AC	0°C to 70°C	SOIC-8 (Pb-Free)	98 Units / Rail	1.0%	
TL431BCDG	BC				0.4%	
TL431CDG	C				2.2%	
TL431ACDR2G	AC			2500 / Tape & Reel	1.0%	
TL431BCDR2G	BC				0.4%	
TL431CDR2G	C				2.2%	
TL431ACDMR2G	TAC		Micro8 (Pb-Free)	4000 / Tape & Reel	1.0%	
TL431BCDMR2G	TBC				0.4%	
TL431CDMR2G	T-C				2.2%	
TL431ACPG	ACP		PDIP-8 (Pb-Free)	50 Units / Rail	1.0%	
TL431BCPG	BCP				0.4%	
TL431CPG	CP				2.2%	
TL431ACLPG	ACLPG		TO-92 (Pb-Free)	2000 Units / Bag	1.0%	
TL431BCLPG	BCLPG				0.4%	
TL431CLPG	CLPG				2.2%	
TL431ACLPRAG	ACLPRAG			2000 / Tape & Reel	1.0%	
TL431BCLPRAG	BCLPRAG				0.4%	
TL431CLPRAG	CLPRAG				2.2%	
TL431ACLPRAG	ACLPRAG				1.0%	
TL431BCLPRAG	BCLPRAG				0.4%	
TL431CLPRAG	CLPRAG				2.2%	
TL431ACLPRAG	ACLPRAG			2000 / Tape & Ammo Box	1.0%	
TL431BCLPRAG	BCLPRAG				0.4%	
TL431CLPRAG	CLPRAG				2.2%	
TL431ACLPRAG	ACLPRAG	2000 / Fan-Fold	1.0%			
TL431BCLPRAG	BCLPRAG		0.4%			
TL431CLPRAG	CLPRAG		2.2%			
TL431AIDG	AI	-40°C to 85°C	SOIC-8 (Pb-Free)	98 Units / Rail	1.0%	
TL431BIDG	BI				0.4%	
TL431IDG	I				2.2%	
TL431AIDR2G	AI			2500s / Tape & Reel	1.0%	
TL431BIDR2G	BI				0.4%	
TL431IDR2G	I				2.2%	
TL431AIDMR2G	TAI		Micro8 (Pb-Free)	4000 / Tape & Reel	1.0%	
TL431BIDMR2G	TBI				0.4%	
TL431IDMR2G	T-I				2.2%	
TL431AIPG	AIP		PDIP-8 (Pb-Free)	50 Units / Rail	1.0%	
TL431BIPG	BIP				0.4%	
TL431IPG	IP				2.2%	
TL431AILPG	AILPG		TO-92 (Pb-Free)	2000 Units / Bag	1.0%	
TL431BILPG	BILPG				0.4%	
TL431ILPG	ILPG				2.2%	
TL431AILPRAG	AILPRAG			2000 / Tape & Reel	1.0%	
TL431BILPRAG	BILPRAG				0.4%	
SC431ILPRAG	ILPRAG				2.2%	
TL431ILPRAG	ILPRAG				1.0%	
TL431AILPRMG	AILP				2000 / Tape & Ammo Box	1.0%
TL431AILPRPG						1.0%
TL431ILPRPG	ILP			2.2%		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NCV/SCV Prefixes for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

# TL431A, B Series, NCV431A, B Series, SCV431A

## ORDERING INFORMATION

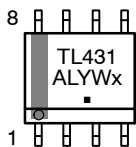
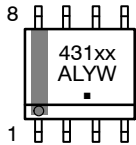
Device	Marking Code	Operating Temperature Range	Package Code	Shipping Information†	Tolerance
TL431BVDG	BV	-40°C to 125°C	SOIC-8 (Pb-Free)	98 Units / Rail	0.4%
TL431BVDR2G				2500 / Tape & Reel	
TL431BVDMR2G	TBV		Micro8 (Pb-Free)	4000 / Tape & Reel	
TL431BVLPG	BVLPG		TO-92 (Pb-Free)	2000 Units / Bag	
TL431BVLPRAG			2000 / Tape & Reel		
TL431BVPG	BVP		PDIP-8 (Pb-Free)	50 Units / Rail	
NCV431AIDMR2G*	RAN		Micro8 (Pb-Free)	4000 / Tape & Reel	1%
SCV431AIDMR2G*	RAP		SOIC-8 (Pb-Free)	2500 / Tape & Reel	
NCV431AIDR2G*	AV		Micro8 (Pb-Free)	4000 / Tape & Reel	0.4%
NCV431BVDMR2G*	NVB		SOIC-8 (Pb-Free)	2500 / Tape & Reel	
NCV431BVDR2G*	BV				

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NCV/SCV Prefixes for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

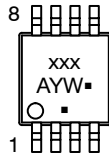
## MARKING DIAGRAMS

**SOIC-8  
D SUFFIX  
CASE 751**

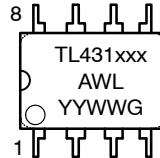


(Exception for the TL431CD and TL431ID only)

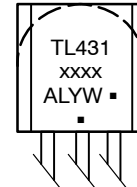
**Micro8  
CASE 846A**



**PDIP-8  
CASE 626**



**TO-92 (TO-226)  
CASE 29**



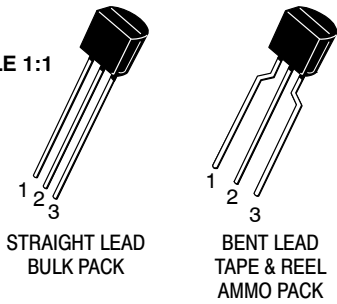
xxxx = See Specific Marking Code  
 A = Assembly Location  
 WL, L = Wafer Lot  
 YY, Y = Year  
 WW, W = Work Week  
 ■ or G = Pb-Free Package  
 (Note: Microdot may be in either location)

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1



TO-92 (TO-226)  
CASE 29-11  
ISSUE AM

DATE 09 MAR 2007



STRAIGHT LEAD  
BULK PACK



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---



BENT LEAD  
TAPE & REEL  
AMMO PACK



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	MILLIMETERS	
	MIN	MAX
A	4.45	5.20
B	4.32	5.33
C	3.18	4.19
D	0.40	0.54
G	2.40	2.80
J	0.39	0.50
K	12.70	---
N	2.04	2.66
P	1.50	4.00
R	2.93	---
V	3.43	---

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42022B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	TO-92 (TO-226)	PAGE 1 OF 3

**TO-92 (TO-226)**  
**CASE 29-11**  
**ISSUE AM**

DATE 09 MAR 2007

STYLE 1:  
 PIN 1. EMITTER  
 2. BASE  
 3. COLLECTOR

STYLE 2:  
 PIN 1. BASE  
 2. EMITTER  
 3. COLLECTOR

STYLE 3:  
 PIN 1. ANODE  
 2. ANODE  
 3. CATHODE

STYLE 4:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. ANODE

STYLE 5:  
 PIN 1. DRAIN  
 2. SOURCE  
 3. GATE

STYLE 6:  
 PIN 1. GATE  
 2. SOURCE & SUBSTRATE  
 3. DRAIN

STYLE 7:  
 PIN 1. SOURCE  
 2. DRAIN  
 3. GATE

STYLE 8:  
 PIN 1. DRAIN  
 2. GATE  
 3. SOURCE & SUBSTRATE

STYLE 9:  
 PIN 1. BASE 1  
 2. EMITTER  
 3. BASE 2

STYLE 10:  
 PIN 1. CATHODE  
 2. GATE  
 3. ANODE

STYLE 11:  
 PIN 1. ANODE  
 2. CATHODE & ANODE  
 3. CATHODE

STYLE 12:  
 PIN 1. MAIN TERMINAL 1  
 2. GATE  
 3. MAIN TERMINAL 2

STYLE 13:  
 PIN 1. ANODE 1  
 2. GATE  
 3. CATHODE 2

STYLE 14:  
 PIN 1. EMITTER  
 2. COLLECTOR  
 3. BASE

STYLE 15:  
 PIN 1. ANODE 1  
 2. CATHODE  
 3. ANODE 2

STYLE 16:  
 PIN 1. ANODE  
 2. GATE  
 3. CATHODE

STYLE 17:  
 PIN 1. COLLECTOR  
 2. BASE  
 3. EMITTER

STYLE 18:  
 PIN 1. ANODE  
 2. CATHODE  
 3. NOT CONNECTED

STYLE 19:  
 PIN 1. GATE  
 2. ANODE  
 3. CATHODE

STYLE 20:  
 PIN 1. NOT CONNECTED  
 2. CATHODE  
 3. ANODE

STYLE 21:  
 PIN 1. COLLECTOR  
 2. EMITTER  
 3. BASE

STYLE 22:  
 PIN 1. SOURCE  
 2. GATE  
 3. DRAIN

STYLE 23:  
 PIN 1. GATE  
 2. SOURCE  
 3. DRAIN

STYLE 24:  
 PIN 1. EMITTER  
 2. COLLECTOR/ANODE  
 3. CATHODE

STYLE 25:  
 PIN 1. MT 1  
 2. GATE  
 3. MT 2

STYLE 26:  
 PIN 1. V<sub>CC</sub>  
 2. GROUND 2  
 3. OUTPUT

STYLE 27:  
 PIN 1. MT  
 2. SUBSTRATE  
 3. MT

STYLE 28:  
 PIN 1. CATHODE  
 2. ANODE  
 3. GATE

STYLE 29:  
 PIN 1. NOT CONNECTED  
 2. ANODE  
 3. CATHODE

STYLE 30:  
 PIN 1. DRAIN  
 2. GATE  
 3. SOURCE

STYLE 31:  
 PIN 1. GATE  
 2. DRAIN  
 3. SOURCE

STYLE 32:  
 PIN 1. BASE  
 2. COLLECTOR  
 3. EMITTER

STYLE 33:  
 PIN 1. RETURN  
 2. INPUT  
 3. OUTPUT

STYLE 34:  
 PIN 1. INPUT  
 2. GROUND  
 3. LOGIC


STYLE 35:  
 PIN 1. GATE  
 2. COLLECTOR  
 3. EMITTER

<b>DOCUMENT NUMBER:</b>	<b>98ASB42022B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>STATUS:</b>	<b>ON SEMICONDUCTOR STANDARD</b>	
<b>NEW STANDARD:</b>		
<b>DESCRIPTION:</b>	<b>TO-92 (TO-226)</b>	<b>PAGE 2 OF 3</b>





ISSUE	REVISION	DATE
AM	ADDED BENT-LEAD TAPE & REEL VERSION. REQ. BY J. SUPINA.	09 MAR 2007

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

PDIP-8  
CASE 626-05  
ISSUE P

DATE 22 APR 2015



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	----	0.210	----	5.33
A1	0.015	----	0.38	----
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	----
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	----	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	----	10°

GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

- STYLE 1:  
PIN 1. AC IN  
2. DC + IN  
3. DC - IN  
4. AC IN  
5. GROUND  
6. OUTPUT  
7. AUXILIARY  
8. V<sub>CC</sub>

DOCUMENT NUMBER:	98ASB42420B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	PDIP-8	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

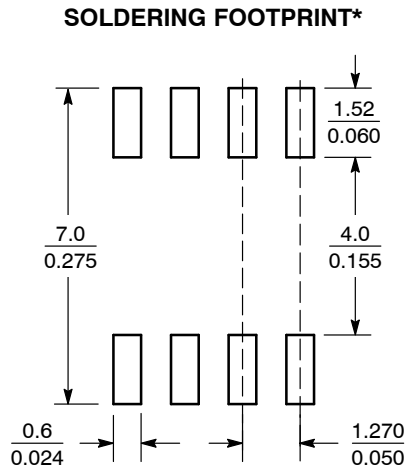
DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

## GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |  |   |   |   |
|--|---|---|---|
| <p><b>STYLE 1:</b><br/>         PIN 1. EMITTER<br/>         2. COLLECTOR<br/>         3. COLLECTOR<br/>         4. EMITTER<br/>         5. EMITTER<br/>         6. BASE<br/>         7. BASE<br/>         8. EMITTER</p>   | <p><b>STYLE 2:</b><br/>         PIN 1. COLLECTOR, DIE, #1<br/>         2. COLLECTOR, #1<br/>         3. COLLECTOR, #2<br/>         4. COLLECTOR, #2<br/>         5. BASE, #2<br/>         6. EMITTER, #2<br/>         7. BASE, #1<br/>         8. EMITTER, #1</p>               | <p><b>STYLE 3:</b><br/>         PIN 1. DRAIN, DIE #1<br/>         2. DRAIN, #1<br/>         3. DRAIN, #2<br/>         4. DRAIN, #2<br/>         5. GATE, #2<br/>         6. SOURCE, #2<br/>         7. GATE, #1<br/>         8. SOURCE, #1</p>                            | <p><b>STYLE 4:</b><br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. ANODE<br/>         4. ANODE<br/>         5. ANODE<br/>         6. ANODE<br/>         7. ANODE<br/>         8. COMMON CATHODE</p>   |
| <p><b>STYLE 5:</b><br/>         PIN 1. DRAIN<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. DRAIN<br/>         5. GATE<br/>         6. GATE<br/>         7. SOURCE<br/>         8. SOURCE</p>   | <p><b>STYLE 6:</b><br/>         PIN 1. SOURCE<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. SOURCE<br/>         5. SOURCE<br/>         6. GATE<br/>         7. GATE<br/>         8. SOURCE</p>  | <p><b>STYLE 7:</b><br/>         PIN 1. INPUT<br/>         2. EXTERNAL BYPASS<br/>         3. THIRD STAGE SOURCE<br/>         4. GROUND<br/>         5. DRAIN<br/>         6. GATE 3<br/>         7. SECOND STAGE Vd<br/>         8. FIRST STAGE Vd</p>                    | <p><b>STYLE 8:</b><br/>         PIN 1. COLLECTOR, DIE #1<br/>         2. BASE, #1<br/>         3. BASE, #2<br/>         4. COLLECTOR, #2<br/>         5. COLLECTOR, #2<br/>         6. EMITTER, #2<br/>         7. EMITTER, #1<br/>         8. COLLECTOR, #1</p>                              |
| <p><b>STYLE 9:</b><br/>         PIN 1. EMITTER, COMMON<br/>         2. COLLECTOR, DIE #1<br/>         3. COLLECTOR, DIE #2<br/>         4. EMITTER, COMMON<br/>         5. EMITTER, COMMON<br/>         6. BASE, DIE #2<br/>         7. BASE, DIE #1<br/>         8. EMITTER, COMMON</p> | <p><b>STYLE 10:</b><br/>         PIN 1. GROUND<br/>         2. BIAS 1<br/>         3. OUTPUT<br/>         4. GROUND<br/>         5. GROUND<br/>         6. BIAS 2<br/>         7. INPUT<br/>         8. GROUND</p>  | <p><b>STYLE 11:</b><br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. DRAIN 2<br/>         7. DRAIN 1<br/>         8. DRAIN 1</p>   | <p><b>STYLE 12:</b><br/>         PIN 1. SOURCE<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p><b>STYLE 13:</b><br/>         PIN 1. N.C.<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>  | <p><b>STYLE 14:</b><br/>         PIN 1. N-SOURCE<br/>         2. N-GATE<br/>         3. P-SOURCE<br/>         4. P-GATE<br/>         5. P-DRAIN<br/>         6. P-DRAIN<br/>         7. N-DRAIN<br/>         8. N-DRAIN</p>   | <p><b>STYLE 15:</b><br/>         PIN 1. ANODE 1<br/>         2. ANODE 1<br/>         3. ANODE 1<br/>         4. ANODE 1<br/>         5. CATHODE, COMMON<br/>         6. CATHODE, COMMON<br/>         7. CATHODE, COMMON<br/>         8. CATHODE, COMMON</p>               | <p><b>STYLE 16:</b><br/>         PIN 1. EMITTER, DIE #1<br/>         2. BASE, DIE #1<br/>         3. EMITTER, DIE #2<br/>         4. BASE, DIE #2<br/>         5. COLLECTOR, DIE #2<br/>         6. COLLECTOR, DIE #2<br/>         7. COLLECTOR, DIE #1<br/>         8. COLLECTOR, DIE #1</p> |
| <p><b>STYLE 17:</b><br/>         PIN 1. VCC<br/>         2. V2OUT<br/>         3. V1OUT<br/>         4. TXE<br/>         5. RXE<br/>         6. VEE<br/>         7. GND<br/>         8. ACC</p>  | <p><b>STYLE 18:</b><br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. CATHODE<br/>         8. CATHODE</p>   | <p><b>STYLE 19:</b><br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. MIRROR 2<br/>         7. DRAIN 1<br/>         8. MIRROR 1</p>   | <p><b>STYLE 20:</b><br/>         PIN 1. SOURCE (N)<br/>         2. GATE (N)<br/>         3. SOURCE (P)<br/>         4. GATE (P)<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p><b>STYLE 21:</b><br/>         PIN 1. CATHODE 1<br/>         2. CATHODE 2<br/>         3. CATHODE 3<br/>         4. CATHODE 4<br/>         5. CATHODE 5<br/>         6. COMMON ANODE<br/>         7. COMMON ANODE<br/>         8. CATHODE 6</p>  | <p><b>STYLE 22:</b><br/>         PIN 1. I/O LINE 1<br/>         2. COMMON CATHODE/VCC<br/>         3. COMMON CATHODE/VCC<br/>         4. I/O LINE 3<br/>         5. COMMON ANODE/GND<br/>         6. I/O LINE 4<br/>         7. I/O LINE 5<br/>         8. COMMON ANODE/GND</p> | <p><b>STYLE 23:</b><br/>         PIN 1. LINE 1 IN<br/>         2. COMMON ANODE/GND<br/>         3. COMMON ANODE/GND<br/>         4. LINE 2 IN<br/>         5. LINE 2 OUT<br/>         6. COMMON ANODE/GND<br/>         7. COMMON ANODE/GND<br/>         8. LINE 1 OUT</p> | <p><b>STYLE 24:</b><br/>         PIN 1. BASE<br/>         2. EMITTER<br/>         3. COLLECTOR/ANODE<br/>         4. COLLECTOR/ANODE<br/>         5. CATHODE<br/>         6. CATHODE<br/>         7. COLLECTOR/ANODE<br/>         8. COLLECTOR/ANODE</p>                                      |
| <p><b>STYLE 25:</b><br/>         PIN 1. VIN<br/>         2. N/C<br/>         3. REXT<br/>         4. GND<br/>         5. IOUT<br/>         6. IOUT<br/>         7. IOUT<br/>         8. IOUT</p>   | <p><b>STYLE 26:</b><br/>         PIN 1. GND<br/>         2. dv/dt<br/>         3. ENABLE<br/>         4. ILIMIT<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. VCC</p>  | <p><b>STYLE 27:</b><br/>         PIN 1. ILIMIT<br/>         2. OVLO<br/>         3. UVLO<br/>         4. INPUT+<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. DRAIN</p>  | <p><b>STYLE 28:</b><br/>         PIN 1. SW_TO_GND<br/>         2. DASIC OFF<br/>         3. DASIC_SW_DET<br/>         4. GND<br/>         5. V_MON<br/>         6. VBULK<br/>         7. VBULK<br/>         8. VIN</p>  |
| <p><b>STYLE 29:</b><br/>         PIN 1. BASE, DIE #1<br/>         2. EMITTER, #1<br/>         3. BASE, #2<br/>         4. EMITTER, #2<br/>         5. COLLECTOR, #2<br/>         6. COLLECTOR, #2<br/>         7. COLLECTOR, #1<br/>         8. COLLECTOR, #1</p>                        | <p><b>STYLE 30:</b><br/>         PIN 1. DRAIN 1<br/>         2. DRAIN 1<br/>         3. GATE 2<br/>         4. SOURCE 2<br/>         5. SOURCE 1/DRAIN 2<br/>         6. SOURCE 1/DRAIN 2<br/>         7. SOURCE 1/DRAIN 2<br/>         8. GATE 1</p>                           |   |   |

<b>DOCUMENT NUMBER:</b>	<b>98ASB42564B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SOIC-8 NB</b>	<b>PAGE 2 OF 2</b>

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 2:1

### Micro8 CASE 846A-02 ISSUE K

DATE 16 JUL 2020



TOP VIEW

NOTE 3



SIDE VIEW



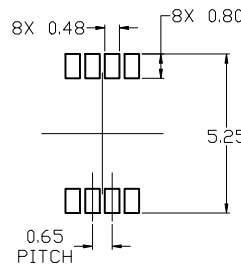
END VIEW

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS *D* AND *E* DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION *E* DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS *D* AND *E* ARE DETERMINED AT DATUM *F*.
5. DATUMS *A* AND *B* ARE TO BE DETERMINED AT DATUM *F*.
6. *A1* IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

⌀ 0.08 (0.003) M C B S A S

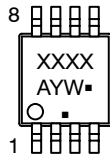
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
<i>b</i>	0.25	0.33	0.40
<i>c</i>	0.13	0.18	0.23
<i>D</i>	2.90	3.00	3.10
<i>E</i>	2.90	3.00	3.10
<i>e</i>	0.65 BSC		
<i>H<sub>E</sub></i>	4.75	4.90	5.05
<i>L</i>	0.40	0.55	0.70



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

### GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**STYLE 1:**

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

**STYLE 2:**

1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

**STYLE 3:**

1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

<b>DOCUMENT NUMBER:</b>	<b>98ASB14087C</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>MICRO8</b>	<b>PAGE 1 OF 1</b>

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

ON Semiconductor Website: [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

North American Technical Support:  
Voice Mail: 1 800-282-9855 Toll Free USA/Canada  
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative