EV13L63A

PL460-EK User Guide

Introduction

PL460-EK (EV13L63A) is an Xplained PRO extension board featuring a PL460 modem that embeds a PLC signal amplification stage, providing a highly integrated solution that reduces the total bill of materials, simplifies the layout and eases the modem design. This board enables the user to evaluate the PL460 device performance.

The PL460 was conceived to be driven by external Microchip host devices, thus providing an additional level of flexibility on the host side. The Microchip host device loads the proper PLC-protocol firmware in the PL460, then controls the modem operation. PL460-EK uses an Xplained PRO client connector to communicate with the host microcontroller (i.e., PIC32CXMT family of EK/DBs, SAM4CMx-DB family, SAME70-Xplained or SAMG55-Xplained boards).

The PL460-EK is a client companion board for the PIC32CXMT family of EK/DBs, SAM4CMx-DB family, SAME70-Xplained and SAMG55-Xplained boards. All these boards include an Xplained PRO (host) connector, and the PL460-EK includes an Xplained PRO connector accordingly (client).

Contents

- One PL460-EK board in an enclosure
- One Power Supply adapter (AC/DC) 15 Vdc with interchangeable plugs

Features

- The PL460-EK board includes a PL460, a programmable modem for narrow-band Power Line Communication (PLC), able to run any PLC protocol in the frequency band below 500 kHz.
- The PL460-EK board implements a PLC multiband configuration: in FCC band, using the main transmission branch with the embedded PLC driver and CENELEC A-Band using the auxiliary transmission branch with discrete components.
- Client Xplained PRO header connector (J2) to interface with other boards.
- The PL460-EK board needs two different power supplies. One power supply of 3.3V coming from the Xplained PRO header connector (J2) and the other one of 15V coming from the DC Jack connector (J4).

Figure 1. PL460-EK

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1. Evaluation Kit Specifications

1.1 Safety Recommendations

The Evaluation Board is intended for further engineering, development, demonstration or evaluation purposes only and is not for commercial use. Therefore, the evaluation board is not fault tolerant and is not designed or manufactured with protective considerations, including but not limited to product safety measures typically found in finished commercial goods.

When the board is connected to mains grid for PLC communication, there is a risk of PERSONAL INJURY, DEATH OR PHYSICAL DAMAGE. Therefore, caution must be exercised when testing these devices. The user must be a skilled person in the practice and art of high voltage circuitry to utilize the circuits in the board. It is highly recommended that the user have qualifications or any certificate for handling AC Power; COMMON SENSE IS ENCOURAGED. The user agrees not to use the board in any situation where damage or injury to persons, property or business could occur. Furthermore, the board is NOT FOR RESALE/COMMERCIAL USE AND MUST BE STRICTLY OPERATED IN A WELL-CONTROLLED LABORATORY ENVIRONMENTS.

> **⚠ DANGER** Not all the board is isolated from mains (PLC Signal). To avoid damage of instruments, do not connect any probe (i.e., debugger, oscilloscopes) to the non-isolated area of the board when the board is connected to mains.
>
> The PLC Signal is identified in the enclosure with this symbol: ⚡.

> **⚠ WARNING** To avoid user access to dangerous parts, PL460-EK must always be used within its enclosure. DC Jack and Xplained PRO connectors are accessible without electrical shock risk due to provided electrical isolation.

> **⚠ WARNING** The socket-outlet is easily accessible.

For any hardware components and/or jumper configuration changes, it is required to switch off the board and disconnect it from the electrical network.

The board must not be subjected to high electrostatic potentials.

> **Tip:** It is strongly recommended to use a grounding strap or similar ESD protective device when handling the board in hostile ESD environments (offices with synthetic carpet, for example). Avoid touching the component pins or any other metallic element on the board.

> **Important:** Microchip does not assume any responsibility for the consequences arising from any improper use of this board.

1.2   Electrical and Board Characteristics

This section contains information about the PL460-EK power supply requirements and consumption. Additionally, this section contains a table with the main board characteristics.

The PL460-EK board has two voltage supplies:
- +3.3V from Xplained PRO connector to power the low voltage domain of PL460
- +15V from the DC jack to power the PL460 amplification stage

Table 1-1. Power Supply Requirements

Electrical Parameter	Power Source	Value
Input Voltage	DC Jack Connector, J4	15 Vdc
Input Voltage	Xplained PRO Connector, J2 (Pin 20)	3.3V
Input Voltage	PLC Connector, J1	0 – 250 Vac, 47 – 63 Hz
Input Voltage	PLC Connector, J1	0 – 325 Vdc

For more details about the power supply system, refer to 3.3.5. Power Supply System.

Table 1-2. Power Consumption

Parameter	Condition	Typ.[1]	Unit
RX Power Consumption	Measured at FB3 (3.3V)	230	mW
TX Power Consumption	Measured at FB3 (3.3V)	280	
	Measured at J5 (12V)	2040	

Note:
1. These measurements were taken running the PHY TX Test Console project with a default configuration in TX and RX modes.

Table 1-3. Board Characteristics

Characteristic	Specification
Operating Temperature	-40 °C to +85 °C
Board Dimensions	134.88 mm x 56.6 mm
RoHS Status	RoHS 3 Compliant
China RoHS Status	EFUP50
REACH Status	REACH Compliant

2.   Getting Started

Unpack and inspect the kit carefully. The board is inside an enclosure made of ABS plastic UL 94 V-0 (150 mm x 80 mm x 50 mm).

Figure 2-1. PL460-EK Unpacked

The PL460-EK is a client board, so a host board with a specific firmware is necessary to use it. The PL460-EK must be connected to the host through the Xplained PRO connector (J2).

The PL460-EK must be powered with 15V by the DC Input connector (J4) and with 3.3V by the Xplained PRO connector (J2).

- When the DC Input connector (J4) is connected, the power LED shines green.
- When the Xplained PRO connector (J2) is connected, the power LED shines green.

> ⚠ **CAUTION** Before starting to transmit, make sure that the 12V power supply is applied and stable to avoid damaging the driver. So, the DC Input connector must be connected and the shunt JP1 must be installed on J5.

For more information about the power supply of PL460-EK, see 3.3.5. Power Supply System.

To connect a host or the AC/DC wall adapter to J4, it is not necessary to open the enclosure.

Figure 2-2. Connection of AC/DC Wall Adapter and Host

The PL460-EK requires a suitable cable to be connected from the connector J1 to the mains for the PLC communication. It is necessary to open the enclosure to connect an AC power source (mains grid) or a DC bus to the J1 connector (PLC output). Once the connection is made, remember to close the enclosure before connecting it to the mains.

To make the connection with the PLC, follow the next steps to open the enclosure securely:

1. Unscrew the four screws of the lid to open the enclosure.

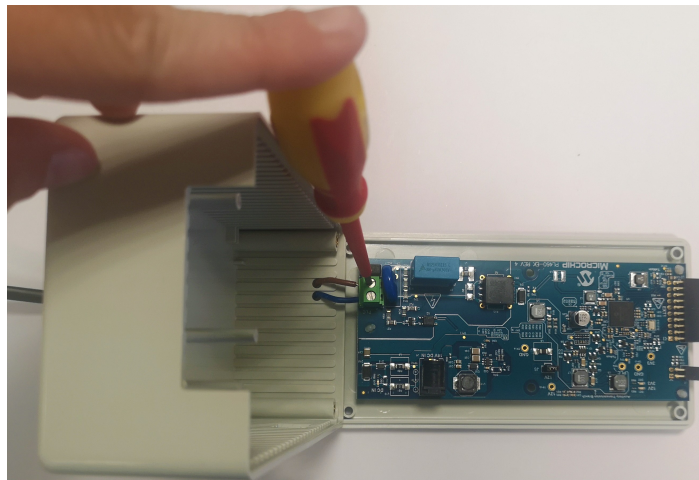   **Figure 2-3. Screws of the Lid to Open the Enclosure**

2. Feed the cables through the holes of the enclosure.

    Figure 2-4. Cables through the Holes of the Enclosure

3. Connect one wire of the 2-wire AC cable to any of the terminals of the J1 connector (PLC+) and the other wire to the other terminal of the J1 connector (PLC-). Screw the wires into the connector.

    Figure 2-5. Screw Wires into the Connector

4. Close the enclosure and screw the four screws of the lid.

Figure 2-6. Screws of the Lid to Close the Enclosure

Once the enclosure is closed, the AC cable can be connected to the mains grid.

Figure 2-7. PL460-EK Powered from Mains Grid with Closed Enclosure

Also, the host can be connected to the board through the Xplained PRO connector and the AC/DC wall adapter can be connected to the mains grid.

Figure 2-8. Connection of PLC, AC/DC Wall Adapter and Host

> ⚠ **WARNING**   When the board is connected to the mains grid for PLC communication, there is a risk of PERSONAL INJURY OR PHYSICAL DAMAGE. Make sure that the enclosure is closed before connecting the board to the mains grid and do not open the lid.

> **Important:** For proper PLC communication, it is necessary to open the enclosure and make the corresponding connection following the steps described in the above section. Once this is done, the enclosure must be closed at any time while PL460-EK is connected to the mains. If, for any reason, it is needed to manipulate the board, make sure that the board is disconnected from the mains before opening the enclosure.

2.1   Technical Support

Note that the latest documentation and support materials are available on www.microchip.com.

For any technical support requests, visit support.microchip.com.

3.   PL460-EK Board

3.1   Overview

This section summarizes the PL460-EK board design. It provides system-level concepts, such as power supply, MCU, PLC coupling, peripherals and board interfaces.

Figure 3-1. PL460-EK Board Description
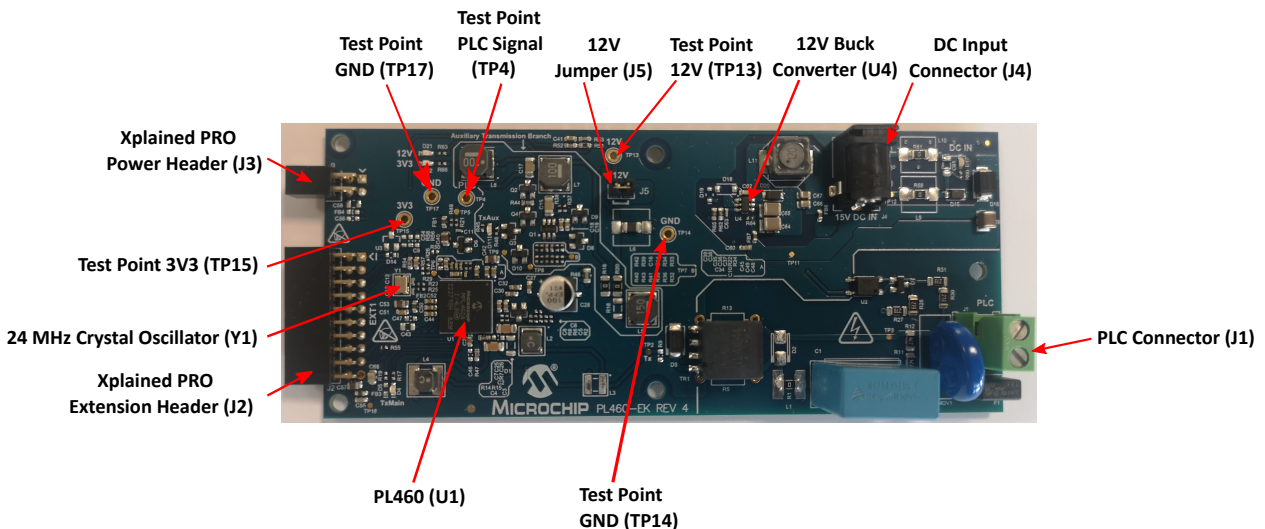
3.2   Features List

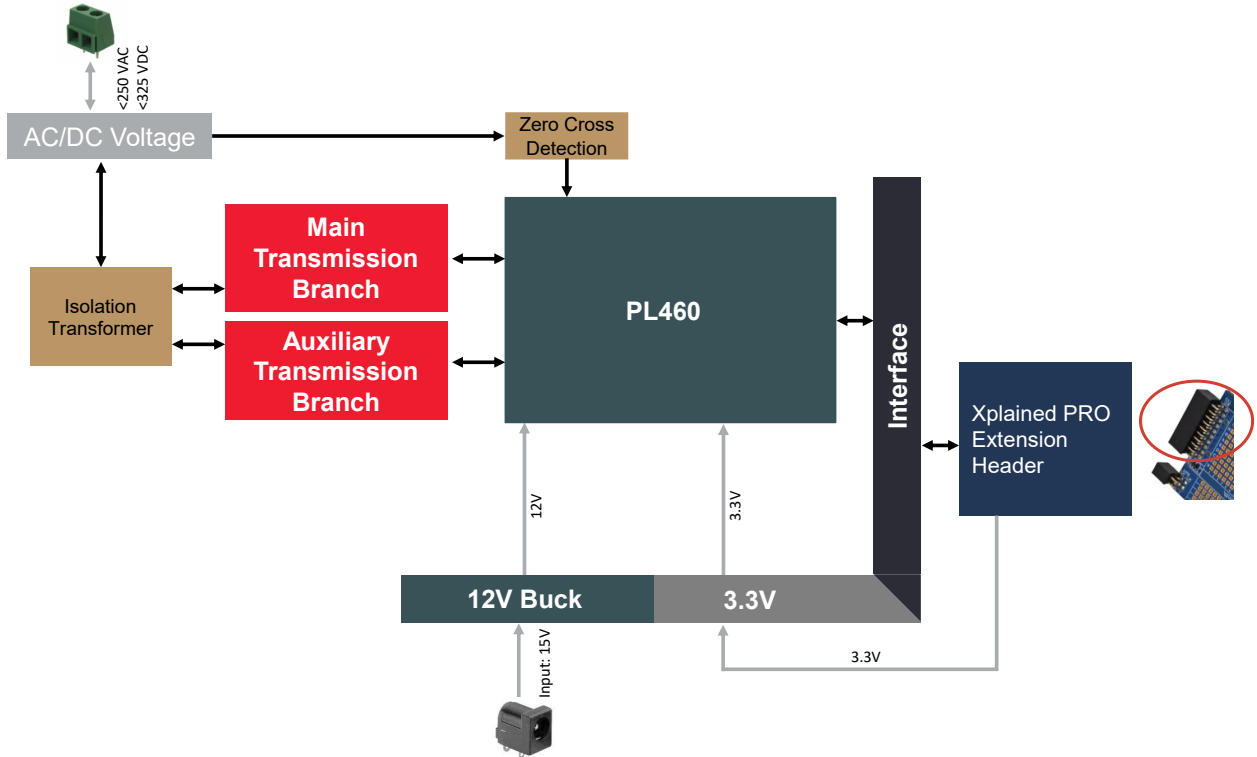The PL460-EK board includes the following features:

- PL460:
  - Embedded PLC Class-D Amplifier
  - Integrated PLC Front End:
    - PGA with automatic gain control and ADC
    - Digital transmission level control
    - Supports two independent transmission branches for the PLC signal
    - Up to 500 kHz PLC signal bandwidth
  - Architecture
    - High performance architecture combining CPU, specific co-processors for digital signal processing and dedicated hardware accelerators for common narrow-band PLC tasks
  - Cryptographic Engine and Secure Boot
    - Secure boot: supports AES-128 CMAC for authentication, AES-128 CBC for decryption
    - Fuse programming control for decryption and authentication 128-bit keys
  - Multi-protocol PLC modem:
    - Protocols:
      - G3-PLC
      - PRIMEv1.3 and PRIMEv1.4
    - Zero-Cross Detection
    - Low-power consumption in transmission and reception
- The PL460-EK board implements a multiband PLC configuration: FCC band transmissions use the main transmission branch and CENELEC A-Band transmissions use the auxiliary transmission branch.

- A 12V buck converter is used to generate the 12V power rail from the 15V input (Vdc).
- Interfaces:
  - Xplained PRO Connector (client)

3.2.1 PL460-EK Block Diagram

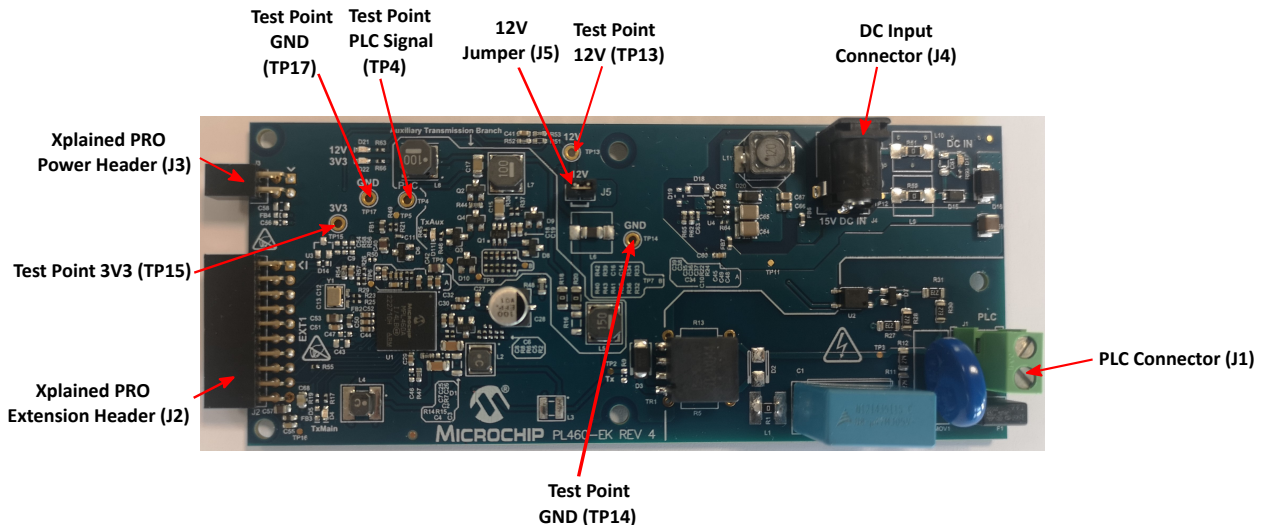The following figure shows the block diagram of the PL460-EK board.

Figure 3-2. PL460-EK Block Diagram

3.2.2 Interface Connection

The following figure shows an overview of the connectors and jumpers of the PL460-EK board.

Figure 3-3. PL460-EK Connectors and Jumpers Overview

3.2.2.1 Connectors

The PL460-EK board includes the following connectors:

1. PLC Connector, J1.

Table 3-1. PLC Connector, J1

Pin	Signal Name	Description
1	+	Positive Voltage / PLC+ Signal
2	-	Negative Voltage / PLC- Signal

2. Xplained PRO Extension Header, J2.

Table 3-2. Xplained PRO Extension Header, J2

Pin	Name	Signal Name	Description
1	ID	XPL_ID	Not connected
2	GND	GND	Ground
3	ADC+	Supply Monitor	Supply Monitor
4	ADC-	—	Not connected
5	GPIO1	—	Not connected
6	GPIO2	—	Not connected
7	PWM+	XPL_NRST[1]	PL460 reset (NRST) pin input
8	PWM-	XPL_ENABLE	PL460 enable (ENABLE) pin input
9	IRQ/GPIO	XPL_EXTIN	PL460 External Interrupt (EXTIN) pin output
10	GPIO	XPL_NTHW0	Thermal Monitor
11	SDA	XPL_STBY[2]	PL460 Standby input
12	SCL	XPL_TXEN	PL460 TX Enable
13	RXD	—	Not connected
14	TXD	XPL_VZC	Zero-crossing detector circuit input/output[3]
15	SS	XPL_CS	Client select for SPI
16	MOSI	XPL_MOSI	Host Out Client In line of serial peripheral interface
17	MISO	XPL_MISO	Host In Client Out line of serial peripheral interface
18	SCK	XPL_SCK	Clock for serial peripheral interface
19	GND	GND	Ground
20	VCC	3V3	Power for extension board

Notes:

1. The XPL_NRST signal must be connected to a GPIO in the host controller with an internal pull-down default reset configuration.
2. The XPL_STBY signal must be connected to GND when not using the Sleep mode functionality. When using it, the XPL_STBY signal must be connected to a GPIO in the host controller with an internal pull-down default reset configuration.
3. See 3.3.4. Zero-Crossing Detector Circuit for more information.

3. Xplained PRO Power Header, J3.

Table 3-3. Xplained PRO Power Header, J3

Pin	Name	Signal Name	Description
1	VEXT_P5V0	—	Not connected
2	GND	GND	Ground
3	VCC_P5V0	—	Not connected
4	Target VTG	3V3	Not connected

4. DC Input Connector, J4.

Table 3-4. DC Input Connector, J4

Pin	Signal Name	Description
1	DC_IN	DC Input voltage (15V)
2	GND	Ground
3	—	—

3.2.2.2 Jumper Configuration

The following table describes the functionality of the jumper.

Table 3-5. Jumper Configuration

Jumper	Label	Default Setting	Function
J5	12V	Closed	12V current measurement

3.2.2.3 Test Points

Some test points (probes and pads) were placed on the PL460-EK board for the verification of the main signals.

Table 3-6. Test Point Probes

Reference	Function	Reference	Function
TP4	PLC RX signal	TP15	3V3
TP13	12V	TP17	GND
TP14	GND	—	—

Table 3-7. Test Point Pads

Reference	Function	Reference	Function
TP1	PLC+	TP8	N0 Channel MOSFET
TP2	PLC Signal	TP9	Pin TXRX1
TP3	PLC-	TP11	VDC
TP5	PLC RX signal	TP12	Input Power DC Jack
TP6	Pin Zero-Crossing	TP16	3V3
TP7	P0 Channel MOSFET	—	—

3.3 Hardware Description – System

3.3.1 PL460

The PL460-EK board is equipped with a PL460 device in 81-Ball TFBGA (10 mm x 10 mm x 1.2 mm, 1 mm ball pitch).

The PL460 is a programmable modem for narrow-band Power Line Communication (PLC), able to run any PLC protocol in the frequency band below 500 kHz. PL460 embeds the PLC signal amplification stage, providing a highly integrated solution that reduces the total bill of materials, simplifies the layout and eases the modem design.

This device was designed to comply with FCC and CENELEC EN50065 regulations matching requirements of Internet of Things and Smart Energy applications. It supports state-of-the-art narrow-band PLC standards, such as ITU G.9903 (G3-PLC®), ITU G.9904 (PRIME) as well as any other narrow-band PLC protocols, being at the same time a future-proof platform able to support the evolution of these standards.

The PL460 is designed to be driven by external Microchip host devices, thus providing an additional level of flexibility on the host side. The Microchip host device loads the proper PLC-protocol firmware in the PL460, then controls the modem operation.

Figure 3-4 shows the different components of the PL460 Schematic.

Figure 3-4. PL460
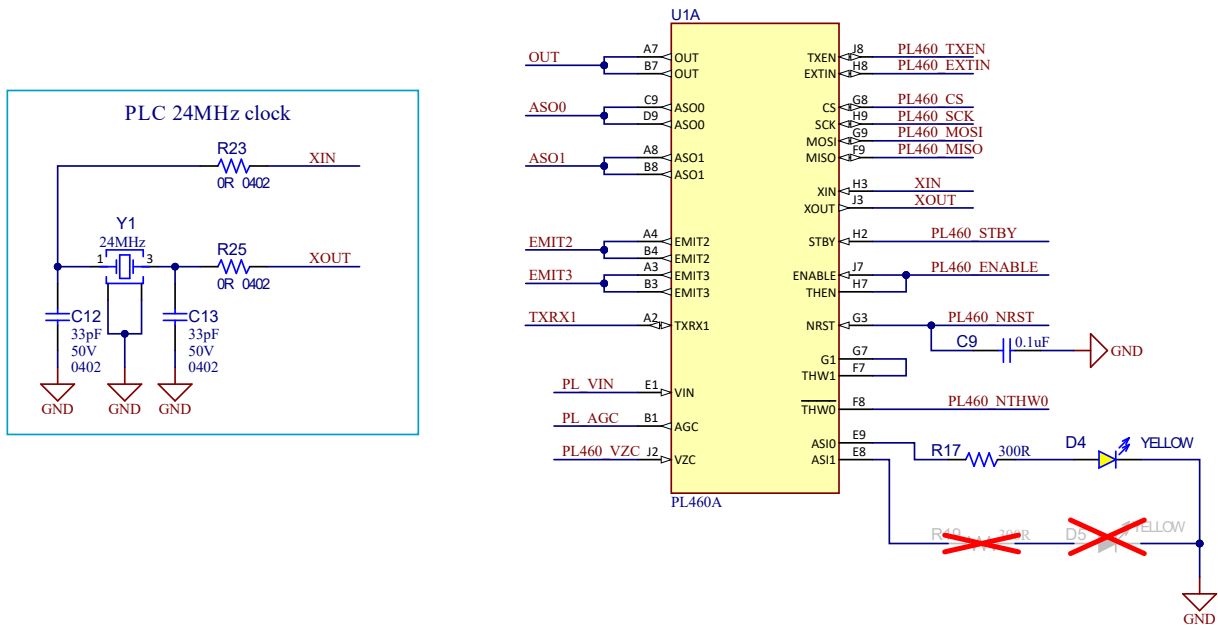
The PL460 decoupling capacitors are shown in the following schematic.

Figure 3-5. PL460 Decoupling Capacitors Schematic
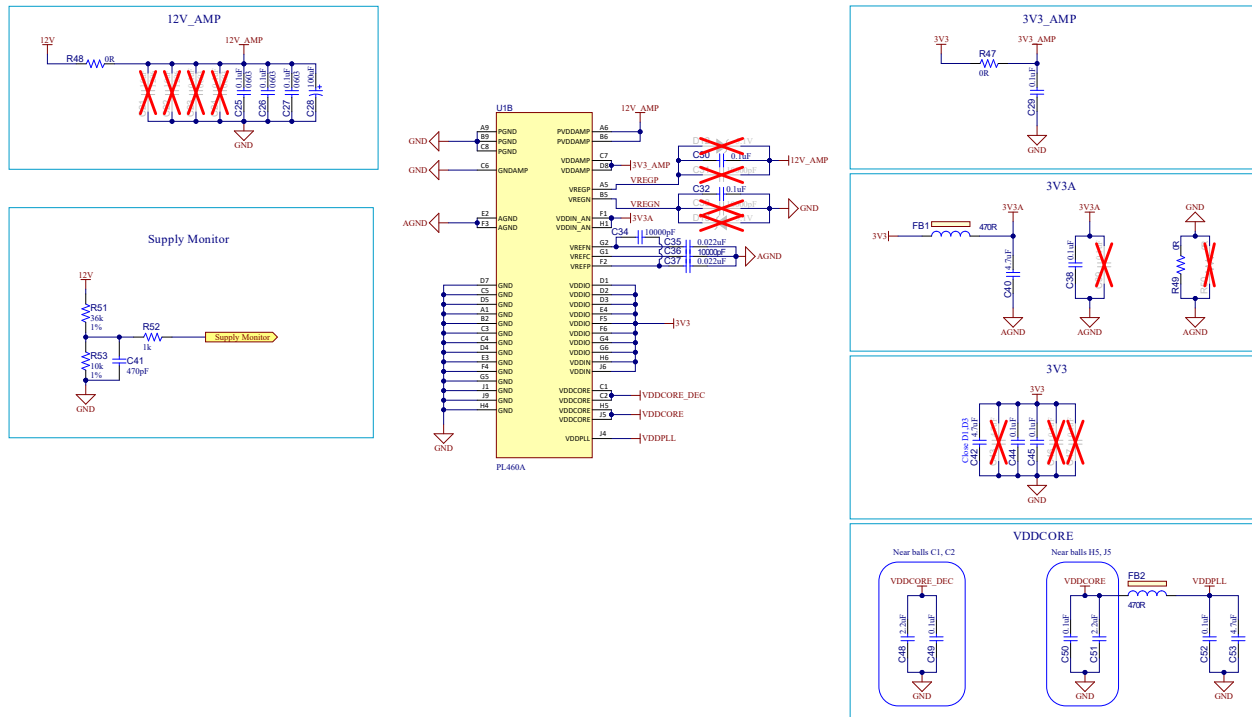
Microchip provides highly efficient and reduced BOM reference designs for the different coupling options, targeting common configurations in all PLC bands (<500 kHz) complying with existing regulations and PLC communication protocols.

**Figure 3-6. PLC Bands Supported by PL460**
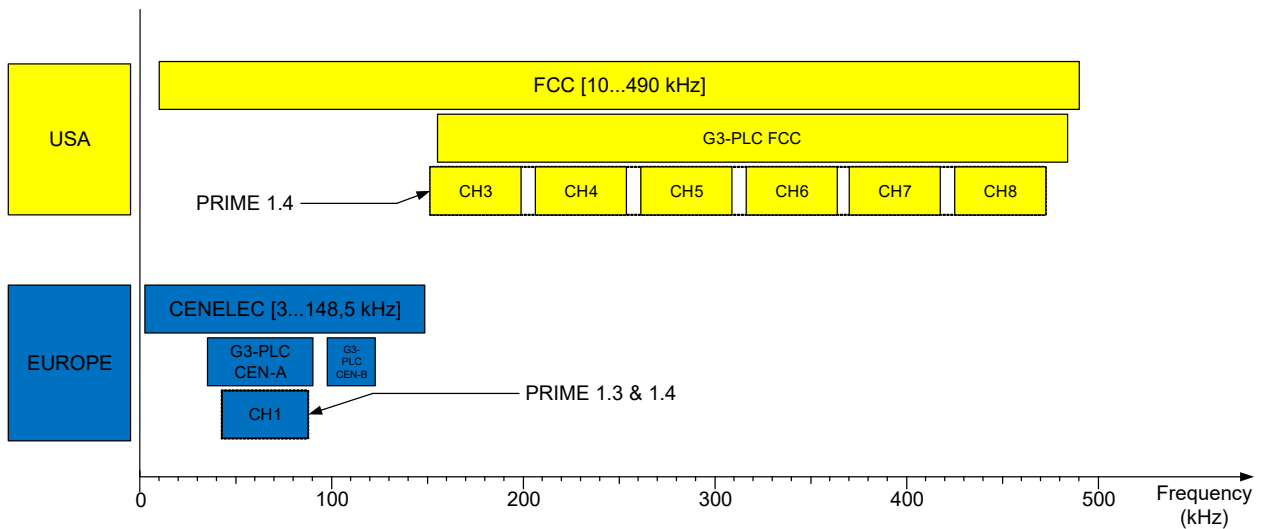
The coupling circuit of the PL460-EK kit is described with more detail in 3.3.3. PLC Coupling Circuitry Description.

3.3.2 Clock Circuitry

A crystal oscillator is assembled on the PL460-EK board to obtain a precise and stable system clock reference:

- A 24 MHz clock signal, Y1, generated for the PLC block. For more information about VXM7-9043-24M0000000, refer to the VXM7 product webpage.

Figure 3-7. 24 MHz Crystal Oscillator Scheme
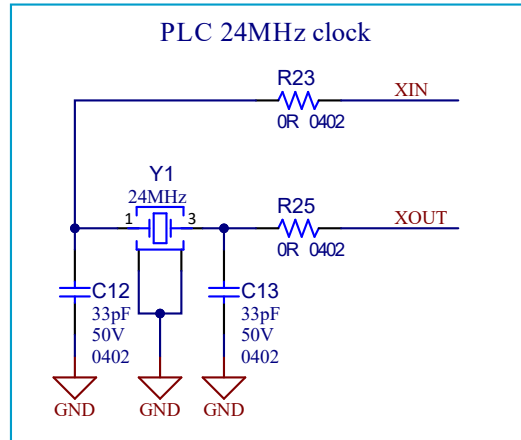
$$Clext = 2x\ (C_{XTAL} - C_{PARA} - C_{PCB})$$

$$Clext = 2x\ (4/18 - 0.6/0.7/0.8 - x)$$

$$Clext = 2x\ (18 - 0.7 - 1) = 33\ pF$$

For further information about the crystal oscillator, see the Crystal Selection Guidelines for PL360, ATPL230, ATPL250, SAM4CP16B & SAM4CP16C Application Note.

3.3.3 PLC Coupling Circuitry Description

FCC 47 CFR Part 15.107 defines the 9-490 kHz frequency band for PLC in North America and Canada. The band from 148.5 to 490 kHz is not yet regulated in Europe.

Figure 3-8. FCC Frequency Bands
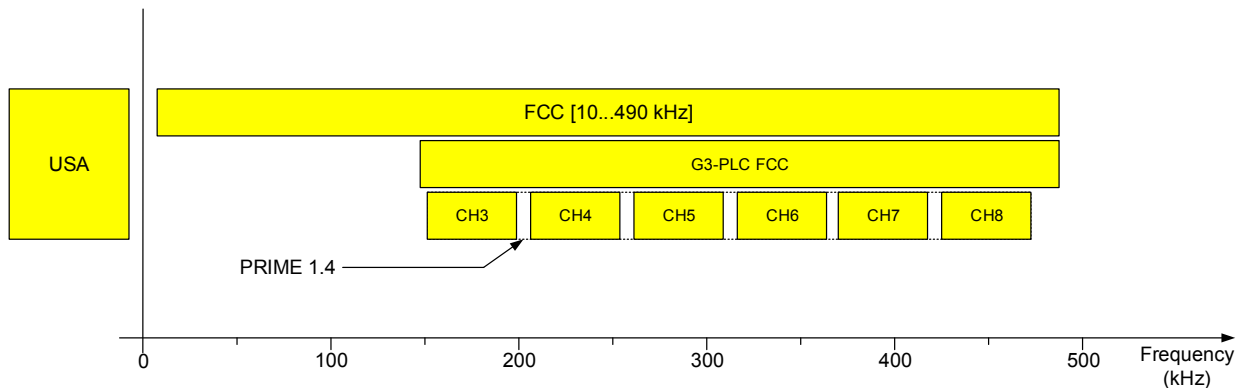
The European regulations concerning Power Line Communications are described in CENELEC standard EN 50065. This standard applies to electrical equipment using signals in the frequency range 3 kHz to 148.5 kHz to transmit information on low voltage electrical systems, either on the public supply system or within installations in consumers' premises. The following figure shows the different frequency bands allocated to the different applications.

Figure 3-9. CENELEC Frequency Bands
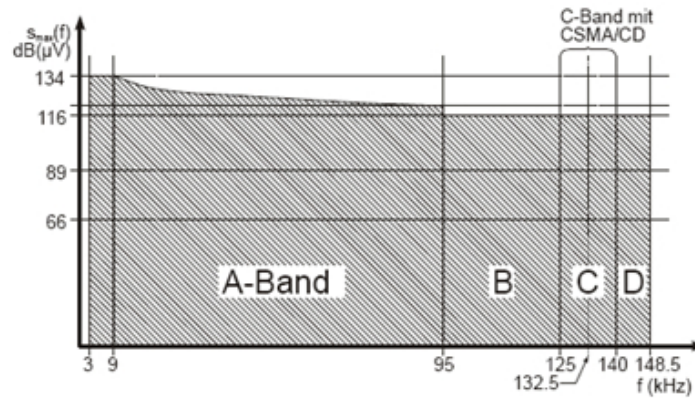
The PL460-EK board communicates in several band frequencies. The use of frequencies in these bands are restricted to consumer use, for example, for end-user applications such as industrial applications.

Microchip has designed several coupling reference designs for these band frequencies with variations in the BOM cost and the communication performance.

The PL460-EK board is assembled with a multiband design:

- Main transmission branch
  - FCC
- Auxiliary transmission branch
  - CENELEC A-Band

The FCC band design is assembled in the Main transmission branch and CENELEC A-Band in the Auxiliary transmission branch. The goal is to provide a cost-optimized fully-featured design according to the G3-PLC and PRIME requirements. Still, the PL460-EK board is designed to allow using other designs by changing the corresponding components and firmware configurations.

Table 3-8 summarizes all the configurations that can support the PL460.

In a multiband design, a configuration of the main transmission branch can be combined with any other of the auxiliary transmission branch.

Table 3-8. PL460 Coupling Configurations

Branch	Configuration Name	Description	Frequency Band (kHz)	PRIME Channel	G3-PLC Band	Applicable Regulation
Main	CEN-A	CENELEC A-Band	35-91	1	G3 CENELEC-A	CENELEC EN50065
	CEN-B	CENELEC B-Band	95-125	—	G3 CENELEC-B	CENELEC EN50065
	FCC	FCC Band	151-472	3,4,5,6,7,8	G3 FCC	CFR Title 47 Part 15 Subpart B
	FCC High-attenuation	FCC Band	151-472	3,4,5,6,7,8	G3 FCC	CFR Title 47 Part 15 Subpart B
	Multiband Single-branch FCC & CEN-A	FCC & CENELEC A-Bands	35-91, 157-472	1,3,4,5,6,7,8	G3 CENELEC-A & G3 FCC	CENELEC EN50065, CFR Title 47 Part 15 Subpart B

Branch	Configuration Name	Description	Frequency Band (kHz)	PRIME Channel	G3-PLC Band	Applicable Regulation
Auxiliary	CEN-A	CENELEC A-Band	35-91	1	G3 CENELEC-A	CENELEC EN50065
	CEN-B	CENELEC B-Band	95-125	—	G3 CENELEC-B	CENELEC EN50065

> **Important:** Check the online resources from the Microchip website to download the proper files according to your desired design.

The PLC coupling circuit is composed of three sub-circuits:
1. Transmission Stage
    a. Main transmission branch, which makes use of the embedded PLC driver
    b. Auxiliary transmission branch, used for multiband designs
2. Reception Stage
3. Coupling Stage

The following sections describe the purpose of every sub-circuit assembled in the PL460-EK board.

3.3.3.1 PLC Transmission Circuit

In the main transmission branch, the transmission stage adapts the output signal with the filtering blocks controlled by the ASO signals. It also provides a DC component and provides protection for received disturbances (see Figure 3-10).
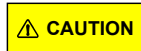
> ⚠ **CAUTION** Before starting to transmit, make sure that the 12V power supply is applied and stable to avoid damaging the driver. So, the DC Input Connector must be connected and the shunt JP1 must be installed on J5.

Figure 3-10. PL460 Main Transmission Stage for FCC Band (Embedded PLC Driver) Schematic
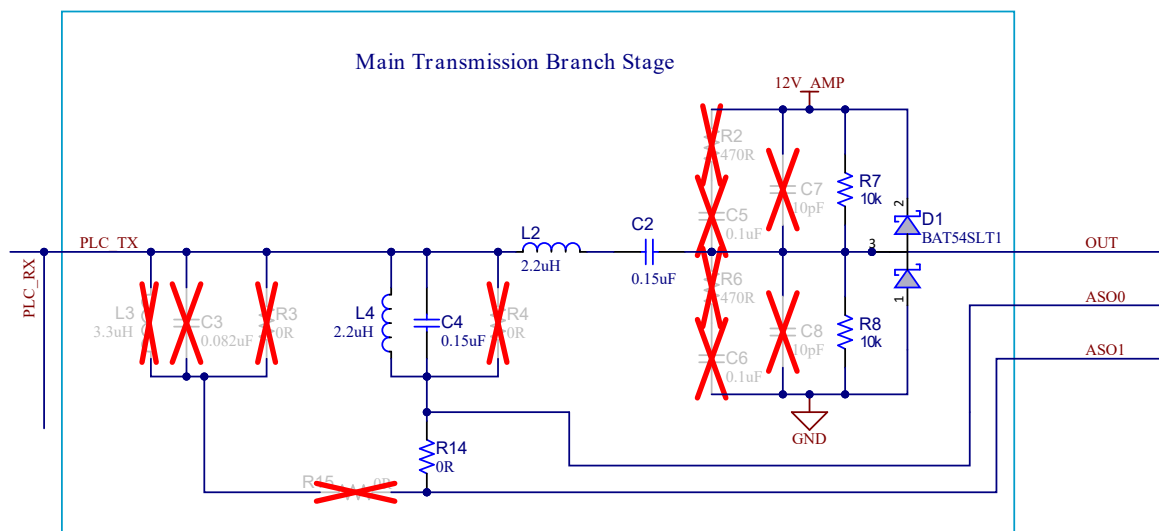
Note: The LED D4 (TX Main), connected to ASI0 of the PL460 (not in Figure 3-10), lights up with every message transmitted on the main branch.

In the auxiliary transmission branch, the transmission stage adapts the EMIT signals and amplifies them. In the PL460-EK board (see Figure 3-11) it is composed of:

- Driver: It adapts the EMIT signals to either control the amplifier or to be filtered by the next stage
- Amplifier: A Class-D amplifier generating a square waveform from 0 to 12V
- Bias and protection: It provides a DC component and provides protection from received disturbances

**Figure 3-11. PL460 Auxiliary Transmission Stage (Discrete Components) Schematic**
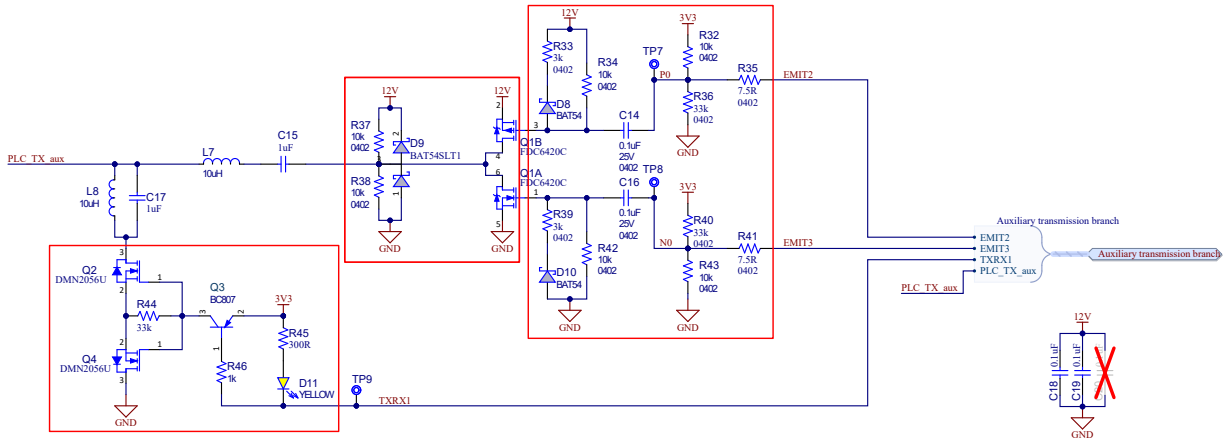
Note: The LED D11 (TX Aux) lights up with every message transmitted on the auxiliary branch.

3.3.3.2 PLC Reception Circuit

The PLC reception circuit used in PL460-EK (see Figure 3-12) is the reference design for the reception stage, and it is composed of:

- Single-pole low pass filter, R21 and C11
- Automatic Gain Control (AGC) circuit. A resistor, R24, is used to attenuate the incoming PLC signal in case its amplitude is high enough to exceed the input dynamic range of the embedded ADC
- A resistor, R22, for impedance matching
- DC decoupling capacitor, C10

Figure 3-12. PL460 Reception Stage Schematic
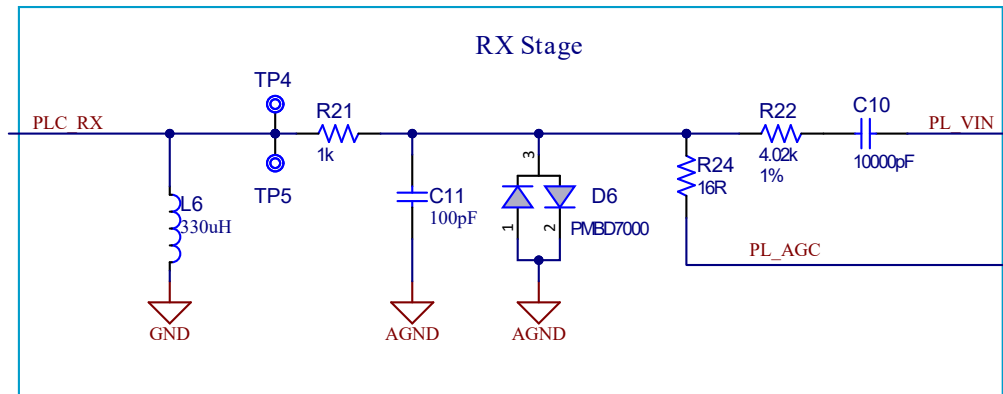
3.3.3.3 PLC Coupling Circuit

The PLC coupling circuit connects the PLC signal directly to the mains grid or even to the DC power rails without requiring any hardware adaptation.

The main purpose of the circuit is to block the mains voltage of the grid to/from which the signal is injected/received. This is carried out in PL460-EK (see Figure 3-13) by a high voltage capacitor, C1. Resistors R10, R11 and R12 allow the high-voltage capacitor to discharge after disconnection from mains.

⚠ **CAUTION**   PLC coupling components are designed for a maximum voltage of 250 Vac or 325 Vdc.

The TR1 transformer (with turn ratio 1:1) provides safety isolation from the L-N connection.

Varistor, fuse and TVS diodes protect the board against overvoltages and high transient voltages (surges and spikes) from mains. For more information about TVS diode, SMAJ12CAE3 (D3), refer to the SMAJ12CAE3 product webpage.

Figure 3-13. Isolated Coupling Schematic
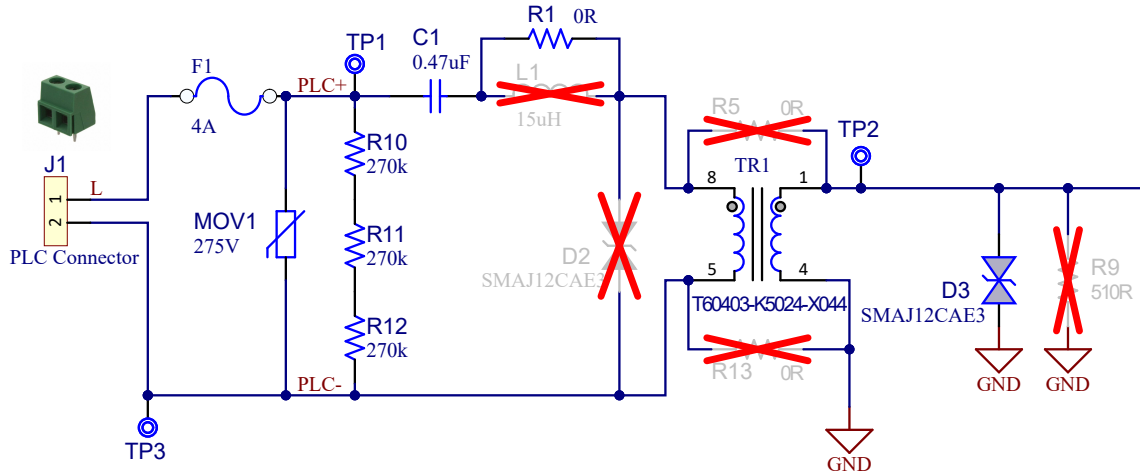

3.3.4   Zero-Crossing Detector Circuit

The phase identification is an important feature of the devices that are connected to Smart Grid networks, such as smart meters. A typical use of the zero-cross detection is to measure the time difference between a specific PLC frame reception and the last zero crossing event of the mains single-phase to which the device is connected.

> **Important:** The phase identification feature is mandatory for G3-PLC and PRIME1.4, but not for PRIME1.3.

The Figure 3-14 shows the Zero-Crossing Detection circuit used in the PL460-EK board, which features detection of rising edges of the mains voltage. The output signal of the detection circuit "Zero-crossing Detector" is connected to the pin VZC of the PL460, and a synchronization algorithm is applied to obtain an accurate measurement of the time between the reception of a PLC frame and the zero-crossing event.

Figure 3-14. Zero-Crossing Detection Circuit
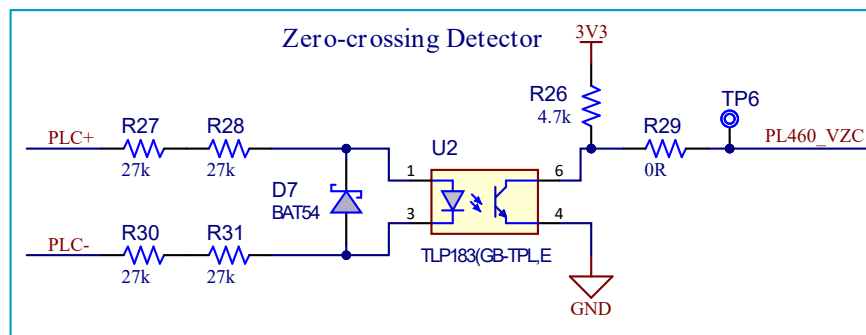
Note: If using an external zero-crossing signal source, it must be made available through the Xplained PRO connector at pin 14/TXD by soldering R57 and removing R29.

Tip: Designs that do not require galvanic isolation can use a simpler Zero-Crossing Detector circuit, such as a Zener diode, instead of the previous circuit.

3.3.5 Power Supply System

The PL460-EK board requires two power sources, as shown in Table 3-9.

Table 3-9. Power Sources for PL460-EK Board

Power Input	Voltage	Max Power
DC Input connector (J4)	15V (±5%)	12W
Xplained PRO connector (J2)	3.3V	—

The PL460-EK board has two voltage rails:

- +12V to power the PL460 amplification stage
- +3.3V to power the low voltage domain of PL460

The +12V rail is supplied by an external 15V 12W AC/DC Wall adapter connected through the DC Jack connector (J4) schematized in Figure 3-15.

Figure 3-15. DC Jack Input Schematic
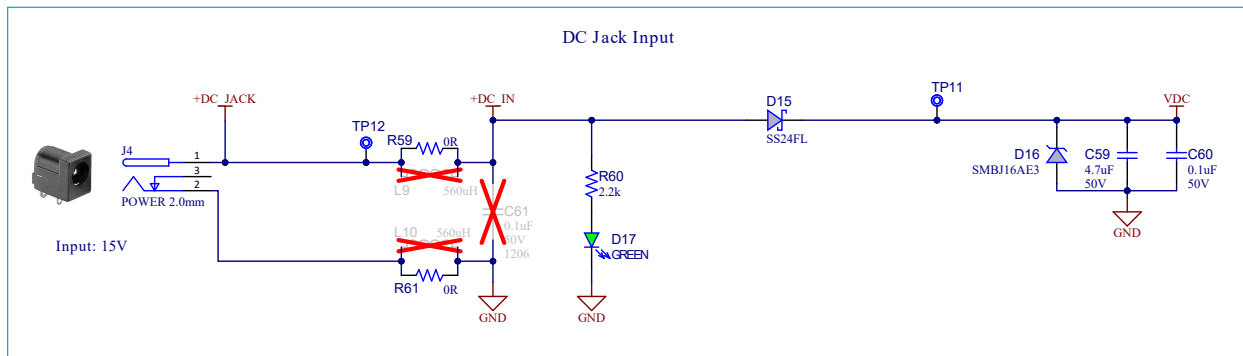
A switched-mode power supply (SMPS) with Buck topology is used to generate the 12V power supply from 15V input (Vdc). The LED D21 and the test point TP13 are connected to the voltage rail to check whether the power supply is operating properly. The jumper J5 allows measuring the current on the 12V rail.

Figure 3-16. 12V Buck Converter Schematic
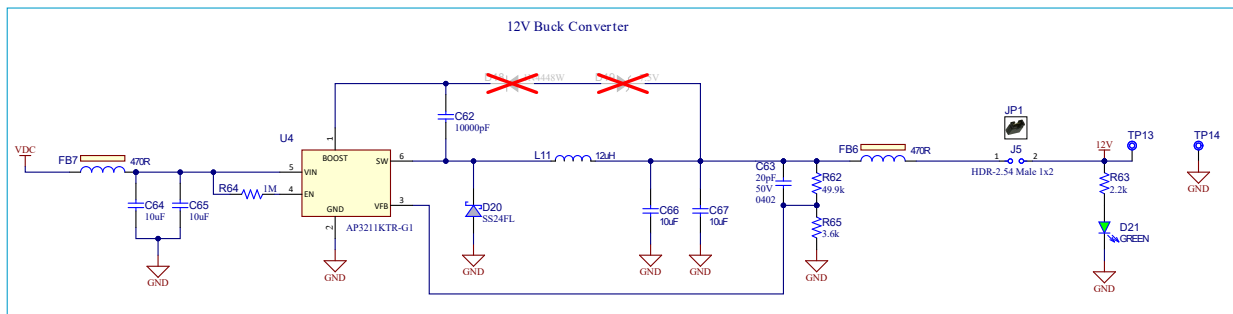
Attention: To avoid noise interferences, the switching frequency of the external SMPS must be out of the PLC band and preferably in frequencies above it to avoid harmonics influence. This is essential to obtain a good reception performance.

> **Tip:** Before starting to transmit, make sure that the 12V power supply is applied and stable to avoid damaging the driver. So, the DC Input Connector must be connected and shunt JP1 must be installed on J5.

In normal operation (Client board hosted by Xplained PRO Host), Xplained PRO will provide the 3.3V power supply.

Figure 3-17. 3V3 Supply Schematic
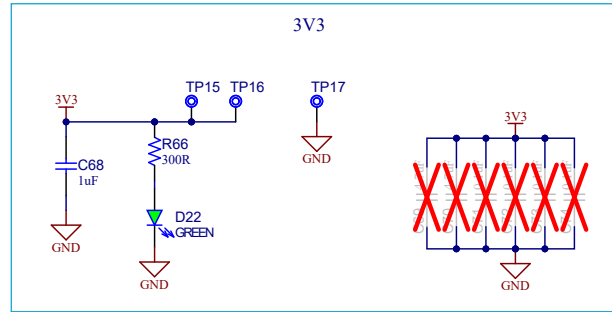
3.4   Hardware Description – MCU Interface Ports

3.4.1   Xplained PRO Extension Header

All Xplained PRO kits have one or more dual row, 20-pin, 100 mil extension header. Xplained PRO extensions have their female counterparts. Note that all pins are not always connected. All connected pins follow the defined pin-out description in the Table 3-2.

The extension headers can be used to connect a variety of Xplained PRO extensions to Xplained PRO MCU boards or to access the pins of the target MCU on Xplained PRO MCU boards directly.

The PL460-EK is a Client companion board for the PIC32CXMT family of EK/DBs, SAM4CMx-DB family, SAME70-Xplained and SAMG55-Xplained boards. All these boards include an Xplained PRO (Host) connector, and PL460 includes a Xplained PRO connector accordingly (Client). See Table 3-10 with the analysis of system interfacing with the required Xplained PRO host platforms.

Figure 3-18. Xplained PRO Extension Header Schematic
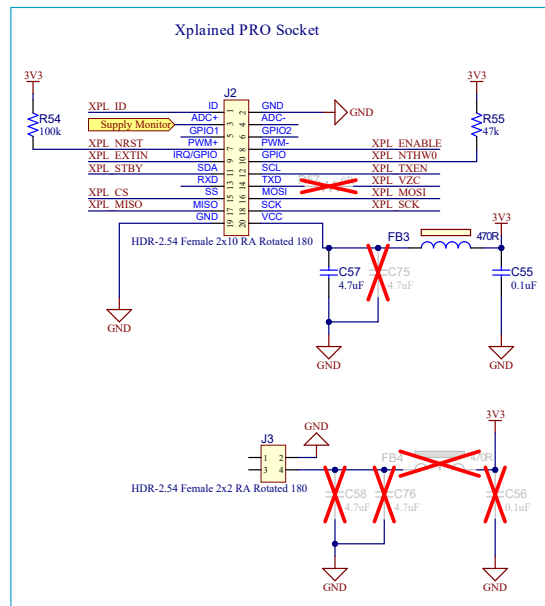
Table 3-10. System Interfacing

Xplained PRO	Client	Host (fixed conf. in existing platforms)					
Spec.	PL460-EK	SAMG55 Xplained	SAME70 Xplained	SAM4CMx-DB[1]	PIC32CXMTG-EK	PIC32CXMTC-DB	PIC32CXMTSH-DB
1[ID]	NC	EDBG	EDBG	NC/TP	NC	NC/TP	NC/TP
2[GND]	GND	GND	GND	GND	GND	GND	GND
3[ADC+]	Supply Monitor	PA17	PC31	NC/TP	PB1	PA30	PA30
4[ADC-]	NC	PA18	PA19	NC/TP	PA31	PB1	PB1
5[GPIO1]	NC	PA26	PB3	NC/TP	PA28	PA20	PA18
6[GPIO2]	NC	PA25	PB2	NC/TP	PA3	PA3	PA20
7[PWM+]	NRST	PA00	PA0	PB0	PD15	PD15	PD3
8[PWM-]	ENABLE	PA23	PC30	PB13	PD19	PD3	PD16
9[IRQ/GPIO]	EXTIN	PA24	PD28	PB3	PA2	PB25	PA3
10[GPIO]	NTHW0	PA29	PC17	PB2	PB15	PB15	PA2
11[SDA]	STBY	PB10	PA3	PA24	PA0	PC21	PA16
12[SCL]	TXEN	PB11	PA4	PA25	PA1	PC20	PA17
13[RXD]	NC	PA09	PB0	PB5	PD12	PA17	PA13
14[TXD]	VZC	PA10	PB1	PB4	PD13	PA16	PA12
15[SS]	CS	PA11	PD25	PA23	PA21	PC6	PA11
16[MOSI]	MOSI	PA13	PD21	PA7	PA24	PC9	PA8
17[MISO]	MISO	PA12	PD20	PA6	PA23	PC8	PA9
18[SCK]	SCK	PA14	PD22	PA8	PA22	PC7	PA10
19[GND]	GND	GND	GND	GND	GND	GND	GND
20[VCC]	VCC	VCC	VCC	VCC	VCC	VCC	VCC

Notes:

1. See 6.1. SAM4CMS-DB/SAM4CMP-DB + PL460-EK to implement the necessary changes in the SAM4CMS-DB or SAM4CMP-DB to have the correct communication.

4. Ordering Information

Table 4-1. Evaluation Kit Ordering Information

Ordering Code	Board Marking
EV13L63A	PL460-EK

5.   Appendix A. Schematics and Layouts

The PL460-EK board is assembled with the FCC in main transmission branch and CENELEC A-Band in auxiliary transmission branch. The goal of this configuration is to have one filtering option per amplification branch. The following sub-sections show the schematics and the layout of this design.

5.1   PL460-EK Schematics

This section contains the schematics by default for the PL460-EK board:

- Block Diagram Schematic, Figure 5-1
- PL460 and Main Transmission Branch Schematic, Figure 5-2
- Auxiliary Transmission Branch Schematic, Figure 5-3
- PL460 Supply Schematic, Figure 5-4
- Interface Schematic, Figure 5-5
- Power Supply Schematic, Figure 5-6

Figure 5-1. Block Diagram Schematic
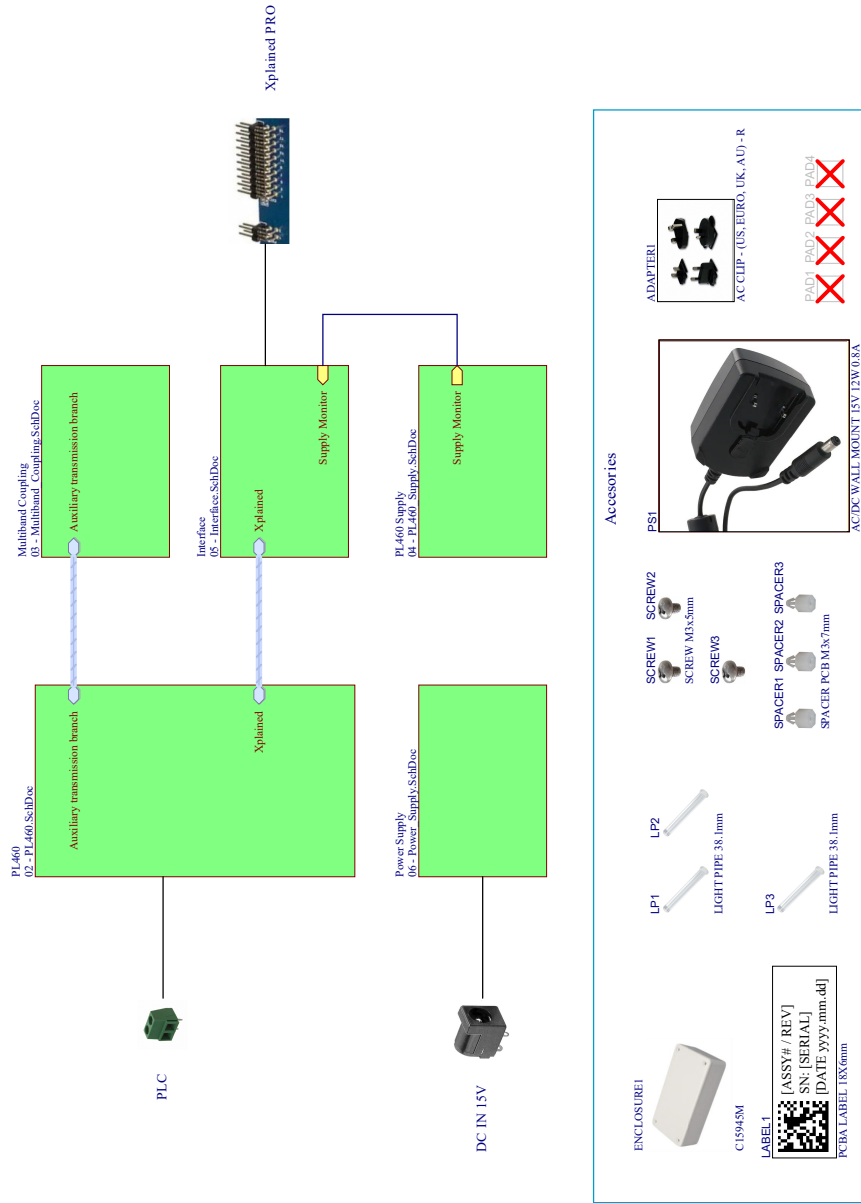
Figure 5-2. PL460 and Main Transmission Branch Schematic

Figure 5-3. Auxiliary Transmission Branch Schematic

Auxiliary Transmission Branch

Variant: Multiband FCC default & CEN-A
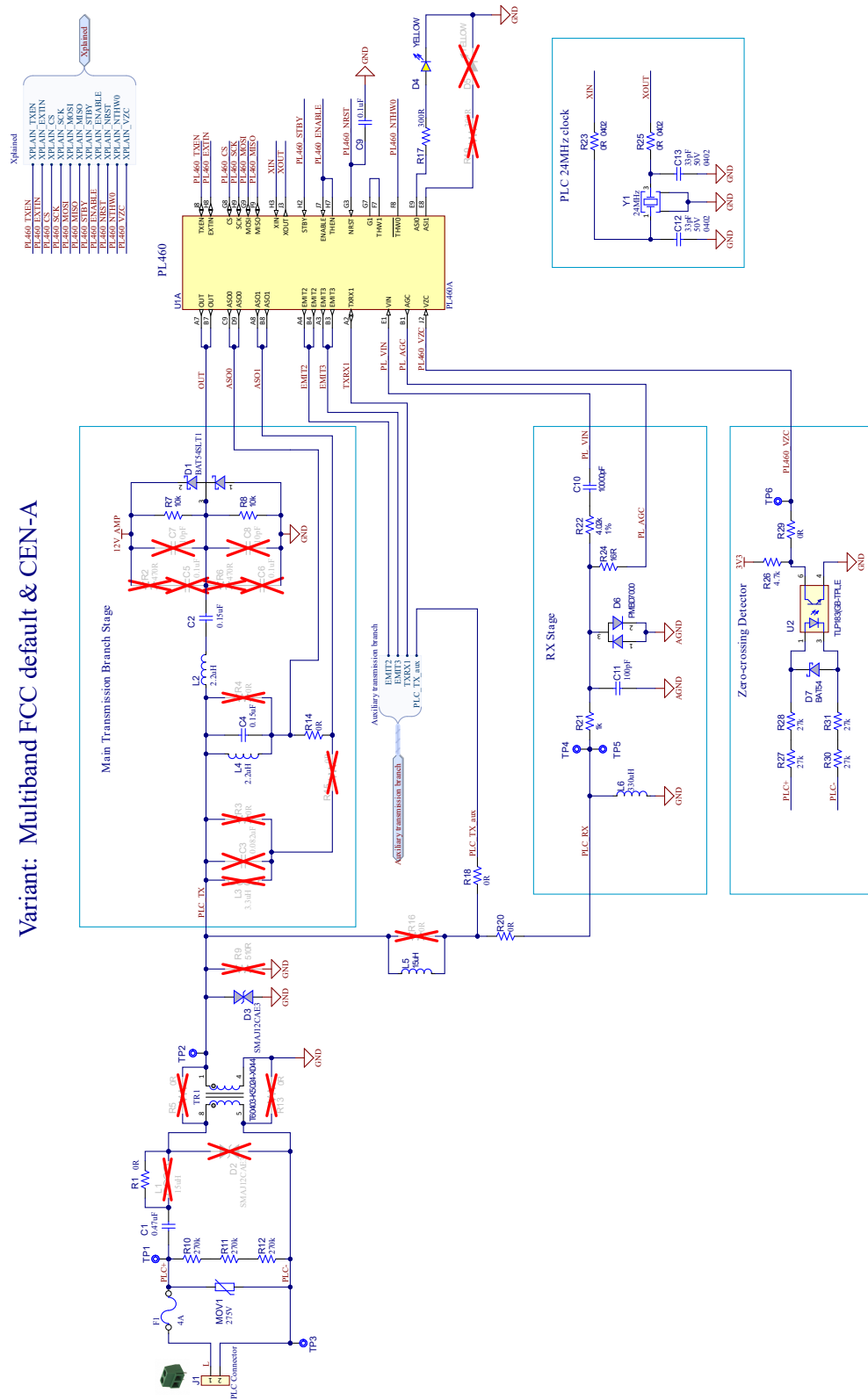
Figure 5-4. PL460 Supply Schematic
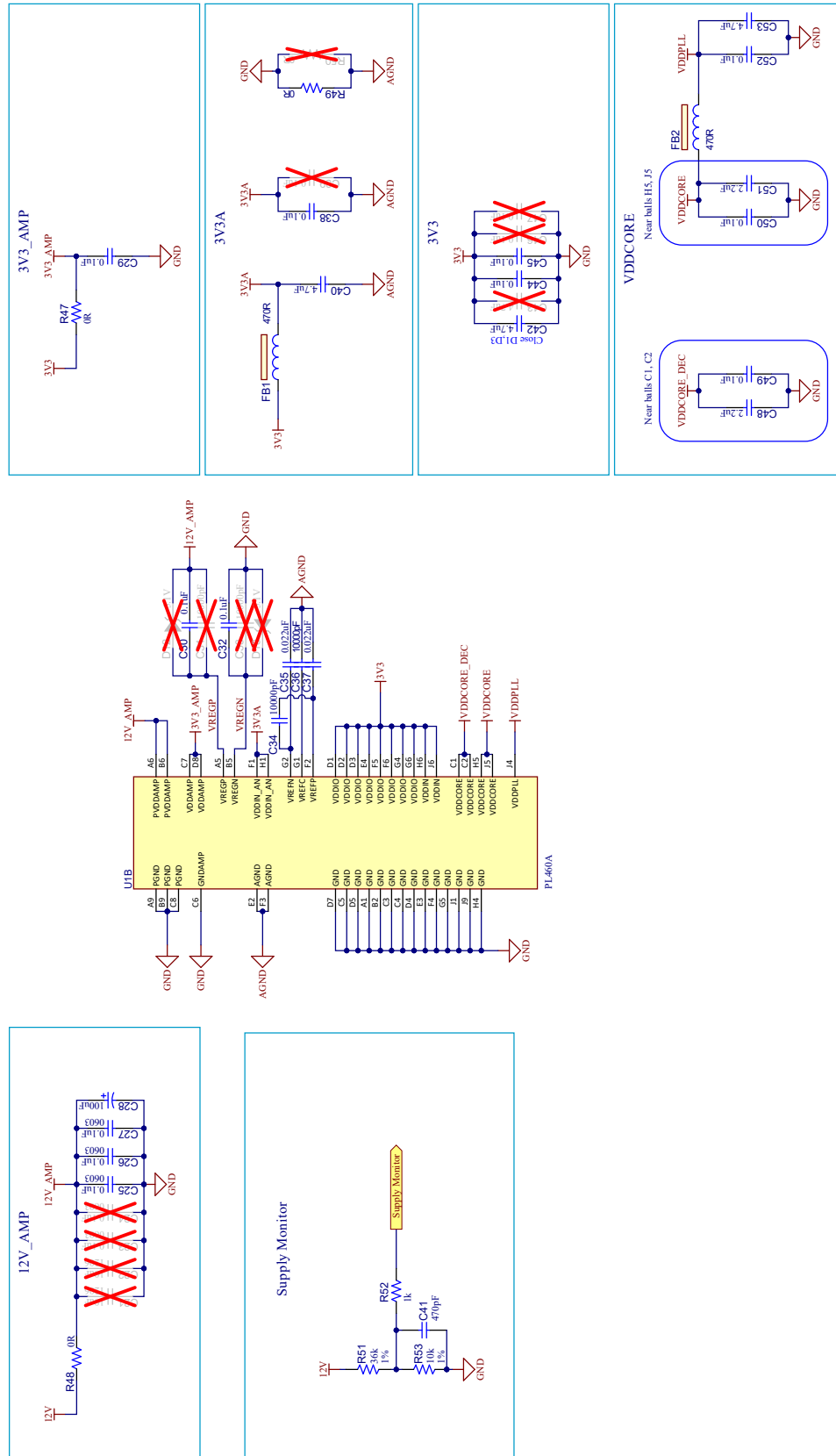
Figure 5-5. Interface Schematic

Figure 5-6. Power Supply Schematic

Power Supply

DC Jack Input

Input: 15V

12V Buck Converter

3V3
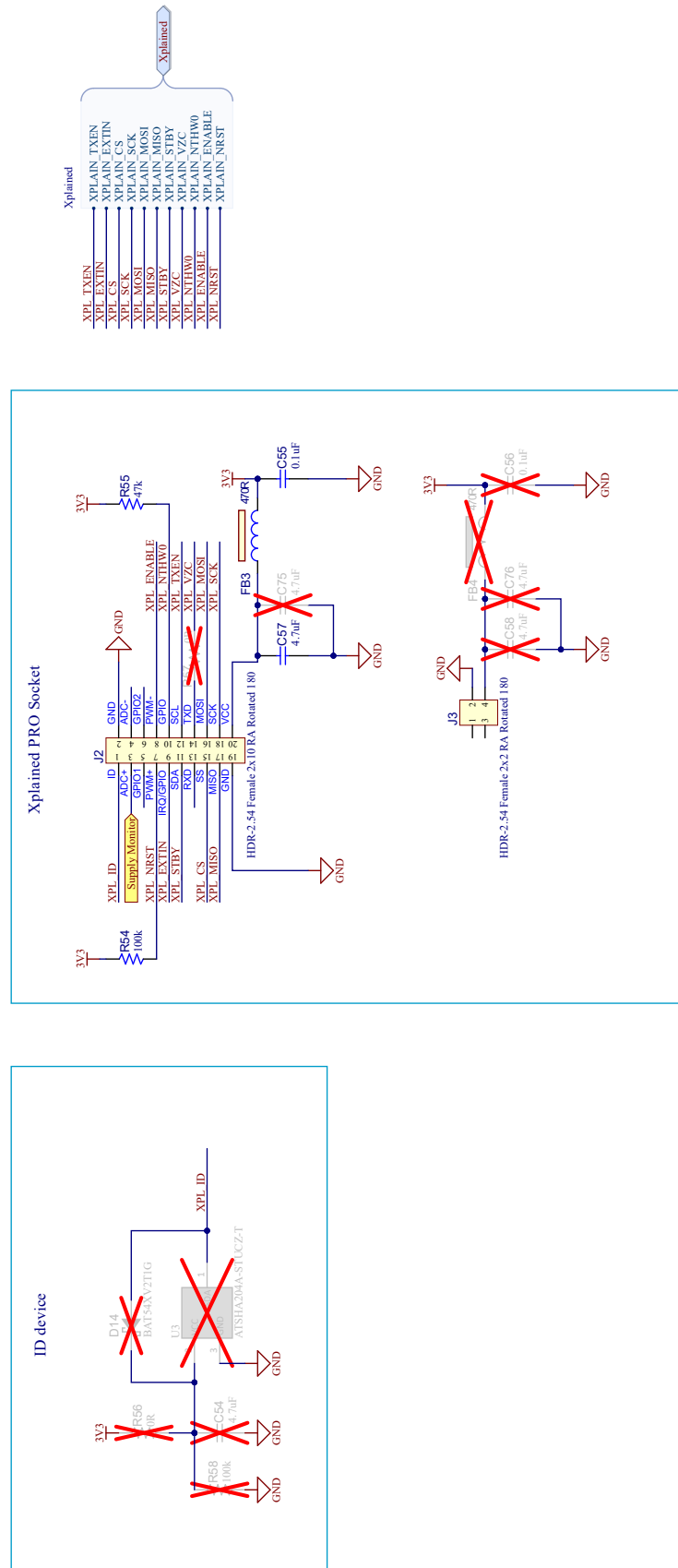
5.2 PL460-EK Layout

This section contains the layout graphics by default for the PL460-EK board:

Figure 5-7. PL460-EK Layout: Top Layer
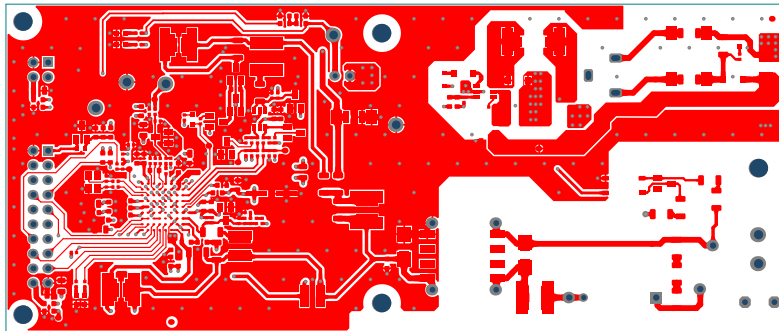
Figure 5-8. PL460-EK Layout: Mid Layer 1 (Ground)
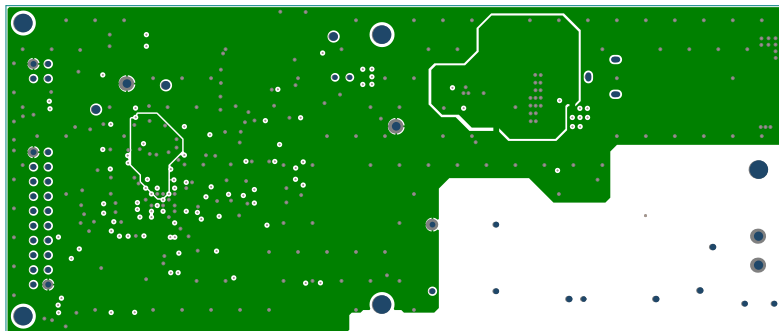
Figure 5-9. PL460-EK Layout: Mid Layer 2 (Power Supplies)
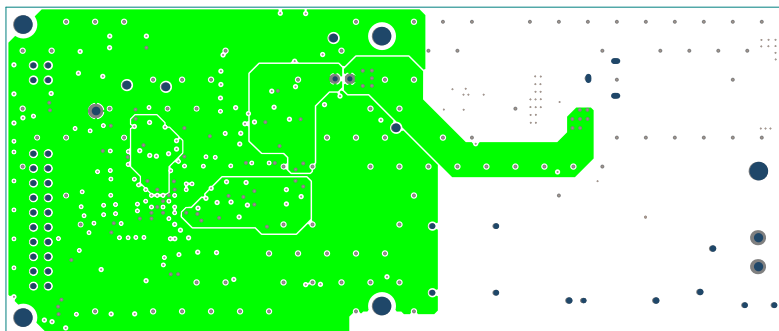
Figure 5-10. PL460-EK Layout: Bottom Layer
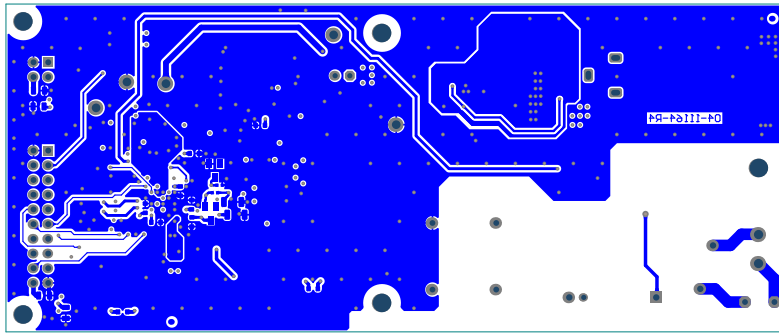
Figure 5-11. PL460-EK Layout: Top Silkscreen
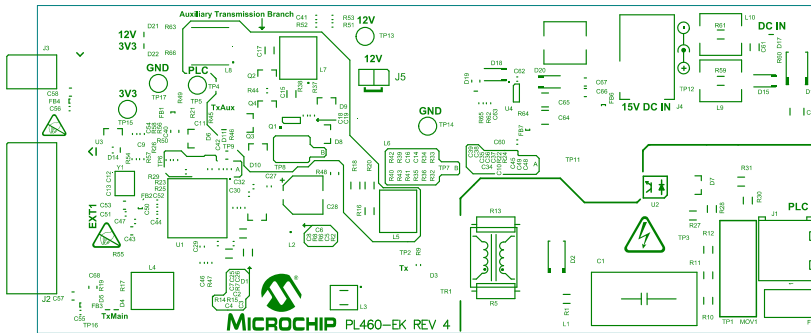
Figure 5-12. PL460-EK Layout: Bottom Silkscreen

6.   Appendix B. Host Platforms for PL460-EK

In some platforms, such as SAM4CMS-DB and SAM4CMP-DB, it is necessary to make modifications in the host board so that the communication between the host board and PL460-EK will be correct.

6.1   SAM4CMS-DB/SAM4CMP-DB + PL460-EK

It is necessary to make the following changes in the SAM4CMS-DB or SAM4CMP-DB to ensure the correct communication between SAM4CMS-DB/SAM4CMP-DB and PL460-EK:

- Remove R346, R354 and R355. These resistors are placed near the Xplained PRO connector (J13). Now, the ports are exclusive to the JTAG
- Join Pin7 of the Xplained PRO connector (J13) with Pin2 of connector J10. So, PL460_NRST is controlled with the PA28 port
- Join Pin9 of the Xplained PRO connector (J13) with Pin1 of connector J10. So, PL460_EXTIN is controlled with the PA26 port

Besides, it is necessary to make the following changes in the SAM4CMS-DB or SAM4CMP-DB to support the PVDD Monitor:

- Remove R345. This resistor is placed near the Xplained PRO connector (J13). So, the PB13 port can be used by the PVDD Monitor
- Join Pin3 of the Xplained PRO connector (J13) with Pin8 of connector J12. So, the PL460_PVDD_Monitor is controlled with the PB13 port
- Join Pin8 of the Xplained PRO connector (J13) with Pin3 of connector J10. So, the PL460_ENABLE is controlled with the PA27 port

In addition, it is necessary to make the following changes in the SAM4CMS-DB or SAM4CMP-DB to support the Thermal Monitor:

- Join Pin10 of Xplained PRO connector (J13) with Pin15 of connector J12. So, the PL460_NTHW0 is controlled with the PA22 port

6.2   Other Host Platforms PL460-EK

There are other host platforms that can be used with PL460-EK without the need to make any modifications to them. The following host platforms could be connected directly to PL460-EK:

- SAMG55 Xplained PRO EK
- SAME70 Xplained EK
- PIC32CXMTG-EK
- PIC32CXMTC-DB
- PIC32CXMTSH-DB

7.   References

- PL460 Data Sheet, reference DS60001666, on the Microchip website
- Crystal Selection Guidelines for PL360, ATPL230, ATPL250, SAM4CP16B & SAM4CP16C Application Note, reference DS00002716, on the Microchip website
- SMBJ5.0 thru SMBJ170A, CA, e3 and SMBG5.0 thru SMBG170A, CA, e3 Data Sheet, 2009
- SMAJ5.0e3 to SMAJ440CAe3 Data Sheet, 2010
- VXM7 Data Sheet, on the Microchip website

8. Revision History

8.1 Rev C - 01/2023

3. PL460-EK Board	Added notes in XPL_NRST and XPL_STBY signals in Table 3-2

8.2 Rev B - 10/2022

Document	Minor updates throughout.
	Added ordering code.
	Removed any reference to J6 and JP2 because is removed in PL460-EK Rev 4.
	Updated all the figures according to PL460-EK Rev 4.
	Updated Table 3-8
2. Getting Started	Updated section.
3. PL460-EK Board	Updated Table 3-2 and Table 3-3 according to PL460-EK Rev 4.
4. Ordering Information	Added section.

8.3 Rev A - 05/2022

Document	Initial release

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