

NC7S02

TinyLogic HS 2-Input NOR Gate

Description

The NC7S02 is a single 2-Input high performance CMOS NOR Gate. Advanced Silicon Gate CMOS fabrication assures high speed and low power circuit operation over a broad V_{CC} range. ESD protection diodes inherently guard both inputs and output with respect to the V_{CC} and GND rails. Three stages of gain between inputs and outputs assures high noise immunity and reduced sensitivity to input edge rate.

Features

- Space Saving SC-74A and SC88A 5-Lead Packages
- Ultra Small MicroPak™ Leadless Package
- High Speed: $t_{PD} = 3.5$ ns Typ
- Low Quiescent Power: $I_{CC} < 1$ μ A
- Balanced Output Drive: 2 mA I_{OL} , -2 mA I_{OH}
- Broad V_{CC} Operating Range: 2 V – 6 V
- Balanced Propagation Delays
- Specified for 3 V Operation
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

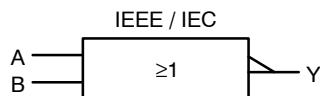


Figure 1. Logic Symbol



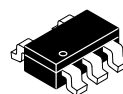
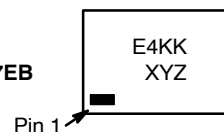
ON Semiconductor®

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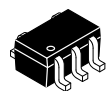
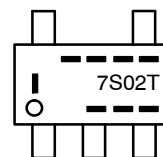
MARKING DIAGRAMS



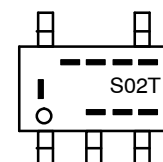
SIP6
CASE 127EB



SC-74A
CASE 318BQ



SC-88A
CASE 419A-02



E4, 7S02, S02 = Specific Device Code
 KK = 2-Digit Lot Run Traceability Code
 XY = 2-Digit Date Code Format
 Z = Assembly Plant Code
 T = Die Run Code
 --- = Year Coding Scheme
 |-- = Plant Code Identifier
 --- = Eight-Week Datacoding Scheme

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

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Pin Configurations

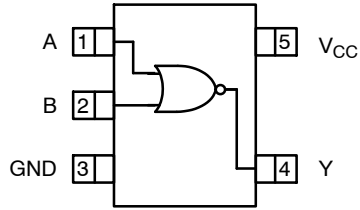


Figure 2. SC-88A and SC-74A (Top View)

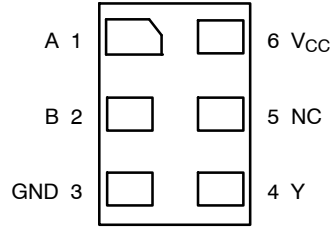


Figure 3. MicroPak (Top Through View)

PIN DESCRIPTIONS

| Pin Name | Description |
|----------|-------------|
| A, B | Inputs |
| Y | Output |
| NC | No Connect |

FUNCTION TABLE ($Y = \overline{A + B}$)

| Inputs | | Output |
|--------|---|--------|
| A | B | Y |
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | L |

H = HIGH Logic Level
L = LOW Logic Level

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | | Min | Max | Unit |
|-----------------------|--|-------------------------------------|------|----------------|--------------------|
| V_{CC} | Supply Voltage | | -0.5 | 6.5 | V |
| I_{IK} | DC Input Diode Current | $V_{IN} \leq -0.5\text{ V}$ | - | -20 | mA |
| | | $V_{IN} \geq V_{CC} + 0.5\text{ V}$ | - | +20 | |
| V_{IN} | DC Input Voltage | | -0.5 | $V_{CC} + 0.5$ | V |
| I_{OK} | DC Output Diode Current | $V_{OUT} < -0.5\text{ V}$ | - | -20 | mA |
| | | $V_{OUT} > V_{CC} + 0.5\text{ V}$ | - | +20 | |
| V_{OUT} | DC Output Voltage | | -0.5 | $V_{CC} + 0.5$ | V |
| I_{OUT} | DC Output Source or Sink Current | | - | ± 12.5 | mA |
| I_{CC} or I_{GND} | DC V_{CC} or Ground Current per Output Pin | | - | ± 25 | mA |
| T_{STG} | Storage Temperature | | -65 | +150 | $^{\circ}\text{C}$ |
| T_J | Junction Temperature | | - | +150 | $^{\circ}\text{C}$ |
| T_L | Lead Temperature (Soldering, 10 Seconds) | | - | +260 | $^{\circ}\text{C}$ |
| P_D | Power Dissipation in Still Air | SC-74A | - | 225 | mW |
| | | SC-88A | - | 190 | |
| | | MicroPak | - | 327 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------|---------------------------|-------------------|-----|----------|------|
| V_{CC} | Supply Voltage | | 2.0 | 6.0 | V |
| V_{IN} | Input Voltage | | 0 | V_{CC} | V |
| V_{OUT} | Output Voltage | | 0 | V_{CC} | V |
| T_A | Operating Temperature | | -40 | +85 | °C |
| t_r, t_f | Input Rise and Fall Times | V_{CC} at 2.0 V | 0 | 20 | ns |
| | | V_{CC} at 3.0 V | 0 | 20 | |
| | | V_{CC} at 4.5 V | 0 | 10 | |
| | | V_{CC} at 6.0 V | 0 | 5 | |
| θ_{JA} | Thermal Resistance | SC-74A | - | 555 | °C/W |
| | | SC-88A | - | 659 | |
| | | MicroPak | - | 382 | |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTRICAL CHARACTERISTICS

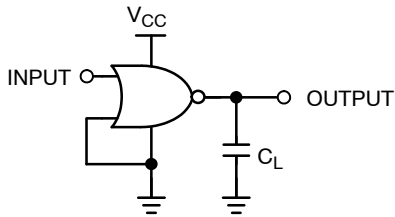
| Symbol | Parameter | V_{CC} (V) | Conditions | $T_A = +25^\circ\text{C}$ | | | $T_A = -40 \text{ to } +85^\circ\text{C}$ | | Unit |
|----------|---------------------------|--------------------------|---|------------------------------|--------------------------|------------------------------|---|------------------------------|---------------|
| | | | | Min | Typ | Max | Min | Max | |
| V_{IH} | HIGH Level Input Voltage | 2.0 3.0 – 6.0 | | 1.50 0.7 V_{CC} | - - | - - | 1.50 0.7 V_{CC} | - - | V |
| V_{IL} | LOW Level Input Voltage | 2.0 3.0 – 6.0 | | - - | - - | 0.50 0.3 V_{CC} | - - | 0.50 0.3 V_{CC} | V |
| V_{OH} | HIGH Level Output Voltage | 2.0 3.0 4.5 6.0 | $I_{OH} = -20 \mu\text{A}$ $V_{IN} = V_{IL}$ | 1.90 2.90 4.40 5.90 | 2.0 3.0 4.5 6.0 | - - - - | 1.90 2.90 4.40 5.90 | - - - - | V |
| | | 3.0 4.5 6.0 | $V_{IN} = V_{IL}$ $I_{OH} = -1.3 \text{ mA}$ $I_{OH} = -2.0 \text{ mA}$ $I_{OH} = -2.6 \text{ mA}$ | 2.68 4.18 5.68 | 2.85 4.35 5.85 | - - - | 2.63 4.13 5.63 | - - - | V |
| V_{OL} | LOW Level Output Voltage | 2.0 3.0 4.5 6.0 | $I_{OL} = 20 \mu\text{A}$ $V_{IN} = V_{IH}$ | - - - - | 0.0 0.0 0.0 0.0 | 0.10 0.10 0.10 0.10 | - - - - | 0.10 0.10 0.10 0.10 | V |
| | | 3.0 4.5 6.0 | $V_{IN} = V_{IH}$ $I_{OL} = 1.3 \text{ mA}$ $I_{OL} = 2.0 \text{ mA}$ $I_{OL} = 2.6 \text{ mA}$ | - - - | 0.1 0.1 0.1 | 0.26 0.26 0.26 | - - - | 0.33 0.33 0.33 | V |
| I_{IN} | Input Leakage Current | 6.0 | $V_{IN} = V_{CC}, \text{GND}$ | - | - | ± 0.1 | - | ± 1.0 | μA |
| I_{CC} | Quiescent Supply Current | 6.0 | $V_{IN} = V_{CC}, \text{GND}$ | - | - | 1.0 | - | 10.0 | μA |

AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = +25°C | | | T _A = -40 to +85°C | | Unit |
|--|--|---------------------|------------------------|------------------------|------|-----|-------------------------------|-----|------|
| | | | | Min | Typ | Max | Min | Max | |
| t _{PLH} , t _{PHL} | Propagation Delay (Figure 4, 6) | 5.0 | C _L = 15 pF | - | 3.5 | 15 | - | - | ns |
| | | 2.0 | C _L = 50 pF | - | 19 | 100 | - | 125 | ns |
| | | 3.0 | | - | 10.5 | 27 | - | 35 | |
| | | 4.5 | | - | 7.5 | 20 | - | 25 | |
| 6.0 | - | 6.5 | 17 | - | 21 | | | | |
| t _{TLH} , t _{THL} | Output Transition Time (Figure 4, 6) | 5.0 | C _L = 15 pF | - | 3 | 10 | - | - | ns |
| | | 2.0 | C _L = 50 pF | - | 25 | 125 | - | 155 | ns |
| | | 3.0 | | - | 16 | 35 | - | 45 | |
| | | 4.5 | | - | 11 | 25 | - | 31 | |
| 6.0 | - | 9 | 21 | - | 26 | | | | |
| C _{IN} | Input Capacitance | Open | | - | 2 | 10 | - | 10 | pF |
| C _{PD} | Power Dissipation Capacitance (Figure 5) | 5.0 | (Note 2) | - | 6 | - | - | - | pF |

2. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression:
 $I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CCstatic})$.

AC Loading and Waveforms



C_L includes load and stray capacitance
 Input PRR = 1.0 MHz; t_w = 500 ns

Figure 4. AC Test Circuit

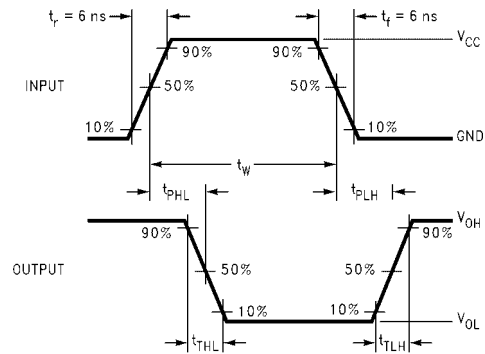
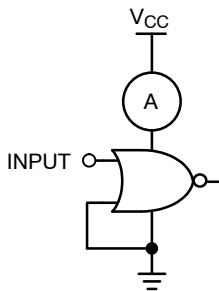


Figure 6. AC Waveforms



Input = AC Waveform;
 PRR = Variable; Duty Cycle = 50%.

Figure 5. I_{CCD} Test Circuit

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ORDERING INFORMATION

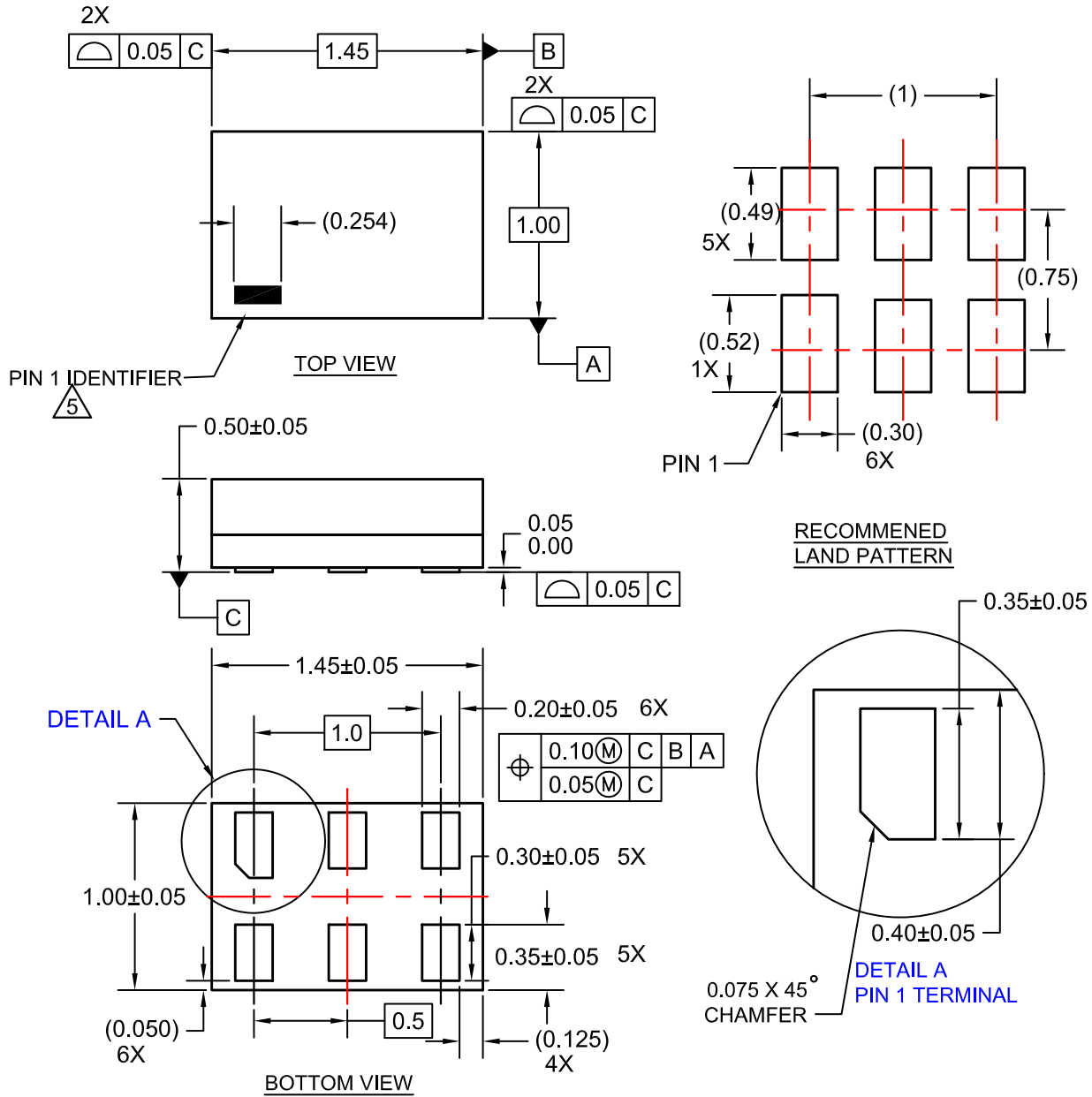
| Order Number | Top Mark | Package Description | Shipping [†] |
|--------------|----------|---------------------|-----------------------|
| NC7S02M5X | 7S02 | SC-74A | 3000 / Tape & Reel |
| NC7S02P5X | S02 | SC-88A | 3000 / Tape & Reel |
| NC7S02L6X | E4 | SIP6, MicroPak | 5000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

SIP6 1.45X1.0
CASE 127EB
ISSUE O



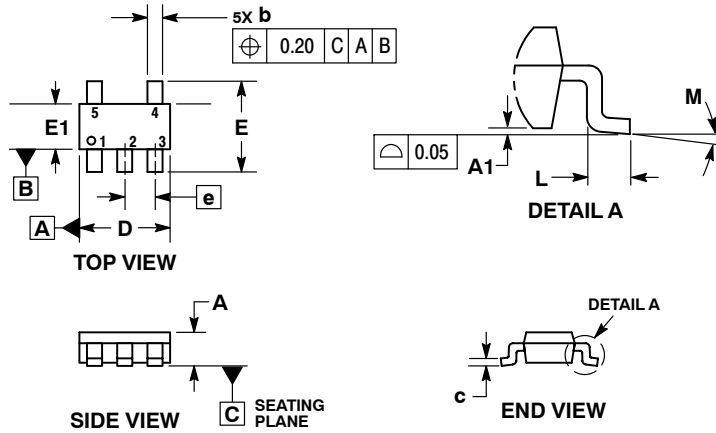
NOTES:

1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

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PACKAGE DIMENSIONS

SC-74A CASE 318BQ ISSUE B

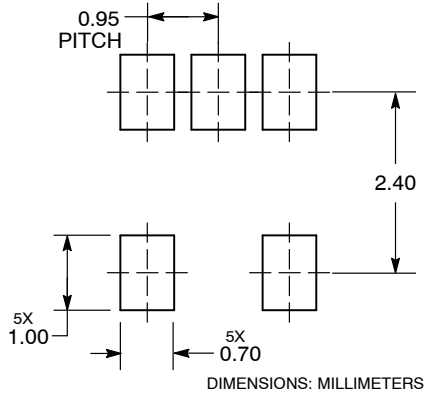


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.90 | 1.10 |
| A1 | 0.01 | 0.10 |
| b | 0.25 | 0.50 |
| c | 0.10 | 0.26 |
| D | 2.85 | 3.15 |
| E | 2.50 | 3.00 |
| E1 | 1.35 | 1.65 |
| e | 0.95 BSC | |
| L | 0.20 | 0.60 |
| M | 0° | 10° |

RECOMMENDED SOLDERING FOOTPRINT*

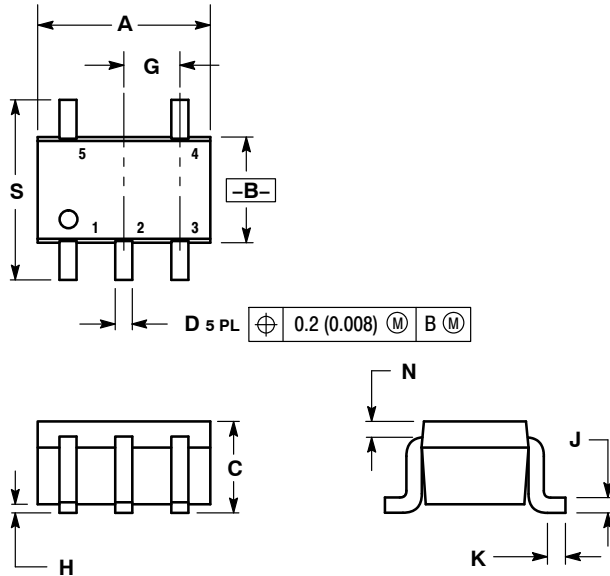


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

SC-88A (SC-70-5/SOT-353)
CASE 419A-02
ISSUE L

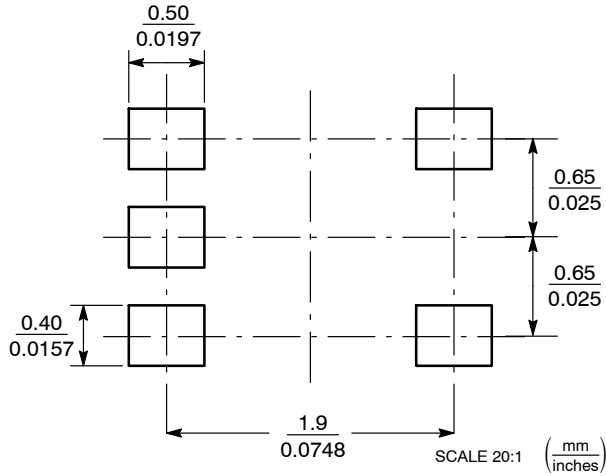


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.071 | 0.087 | 1.80 | 2.20 |
| B | 0.045 | 0.053 | 1.15 | 1.35 |
| C | 0.031 | 0.043 | 0.80 | 1.10 |
| D | 0.004 | 0.012 | 0.10 | 0.30 |
| G | 0.026 BSC | | 0.65 BSC | |
| H | --- | 0.004 | --- | 0.10 |
| J | 0.004 | 0.010 | 0.10 | 0.25 |
| K | 0.004 | 0.012 | 0.10 | 0.30 |
| N | 0.008 REF | | 0.20 REF | |
| S | 0.079 | 0.087 | 2.00 | 2.20 |

SOLDER FOOTPRINT



STYLE 1:

- PIN 1. BASE
- 2. EMITTER
- 3. BASE
- 4. COLLECTOR
- 5. COLLECTOR

STYLE 2:

- PIN 1. ANODE
- 2. EMITTER
- 3. BASE
- 4. COLLECTOR
- 5. CATHODE

STYLE 3:

- PIN 1. ANODE 1
- 2. N/C
- 3. ANODE 2
- 4. CATHODE 2
- 5. CATHODE 1

STYLE 4:

- PIN 1. SOURCE 1
- 2. DRAIN 1/2
- 3. SOURCE 1
- 4. GATE 1
- 5. GATE 2

STYLE 5:

- PIN 1. CATHODE
- 2. COMMON ANODE
- 3. CATHODE 2
- 4. CATHODE 3
- 5. CATHODE 4

STYLE 6:

- PIN 1. EMITTER 2
- 2. BASE 2
- 3. EMITTER 1
- 4. COLLECTOR
- 5. COLLECTOR 2/BASE 1

STYLE 7:

- PIN 1. BASE
- 2. EMITTER
- 3. BASE
- 4. COLLECTOR
- 5. COLLECTOR


STYLE 8:

- PIN 1. CATHODE
- 2. COLLECTOR
- 3. N/C
- 4. BASE
- 5. EMITTER

STYLE 9:

- PIN 1. ANODE
- 2. CATHODE
- 3. ANODE
- 4. ANODE
- 5. ANODE

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