LAN9303M/LAN9303Mi

Small Form Factor Three Port 10/100 Managed Ethernet Switch with Dual MII/RMII/Turbo MII

PRODUCT FEATURES

Datasheet

Highlights

- Up to 200Mbps via Turbo MII Interface
- 2nd MII/RMII/Turbo MII interface allows connection to an external MOCA, HomePNA, HomePlug, cable/DSL modem module or 2nd SOC with speeds up to 200Mbps
- High performance, full featured 3 port switch with VLAN, QoS packet prioritization, Rate Limiting, IGMP monitoring and management functions
- Serial management via I^2C or SMI
- Unique Virtual PHY feature simplifies software development by mimicking the multiple switch ports as a single port PHY

Target Applications

- Cable, satellite, and IP set-top boxes
- Digital televisions
- Digital video recorders
- VoIP/Video phone systems
- Home gateways
- Test/Measurement equipment
- Industrial automation systems

Key Benefits

- Ethernet Switch Fabric
  - 32K buffer RAM
  - 512 entry forwarding table
  - Port based IEEE 802.1Q VLAN support (16 groups)
    - Programmable IEEE 802.1Q tag insertion/removal
  - IEEE 802.1D spanning tree protocol support
  - 4 separate transmit queues available per port
  - Fixed or weighted egress priority servicing
  - QoS/CoS Packet prioritization
    - Input priority determined by VLAN tag, DA lookup, TOS, DIFFSERV or port default value
    - Programmable Traffic Class map based on input priority on per port basis
    - Remapping of 802.1Q priority field on per port basis
    - Programmable rate limiting at the ingress with coloring and random early discard, per port / priority
    - Programmable rate limiting at the egress with leaky bucket algorithm, per port / priority
  - IGMP v1/v2/v3 monitoring for Multicast packet filtering
  - Programmable broadcast storm protection with global % control and enable per port
  - Programmable buffer usage limits
  - Dynamic queues on internal memory
  - Programmable filter by MAC address
- Switch Management
  - Port mirroring/monitoring/sniffing: ingress and/or egress traffic on any port or port pair
  - Fully compliant statistics (MIB) gathering counters
  - Control registers configurable on-the-fly
- Ports
  - Port 0 - MII MAC, MII PHY, RMII PHY modes
  - Port 1 - MII MAC, MII PHY, RMII PHY mode options
  - 2 internal 10/100 PHYs with HP Auto-MDIX support
  - 200Mbps Turbo MII (PHY or MAC mode)
  - Fully compliant with IEEE 802.3 standards
  - 10BASE-T and 100BASE-TX support
  - Full and half duplex support
  - Full duplex flow control
  - Backpressure (forced collision) half duplex flow control
  - Automatic flow control based on programmable levels
  - Automatic 32-bit CRC generation and checking
  - 2K Jumbo packet support
  - Programmable interframe gap, flow control pause value
  - Full transmit/receive statistics
  - Full LED support per port
  - Auto-negotiation
  - Automatic polarity correction
  - Automatic MDI/MDI-X
  - Loop-back mode
- Serial Management
  - I^2C (slave) access to all internal registers
  - MIIM (MDIO) access to PHY related registers
  - SMI (extended MIIM) access to all internal registers
- Other Features
  - General Purpose Timer
  - I^2C Serial EEPROM interface
  - Programmable GPIOs/LEDs
- Single 3.3V power supply
- ESD Protection Levels
  - ±8kV HBM without External Protection Devices
  - ±8kV contact mode (IEC61000-4-2)
  - ±15kV air-gap discharge mode (IEC61000-4-2)
- Latch-up exceeds ±150mA per EIA/JESD 78
- 72-pin QFN (10x10 mm) Lead-Free RoHS Compliant Package
- Available in Commercial & Industrial Temp. Ranges

Order Number(s):

LAN9303M-AKZE for 72-Pin, QFN Lead-Free RoHS Compliant Package (0 to 70°C Temp Range)

LAN9303Mi-AKZE for 72-Pin, QFN Lead-Free RoHS Compliant Package (-40 to 85°C Temp Range)

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

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Chapter 1 Preface

1.1 General Terms

10BASE-T	10BASE-T (10Mbps Ethernet, IEEE 802.3)
100BASE-TX	100BASE-TX (100Mbps Fast Ethernet, IEEE 802.3u)
ADC	Analog-to-Digital Converter
ALR	Address Logic Resolution
BLW	Baseline Wander
BM	Buffer Manager - Part of the switch fabric
BPDU	Bridge Protocol Data Unit - Messages which carry the Spanning Tree Protocol information
Byte	8-bits
CSMA/CD	Carrier Sense Multiple Access / Collision Detect
CSR	Control and Status Registers
CTR	Counter
DA	Destination Address
DWORD	32-bits
EPC	EEPROM Controller
FCS	Frame Check Sequence - The extra checksum characters added to the end of an Ethernet frame, used for error detection and correction.
FIFO	First In First Out buffer
FSM	Finite State Machine
GPIO	General Purpose I/O
Host	External system (Includes processor, application software, etc.)
IGMP	Internet Group Management Protocol
Inbound	Refers to data input to the device from the host
Level-Triggered Sticky Bit	This type of status bit is set whenever the condition that it represents is asserted. The bit remains set until the condition is no longer true, and the status bit is cleared by writing a zero.
lsb	Least Significant Bit
LSB	Least Significant Byte
MDI	Medium Dependant Interface
MDIX	Media Independent Interface with Crossover
MII	Media Independent Interface

MIIM	Media Independent Interface Management
MIL	MAC Interface Layer
MLT-3	Multi-Level Transmission Encoding (3-Levels). A tri-level encoding method where a change in the logic level represents a code bit “1” and the logic output remaining at the same level represents a code bit “0”.
msb	Most Significant Bit
MSB	Most Significant Byte
NRZI	Non Return to Zero Inverted. This encoding method inverts the signal for a “1” and leaves the signal unchanged for a “0”
N/A	Not Applicable
NC	No Connect
OUI	Organizationally Unique Identifier
Outbound	Refers to data output from the device to the host
PISO	Parallel In Serial Out
PLL	Phase Locked Loop
PTP	Precision Time Protocol
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
RTC	Real-Time Clock
SA	Source Address
SFD	Start of Frame Delimiter - The 8-bit value indicating the end of the preamble of an Ethernet frame.
SIPO	Serial In Parallel Out
SMI	Serial Management Interface
SQE	Signal Quality Error (also known as “heartbeat”)
SSD	Start of Stream Delimiter
UDP	User Datagram Protocol - A connectionless protocol run on top of IP networks
UUID	Universally Unique IDentifier
WORD	16-bits

Chapter 2 Introduction

2.1 General Description

The LAN9303M/LAN9303Mi is a full featured, 3 port 10/100 managed Ethernet switch designed for embedded applications where performance, flexibility, ease of integration and system cost control are required. The LAN9303M/LAN9303Mi combines all the functions of a 10/100 switch system, including the Switch Fabric, packet buffers, Buffer Manager, Media Access Controllers (MACs), PHY transceivers, and serial management. The LAN9303M/LAN9303Mi complies with the IEEE 802.3 (full/half-duplex 10BASE-T and 100BASE-TX) Ethernet protocol specification and 802.1D/802.1Q network management protocol specifications, enabling compatibility with industry standard Ethernet and Fast Ethernet applications.

At the core of the device is the high performance, high efficiency 3 port Ethernet Switch Fabric. The Switch Fabric contains a 3 port VLAN layer 2 Switch Engine that supports untagged, VLAN tagged, and priority tagged frames. The Switch Fabric provides an extensive feature set which includes spanning tree protocol support, multicast packet filtering and Quality of Service (QoS) packet prioritization by VLAN tag, destination address, port default value or DIFFSERV/TOS, allowing for a range of prioritization implementations. 32K of buffer RAM allows for the storage of multiple packets while forwarding operations are completed, and a 512 entry forwarding table provides ample room for MAC address forwarding tables. Each port is allocated a cluster of 4 dynamic QoS queues which allow each queue size to grow and shrink with traffic, effectively utilizing all available memory. This memory is managed dynamically via the Buffer Manager block within the Switch Fabric. All aspects of the Switch Fabric are managed via the Switch Fabric configuration and status registers, which are indirectly accessible via the system control and status registers.

The LAN9303M/LAN9303Mi provides 3 switched ports. Each port is fully compliant with the IEEE 802.3 standard and all internal MACs and PHYs support full/half duplex 10BASE-T and 100BASE-TX operation. The LAN9303M/LAN9303Mi provides 2 on-chip PHYs, 1 Virtual PHY and 3 MACs. The Virtual PHY and the third MAC are used to connect the Switch Fabric to an external MAC or PHY. In MAC mode, the device can be connected to an external PHY via the MII/Turbo MII interface. In PHY mode, the device can be connected to an external MAC via the MII/RMII/Turbo MII interface. Optionally, the internal PHY on Port 1 can be disabled and the associated Switch Fabric port operated in the MII/Turbo MII PHY, RMII PHY, or MII/Turbo MII MAC modes. All ports support automatic or manual full duplex flow control or half duplex backpressure (forced collision) flow control. 2K jumbo packet (2048 byte) support allows for oversized packet transfers, effectively increasing throughput while decreasing CPU load. All MAC and PHY related settings are fully configurable via their respective registers within the device.

The integrated I^2C and SMI slave controllers allow for full serial management of the device via the integrated I^2C or MII interface, respectively. The inclusion of these interfaces allows for greater flexibility in the incorporation of the device into various designs. It is this flexibility which allows the device to operate in 2 different modes and under various management conditions. In both MAC and PHY modes, the device can be SMI managed or I^2C managed. This flexibility in management makes the LAN9303M/LAN9303Mi a candidate for virtually all switch applications.

The LAN9303M/LAN9303Mi contains an I^2C master EEPROM controller for connection to an optional EEPROM. This allows for the storage and retrieval of static data. The internal EEPROM Loader can be optionally configured to automatically load stored configuration settings from the EEPROM into the device at reset. The I^2C management slave and master EEPROM controller share common pins.

In addition to the primary functionality described above, the LAN9303M/LAN9303Mi provides additional features designed for extended functionality. These include a configurable 16-bit General Purpose Timer (GPT), a 32-bit 25MHz free running counter, and 6-bit configurable GPIO/LED interface.

The LAN9303M/LAN9303Mi's performance, features and small size make it an ideal solution for many applications in the consumer electronics and industrial automation markets. Targeted applications include: set top boxes (cable, satellite and IP), digital televisions, digital video recorders, voice over IP and video phone systems, home gateways, and test and measurement equipment.

2.2 Block Diagram

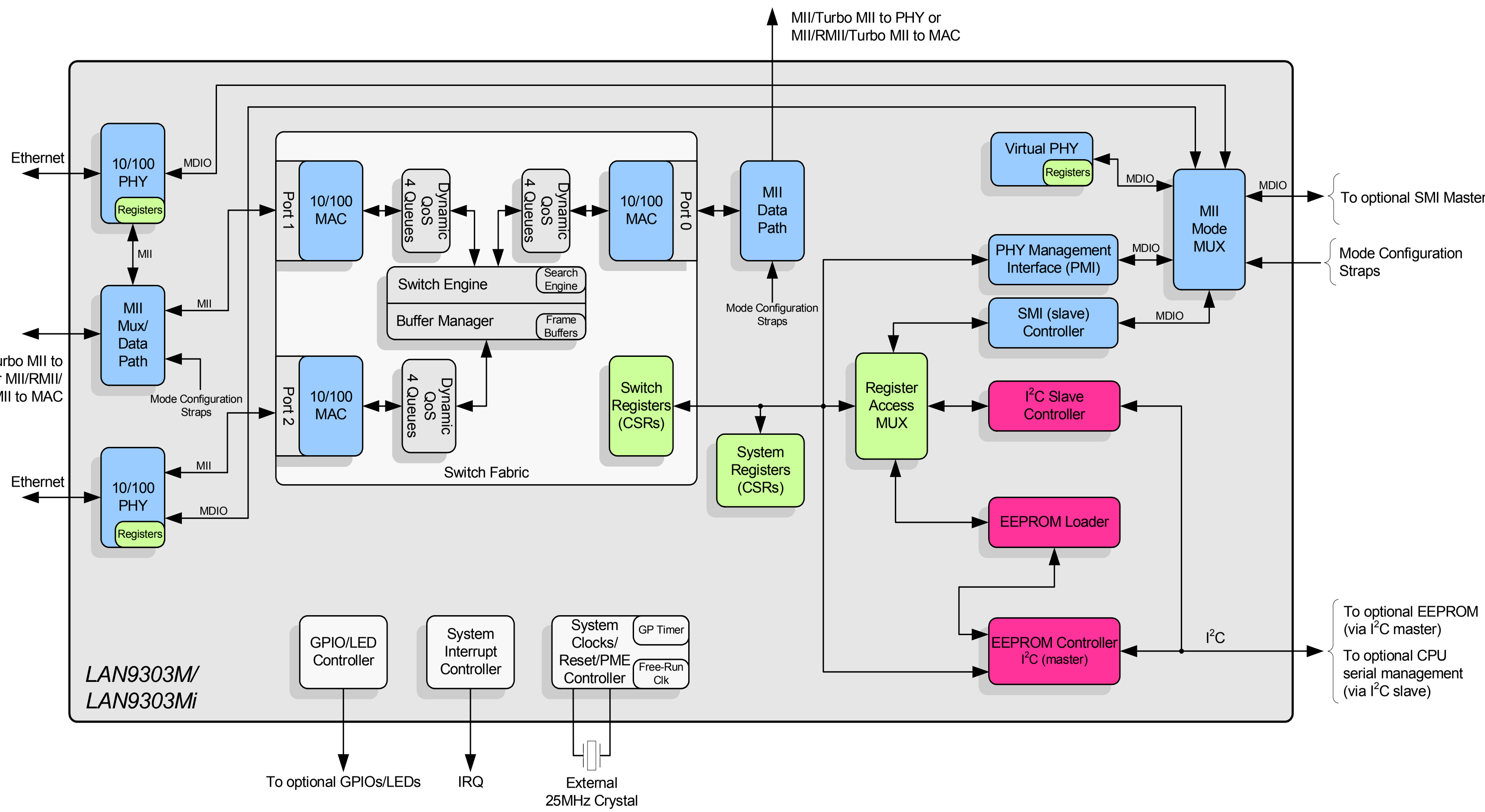


Figure 2.1 Internal Block Diagram

2.2.1 System Clocks/Reset/PME Controller

A clock module generates all the system clocks required by the device. This module interfaces directly with the external 25MHz crystal/oscillator to generate the required clock divisions for each internal module. A 16-bit general purpose timer and 32-bit free-running clock are provided by this module for general purpose use. The Port 1 & 2 PHYs provide general power-down and energy detect power-down modes, which allow a reduction in PHY power consumption.

The device reset events are categorized as chip-level resets, multi-module resets, and single-module resets. These reset events are summarized below:

- **Chip Level Resets**
  —Power-On Reset (Entire chip reset)
  —nRST Pin Reset (Entire chip reset)
- **Multi-Module Reset**
  —Digital Reset (All sub-modules except Ethernet PHYs)
- **Single-Module Resets**
  —Port 2 PHY Reset
  —Port 1 PHY Reset
  —Virtual PHY Reset

2.2.2 System Interrupt Controller

The device provides a multi-tier programmable interrupt structure which is controlled by the System Interrupt Controller. Top level interrupt registers aggregate and control all interrupts from the various sub-modules. The device is capable of generating interrupt events from the following:

- **Switch Fabric**
- **Ethernet PHYs**
- **GPIOs**
- **General Purpose Timer**
- **Software (general purpose)**

A dedicated programmable IRQ interrupt output pin is provided for external indication of any device interrupts. The IRQ buffer type, polarity, and de-assertion interval are register configurable.

2.2.3 Switch Fabric

The Switch Fabric consists of the following major function blocks:

- **10/100 MACs**
  There is one 10/100 Ethernet MAC per Switch Fabric port, which provides basic 10/100 Ethernet functionality, including transmission deferral, collision back-off/retry, TX/RX FCS checking/generation, TX/RX pause flow control, and transmit back pressure. The 10/100 MACs act as an interface between the Switch Engine and the 10/100 PHYs (for ports 1 and 2) or optional external PHY/MAC on port 1. The port 0 10/100 MAC interfaces the Switch Engine to the external MAC/PHY (see Section 2.3, "Modes of Operation"). Each 10/100 MAC includes RX and TX FIFOs and per port statistic counters.
- **Switch Engine**
  This block, consisting of a 3 port VLAN layer 2 switching engine, provides the control for all forwarding/filtering rules and supports untagged, VLAN tagged, and priority tagged frames. The Switch Engine provides an extensive feature set which includes spanning tree protocol support, multicast packet filtering and Quality of Service (QoS) packet prioritization by VLAN tag, destination address, and port default value or DIFFSERV/TOS, allowing for a range of prioritization implementations. A 512 entry forwarding table provides ample room for MAC address forwarding tables.

- **Buffer Manager**
  This block controls the free buffer space, multi-level transmit queues, transmission scheduling, and packet dropping of the Switch Fabric. 32K of buffer RAM allows for the storage of multiple packets while forwarding operations are completed. Each port is allocated a cluster of 4 dynamic QoS queues which allow each queue size to grow and shrink with traffic, effectively utilizing all available memory. This memory is managed dynamically via the Buffer Manager block.
- **Switch CSRs**
  This block contains all switch related control and status registers, and allows all aspects of the Switch Fabric to be managed. These registers are indirectly accessible via the system control and status registers.

2.2.4 Ethernet PHYs

The device contains three PHYs: Port 1 PHY, Port 2 PHY and a Virtual PHY. The Port 1 & 2 PHYs are identical in functionality and each connect their corresponding Ethernet signal pins to the Switch Fabric MAC of their respective port. These PHYs interface with their respective MAC via an internal MII interface. The Virtual PHY provides the virtual functionality of a PHY and allows connection of an external MAC to port 0 of the Switch Fabric as if it was connected to a single port PHY. All PHYs comply with the IEEE 802.3 Physical Layer for Twisted Pair Ethernet and can be configured for full/half duplex 100 Mbps (100BASE-TX) or 10Mbps (10BASE-T) Ethernet operation. All PHY registers follow the IEEE 802.3 (clause 22.2.4) specified MII management register set.

2.2.5 PHY Management Interface (PMI)

The PHY Management Interface (PMI) is used to serially access the internal PHYs as well as the external PHY on the MII pins (in MAC mode only, see Section 2.3, "Modes of Operation"). The PMI implements the IEEE 802.3 management protocol, providing read/write commands for PHY configuration.

2.2.6 I^{2}C Slave Controller

This module provides an I^{2}C slave interface which can be used for CPU serial management of the device. The I^{2}C slave controller implements the low level I^{2}C slave serial interface (start and stop condition detection, data bit transmission/reception, and acknowledge generation/reception), handles the slave command protocol, and performs system register reads and writes. The I^{2}C slave controller conforms to the NXP *I^{2}C-Bus Specification*. A list of management modes and configurations settings for these modes is discussed in Section 2.3, "Modes of Operation"

2.2.7 SMI Slave Controller

This module provides a SMI slave interface which can be used for CPU management of the device via the MII pins, and allows CPU access to all system CSRs. SMI uses the same pins and protocol of the IEEE MII management function, and differs only in that SMI provides access to all internal registers by using a non-standard extended addressing map. The SMI protocol co-exists with the MII management protocol by using the upper half of the PHY address space (16 through 31). A list of management modes and configurations settings for these modes is discussed in Section 2.3, "Modes of Operation"

2.2.8 EEPROM Controller/Loader

The EEPROM Controller is an I^{2}C master module which interfaces an optional external EEPROM with the system register bus and the EEPROM Loader. Multiple sizes of external EEPROMs are supported along with various EEPROM commands, allowing for the efficient storage and retrieval of static data. The I^{2}C interface conforms to the NXP *I^{2}C-Bus Specification*.

The EEPROM Loader module interfaces to the EEPROM Controller, Ethernet PHYs, and the system CSRs. The EEPROM Loader provides the automatic loading of configuration settings from the EEPROM into the device at reset, allowing the device to operate unmanaged. The EEPROM Loader runs upon a pin reset (nRST), power-on reset (POR), digital reset, or upon the issuance of a EEPROM RELOAD command.

2.2.9 GPIO/LED Controller

Six configurable general-purpose input/output pins are provided which are controlled via this module. These pins can be individually configured via the GPIO/LED CSRs to function as inputs, push-pull outputs, or open drain outputs and each is capable of interrupt generation with configurable polarity. The GPIO pins can be alternatively configured as LED outputs to drive Ethernet status LEDs for external indication of various attributes of the switch ports.

2.3 Modes of Operation

The LAN9303M/LAN9303Mi is designed to integrate into various embedded environments. To accomplish compatibility with a wide range of applications, the LAN9303M/LAN9303Mi ports can operate in the following modes:

- Port 0 - Independently configured for MII MAC, MII PHY, RMII PHY modes
- Port 1 - Independently configured for internal PHY, MII MAC, MII PHY, RMII PHY modes
- Port 2 - Internal PHY mode

The mode of the device is determined by the P0_MODE[2:0] (Port 0) and P1_MODE[2:0] (Port 1) pin straps.

The device can also be placed into the following management modes:

- SMI managed
- I^2C managed

The management mode is determined by the MNGT1_LED4P and MNGT0_LED3P pin straps. These modes are detailed in the following sections. Figure 2.4 displays a typical system configuration for each Port 0 mode and management type supported by the device. Refer to Chapter 9, "MII Data Interfaces," on page 129 for additional information on the usage of MII signals in each supported mode.

2.3.1 Internal PHY Mode

Internal PHY mode (Port 1 and Port 2) utilizes the internal PHY for the network connection. The Switch Engine MAC's MII port is connected internally to the internal PHY in this mode. Internal PHY mode can operate at 10Mbps or 100Mbps.

When an EEPROM is connected, the EEPROM loader can be used to load the initial device configuration from the external EEPROM via the I^2C interface. Once operational, if managed, the CPU can use the I^2C interface to read or write the EEPROM.

2.3.2 MAC Mode

Both Port 0 and Port 1 can be configured independently into MAC mode. MAC mode utilizes an external PHY, which is connected to the port's MII pins, to provide an Ethernet network connection. In this mode, the port acts as a MAC, providing a communication path between the Switch Fabric and the external PHY. MAC mode can operate at 10, 100, or 200Mbps (Turbo mode). In MAC mode, the device may be SMI managed or I^2C managed as detailed in Section 2.3.4, "Management Modes".

When an EEPROM is connected, the EEPROM loader can be used to load the initial device configuration from the external EEPROM via the I^2C interface. Once operational, if managed, the CPU can use the I^2C interface to read or write the EEPROM.

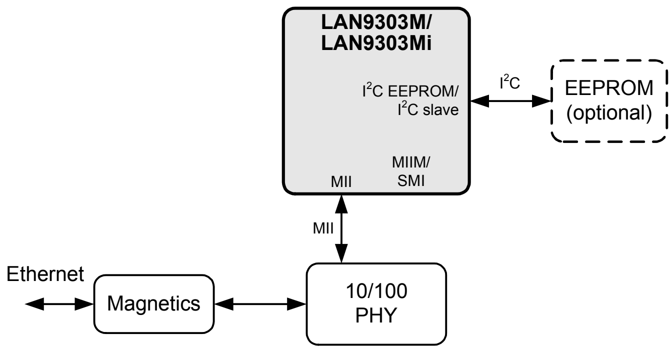


Figure 2.2 MII MAC Mode

2.3.3 PHY Mode

Both Port 0 and Port 1 can be configured independently into PHY mode. PHY mode utilizes an external MAC to provide a network path for the CPU. PHY mode supports MII and RMII interfaces. The external MII/RMII pins must be connected to an external MAC, providing a communication path to the Switch Fabric. MII PHY mode can operate at 10, 100, or 200Mbps (Turbo mode). RMII PHY mode can operate at 10 or 100Mbps. In PHY mode, the device may be SMI managed or I^2C managed as detailed in Section 2.3.4, "Management Modes".

When an EEPROM is connected, the EEPROM loader can be used to load the initial device configuration from the external EEPROM via the I^2C interface. Once operational, if managed, the CPU can use the I^2C interface to read or write the EEPROM.

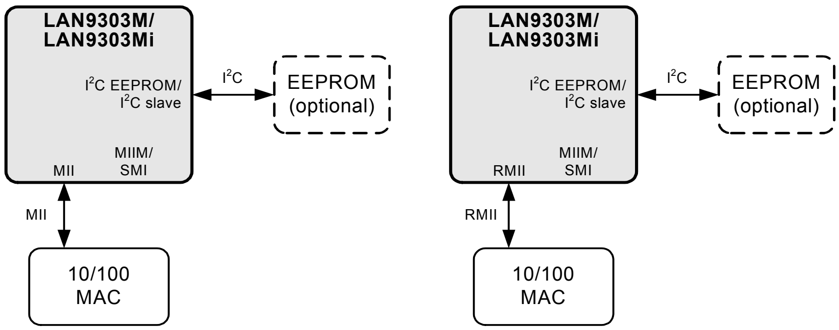


Figure 2.3 MII/RMII PHY Mode

2.3.4 Management Modes

Various modes of management are provided in both MAC and PHY modes of operation. Two separate interfaces may be used for management: the I^2C interface or the SMI/MIIM (Media Independent Interface Management) slave interface.

The I^2C interface runs as an I^2C slave. The slave mode is used as a register access path for an external CPU. The I^2C slave and I^2C master EEPROM interface are shared interfaces.

The SMI/MIIM interface runs as either an SMI/MIIM slave or MIIM master. The master mode is used to access an external PHYs registers under CPU control (assuming the CPU is using I^2C). The slave mode is used for register access by the CPU or external MAC and provides access to either the internal Port 1&2 PHY registers or to all non-PHY registers (using addresses 16-31 and a non-standard extended address map). MIIM and SMI use the same pins and protocol and differ only in that SMI provides access to all internal registers while MIIM provides access to only the Port 1&2 PHY registers. A special mode provides access to the Virtual PHY, which mimics the register operation of a single port standalone PHY. This is used for software compatibility in managed operation.

The selection of management modes is determined at startup via the P0_MODE[2:0], MNGT1_LED4P, and MNGT0_LED3P straps as detailed in Table 2.1. System configuration diagrams for each mode are provided in Figure 2.4.

Note: The management mode is dependant on the mode of Port 0 (MAC or PHY mode). The Port 1 mode (MAC, PHY, or internal) is configured independently from the management mode.

Table 2.1 Device Modes

MODE	I^2C INTERFACE (MASTER/SLAVE)	SMI/MIIM INTERFACE	P0_MODE[2:0] STRAP VALUE	MNGT1_LED4P, MNGT0_LED3PSTRAP VALUE
MAC SMI	I^2C master used to load initial configuration from EEPROM and for CPU R/W access to EEPROM	SMI/MIIM slave, used for CPU access to internal PHYs and non-PHY registers	000	01
MAC I^2C	I^2C master used to load initial configuration from EEPROM and for CPU R/W access to EEPROM I^2C slave used for management	MIIM master, used for CPU access to external PHY registers	000	10
PHY SMI	I^2C master used to load initial configuration from EEPROM and for CPU R/W access to EEPROM	SMI/MIIM slave, used for CPU access to internal PHYs, Virtual PHY, and non-PHY registers	001, 010, 011, 100, 101, or 110	01
PHY I^2C	I^2C master used to load initial configuration from EEPROM and for CPU R/W access to EEPROM I^2C slave used for management	Virtual MIIM slave, used for external MAC access to Virtual PHY registers	001, 010, 011, 100, 101, or 110	10

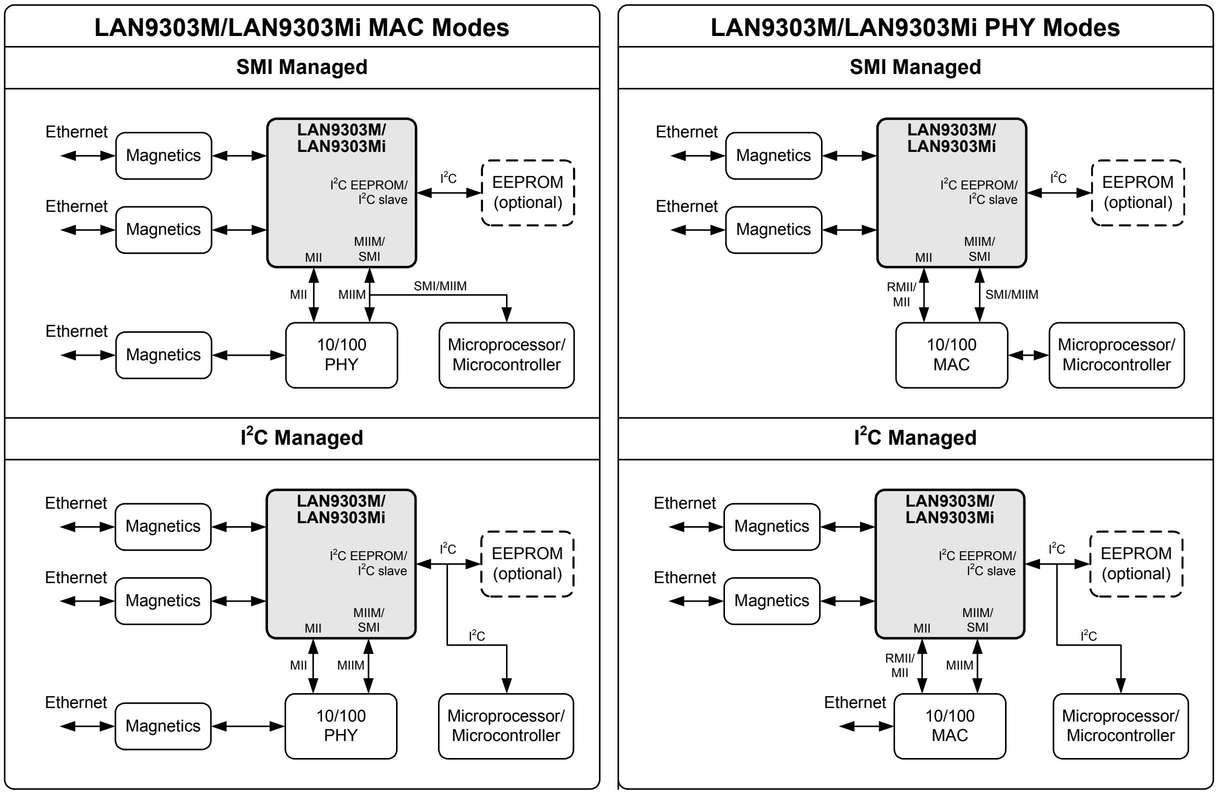
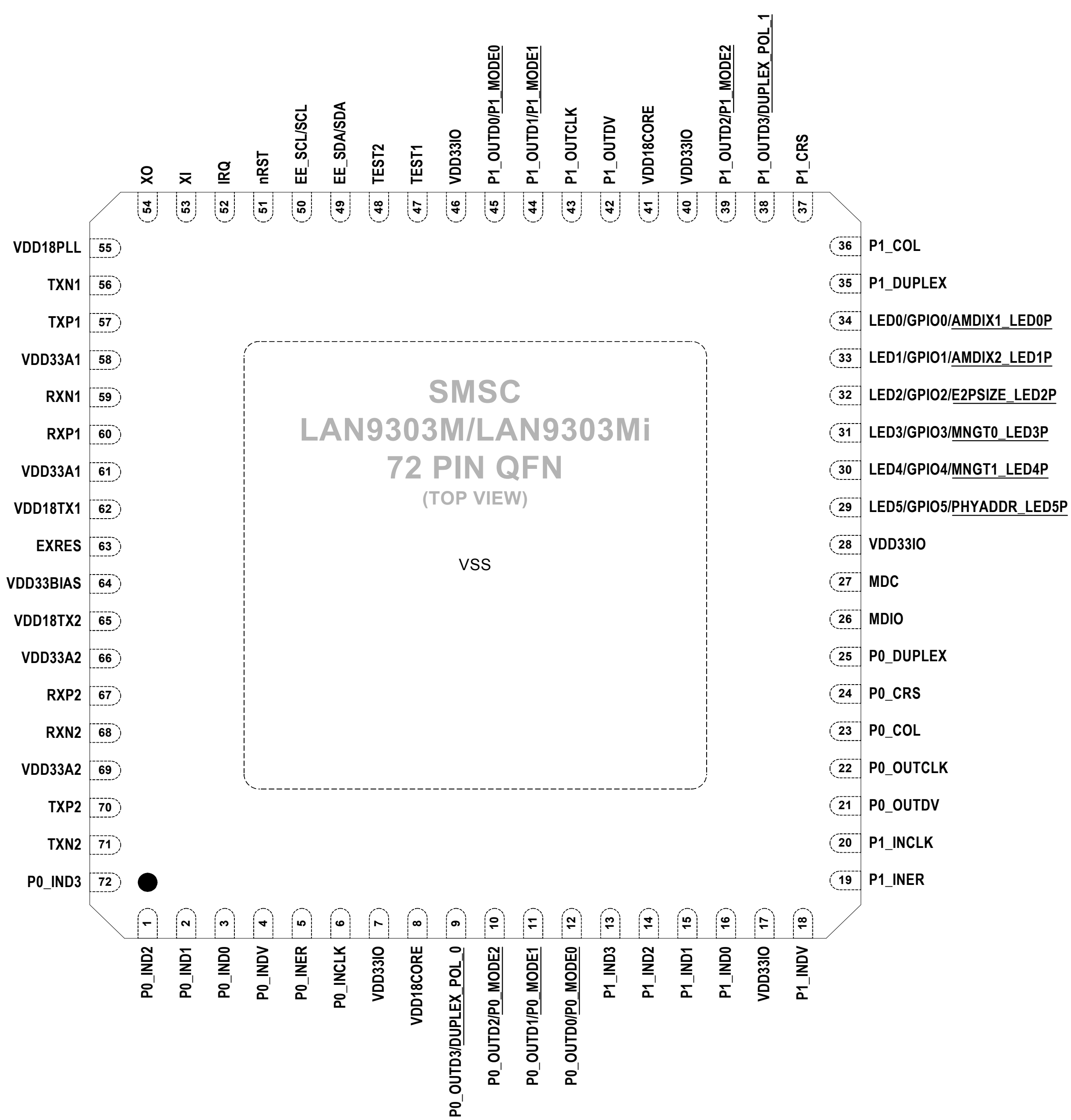


Figure 2.4 Port 0 MAC/PHY Management Modes

Chapter 3 Pin Description and Configuration

3.1 Pin Diagram

3.1.1 72-QFN Pin Diagram



NOTE: When HP Auto-MDIX is activated, the TXN/TXP pins can function as RXN/RXP and vice-versa

NOTE: Exposed pad (VSS) on bottom of package must be connected to ground

Figure 3.1 Pin Assignments (TOP VIEW)

3.2 Pin Descriptions

This section contains the descriptions of the device pins. The pin descriptions have been broken into functional groups as follows:

- LAN Port 1 Pins
- LAN Port 2 Pins
- LAN Port 1 & 2 Power and Common Pins
- Port 1 MII/RMII Pins
- Port 0 MII/RMII Pins
- GPIO/LED/Configuration Straps
- Serial Management/EEPROM Pins
- Miscellaneous Pins
- PLL Pins
- Core and I/O Power and Ground Pins

Note: A list of buffer type definitions is provided in Section 3.3, "Buffer Types," on page 47.

Note: Please refer to the LAN9303M/LAN9303Mi Reference Schematic and LANCheck Schematic Checklist on the SMSC website for additional connection information.

Table 3.1 LAN Port 1 Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Port 1 Ethernet TX Negative	TXN1	AIO	Negative output of Port 1 Ethernet transmitter. See Note 3.1.
1	Port 1 Ethernet TX Positive	TXP1	AIO	Positive output of Port 1 Ethernet transmitter. See Note 3.1.
1	Port 1 Ethernet RX Negative	RXN1	AIO	Negative input of Port 1 Ethernet receiver. See Note 3.1.
1	Port 1 Ethernet RX Positive	RXP1	AIO	Positive input of Port 1 Ethernet receiver. See Note 3.1.

Note 3.1 The pin names for the twisted pair pins apply to a normal connection. If HP Auto-MDIX is enabled and a reverse connection is detected or manually selected, the RX and TX pins will be swapped internally.

Table 3.2 LAN Port 2 Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Port 2 Ethernet TX Negative	TXN2	AIO	Negative output of Port 2 Ethernet transmitter. See Note 3.2.
1	Port 2 Ethernet TX Positive	TXP2	AIO	Positive output of Port 2 Ethernet transmitter. See Note 3.2.

Table 3.2 LAN Port 2 Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Port 2 Ethernet RX Negative	RXN2	AIO	Negative input of Port 2 Ethernet receiver. See Note 3.2.
1	Port 2 Ethernet RX Positive	RXP2	AIO	Positive input of Port 2 Ethernet receiver. See Note 3.2.

Note 3.2 The pin names for the twisted pair pins apply to a normal connection. If HP Auto-MDIX is enabled and a reverse connection is detected or manually selected, the RX and TX pins will be swapped internally.

Table 3.3 LAN Port 1 & 2 Power and Common Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Bias Reference	EXRES	AI	Used for internal bias circuits. Connect to an external 12.4K ohm, 1% resistor to ground.
2	+3.3V Port 1 Analog Power Supply	VDD33A1	P	See Note 3.3.
2	+3.3V Port 2 Analog Power Supply	VDD33A2	P	See Note 3.3.
1	+3.3V Master Bias Power Supply	VDD33BIAS	P	See Note 3.3.
1	Port 2 Transmitter +1.8V Power Supply	VDD18TX2	P	This pin is supplied from the internal PHY voltage regulator. This pin must be tied to the VDD18TX1 pin for proper operation. See Note 3.3.
1	Port 1 Transmitter +1.8V Power Supply	VDD18TX1	P	This pin must be connected directly to the VDD18TX2 pin for proper operation. See Note 3.3.

Note 3.3 Please refer to the LAN9303M/LAN9303Mi Reference Schematic and LANCheck Schematic Checklist on the SMSC website for additional connection information.

Table 3.4 Port 1 MII/RMII Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Port 1 MII Input Data 3	P1_IND3	IS (PD)	**MII MAC Mode:** This pin is the receive data 3 bit from the external PHY to the switch.
			IS (PD)	**MII PHY Mode:** This pin is the transmit data 3 bit from the external MAC to the switch. The pull-down and input buffer are disabled when the Isolate bit is set in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL).
			-	**RMII PHY Mode:** This pin is not used.
			(PD)	**Internal PHY Mode:** This pin is not used.
1	Port 1 MII Input Data 2	P1_IND2	IS (PD)	**MII MAC Mode:** This pin is the receive data 2 bit from the external PHY to the switch.
			IS (PD)	**MII PHY Mode:** This pin is the transmit data 2 bit from the external MAC to the switch. The pull-down and input buffer are disabled when the Isolate bit is set in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL).
			-	**RMII PHY Mode:** This pin is not used.
			(PD)	**Internal PHY Mode:** This pin is not used.
1	Port 1 MII Input Data 1	P1_IND1	IS (PD)	**MII MAC Mode:** This pin is the receive data 1 bit from the external PHY to the switch.
			IS (PD)	**MII PHY Mode:** This pin is the transmit data 1 bit from the external MAC to the switch. The pull-down and input buffer are disabled when the Isolate bit is set in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL).
			IS (PD)	**RMII PHY Mode:** This pin is the transmit data 1 bit from the external MAC to the switch. The pull-down and input buffer are disabled when the Isolate bit is set in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL).
			(PD)	**Internal PHY Mode:** This pin is not used.
1	Port 1 MII Input Data 0	P1_IND0	IS (PD)	**MII MAC Mode:** This pin is the receive data 0 bit from the external PHY to the switch.
			IS (PD)	**MII PHY Mode:** This pin is the transmit data 0 bit from the external MAC to the switch. The pull-down and input buffer are disabled when the Isolate bit is set in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL).
			IS (PD)	**RMII PHY Mode:** This pin is the transmit data 0 bit from the external MAC to the switch. The pull-down and input buffer are disabled when the Isolate bit is set in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL).
			(PD)	**Internal PHY Mode:** This pin is not used.

Table 3.4 Port 1 MII/RMII Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Port 1 MII Input Data Valid	P1_INDV	IS (PD)	**MII MAC Mode:** This pin is the RX_DV signal from the external PHY and indicates valid data on P1_IND[3:0] and P1_INER.
			IS (PD)	**MII PHY Mode:** This pin is the TX_EN signal from the external MAC and indicates valid data on P1_IND[3:0] and P1_INER. The pull-down and input buffer are disabled when the Isolate bit is set in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL).
			IS (PD)	**RMII PHY Mode:** This pin is the TX_EN signal from the external MAC and indicates valid data on P1_IND[1:0]. The pull-down and input buffer are disabled when the Isolate bit is set in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL).
			(PD)	**Internal PHY Mode:** This pin is not used.
1	Port 1 MII Input Error	P1_INER	IS (PD)	**MII MAC Mode:** This pin is the RX_ER signal from the external PHY and indicates a receive error in the packet.
			IS (PD)	**MII PHY Mode:** This pin is the TX_ER signal from the external MAC and indicates that the current packet should be aborted. The pull-down and input buffer are disabled when the Isolate bit is set in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL).
			-	**RMII PHY Mode:** This pin is not used.
			(PD)	**Internal PHY Mode:** This pin is not used.
1	Port 1 MII Input Reference Clock	P1_INCLK	IS (PD)	**MII MAC Mode:** This pin is an input and is used as the reference clock for the P1_IND[3:0], P1_INER, and P1_INDV pins. It is connected to the receive clock of the external PHY.
			O12/O16	**MII PHY Mode:** This pin is an output and is used as the reference clock for the P1_IND[3:0], P1_INER, and P1_INDV pins. It is connected to the transmit clock of the external MAC. The output driver is disabled when the Isolate bit is set in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL). When operating at 200MBps, the choice of drive strength is based on the setting of the RMII/Turbo MII Clock Strength bit in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL). A low selects a 12 mA drive, while a high selects a 16 mA drive. A series terminating resistor is recommended for the best PCB signal integrity.
			-	**RMII PHY Mode:** This pin is not used.
			(PD)	**Internal PHY Mode:** This pin is not used.

Table 3.4 Port 1 MII/RMII Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Port 1 MII Output Data 3	P1_OUTD3	O8	**MII MAC Mode:** This pin is the transmit data 3 bit from the switch to the external PHY.
			O8	**MII PHY Mode:** This pin is the receive data 3 bit from the switch to the external MAC. The output driver is disabled when the Isolate bit is set in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL).
			-	**RMII PHY Mode:** This pin is not used.
			-	**Internal PHY Mode:** This pin is not used.
	Port 1 Duplex Polarity Configuration Strap	DUPLEX_POL_1	IS (PU) Note 3.5	This strap selects the default of the duplex polarity strap for Port 1 MII (duplex_pol_strap_1) and is used only in MII PHY, RMII PHY, and MII MAC modes. See Note 3.4. If the strap is value is 0, a 0 on P1_DUPLEX means full duplex while a 1 means half duplex. If the strap value is 1, a 1 on P1_DUPLEX means full duplex, while a 0 means half duplex.
1	Port 1 MII Output Data 2	P1_OUTD2	O8	**MII MAC Mode:** This pin is the transmit data 2 bit from the switch to the external PHY.
			O8	**MII PHY Mode:** This pin is the receive data 2 bit from the switch to the external MAC. The output driver is disabled when the Isolate bit is set in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL).
			-	**RMII PHY Mode:** This pin is not used.
			-	**Internal PHY Mode:** This pin is not used.
	Port 1 Mode[2] Configuration Strap	P1_MODE2	IS (PU) Note 3.5	This strap configures the mode for the Port 1 MII pins. See Note 3.4. Please refer to the P1_MODE0 strap entry for mode encoding details.
1	Port 1 MII Output Data 1	P1_OUTD1	O8	**MII MAC Mode:** This pin is the transmit data 1 bit from the switch to the external PHY.
			O8	**MII PHY Mode:** This pin is the receive data 1 bit from the switch to the external MAC. The output driver is disabled when the Isolate bit is set in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL).
			O8	**RMII PHY Mode:** This pin is the receive data 1 bit from the switch to the external MAC. The output driver is disabled when the Isolate bit is set in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL).
			-	**Internal PHY Mode:** This pin is not used.
	Port 1 Mode[1] Configuration Strap	P1_MODE1	IS (PU) Note 3.5	This strap configures the mode for the Port 1 MII pins. See Note 3.4. Please refer to the P1_MODE0 strap entry for mode encoding details.

Table 3.4 Port 1 MII/RMII Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Port 1 MII Output Data 0	P1_OUTD0	O8	**MII MAC Mode:** This pin is the transmit data 0 bit from the switch to the external PHY.
			O8	**MII PHY Mode:** This pin is the receive data 0 bit from the switch to the external MAC. The output driver is disabled when the Isolate bit is set in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL).
			O8	**RMII PHY Mode:** This pin is the receive data 0 bit from the switch to the external MAC. The output driver is disabled when the Isolate bit is set in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL).
			-	**Internal PHY Mode:** This pin is not used.
	Port 1 Mode[0] Configuration Strap	P1_MODE0	IS (PU) Note 3.5	This strap configures the mode for the Port 1 MII pins. See Note 3.4. The P1_MODE[2:0] configuration strap encoding is as follows: 000 = MII MAC mode 001 = MII PHY mode 010 = MII PHY mode 200 Mbps 12 ma clock output 011 = MII PHY mode 200 Mbps 16 ma clock output 100 = RMII PHY mode clock is 12 ma output 101 = RMII PHY mode clock is 16 ma output 110 = RMII PHY mode clock is input 111 = Internal PHY mode
1	Port 1 MII Output Data Valid	P1_OUTDV	O8	**MII MAC Mode:** This pin is the TX_EN signal to the external PHY and indicates valid data on P1_OUTD[3:0].
			O8	**MII PHY Mode:** This pin is the RX_DV signal to the external MAC. The output driver is disabled when the Isolate bit is set in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL).
			O8	**RMII PHY Mode:** This pin is the CRS_DV signal to the external MAC. The output driver is disabled when the Isolate bit is set in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL).
			-	**Internal PHY Mode:** This pin is not used.

Table 3.4 Port 1 MII/RMII Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Port 1 MII Output Reference Clock	P1_OUTCLK	IS (PD)	**MII MAC Mode:** This pin is an input and is used as the reference clock for the P1_OUTD[3:0] and P1_OUTDV pins. It is connected to the transmit clock of the external PHY.
			O12/O16	**MII PHY Mode:** This pin is an output and is used as the reference clock for the P1_OUT[3:0] and P1_OUTDV pins. It is connected to the receive clock of the external MAC. The output driver is disabled when the Isolate bit is set in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL). When operating at 200MBps, the choice of drive strength is based on the setting of the RMII/Turbo MII Clock Strength bit in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL). A low selects a 12 mA drive, while a high selects a 16 mA drive. A series terminating resistor is recommended for the best PCB signal integrity.
			IS/O12/ O16 (PD)	**RMII PHY Mode:** This pin is an input or an output running at 50 MHz and is used as the reference clock for the P1_IND[1:0], P1_INDV, P1_OUTD[1:0], and P1_OUTDV pins. The choice of input verses output is based on the setting of the RMII Clock Direction bit in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL). A low selects P1_OUTCLK as an input and a high selects P1_OUTCLK as an output. As an input, the pull-down is normally enabled. The input buffer and pull-down are disabled when the Isolate bit is set in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL). As an output, the input buffer and pull-down are disabled. The choice of drive strength is based on the setting of the RMII/Turbo MII Clock Strength bit in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL). A low selects a 12 mA drive, while a high selects a 16 mA drive. The output driver is disabled when the Isolate bit is set in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL). A series terminating resistor is recommended for the best PCB signal integrity.
			(PD)	**Internal PHY Mode:** This pin is not used.
1	Port 1 MII Collision	P1_COL	IS (PU)	**MII MAC Mode:** This pin is an input from the external PHY and indicates a collision event.
			O8	**MII PHY Mode:** This pin is an output to the external MAC indicating a collision event. The output driver is disabled when the Isolate bit is set in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL).
			-	**RMII PHY Mode:** This pin is not used.
			(PU)	**Internal PHY Mode:** This pin is not used.

Table 3.4 Port 1 MII/RMII Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Port 1 MII Carrier Sense	P1_CRS	IS (PD)	**MII MAC Mode:** This pin is an input from the external PHY indicating a network carrier.
			O8	**MII PHY Mode:** This pin is an output to the external MAC indicating a network carrier. The output driver is disabled when the Isolate bit is set in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL).
			-	**RMII PHY Mode:** This pin is not used.
			(PD)	**Internal PHY Mode:** This pin is not used.
1	Port 1 MII Duplex	P1_DUPLEX	IS (PU)	**MII MAC Mode:** This pin can be changed at any time (live value) and can be overridden by enabling the Manual Duplex bit in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL). It is typically tied to the duplex indication from the external PHY. Please refer to the definition of the DUPLEX_POL_1 strap for further details.
			IS (PU)	**MII PHY and RMII PHY Modes:** This pin sets the default of the Duplex Mode bit in the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL) and is typically tied high or low as needed. The pull-up is enabled. Please refer to the definition of the DUPLEX_POL_1 strap for further details.
			(PU)	**Internal PHY Mode:** This pin is not used.

Note 3.4 Configuration strap pins are identified by an underlined symbol name. Configuration strap values are latched on power-on reset or nRST de-assertion. Each port has configuration straps that control its operation. Additional strap pins, which share functionality with the GPIO/LED pins, are described in Table 3.6. Some configuration straps can be overridden by values from the EEPROM Loader. Please refer to Section 4.2.4, "Configuration Straps," on page 52 for further information.

Note 3.5 An external supplemental pull-up may be needed, depending upon the input current loading of the external MAC/PHY device.

Table 3.5 Port 0 MII/RMII Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Port 0 MII Input Data 3	P0_IND3	IS (PD)	**MII MAC Mode:** This pin is the receive data 3 bit from the external PHY to the switch.
			IS (PD)	**MII PHY Mode:** This pin is the transmit data 3 bit from the external MAC to the switch. The pull-down and input buffer are disabled when the Isolate (VPHY_ISO) bit is set in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).
			-	**RMII PHY Mode:** This pin is not used.

Table 3.5 Port 0 MII/RMII Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Port 0 MII Input Data 2	P0_IND2	IS (PD)	**MII MAC Mode:** This pin is the receive data 2 bit from the external PHY to the switch.
			IS (PD)	**MII PHY Mode:** This pin is transmit data 2 bit from the external MAC to the switch. The pull-down and input buffer are disabled when the Isolate (VPHY_ISO) bit is set in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).
			-	**RMII PHY Mode:** This pin is not used.
1	Port 0 MII Input Data 1	P0_IND1	IS (PD)	**MII MAC Mode:** This pin is the receive data 1 bit from the external PHY to the switch.
			IS (PD)	**MII PHY Mode:** This pin is the transmit data 1 bit from the external MAC to the switch. The pull-down and input buffer are disabled when the Isolate (VPHY_ISO) bit is set in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).
			IS (PD)	**RMII PHY Mode:** This pin is the transmit data 1 bit from the external MAC to the switch. The pull-down and input buffer are disabled when the Isolate (VPHY_ISO) bit is set in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).
1	Port 0 MII Input Data 0	P0_IND0	IS (PD)	**MII MAC Mode:** This pin is the receive data 0 bit from the external PHY to the switch.
			IS (PD)	**MII PHY Mode:** This pin is the transmit data 0 bit from the external MAC to the switch. The pull-down and input buffer are disabled when the Isolate (VPHY_ISO) bit is set in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).
			IS (PD)	**RMII PHY Mode:** This pin is the transmit data 0 bit from the external MAC to the switch. The pull-down and input buffer are disabled when the Isolate (VPHY_ISO) bit is set in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).
1	Port 0 MII Input Data Valid	P0_INDV	IS (PD)	**MII MAC Mode:** This pin is the RX_DV signal from the external PHY and indicates valid data on P0_IND[3:0] and P0_INER.
			IS (PD)	**MII PHY Mode:** This pin is the TX_EN signal from the external MAC and indicates valid data on P0_IND[3:0] and P0_INER. The pull-down and input buffer are disabled when the Isolate (VPHY_ISO) bit is set in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).
			IS (PD)	**RMII PHY Mode:** This pin is the TX_EN signal from the external MAC and indicates valid data on P0_IND[1:0]. The pull-down and input buffer are disabled when the Isolate (VPHY_ISO) bit is set in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).

Table 3.5 Port 0 MII/RMII Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Port 0 MII Input Error	P0_INER	IS (PD)	**MII MAC Mode:** This pin is the RX_ER signal from the external PHY and indicates a receive error in the packet.
			IS (PD)	**MII PHY Mode:** This pin is the TX_ER signal from the external MAC and indicates that the current packet should be aborted. The pull-down and input buffer are disabled when the Isolate (VPHY_ISO) bit is set in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).
			-	**RMII PHY Mode:** This pin is not used.
1	Port 0 MII Input Reference Clock	P0_INCLK	IS (PD)	**MII MAC Mode:** This pin is an input and is used as the reference clock for the P0_IND[3:0], P0_INER, and P0_INDV pins. It is connected to the receive clock of the external PHY.
			O12/O16	**MII PHY Mode:** This pin is an output and is used as the reference clock for the P0_IND[3:0], P0_INER, and P0_INDV pins. It is connected to the transmit clock of the external MAC. The output driver is disabled when the Isolate (VPHY_ISO) bit is set in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL). When operating at 200MBps, the choice of drive strength is based on the setting of the RMII/Turbo MII Clock Strength bit in the Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS). A low selects a 12 mA drive, while a high selects a 16 mA drive. A series terminating resistor is recommended for the best PCB signal integrity.
			-	**RMII PHY Mode:** This pin is not used.
1	Port 0 MII Output Data 3	P0_OUTD3	O8	**MII MAC Mode:** This pin is the transmit data 3 bit from the switch to the external PHY.
			O8	**MII PHY Mode:** This pin is the receive data 3 bit from the switch to the external MAC. The output driver is disabled when the Isolate (VPHY_ISO) bit is set in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).
			-	**RMII PHY Mode:** This pin is not used
	Port 0 Duplex Polarity Configuration Strap	DUPLEX_POL_0	IS (PU) Note 3.7	This strap selects the default of the duplex polarity strap for Port 0 MII (duplex_pol_strap_0). See Note 3.6. If the strap is value is 0, a 0 on P0_DUPLEX means full duplex while a 1 means half duplex. If the strap value is 1, a 1 on P0_DUPLEX means full duplex, while a 0 means half duplex.

Table 3.5 Port 0 MII/RMII Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Port 0 MII Output Data 2	P0_OUTD2	O8	**MII MAC Mode:** This pin is the transmit data 2 bit from the switch to the external PHY.
			O8	**MII PHY Mode:** This pin is the receive data 2 bit from the switch to the external MAC. The output driver is disabled when the Isolate (VPHY_ISO) bit is set in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).
			-	**RMII PHY Mode:** This pin is not used
	Port 0 Mode[2] Configuration Strap	P0_MODE2	IS (PU) Note 3.7	This strap configures the mode for Port 0. See Note 3.6. Please refer to the P0_MODE0 strap entry for mode encoding details.
1	Port 0 MII Output Data 1	P0_OUTD1	O8	**MII MAC Mode:** This pin is the transmit data 1 bit from the switch to the external PHY.
			O8	**MII PHY Mode:** This pin is the receive data 1 bit from the switch to the external MAC. The output driver is disabled when the Isolate (VPHY_ISO) bit is set in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).
			O8	**RMII PHY Mode:** This pin is the receive data 1 bit from the switch to the external MAC. The output driver is disabled when the Isolate (VPHY_ISO) bit is set in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).
	Port 0 Mode[1] Configuration Strap	P0_MODE1	IS (PU) Note 3.7	This strap configures the mode for Port 0. See Note 3.6. Please refer to the P0_MODE0 strap entry for mode encoding details.

Table 3.5 Port 0 MII/RMII Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Port 0 MII Output Data 0	P0_OUTD0	O8	**MII MAC Mode:** This pin is the transmit data 0 bit from the switch to the external PHY.
			O8	**MII PHY Mode:** This pin is the receive data 0 bit from the switch to the external MAC. The output driver is disabled when the Isolate (VPHY_ISO) bit is set in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).
			O8	**RMII PHY Mode:** This pin is the receive data 0 bit from the switch to the external MAC. The output driver is disabled when the Isolate (VPHY_ISO) bit is set in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).
	Port 0 Mode[0] Configuration Strap	P0_MODE0	IS (PU) Note 3.7	This strap configures the mode for Port 0. See Note 3.6. The P0_MODE[2:0] configuration strap encoding is as follows: 000 = MII MAC mode 001 = MII PHY mode 010 = MII PHY mode 200 Mbps 12 ma clock output 011 = MII PHY mode 200 Mbps 16 ma clock output 100 = RMII PHY mode clock is 12 ma output 101 = RMII PHY mode clock is 16 ma output 110 = RMII PHY mode clock is input 111 = RESERVED
1	Port 0 MII Output Data Valid	P0_OUTDV	O8	**MII MAC Mode:** This pin is the TX_EN signal to the external PHY and indicates valid data on P0_OUTD[3:0].
			O8	**MII PHY Mode:** This pin is the RX_DV signal to the external MAC. The output driver is disabled when the Isolate (VPHY_ISO) bit is set in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).
			O8	**RMII PHY Mode:** This pin is the CRS_DV signal to the external MAC. The output driver is disabled when the Isolate (VPHY_ISO) bit is set in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).

Table 3.5 Port 0 MII/RMII Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Port 0 MII Output Reference Clock	P0_OUTCLK	IS (PD)	**MII MAC Mode:** This pin is an input and is used as the reference clock for the P0_OUTD[3:0] and P0_OUTDV pins. It is connected to the transmit clock of the external PHY.
			O12/O16	**MII PHY Mode:** This pin is an output and is used as the reference clock for the P0_OUT[3:0] and P0_OUTDV pins. It is connected to the receive clock of the external MAC. The output driver is disabled when the Isolate (VPHY_ISO) bit is set in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL). When operating at 200MBps, the choice of drive strength is based on the setting of the RMII/Turbo MII Clock Strength bit in the Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS). A low selects a 12 mA drive, while a high selects a 16 mA drive. A series terminating resistor is recommended for the best PCB signal integrity.
			IS/O12/ O16 (PD)	**RMII PHY Mode:** This pin is an input or an output running at 50 MHz and is used as the reference clock for the P0_IND[1:0], P0_INDV, P0_OUTD[1:0], and P0_OUTDV pins. The choice of input verses output is based on the setting of the RMII Clock Direction bit in the Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS). A low selects P0_OUTCLK as an input and a high selects P0_OUTCLK as an output. As an input, the pull-down is normally enabled. The input buffer and pull-down are disabled when the Isolate (VPHY_ISO) bit is set in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL). As an output, the input buffer and pull-down are disabled. The choice of drive strength is based on the MII Virtual PHY RMII/Turbo MII Clock Strength bit. A low selects a 12 mA drive, while a high selects a 16 mA drive. The output driver is disabled when the Isolate (VPHY_ISO) bit is set in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL). A series terminating resistor is recommended for the best PCB signal integrity.
1	Port 0 MII Collision	P0_COL	IS (PU)	**MII MAC Mode:** This pin is an input from the external PHY and indicates a collision event.
			O8	**MII PHY Mode:** This pin is an output to the external MAC indicating a collision event. The output driver is disabled when the Isolate (VPHY_ISO) bit is set in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).
			-	**RMII PHY Mode:** This pin is not used.

Table 3.5 Port 0 MII/RMII Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Port 0 MII Carrier Sense	P0_CRS	IS (PD)	**MII MAC Mode:** This pin is an input from the external PHY indicating a network carrier.
			O8	**MII PHY Mode:** This pin is an output to the external MAC indicating a network carrier. The output driver is disabled when the Isolate (VPHY_ISO) bit is set in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).
			-	**RMII PHY Mode:** This pin is not used.
1	Port 0 MII Duplex	P0_DUPLEX	IS (PU)	**MII MAC Mode:** This pin can be changed at any time (live value) and can be overridden by enabling the Auto-Negotiation (VPHY_AN) bit in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL). It is typically tied to the duplex indication from the external PHY. Please refer to the definition of the DUPLEX_POL_0 strap for further details.
			IS (PU)	**MII PHY and RMII PHY Modes:** This pin is used to determine the virtual link partner's ability bits and is typically tied high or low, as needed. Please refer to the definition of the DUPLEX_POL_0 strap for further details.
1	Management Data Input/Output	MDIO	IS/O8	**SMI/MII Slave Management Modes:** This is the data to/from an external master **MII Master Management Modes:** This is the data to/from an external PHY. **Note:** An external pull-up is required when the SMI or MII management interface is used, to ensure that the IDLE state of the MDIO signal is a logic one. **Note:** An external pull-up is recommended when the SMI or MII management interface is not used, to avoid a floating signal.
1	MII Management Clock	MDC	IS	**SMI/MII Slave Management Modes:** This is the clock input from an external master. **Note:** When SMI or MII is not used, an external pull-down is recommended to avoid a floating signal.
			O8	**MII Master Management Modes:** This is the clock output to an external PHY.

Note 3.6 Configuration strap pins are identified by an underlined symbol name. Configuration strap values are latched on power-on reset or nRST de-assertion. Each port has configuration straps that control its operation. Additional strap pins, which share functionality with the GPIO/LED pins, are described in Table 3.6. Some configuration straps can be overridden by values from the EEPROM Loader. Please refer to Section 4.2.4, "Configuration Straps," on page 52 for further information.

Note 3.7 An external supplemental pull-up may be needed, depending upon the input current loading of the external MAC/PHY device.

Table 3.6 GPIO/LED/Configuration Straps

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	LED 5	LED5	O12/ OD12/ OS12	This pin is configured to operate as an LED when the LED 5 Enable bit of the LED Configuration Register (LED_CFG) is set. The buffer type depends on the setting of the LED Function 1-0 (LED_FUN[1:0]) field in the LED Configuration Register (LED_CFG) and is configured to be either an push-pull or open-drain/open-source output. When selected as an open-drain/open-source output, the polarity of this pin depends upon the PHYADDR_LED5P strap value sampled at reset.
	GPIO 5	GPIO5	IS/O12/ OD12 (PU)	This pin is configured to operate as a GPIO when the LED 5 Enable bit of the LED Configuration Register (LED_CFG) is clear. The pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input by writing the General Purpose I/O Configuration Register (GPIO_CFG) and the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR).
	PHY Address and LED 5 Polarity Configuration Strap	PHYADDR_LED5P	IS (PU)	This strap configures the default value of the MII management address for the PHYs and Virtual PHY, as well as the polarity of the LED 5 pin when it is an open-drain or open-source output. See Note 3.8. If the strap value is 0: The PHY address values are as follows: Virtual PHY = 0 PHY Port 1 = 1 PHY Port 2 = 2 The LED is set as active high, since it is assumed that a LED to ground is used as the pull-down. If the strap value is 1: The PHY address values are as follows: Virtual PHY = 1 PHY Port 1 = 2 PHY Port 2 = 3 The LED is set as active low, since it is assumed that a LED to VDD is used as the pull-up.

Table 3.6 GPIO/LED/Configuration Straps (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	LED 4	LED4	O12/ OD12/ OS12	This pin is configured to operate as an LED when the LED 4 Enable bit in the LED Configuration Register (LED_CFG) is set. The buffer type depends on the setting of the LED Function 1-0 (LED_FUN[1:0]) field in the LED Configuration Register (LED_CFG) and is configured to be either an push-pull or open-drain/open-source output. When selected as an open-drain/open-source output, the polarity of this pin depends up the MNGT1_LED4P strap value sampled at reset.
	GPIO 4	GPIO4	IS/O12/ OD12 (PU)	This pin is configured to operate as a GPIO when the LED 4 Enable bit of the LED Configuration Register (LED_CFG) is clear. The pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input by writing the General Purpose I/O Configuration Register (GPIO_CFG) and the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR).
	Serial Management Mode[1] and LED 4 Polarity Configuration Strap	MNGT1_LED4P	IS (PU)	This strap configures the Serial Management Mode, as well as the polarity of the LED 4 pin when it is an open-drain or open-source output. See Note 3.8. If the strap value is 0: The LED is set as active high, since it is assumed that a LED to ground is used as the pull-down. If the strap value is 1: The LED is set as active low, since it is assumed that a LED to VDD is used as the pull-up.

Table 3.6 GPIO/LED/Configuration Straps (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	LED 3	LED3	O12/ OD12/ OS12	This pin is configured to operate as an LED when the LED 3 Enable bit in the LED Configuration Register (LED_CFG) is set. The buffer type depends on the setting of the LED Function 1-0 (LED_FUN[1:0]) field in the LED Configuration Register (LED_CFG) and is configured to be either an push-pull or open-drain/open-source output. When selected as an open-drain/open-source output, the polarity of this pin depends up the MNGT0_LED3P strap value sampled at reset.
	GPIO 3	GPIO3	IS/O12/ OD12 (PU)	This pin is configured to operate as a GPIO when the LED 3 Enable bit of the LED Configuration Register (LED_CFG) is clear. The pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input by writing the General Purpose I/O Configuration Register (GPIO_CFG) and the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR).
	Serial Management Mode[0] and LED 3 Polarity Configuration Strap	MNGT0_LED3P	IS (PU)	This strap configures the Serial Management Mode, as well as the polarity of the LED 3 pin when it is an open-drain or open-source output. See Note 3.8. For LED3, If the strap value is 0: The LED is set as active high, since it is assumed that a LED to ground is used as the pull-down. If the strap value is 1: The LED is set as active low, since it is assumed that a LED to VDD is used as the pull-up.

Table 3.6 GPIO/LED/Configuration Straps (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	LED 2	LED2	O12/ OD12/ OS12	This pin is configured to operate as an LED when the LED 2 Enable bit in the LED Configuration Register (LED_CFG) is set. The buffer type depends on the setting of the LED Function 1-0 (LED_FUN[1:0]) field in the LED Configuration Register (LED_CFG) and is configured to be either an push-pull or open-drain/open-source output. When selected as an open-drain/open-source output, the polarity of this pin depends up the E2PSIZE_LED2P strap value sampled at reset.
	GPIO 2	GPIO2	IS/O12/ OD12 (PU)	This pin is configured to operate as a GPIO when the LED 2 Enable bit of the LED Configuration Register (LED_CFG) is clear. The pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input by writing the General Purpose I/O Configuration Register (GPIO_CFG) and the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR).
	EEPROM Size and LED 2 Polarity Configuration Strap	E2PSIZE_LED2P	IS (PU)	This strap configures the EEPROM size, as well as the polarity of the LED 2 pin when it is an open-drain or open-source output. See Note 3.8. The low bit of the EEPROM size range is set to the strap value. When 0, EEPROM sizes 16 x 8 through 2048 x 8 are supported. When 1, EEPROM sizes 4096 x 8 through 65536 x 8 are supported. For LED 2, If the strap value is 0: The LED is set as active high, since it is assumed that a LED to ground is used as the pull-down. If the strap value is 1: The LED is set as active low, since it is assumed that a LED to VDD is used as the pull-up.

Table 3.6 GPIO/LED/Configuration Straps (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	LED 1	LED1	O12/ OD12/ OS12	This pin is configured to operate as an LED when the LED 1 Enable bit in the LED Configuration Register (LED_CFG) is set. The buffer type depends on the setting of the LED Function 1-0 (LED_FUN[1:0]) field in the LED Configuration Register (LED_CFG) and is configured to be either an push-pull or open-drain/open-source output. When selected as an open-drain/open-source output, the polarity of this pin depends up the AMDIX2_LED1P strap value sampled at reset.
	GPIO 1	GPIO1	IS/O12/ OD12 (PU)	This pin is configured to operate as a GPIO when the LED 1 Enable bit of the LED Configuration Register (LED_CFG) is clear. The pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input by writing the General Purpose I/O Configuration Register (GPIO_CFG) and the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR).
	Port 2 Auto-MDIX Enable and LED 1 Polarity Configuration Strap	AMDIX2_LED1P	IS (PU)	This strap configures the default for the Auto-MDIX soft-strap for LAN Port 2, as well as the polarity of the LED 1 pin when it is an open-drain or open-source output. See Note 3.8. The strap value determines whether or not LAN Port 2 Auto-MDIX is enables as follows: 0 = Disabled 1 = Enabled For LED 1, If the strap value is 0: The LED is set as active high, since it is assumed that a LED to ground is used as the pull-down. If the strap value is 1: The LED is set as active low, since it is assumed that a LED to VDD is used as the pull-up.

Table 3.6 GPIO/LED/Configuration Straps (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	LED 0	LED0	O12/ OD12/ OS12	This pin is configured to operate as an LED when the LED 0 Enable bit in the LED Configuration Register (LED_CFG) is set. The buffer type depends on the setting of the field in the LED Configuration Register (LED_CFG) and is configured to be either an push-pull or open-drain/open-source output. When selected as an open-drain/open-source output, the polarity of this pin depends up the AMDIX1_LED0P strap value sampled at reset.
	GPIO 0	GPIO0	IS/O12/ OD12 (PU)	This pin is configured to operate as a GPIO when the LED 0 Enable bit of the LED Configuration Register (LED_CFG) is clear. The pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input by writing the General Purpose I/O Configuration Register (GPIO_CFG) and the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR).
	Port 1 Auto-MDIX Enable and LED 0 Polarity Configuration Strap	AMDIX1_LED0P	IS (PU)	This strap configures the default for the Auto-MDIX soft-strap for LAN Port 1, as well as the polarity of the LED 0 pin when it is an open-drain or open-source output. See Note 3.8. The strap value determines whether or not LAN Port 1 Auto-MDIX is enabled as follows: 0 = Disabled 1 = Enabled For LED 0, If the strap value is 0: The LED is set as active high, since it is assumed that a LED to ground is used as the pull-down. If the strap value is 1: The LED is set as active low, since it is assumed that a LED to VDD is used as the pull-up.

Note 3.8 Configuration strap pins are identified by an underlined symbol name. Configuration strap values are latched on power-on reset or nRST de-assertion. In addition to the configuration strap pins that control GPIO/LED and Auto-MDIX operation listed in Table 3.6, configuration strap pins are associated with each port and control their operation. They are described in Table 3.4 and Table 3.5. Some configuration straps can be overridden by values from the EEPROM Loader. Please refer to Section 4.2.4, "Configuration Straps," on page 52 for further information.

Table 3.7 Serial Management/EEPROM Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	EEPROM I^2C Serial Data Input/Output	EE_SDA	IS/OD8	When the device is accessing an external EEPROM, this pin is the I^2C serial data input/output. **Note:** This pin must be pulled-up by an external resistor at all times.
	I^2C Slave Serial Data Input/Output (I^2C Slave Mode)	SDA	IS/OD8	In I^2C slave mode, this pin is the I^2C serial data input/output from/to the external master. **Note:** This pin must be pulled-up by an external resistor at all times.
1	EEPROM I^2C Serial Clock	EE_SCL	IS/OD8	When the device is accessing an external EEPROM, this pin is the I^2C clock input/open-drain output. **Note:** This pin must be pulled-up by an external resistor at all times.
	I^2C Slave Serial Clock (I^2C Slave Mode)	SCL	IS	In I^2C slave mode, this pin is the I^2C clock input from the external master. **Note:** This pin must be pulled-up by an external resistor at all times.

Note: Please refer to Chapter 8, "Serial Management," on page 114 for additional information regarding serial management configuration and functionality.

Table 3.8 Miscellaneous Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Interrupt Output	IRQ	O8/OD8	The polarity, source and buffer type of this signal is programmable via the Interrupt Configuration Register (IRQ_CFG). Please refer to Chapter 5, "System Interrupts," on page 62 for further details.
1	System Reset Input	nRST	IS (PU)	This active low signal allows external hardware to reset the device. The device also contains an internal power-on reset circuit. Thus, this signal may be left unconnected if an external hardware reset is not needed. When used, this signal must adhere to the reset timing requirements as detailed in the Section 14.5.2, "Reset and Configuration Strap Timing," on page 368.
1	Test 1	TEST1	AI	This pin must be tied to VDD33IO for proper operation.
1	Test 2	TEST2	IS (PD)	This pin must be tied to VSS for proper operation.

Table 3.9 PLL Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	PLL +1.8V Power Supply	VDD18PLL	P	This pin must be connected to VDD18CORE for proper operation. See Note 3.9.
1	Crystal Input	XI	ICLK	External 25MHz crystal input. This signal can also be driven by a single-ended clock oscillator. When this method is used, XO should be left unconnected.
1	Crystal Output	XO	OCLK	External 25MHz crystal output.

Note 3.9 Please refer to the LAN9303M/LAN9303Mi Reference Schematic and LANCheck Schematic Checklist on the SMSC website for additional connection information.

Table 3.10 Core and I/O Power and Ground Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
5	+3.3V I/O Power	VDD33IO	P	+3.3V Power Supply for I/O Pins and Internal Regulator. See Note 3.10.
2	Digital Core +1.8V Power Supply Output	VDD18CORE	P	+1.8V power from the internal core voltage regulator. All VDD18CORE pins must be tied together for proper operation. See Note 3.10.
1 PAD	Common Ground	VSS	P	Ground

Note 3.10 Please refer to the LAN9303M/LAN9303Mi Reference Schematic and LANCheck Schematic Checklist on the SMSC website for additional connection information.

Table 3.11 LAN9303M/LAN9303Mi 72-QFN Package Pin Assignments

PIN NUM	PIN NAME	PIN NUM	PIN NAME	PIN NUM	PIN NAME	PIN NUM	PIN NAME
1	P0_IND2	19	P1_INER	37	P1_CRS	55	VDD18PLL
2	P0_IND1	20	P1_INCLK	38	P1_OUTD3/ DUPLEX_POL_1	56	TXN1
3	P0_IND0	21	P0_OUTDV	39	P1_OUTD2/ P1_MODE2	57	TXP1
4	P0_INDV	22	P0_OUTCLK	40	VDD33IO	58	VDD33A1
5	P0_INER	23	P0_COL	41	VDD18CORE	59	RXN1
6	P0_INCLK	24	P0_CRS	42	P1_OUTDV	60	RXP1
7	VDD33IO	25	P0_DUPLEX	43	P1_OUTCLK	61	VDD33A1
8	VDD18CORE	26	MDIO	44	P1_OUTD1/ P1_MODE1	62	VDD18TX1
9	P0_OUTD3/ DUPLEX_POL_0	27	MDC	45	P1_OUTD0/ P1_MODE0	63	EXRES
10	P0_OUTD2/ P0_MODE2	28	VDD33IO	46	VDD33IO	64	VDD33BIAS
11	P0_OUTD1/ P0_MODE1	29	LED5/ GPIO5/ PHYADDR_LED5P	47	TEST1	65	VDD18TX2
12	P0_OUTD0/ P0_MODE0	30	LED4/ GPIO4/ MNGT1_LED4P	48	TEST2	66	VDD33A2
13	P1_IND3	31	LED3/ GPIO3/ MNGT0_LED3P	49	EE_SDA/ SDA	67	RXP2
14	P1_IND2	32	LED2/ GPIO2/ E2PSIZE_LED2P	50	EE_SCL/ SCL	68	RXN2
15	P1_IND1	33	LED1/ GPIO1/ AMDIX2_LED1P	51	nRST	69	VDD33A2
16	P1_IND0	34	LED0/ GPIO0/ AMDIX1_LED0P	52	IRQ	70	TXP2
17	VDD33IO	35	P1_DUPLEX	53	XI	71	TXN2
18	P1_INDV	36	P1_COL	54	XO	72	P0_IND3
EXPOSED PAD MUST BE CONNECTED TO VSS							

3.3 Buffer Types

Table 3.12 Buffer Types

BUFFER TYPE	DESCRIPTION
IS	Schmitt-triggered Input
O8	Output with 8mA sink and 8mA source
OD8	Open-drain output with 8mA sink
O12	Output with 12mA sink and 12mA source
OD12	Open-drain output with 12mA sink
OS12	Open-source output with 12 mA source
O16	Output with 16mA sink and 16mA source
PU	50uA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. **Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	50uA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. **Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
AI	Analog input
AIO	Analog bi-directional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
P	Power pin

Chapter 4 Clocking, Resets, and Power Management

4.1 Clocks

The device includes a clock module which provides generation of all system clocks as required by the various sub-modules of the device. The device requires a fixed-frequency 25MHz clock source for use by the internal clock oscillator and PLL. This is typically provided by attaching a 25MHz crystal to the XI and XO pins as specified in Section 14.6, "Clock Circuit," on page 382. Optionally, this clock can be provided by driving the XI input pin with a single-ended 25MHz clock source. If a single-ended source is selected, the clock input must run continuously for normal device operation. The internal PLL generates a fixed 200MHz base clock which is used to derive all sub-system clocks.

In addition to the sub-system clocks, the clock module is also responsible for generating the clocks used for the general purpose timer and free-running clock. Refer to Chapter 11, "General Purpose Timer & Free-Running Clock," on page 143 for additional details.

Note: Crystal specifications are provided in Table 14.20, “Crystal Specifications,” on page 382.

4.2 Resets

The device provides multiple hardware and software reset sources, which allow varying levels of the chip to be reset. All resets can be categorized into three reset types as described in the following sections:

- Chip-Level Resets
  —Power-On Reset (POR)
  —nRST Pin Reset
- Multi-Module Resets
  —Digital Reset (DIGITAL_RST)
- Single-Module Resets
  —Port 2 PHY Reset
  —Port 1 PHY Reset
  —Virtual PHY Reset

The device supports the use of configuration straps to allow automatic custom configurations of various parameters. These configuration strap values are set upon de-assertion of all chip-level resets and can be used to easily set the default parameters of the chip at power-on or pin (nRST) reset. Refer to Section 4.2.4, "Configuration Straps," on page 52 for detailed information on the usage of these straps.

Note: The EEPROM Loader is run upon a power-on reset, nRST pin reset, and digital reset. Refer to Section 8.4, "EEPROM Loader," on page 121 for additional information.

Table 4.1 summarizes the effect of the various reset sources on the device. Refer to the following sections for detailed information on each of these reset types.

Table 4.1 Reset Sources and Affected Device Circuitry

RESET SOURCE	SYSTEM CLOCKS/RESET	SYS INTERRUPTS	SWITCH FABRIC	ETHERNET PHYS	PMI	I²C SLAVE	SMI SLAVE	EEPROM CONTROLLER	GPIO/LED CONTROLLER	CONFIG. STRAPS LATCHED	EEPROM LOADER RUN
POR	X	X	X	X	X	X	X	X	X	X	X
nRST Pin	X	X	X	X	X	X	X	X	X	X	X
Digital Reset	X	X	X		X	X	X	X	X		X
Port 2 PHY				X							
Port 1 PHY				X							
Virtual PHY				X							

4.2.1 Chip-Level Resets

A chip-level reset event activates all internal resets, effectively resetting the entire device. Configuration straps are latched, and the EEPROM Loader is run as a result of chip-level resets. A chip-level reset is initiated by assertion of any of the following input events:

- Power-On Reset (POR)
- nRST Pin Reset

Chip-level reset/configuration completion can be determined by first polling the Byte Order Test Register (BYTE_TEST). The returned data will be invalid until the serial interface resets are complete. Once the returned data is the correct byte ordering value, the serial interface resets have completed. The completion of the entire chip-level reset must then be determined by polling the Device Ready (READY) bit of the Hardware Configuration Register (HW_CFG) until it is set. When set, the Device Ready (READY) bit indicates that the reset has completed and the device is ready to be accessed.

With the exception of the Hardware Configuration Register (HW_CFG), Byte Order Test Register (BYTE_TEST), and Reset Control Register (RESET_CTL), read access to any internal resources is forbidden while the Device Ready (READY) bit is cleared. Writes to any address are invalid until the Device Ready (READY) bit is set.

4.2.1.1 Power-On Reset (POR)

A power-on reset occurs whenever power is initially applied to the device, or if the power is removed and reapplied to the device. This event resets all circuitry within the device. Configuration straps are latched, and the EEPROM Loader is run as a result of this reset.

A POR reset typically takes approximately 23mS, plus an additional 91uS per byte of data loaded from the EEPROM via the EEPROM Loader. A full EEPROM load of 64KB will complete in approximately 6.0 seconds.

4.2.1.2 nRST Pin Reset

Driving the nRST input pin low initiates a chip-level reset. This event resets all circuitry within the device. Use of this reset input is optional, but when used, it must be driven for the period of time specified in Section 14.5.2, "Reset and Configuration Strap Timing," on page 368. Configuration straps are latched, and the EEPROM Loader is run as a result of this reset.

A nRST pin reset typically takes approximately 760uS, plus an additional 91uS per byte of data loaded from the EEPROM via the EEPROM Loader. A full EEPROM load of 64KB will complete in approximately 6.0 seconds.

Note: The nRST pin is pulled-high internally. If unused, this signal can be left unconnected. Do not rely on internal pull-up resistors to drive signals external to the device.

Please refer to Section Table 3.8, "Miscellaneous Pins," on page 44 for a description of the nRST pin.

4.2.2 Multi-Module Resets

Multi-module resets activate multiple internal resets, but do not reset the entire chip. Configuration straps are *not* latched upon multi-module resets. A multi-module reset is initiated by assertion of the following:

- Digital Reset (DIGITAL_RST)

Multi-module reset/configuration completion can be determined by first polling the Byte Order Test Register (BYTE_TEST). The returned data will be invalid until the serial interface resets are complete. Once the returned data is the correct byte ordering value, the serial interface resets have completed. The completion of the entire chip-level reset must then be determined by polling the Device Ready (READY) bit of the Hardware Configuration Register (HW_CFG) until it is set. When set, the Device Ready (READY) bit indicates that the reset has completed and the device is ready to be accessed.

With the exception of the Hardware Configuration Register (HW_CFG), Byte Order Test Register (BYTE_TEST), and Reset Control Register (RESET_CTL), read access to any internal resources is forbidden while the Device Ready (READY) bit is cleared. Writes to any address are invalid until the Device Ready (READY) bit is set.

Note: The digital reset does not reset register bits designated as NASR.

4.2.2.1 Digital Reset (DIGITAL_RST)

A digital reset is performed by setting the Digital Reset (DIGITAL_RST) bit of the Reset Control Register (RESET_CTL). A digital reset will reset all sub-modules except the Ethernet PHYs (Port 1 PHY, Port 2 PHY, and Virtual PHY). The EEPROM Loader will automatically run following this reset. Configuration straps are *not* latched as a result of a digital reset.

A digital reset typically takes approximately 760uS, plus an additional 91uS per byte of data loaded from the EEPROM via the EEPROM Loader. A full EEPROM load of 64KB will complete in approximately 6.0 seconds.

4.2.3 Single-Module Resets

A single-module reset will reset only the specified module. Single-module resets do *not* latch the configuration straps or initiate the EEPROM Loader. A single-module reset is initiated by assertion of the following:

- Port 2 PHY Reset
- Port 1 PHY Reset
- Virtual PHY Reset

4.2.3.1 Port 2 PHY Reset

A Port 2 PHY reset is performed by setting the Port 2 PHY Reset (PHY2_RST) bit of the Reset Control Register (RESET_CTL) or the Reset (PHY_RST) bit in the (x=2) Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x). Upon completion of the Port 2 PHY reset, the Port 2 PHY Reset

(PHY2_RST) and Reset (PHY_RST) bits are automatically cleared. No other modules of the device are affected by this reset.

In addition to the methods above, the Port 2 PHY is automatically reset after returning from a PHY power-down mode. This reset differs in that the PHY power-down mode reset does not reload or reset any of the PHY registers. Refer to Section 7.2.9, "PHY Power-Down Modes," on page 109 for additional information.

Port 2 PHY reset completion can be determined by polling the Port 2 PHY Reset (PHY2_RST) bit in the Reset Control Register (RESET_CTL) or the Reset (PHY_RST) bit in the (x=2) Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) until it clears. Under normal conditions, these bits will clear approximately 110uS after the Port 2 PHY reset occurrence.

Note: When using the Reset (PHY_RST) bit to reset the Port 2 PHY, register bits designated as NASR are not reset.

Refer to Section 7.2.10, "PHY Resets," on page 109 for additional information on Port 2 PHY resets.

4.2.3.2 Port 1 PHY Reset

A Port 1 PHY reset is performed by setting the Port 1 PHY Reset (PHY1_RST) bit of the Reset Control Register (RESET_CTL) or the Reset (PHY_RST) bit in the (x=1) Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x). Upon completion of the Port 1 PHY reset, the Port 1 PHY Reset (PHY1_RST) and Reset (PHY_RST) bits are automatically cleared. No other modules of the device are affected by this reset.

In addition to the methods above, the Port 1 PHY is automatically reset after returning from a PHY power-down mode. This reset differs in that the PHY power-down mode reset does not reload or reset any of the PHY registers. Refer to Section 7.2.9, "PHY Power-Down Modes," on page 109 for additional information.

Port 1 PHY reset completion can be determined by polling the Port 1 PHY Reset (PHY1_RST) bit in the Reset Control Register (RESET_CTL) or the Reset (PHY_RST) bit in the (x=1) Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) until it clears. Under normal conditions, these bits will clear approximately 110uS after the Port 1 PHY reset occurrence.

Note: When using the Reset (PHY_RST) bit to reset the Port 1 PHY, register bits designated as NASR are not reset.

Refer to Section 7.2.10, "PHY Resets," on page 109 for additional information on Port 1 PHY resets.

4.2.3.3 Virtual PHY Reset

A Virtual PHY reset is performed by setting the Virtual PHY Reset (VPHY_RST) bit of the Reset Control Register (RESET_CTL) or Reset (VPHY_RST) in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL). No other modules of the device are affected by this reset.

Virtual PHY reset completion can be determined by polling the Virtual PHY Reset (VPHY_RST) bit in the Reset Control Register (RESET_CTL) or the Reset (VPHY_RST) bit in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) until it clears. Under normal conditions, these bits will clear approximately 1uS after the Virtual PHY reset occurrence.

Refer to Section 7.3.3, "Virtual PHY Resets," on page 113 for additional information on Virtual PHY resets.

4.2.4 Configuration Straps

Configuration straps allow various features of the device to be automatically configured to user defined values. Configuration straps can be organized into two main categories: hard-straps and soft-straps. Both hard-straps and soft-straps are latched upon Power-On Reset (POR) or pin reset (nRST). The primary difference between these strap types is that soft-strap default values can be overridden by the EEPROM Loader, while hard-straps cannot.

Configuration straps which have a corresponding external pin include internal resistors in order to prevent the signal from floating when unconnected. If a particular configuration strap is connected to a load, an external pull-up or pull-down resistor should be used to augment the internal resistor to ensure that it reaches the required voltage level prior to latching. The internal resistor can also be overridden by the addition of an external resistor.

Note: The system designer must guarantee that configuration strap pins meet the timing requirements specified in Section 14.5.2, "Reset and Configuration Strap Timing," on page 368. If configuration strap pins are not at the correct voltage level prior to being latched, the device may capture incorrect strap values.

4.2.4.1 Soft-Straps

Soft-strap values are latched on the release of POR or nRST and are overridden by values from the EEPROM Loader (when an EEPROM is present). These straps are used as direct configuration values or as defaults for CPU registers. Some, but not all, soft-straps have an associated pin. Those that do not have an associated pin have a tie off default value. All soft-strap values can be overridden by the EEPROM Loader. Table 4.2 provides a list of all soft-straps and their associated pin or default value. Straps which have an associated pin are also fully defined in Chapter 3, "Pin Description and Configuration," on page 23. Refer to Section 8.4, "EEPROM Loader," on page 121 for information on the operation of the EEPROM Loader and the loading of strap values. The use of the term “configures” in the “Description” section of Table 4.2 means the register bit is loaded with the strap value, while the term “Affects” means the value of the register bit is determined by the strap value and some other condition(s).

Upon setting the Digital Reset (DIGITAL_RST) bit in the Reset Control Register (RESET_CTL) or upon issuing a RELOAD command via the EEPROM Command Register (E2P_CMD), these straps return to their original latched (non-overridden) values if an EEPROM is no longer attached or has been erased. The associated pins are not re-sampled. (i.e. The value latched on the pin during the last POR or nRST will be used, not the value on the pin during the digital reset or RELOAD command issuance). If it is desired to re-latch the current configuration strap pin values, a POR or nRST must be issued.

Table 4.2 Soft-Strap Configuration Strap Definitions

STRAP NAME	DESCRIPTION	PIN / DEFAULT VALUE
LED_en_strap[5:0]	**LED Enable Straps:** Configures the default value for the LED Enable 5-0 (LED_EN[5:0]) bits of the LED Configuration Register (LED_CFG).	1b
LED_fun_strap[1:0]	**LED Function Straps:** Configures the default value for the LED Function 1-0 (LED_FUN[1:0]) bits of the LED Configuration Register (LED_CFG).	00b
auto_mdix_strap_1	**Port 1 Auto-MDIX Enable Strap:** Configures the default value of the AMDIX_EN Strap State Port 1 bit of the Hardware Configuration Register (HW_CFG). This strap is also used in conjunction with manual_mdix_strap_1 to configure Port 1 Auto-MDIX functionality when the Auto-MDIX Control (AMDIXCTRL) bit in the (x=1) Port x PHY Special Control/Status Indication Register (PHY_SPECIAL_CONTROL_STAT_IND_x) indicates the strap settings should be used for auto-MDIX configuration. **Note:** Not used in MII PHY, RMII PHY, or MII MAC mode. Refer to the respective register definition sections for additional information.	AMDIX1_LED0P Note 4.1
manual_mdix_strap_1	**Port 1 Manual MDIX Strap:** Configures MDI(0) or MDIX(1) for Port 1 when the auto_mdix_strap_1 is low and the Auto-MDIX Control (AMDIXCTRL) bit of the (x=1) Port x PHY Special Control/Status Indication Register (PHY_SPECIAL_CONTROL_STAT_IND_x) indicates the strap settings are to be used for auto-MDIX configuration. **Note:** Not used in MII PHY, RMII PHY, or MII MAC mode.	0b
autoneg_strap_1	**Port 1 Auto Negotiation Enable Strap:** Configures the default value of the Auto-Negotiation (PHY_AN) enable bit of the (x=1) Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x). This strap also may affect the default value of the following register bits (x=1): ▪ Speed Select LSB (PHY_SPEED_SEL_LSB) and Duplex Mode (PHY_DUPLEX) bits of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) ▪ 10BASE-T Full Duplex and 10BASE-T Half Duplex bits of the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) ▪ PHY Mode (MODE[2:0]) bits of the Port x PHY Special Modes Register (PHY_SPECIAL_MODES_x) Refer to the respective register definition sections for additional information.	1b when in internal PHY mode (P1_MODE[2:0] = 111b)
SQE_test_disable_strap_1	Configures the default value of the SQEOFF bit of the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL) when in MII PHY mode. It is not used in internal PHY, RMII PHY, or MII MAC mode.	else 0b

Table 4.2 Soft-Strap Configuration Strap Definitions (continued)

STRAP NAME	DESCRIPTION	PIN / DEFAULT VALUE
speed_strap_1	**Port 1 Speed Select Strap:** This strap configures the default value of the Speed Select LSB bit of the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL). This strap may affect the default value of the following register bits (x=1): ▪ Speed Select LSB (PHY_SPEED_SEL_LSB) bit of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) ▪ PHY Mode (MODE[2:0]) bits of the Port x PHY Special Modes Register (PHY_SPECIAL_MODES_x) ▪ 10BASE-T Full Duplex and 10BASE-T Half Duplex bits of the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) Refer to the respective register definition sections for additional information.	1b
duplex_strap_1	**Port 1 Duplex Select Strap:** This strap affects the default value of the following register bits (x=1): ▪ Duplex Mode (PHY_DUPLEX) bit of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) ▪ PHY Mode (MODE[2:0]) bits of the Port x PHY Special Modes Register (PHY_SPECIAL_MODES_x) ▪ 10BASE-T Full Duplex bit of the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) Refer to the respective register definition sections for additional information.	1b when in internal PHY mode (P1_MODE[2:0] = 111b) else
duplex_pol_strap_1	This strap affects the default value of the Duplex Mode bit of the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL). It also determines the polarity of the P1_DUPLEX pin in MII MAC mode.	DUPLEX_POL_1 when in MII PHY, RMII PHY, or MII MAC mode
BP_EN_strap_1	**Port 1 Backpressure Enable Strap:** Configures the default value for the Port 1 Backpressure Enable (BP_EN_1) bit of the Port 1 Manual Flow Control Register (MANUAL_FC_1).	1b

Table 4.2 Soft-Strap Configuration Strap Definitions (continued)

STRAP NAME	DESCRIPTION	PIN / DEFAULT VALUE
FD_FC_strap_1	**Port 1 Full-Duplex Flow Control Enable Strap:** This strap is used to configure the default value of the following register bits (x=1): ■ Port 1 Full-Duplex Transmit Flow Control Enable (TX_FC_1) and Port 1 Full-Duplex Receive Flow Control Enable (RX_FC_1) bits of the Port 1 Manual Flow Control Register (MANUAL_FC_1) This strap may affect the default value of the following register bits (x=1): ■ Asymmetric Pause bit of the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) Refer to the respective register definition sections for additional information.	1b
manual_FC_strap_1	**Port 1 Manual Flow Control Enable Strap:** Configures the default value of the Port 1 Full-Duplex Manual Flow Control Select (MANUAL_FC_1) bit in the Port 1 Manual Flow Control Register (MANUAL_FC_1). This strap affects the default value of the following register bits (x=1): ■ Asymmetric Pause and Symmetric Pause bits of the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) **Note:** This strap is not used in Port 1 MII PHY, RMII PHY, or MII MAC mode. Full-duplex flow control should be controlled manually by the host, if desired.	0b
auto_mdix_strap_2	**Port 2 Auto-MDIX Enable Strap:** Configures the default value of the AMDIX_EN Strap State Port 2 bit of the Hardware Configuration Register (HW_CFG). This strap is used in conjunction with manual_mdix_strap_2 to configure Port 2 Auto-MDIX functionality when the Auto-MDIX Control (AMDIXCTRL) bit in the (x=2) Port x PHY Special Control/Status Indication Register (PHY_SPECIAL_CONTROL_STAT_IND_x) indicates the strap settings should be used for auto-MDIX configuration. Refer to the respective register definition sections for additional information.	AMDIX2 LED1P Note 4.1
manual_mdix_strap_2	**Port 2 Manual MDIX Strap:** Configures MDI(0) or MDIX(1) for Port 2 when the auto_mdix_strap_2 is low and the Auto-MDIX Control (AMDIXCTRL) bit of the (x=2) Port x PHY Special Control/Status Indication Register (PHY_SPECIAL_CONTROL_STAT_IND_x) indicates the strap settings are to be used for auto-MDIX configuration.	0b

Table 4.2 Soft-Strap Configuration Strap Definitions (continued)

STRAP NAME	DESCRIPTION	PIN / DEFAULT VALUE
autoneg_strap_2	**Port 2 Auto Negotiation Enable Strap:** Configures the default value of the Auto-Negotiation (PHY_AN) enable bit in the (x=2) Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x). This strap may also affect the default value of the following register bits (x=2): ■ Speed Select LSB (PHY_SPEED_SEL_LSB) and Duplex Mode (PHY_DUPLEX) bits of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) ■ 10BASE-T Full Duplex and 10BASE-T Half Duplex bits of the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) ■ PHY Mode (MODE[2:0]) bits of the Port x PHY Special Modes Register (PHY_SPECIAL_MODES_x) Refer to the respective register definition sections for additional information.	1b
speed_strap_2	**Port 2 Speed Select Strap:** This strap affects the default value of the following register bits (x=2): ■ Speed Select LSB (PHY_SPEED_SEL_LSB) bit of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) ■ 10BASE-T Full Duplex bit and 10BASE-T Half Duplex bit of the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) ■ PHY Mode (MODE[2:0]) bits of the Port x PHY Special Modes Register (PHY_SPECIAL_MODES_x) Refer to the respective register definition sections for additional information.	1b
duplex_strap_2	**Port 2 Duplex Select Strap:** This strap affects the default value of the following register bits (x=2): ■ Duplex Mode (PHY_DUPLEX) bit of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) ■ 10BASE-T Full Duplex bit of the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) ■ PHY Mode (MODE[2:0]) bits of the Port x PHY Special Modes Register (PHY_SPECIAL_MODES_x) Refer to the respective register definition sections for additional information.	1b
BP_EN_strap_2	**Port 2 Backpressure Enable Strap:** Configures the default value for the Port 2 Backpressure Enable (BP_EN_2) bit of the Port 2 Manual Flow Control Register (MANUAL_FC_2).	1b

Table 4.2 Soft-Strap Configuration Strap Definitions (continued)

STRAP NAME	DESCRIPTION	PIN / DEFAULT VALUE
FD_FC_strap_2	**Port 2 Full-Duplex Flow Control Enable Strap:** This strap is used to configure the default value of the following register bits: ■ Port 2 Full-Duplex Transmit Flow Control Enable (TX_FC_2) and Port 2 Full-Duplex Receive Flow Control Enable (RX_FC_2) bits of the Port 2 Manual Flow Control Register (MANUAL_FC_2). This strap may affect the default value of the following register bits (x=2): ■ Asymmetric Pause bit of the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) Refer to the respective register definition sections for additional information.	1b
manual_FC_strap_2	**Port 2 Manual Flow Control Enable Strap:** Configures the default value of the Port 2 Full-Duplex Manual Flow Control Select (MANUAL_FC_2) bit in the Port 2 Manual Flow Control Register (MANUAL_FC_2). This strap affects the default value of the following register bits (x=2): ■ Asymmetric Pause and Symmetric Pause bits of the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x).	0b
speed_strap_0	**Port 0 (External MII) Speed Select Strap:** This strap affects the default value of the following bits in the Virtual PHY Auto-Negotiation Link Partner Base Page Ability Register (VPHY_AN_LP_BASE_ABILITY): ■ 100BASE-X Full Duplex ■ 100BASE-X Half Duplex ■ 10BASE-T Full Duplex ■ 10BASE-T Half Duplex Refer to Section 13.2.6.6 and Table 13.7 for more information. This strap also configures the speed for Port 0 when Virtual Auto-Negotiation fails. Refer to Section 7.3.1.1, "Parallel Detection," on page 112 for additional information.	1b

Table 4.2 Soft-Strap Configuration Strap Definitions (continued)

STRAP NAME	DESCRIPTION	PIN / DEFAULT VALUE
duplex_pol_strap_0	**Port 0 (External MII) Duplex Polarity Strap:** This strap determines the polarity of the P0_DUPLEX pin in MII MAC mode and affects the default value of the following bits in the Virtual PHY Auto-Negotiation Link Partner Base Page Ability Register (VPHY_AN_LP_BASE_ABILITY): ▪ 100BASE-X Full Duplex ▪ 100BASE-X Half Duplex ▪ 10BASE-T Full Duplex ▪ 10BASE-T Half Duplex Refer to Section 13.2.6.6 and Table 13.7 for more information.	DUPLEX_POL_0
BP_EN_strap_0	**Port 0 (External MII) Backpressure Enable Strap:** Configures the default value of the Port 0 Backpressure Enable (BP_EN_0) bit of the Port 0 Manual Flow Control Register (MANUAL_FC_0).	1b
FD_FC_strap_0	**Port 0 (External MII) Full-Duplex Flow Control Enable Strap**: Configures the default value of the Port 0 Transmit Flow Control Enable (TX_FC_0) and Port 0 Receive Flow Control Enable (RX_FC_0) bits in the Port 0 Manual Flow Control Register (MANUAL_FC_0). This strap affects the default value of the following register bits: ▪ Asymmetric Pause and Pause bits of the Virtual PHY Auto-Negotiation Link Partner Base Page Ability Register (VPHY_AN_LP_BASE_ABILITY)	1b
manual_FC_strap_0	**Port 0 (External MII) Manual Flow Control Enable Strap:** This strap affects the default value of the following register bits: ▪ Port 0 Full-Duplex Manual Flow Control Select (MANUAL_FC_0) bit in the Port 0 Manual Flow Control Register (MANUAL_FC_0) ▪ Asymmetric Pause and Symmetric Pause bits of the Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV) Refer to the respective register definition sections for additional information. **Note:** In MAC mode, this strap is not used. In this mode, the Virtual PHY is not applicable, and full-duplex flow control must be controlled manually by the host, based upon the external PHYs Auto-negotiation results.	0b
SQE_test_disable_strap_0	**SQE Heartbeat Disable Strap:** Configures the default value of the SQEOFF bit of the Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS) when in MII PHY mode. It is not used in RMII PHY or MII MAC modes.	0b

4.2.4.2 Hard-Straps

Hard-straps are latched upon Power-On Reset (POR) or pin reset (nRST) only. Unlike soft-straps, hard-straps always have an associated pin and cannot be overridden by the EEPROM Loader. These straps are used as either direct configuration values or as register defaults. Table 4.3 provides a list of all hard-straps and their associated pins. These straps, along with their pin assignments are also defined in Chapter 3, "Pin Description and Configuration," on page 23.

Table 4.3 Hard-Strap Configuration Strap Definitions

STRAP NAME	DESCRIPTION	PIN(S)
mngt_mode_strap[1:0]	**Serial Management Mode Strap:** Configures the default serial management mode. **00 = RESERVED** **01 = SMI Managed Mode** **10 = I^2C Managed Mode** **11 = RESERVED** Refer to Section 2.3, "Modes of Operation," on page 19 for additional information on the various modes of the device.	MNGT1_LED4P : MNGT0_LED3P Note 4.1
eeprom_size_strap	**EEPROM Size Strap:** Configures the EEPROM size range as specified in Section 8.3, "I2C Master EEPROM Controller," on page 115.	E2PSIZE_LED2P Note 4.1
P0_mode_strap[1:0]	**Port 0 Mode Strap:** Configures the default mode of operation for Port 0. **00 = MII MAC Mode** **01 = MII PHY Mode** **10 = RMII PHY Mode** **11 = RESERVED** These operating modes result from the following mapping: **P0_MODE[2:0]** → **P0_mode_strap[1:0]** 000 → 00 (MII MAC) 001, 010, or 011 → 01 (MII PHY) 100, 101, or 110 → 10 (RMII PHY) 111 → RESERVED Refer to Section 2.3, "Modes of Operation," on page 19 for additional information on the various modes of the device.	P0_MODE2 : P0_MODE1 : P0_MODE0
P0_rmii_clock_dir_strap	**Port 0 RMII Clock Direction Strap:** Configures the default value of the RMII Clock Direction bit of the Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS). **Note:** The value of this strap is the inverse of the P0_MODE1 pin.	P0_MODE1
P0_clock_strength_strap	**Port 0 Clock Strength Strap:** Configures the default value of the RMII/Turbo MII Clock Strength bit of the Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS).	P0_MODE0

Table 4.3 Hard-Strap Configuration Strap Definitions (continued)

<table>
<tr><th>STRAP NAME</th><th>DESCRIPTION</th><th>PIN(S)</th></tr>
<tr><td>turbo_mii_enable_strap_0</td><td>Port 0 Turbo MII Enable Strap: Configures the default value of the Turbo MII Enable bit of the Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS) when in MII PHY mode.</td><td>P0_MODE1</td></tr>
<tr><td>P1_mode_strap[1:0]</td><td>Port 1 Mode Strap: Configures the default mode of operation for Port 1.

00 = MII MAC Mode
01 = MII PHY Mode
10 = RMII PHY Mode
11 = Internal PHY

These operating modes result from the following mapping:
<table>
<tr><th>P1_MODE[2:0]</th><th>P1_mode_strap[1:0]</th></tr>
<tr><td>000</td><td>00 (MII MAC)</td></tr>
<tr><td>001, 010, or 011</td><td>01 (MII PHY)</td></tr>
<tr><td>100, 101, or 110</td><td>10 (RMII PHY)</td></tr>
<tr><td>111</td><td>11 (internal PHY)</td></tr>
</table>

Refer to Section 2.3, "Modes of Operation," on page 19 for additional information on the various modes of the device.</td><td>P1_MODE2 :
P1_MODE1 :
P1_MODE0</td></tr>
<tr><td>P1_rmii_clock_dir_strap</td><td>Port 1 RMII Clock Direction Strap: Configures the default value of the RMII Clock Direction bit of the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL).

Note: The value of this strap is the inverse of the P1_MODE1 pin.</td><td>P1_MODE1</td></tr>
<tr><td>P1_clock_strength_strap</td><td>Port 1 Clock Strength Strap: Configures the default value of the RMII/Turbo MII Clock Strength bit of the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL).</td><td>P1_MODE0</td></tr>
<tr><td>turbo_mii_enable_strap_1</td><td>Port 1 Turbo MII Enable Strap: Configures the default value of the Turbo MII Enable bit of the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL) when in MII PHY MODE.</td><td>P1_MODE1</td></tr>
<tr><td>phy_addr_sel_strap</td><td>PHY Address Select Strap: Configures the default MII management address values for the PHYs and Virtual PHY as detailed in Section 7.1.1, "PHY Addressing," on page 96.</td><td>PHYADDR_LED5P
Note 4.1</td></tr>
<tr><td>led_pol_strap[5:0]</td><td>LED Polarity Strap: Configures the default polarity for each of the LEDs when they are an open-drain or open-source output.

0 = The LED is set as active high, since it is assumed that a LED to ground is used as the pull-down.

1 = The LED is set as active low, since it is assumed that a LED to VDD is used as the pull-up.</td><td>PHYADDR_LED5P :
MNGT1_LED4P :
MNGT0_LED3P :
E2PSIZE_LED2P :
AMDIX2_LED1P :
AMDIX1_LED0P</td></tr>
</table>

Note 4.1 This pin has shared strap functionality. Refer to Table 4.4 for details.

Table 4.4 PIN/Shared Strap Mapping

PIN	STRAP NAME 1	STRAP NAME 2
PHYADDR_LED5P	phy_addr_sel_strap	led_pol_strap[5]
MNGT1_LED4P	mngt_mode_strap[1]	led_pol_strap[4]
MNGT0_LED3P	mngt_mode_strap[0]	led_pol_strap[3]
E2PSIZE_LED2P	eeprom_size_strap	led_pol_strap[2]
AMDIX2_LED1P	auto_mdix_strap_2	led_pol_strap[1]
AMDIX1_LED0P	auto_mdix_strap_1	led_pol_strap[0]

4.3 Power Management

The Port 1 and Port 2 PHYs support several power management and wakeup features.

4.3.1 Port 1 & 2 PHY Power Management

The Port 1 & 2 PHYs provide independent general power-down and energy-detect power-down modes which reduce PHY power consumption. General power-down mode provides power savings by powering down the entire PHY, except the PHY management control interface. General power-down mode must be manually enabled and disabled as described in Section 7.2.9.1, "PHY General Power-Down," on page 109.

In energy-detect power-down mode, the PHY will resume from power-down when energy is seen on the cable (typically from link pulses). If the ENERGYON interrupt (INT7) of either PHYs Port x PHY Interrupt Mask Register (PHY_INTERRUPT_MASK_x) is unmasked, then the corresponding PHY will generate an interrupt. These interrupts are reflected in the Interrupt Status Register (INT_STS) Port 2 PHY Interrupt Event (PHY_INT2) for the Port 2 PHY, and Port 1 PHY Interrupt Event (PHY_INT1) for the Port 1 PHY. These interrupts can be used to trigger the IRQ interrupt output pin, as described in Section 5.2.2, "Ethernet PHY Interrupts," on page 64. Refer to Section 7.2.9.2, "PHY Energy Detect Power-Down," on page 109 for details on the operation and configuration of the PHY energy-detect power-down mode.

Note: The Port 1 PHY is set into general power-down mode when Port 1 is configured to MII PHY, RMII PHY, or MII MAC mode.

Chapter 5 System Interrupts

5.1 Functional Overview

This chapter describes the system interrupt structure. The device provides a multi-tier programmable interrupt structure which is controlled by the System Interrupt Controller. The programmable system interrupts are generated internally by the various sub-modules and can be configured to generate a single external host interrupt via the IRQ interrupt output pin. The programmable nature of the host interrupt provides the user with the ability to optimize performance dependent upon the application requirements. The IRQ interrupt buffer type, polarity, and de-assertion interval are modifiable. The IRQ interrupt can be configured as an open-drain output to facilitate the sharing of interrupts with other devices. All internal interrupts are maskable and capable of triggering the IRQ interrupt.

5.2 Interrupt Sources

The device is capable of generating the following interrupt types:

- Switch Fabric Interrupts (Buffer Manager, Switch Engine, and Port 2,1,0 MACs)
- Ethernet PHY Interrupts (Port 1,2 PHYs)
- GPIO Interrupts (GPIO[5:0])
- General Purpose Timer Interrupt (GPT)
- Software Interrupt (General Purpose)
- Device Ready Interrupt

All interrupts are accessed and configured via registers arranged into a multi-tier, branch-like structure, as shown in Figure 5.1. At the top level of the interrupt structure are the Interrupt Status Register (INT_STS), Interrupt Enable Register (INT_EN), and Interrupt Configuration Register (IRQ_CFG).

The Interrupt Status Register (INT_STS) and Interrupt Enable Register (INT_EN) aggregate and enable/disable all interrupts from the various sub-modules, combining them together to create the IRQ interrupt. These registers provide direct interrupt access/configuration to the General Purpose Timer, software, and device ready interrupts. These interrupts can be monitored, enabled/disabled, and cleared, directly within these two registers. In addition, interrupt event indications are provided for the Switch Fabric, Port 1 & 2 Ethernet PHYs, and GPIO interrupts. These interrupts differ in that the interrupt sources are generated and cleared in other sub-block registers. The Interrupt Status Register (INT_STS) does not provide details on what specific event within the sub-module caused the interrupt, and requires the software to poll an additional sub-module interrupt register (as shown in Figure 5.1) to determine the exact interrupt source and clear it. For interrupts which involve multiple registers, only after the interrupt has been serviced and cleared at its source will it be cleared in the Interrupt Status Register (INT_STS).

The Interrupt Configuration Register (IRQ_CFG) is responsible for enabling/disabling the IRQ interrupt output pin as well as configuring its properties. This register allows the modification of the IRQ pin buffer type, polarity, and de-assertion interval. The de-assertion timer guarantees a minimum interrupt de-assertion period for the IRQ output and is programmable via the Interrupt De-assertion Interval (INT_DEAS) field of the Interrupt Configuration Register (IRQ_CFG). A setting of all zeros disables the de-assertion timer. The de-assertion interval starts when the IRQ pin de-asserts, regardless of the reason.

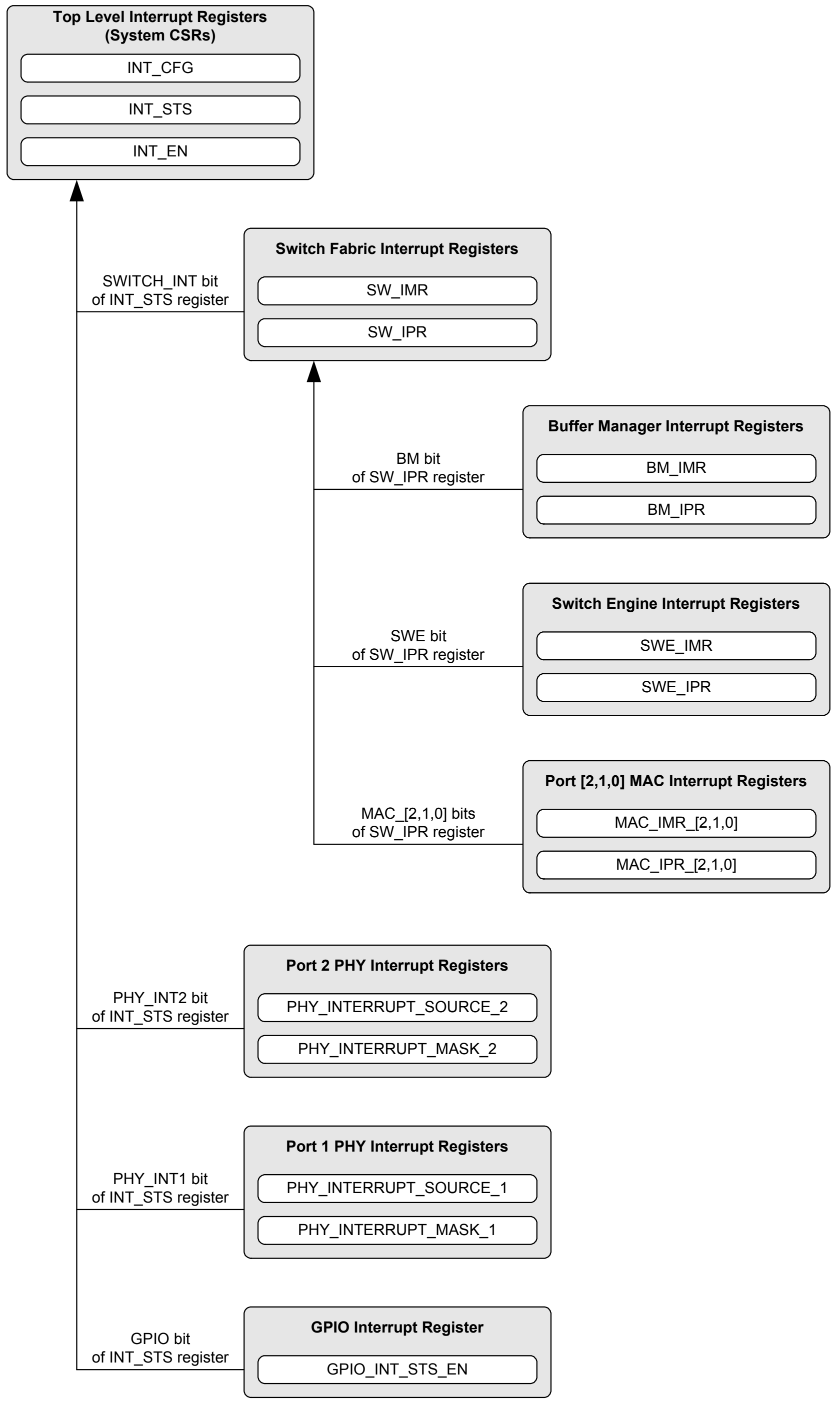


Figure 5.1 Functional Interrupt Register Hierarchy

The following sections detail each category of interrupts and their related registers. Refer to Chapter 13, "Register Descriptions," on page 148 for bit-level definitions of all interrupt registers.

5.2.1 Switch Fabric Interrupts

Multiple Switch Fabric interrupt sources are provided in a three-tiered register structure as shown in Figure 5.1. The top-level Switch Fabric Interrupt Event (SWITCH_INT) bit of the Interrupt Status Register (INT_STS) provides indication that a Switch Fabric interrupt event occurred in the Switch Global Interrupt Pending Register (SW_IPR).

The Switch Engine Interrupt Pending Register (SWE_IPR) and Switch Engine Interrupt Mask Register (SWE_IMR) provide status and enabling/disabling of all Switch Fabric sub-modules interrupts (Buffer Manager, Switch Engine, and Port 2,1,0 MACs).

The low-level Switch Fabric sub-module interrupt pending and mask registers of the Buffer Manager, Switch Engine, and Port 2,1,0 MACs provide multiple interrupt sources from their respective sub-modules. These low-level registers provide the following interrupt sources:

- **Buffer Manager** (Buffer Manager Interrupt Mask Register (BM_IMR) and Buffer Manager Interrupt Pending Register (BM_IPR))
  —Status B Pending
  —Status A Pending
- **Switch Engine** (Switch Engine Interrupt Mask Register (SWE_IMR) and Switch Engine Interrupt Pending Register (SWE_IPR))
  —Interrupt Pending
- **Port 2,1,0 MACs** (Port x MAC Interrupt Mask Register (MAC_IMR_x) and Port x MAC Interrupt Pending Register (MAC_IPR_x))
  —No currently supported interrupt sources. These registers are reserved for future use.

In order for a Switch Fabric interrupt event to trigger the external IRQ interrupt pin, the following must be configured:

- The desired Switch Fabric sub-module interrupt event must be enabled in the corresponding mask register (Buffer Manager Interrupt Mask Register (BM_IMR) for the Buffer Manager, Switch Engine Interrupt Mask Register (SWE_IMR) for the Switch Engine, and/or Port x MAC Interrupt Mask Register (MAC_IMR_x) for the Port 2,1,0 MACs)
- The desired Switch Fabric sub-module interrupt event must be enabled in the Switch Global Interrupt Mask Register (SW_IMR)
- Switch Fabric Interrupt Event Enable (SWITCH_INT_EN) bit of the Interrupt Enable Register (INT_EN) must be set
- IRQ output must be enabled via the IRQ Enable (IRQ_EN) bit of the Interrupt Configuration Register (IRQ_CFG)

For additional details on the Switch Fabric interrupts, refer to Section 6.6, "Switch Fabric Interrupts," on page 95.

5.2.2 Ethernet PHY Interrupts

The Port 1 and Port 2 PHYs each provide a set of identical interrupt sources. The top-level Port 1 PHY Interrupt Event (PHY_INT1) and Port 2 PHY Interrupt Event (PHY_INT2) bits of the Interrupt Status Register (INT_STS) provide indication that a PHY interrupt event occurred in the respective Port x PHY Interrupt Source Flags Register (PHY_INTERRUPT_SOURCE_x).

Port 1 and Port 2 PHY interrupts are enabled/disabled via their respective Port x PHY Interrupt Mask Register (PHY_INTERRUPT_MASK_x). The source of a PHY interrupt can be determined and cleared via the Port x PHY Interrupt Source Flags Register (PHY_INTERRUPT_SOURCE_x). The Port 1 and Port 2 PHYs are each capable of generating unique interrupts based on the following events:

- ENERGYON Activated
- Auto-Negotiation Complete
- Remote Fault Detected

- Link Down (Link Status Negated)
- Auto-Negotiation LP Acknowledge
- Parallel Detection Fault
- Auto-Negotiation Page Received

In order for a Port 1 or Port 2 interrupt event to trigger the external IRQ interrupt pin, the desired PHY interrupt event must be enabled in the corresponding Port x PHY Interrupt Mask Register (PHY_INTERRUPT_MASK_x), the Port 1 PHY Interrupt Event (PHY_INT1) and/or Port 2 PHY Interrupt Event (PHY_INT2) bits of the Interrupt Enable Register (INT_EN) must be set, and IRQ output must be enabled via the IRQ Enable (IRQ_EN) bit of the Interrupt Configuration Register (IRQ_CFG). For additional details on the Ethernet PHY interrupts, refer to Section 7.2.8.1, "PHY Interrupts," on page 108.

5.2.3 GPIO Interrupts

Each GPIO[5:0] is provided with its own interrupt. The top-level GPIO Interrupt Event (GPIO) bit of the Interrupt Status Register (INT_STS) provides indication that a GPIO interrupt event occurred in the General Purpose I/O Interrupt Status and Enable Register (GPIO_INT_STS_EN). The General Purpose I/O Interrupt Status and Enable Register (GPIO_INT_STS_EN) provides enabling/disabling and status of each GPIO[5:0] interrupt.

In order for a GPIO interrupt event to trigger the external IRQ interrupt pin, the desired GPIO interrupt must be enabled in the General Purpose I/O Interrupt Status and Enable Register (GPIO_INT_STS_EN), the GPIO Interrupt Event Enable (GPIO_EN) bit of the Interrupt Enable Register (INT_EN) must be set, and IRQ output must be enabled via the IRQ Enable (IRQ_EN) bit of the Interrupt Configuration Register (IRQ_CFG). For additional details on the GPIO interrupts, refer to Section 12.2.1, "GPIO Interrupts," on page 144.

5.2.4 General Purpose Timer Interrupt

A GP Timer (GPT_INT) interrupt is provided in the top-level Interrupt Status Register (INT_STS) and Interrupt Enable Register (INT_EN). This interrupt is issued when the General Purpose Timer Configuration Register (GPT_CFG) wraps past zero to FFFFh, and is cleared when the GP Timer (GPT_INT) bit of the Interrupt Status Register (INT_STS) is written with 1.

In order for a General Purpose Timer interrupt event to trigger the external IRQ interrupt pin, the GPT must be enabled via the General Purpose Timer Enable (TIMER_EN) bit of the General Purpose Timer Configuration Register (GPT_CFG), the GP Timer Interrupt Enable (GPT_INT_EN) bit of the Interrupt Enable Register (INT_EN) must be set, and IRQ output must be enabled via the IRQ Enable (IRQ_EN) bit of the Interrupt Configuration Register (IRQ_CFG). For additional details on the General Purpose Timer, refer to Section 11.1, "General Purpose Timer," on page 143.

5.2.5 Software Interrupt

A general purpose software interrupt is provided in the top level Interrupt Status Register (INT_STS) and Interrupt Enable Register (INT_EN). The Software Interrupt (SW_INT) bit of the Interrupt Status Register (INT_STS) is generated when the Software Interrupt Enable (SW_INT_EN) bit of the Interrupt Enable Register (INT_EN) is set. This interrupt provides an easy way for software to generate an interrupt, and is designed for general software usage.

5.2.6 Device Ready Interrupt

A device ready interrupt is provided in the top-level Interrupt Status Register (INT_STS) and Interrupt Enable Register (INT_EN). The Device Ready (READY) bit of the Interrupt Status Register (INT_STS) indicates that the device is ready to be accessed after a power-up or reset condition. Writing a 1 to this bit in the Interrupt Status Register (INT_STS) will clear it.

In order for a device ready interrupt event to trigger the external IRQ interrupt pin, the Device Ready Enable (READY_EN) bit of the Interrupt Enable Register (INT_EN) must be set, and IRQ output must be enabled via the IRQ Enable (IRQ_EN) bit of the Interrupt Configuration Register (IRQ_CFG).

Chapter 6 Switch Fabric

6.1 Functional Overview

At the core of the device is the high performance, high efficiency 3 port Ethernet Switch Fabric. The Switch Fabric contains a 3 port VLAN layer 2 Switch Engine that supports untagged, VLAN tagged, and priority tagged frames. The Switch Fabric provides an extensive feature set which includes spanning tree protocol support, multicast packet filtering and Quality of Service (QoS) packet prioritization by VLAN tag, destination address, port default value or DIFFSERV/TOS, allowing for a range of prioritization implementations. 32K of buffer RAM allows for the storage of multiple packets while forwarding operations are completed, and a 512 entry forwarding table provides room for MAC address forwarding tables. Each port is allocated a cluster of 4 dynamic QoS queues which allow each queue size to grow and shrink with traffic, effectively utilizing all available memory. This memory is managed dynamically via the Buffer Manager block within the Switch Fabric. All aspects of the Switch Fabric are managed via the Switch Fabric configuration and status registers (CSR), which are indirectly accessible via the system control and status registers.

The Switch Fabric consists of four major block types:

- Switch Fabric CSRs - These registers provide access to various Switch Fabric parameters for configuration and monitoring.
- 10/100 Ethernet MACs - A total of three MACs are included in the Switch Fabric which provide basic 10/100 Ethernet functionality for each Switch Fabric port.
- Switch Engine (SWE) - This block is the core of the Switch Fabric and provides VLAN layer 2 switching for all three switch ports.
- Buffer Manager (BM) - This block provides control of the free buffer space, transmit queues, and scheduling.

Refer to Figure 2.1 Internal Block Diagram on page 16 for details on the interconnection of the Switch Fabric blocks within the device.

6.2 Switch Fabric CSRs

The Switch Fabric CSRs provide register level access to the various parameters of the Switch Fabric. Switch Fabric related registers can be classified into two main categories based upon their method of access: direct and indirect.

The directly accessible Switch Fabric registers are part of the main system CSRs and are detailed in Section 13.2.4, "Switch Fabric," on page 164. These registers provide Switch Fabric manual flow control (Ports 0-2), data/command registers (for access to the indirect Switch Fabric registers), and switch MAC address configuration.

The indirectly accessible Switch Fabric registers reside within the Switch Fabric and must be accessed indirectly via the Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA) and Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD), or the set of Switch Fabric CSR Interface Direct Data Registers (SWITCH_CSR_DIRECT_DATA). The indirectly accessible Switch Fabric CSRs provide full access to the many configurable parameters of the Switch Engine, Buffer Manager, and each switch port. The Switch Fabric CSRs are detailed in Section 13.4, "Switch Fabric Control and Status Registers," on page 228.

For detailed descriptions of all Switch Fabric related registers, refer to Chapter 13, "Register Descriptions," on page 148.

6.2.1 Switch Fabric CSR Writes

To perform a write to an individual Switch Fabric register, the desired data must first be written into the Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA). The write cycle is initiated by performing a single write to the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD) with the CSR Busy (CSR_BUSY) bit set, the CSR Address (CSR_ADDR[15:0]) field set to the desired register address, the Read/Write (R_nW) bit cleared, the Auto Increment (AUTO_INC) and Auto Decrement (AUTO_DEC) fields cleared, and the desired CSR Byte Enable (CSR_BE[3:0]) bits selected. The completion of the write cycle is indicated by the clearing of the CSR Busy (CSR_BUSY) bit.

A second write method may be used which utilizes the auto increment/decrement function of the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD) for writing sequential register addresses. When using this method, the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD) must first be written with the Auto Increment (AUTO_INC) or Auto Decrement (AUTO_DEC) bit set, the CSR Address (CSR_ADDR[15:0]) field written with the desired register address, the Read/Write (R_nW) bit cleared, and the desired CSR byte enable bits selected (typically all set). The write cycles are then initiated by writing the desired data into the Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA). The completion of the write cycle is indicated by the clearing of the CSR Busy (CSR_BUSY) bit, at which time the address in the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD) is incremented or decremented accordingly. The user may then initiate a subsequent write cycle by writing the desired data into the Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA).

The third write method is to use the direct data range write function. Writes within the Switch Fabric CSR Interface Direct Data Registers (SWITCH_CSR_DIRECT_DATA) address range automatically set the appropriate register address, set all four CSR Byte Enable (CSR_BE[3:0]) bits, clears the Read/Write (R_nW) bit, and set the CSR Busy (CSR_BUSY) bit of the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD). The completion of the write cycle is indicated by the clearing of the CSR Busy (CSR_BUSY) bit. Since the address range of the Switch Fabric CSRs exceeds that of the Switch Fabric CSR Interface Direct Data Registers (SWITCH_CSR_DIRECT_DATA) address range, a sub-set of the Switch Fabric CSRs are mapped to the Switch Fabric CSR Interface Direct Data Registers (SWITCH_CSR_DIRECT_DATA) address range as detailed in Table 13.4, “Switch Fabric CSR to SWITCH_CSR_DIRECT_DATA Address Range Map,” on page 176.

Figure 6.1 illustrates the process required to perform a Switch Fabric CSR write.

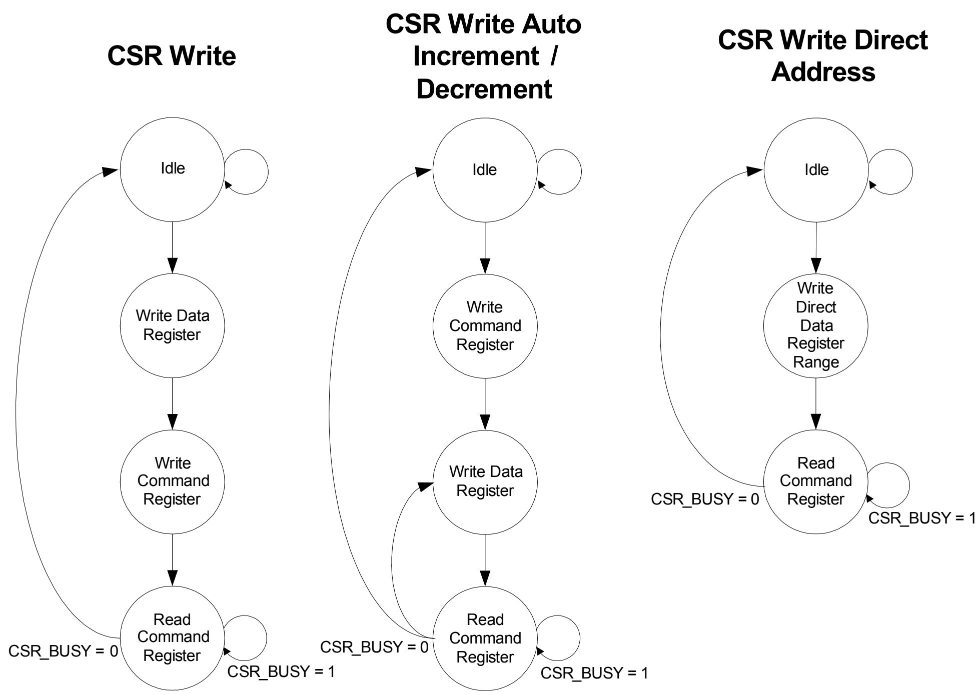


Figure 6.1 Switch Fabric CSR Write Access Flow Diagram

6.2.2 Switch Fabric CSR Reads

To perform a read of an individual Switch Fabric register, the read cycle must be initiated by performing a single write to the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD) with the CSR Busy (CSR_BUSY) bit set, the CSR Address (CSR_ADDR[15:0]) field set to the desired register address, the Read/Write (R_nW) bit set, and the Auto Increment (AUTO_INC) and Auto Decrement (AUTO_DEC) fields cleared. Valid data is available for reading when the CSR Busy (CSR_BUSY) bit is cleared, indicating that the data can be read from the Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA).

A second read method may be used which utilizes the auto increment/decrement function of the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD) for reading sequential register addresses. When using this method, the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD) must first be written with the Auto Increment (AUTO_INC) or Auto Decrement (AUTO_DEC) bit set, the CSR Address (CSR_ADDR[15:0]) field written with the desired register address, and the Read/Write (R_nW) bit set. The completion of a read cycle is indicated by the clearing of the CSR Busy (CSR_BUSY) bit, at which time the data can be read from the Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA). When the data is read, the address in the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD) is incremented or decremented accordingly, and another read cycle is started automatically. The user should clear the Auto Increment (AUTO_INC) and Auto Decrement (AUTO_DEC) bits before reading the last data to avoid an unintended read cycle.

Figure 6.2 illustrates the process required to perform a Switch Fabric CSR read.

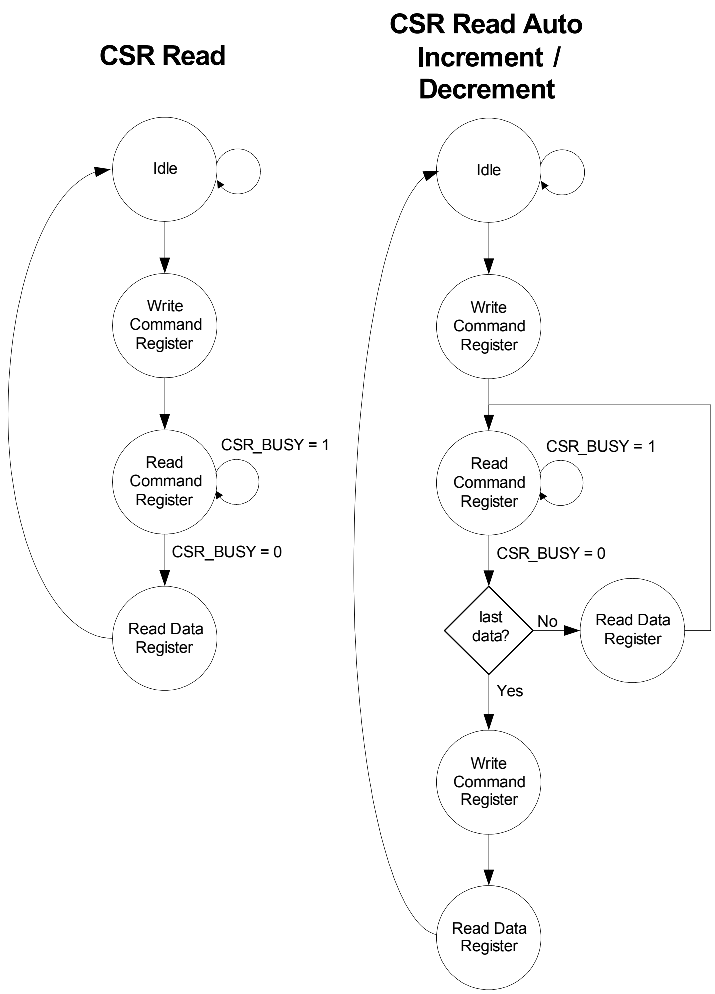


Figure 6.2 Switch Fabric CSR Read Access Flow Diagram

6.2.3 Flow Control Enable Logic

Each Switch Fabric port (0,1,2) is provided with two flow control enable inputs per port, one for transmission and one for reception. Flow control on transmission allows the transmitter to generate back pressure in half-duplex mode, and pause packets in full-duplex. Flow control in reception enables the reception of pause packets to pause transmissions.

The state of these enables is based on the state of the port's duplex and Auto-negotiation settings and the values of the corresponding Manual Flow Control register (Port 1 Manual Flow Control Register (MANUAL_FC_1), Port 2 Manual Flow Control Register (MANUAL_FC_2), or Port 0 Manual Flow Control Register (MANUAL_FC_0)). Table 6.1 details the Switch Fabric flow control enable logic.

When in half-duplex mode, the transmit flow control (back pressure) enable is determined directly by the BP_EN_x bit of the port's manual flow control register. When Auto-negotiation is disabled, or the MANUAL_FC_x bit of the port's manual flow control register is set, the switch port flow control enables during full-duplex are determined by the TX_FC_x and RX_FC_x bits of the port's manual flow control register. When Auto-negotiation is enabled and the MANUAL_FC_x bit is cleared, the switch port flow control enables during full-duplex are determined by Auto-negotiation.

Note: The flow control values in the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) and Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV) are not affected by the values of the manual flow control register. Refer to Section 7.2.5.1, "PHY Pause Flow Control," on page 106 and Section 7.3.1.3, "Virtual PHY Pause Flow Control," on page 112 for additional information on PHY and Virtual PHY flow control settings respectively.

Table 6.1 Switch Fabric Flow Control Enable Logic

CASE	MANUAL_FC_X	AN ENABLE	AN COMPLETE	LP AN ABLE	DUPLEX	AN PAUSE ADVERTISEMENT (Note 6.2)	AN ASYM PAUSE ADVERTISEMENT (Note 6.2)	LP PAUSE ABILITY (Note 6.2)	LP ASYM PAUSE ABILITY (Note 6.2)	RX FLOW CONTROL ENABLE	TX FLOW CONTROL ENABLE
-	1	X	X	X	Half	X	X	X	X	0	BP_EN_x
-	X	0	X	X	Half	X	X	X	X	0	BP_EN_x
-	1	X	X	X	Full	X	X	X	X	RX_FC_x	TX_FC_x
-	X	0	X	X	Full	X	X	X	X	RX_FC_x	TX_FC_x
1	0	1	0	X	X	X	X	X	X	0	0
2	0	1	1	0	Half (Note 6.1)	X	X	X	X	0	BP_EN_x
3	0	1	1	1	Half	X	X	X	X	0	BP_EN_x
4	0	1	1	1	Full	0	0	X	X	0	0
5	0	1	1	1	Full	0	1	0	X	0	0
6	0	1	1	1	Full	0	1	1	0	0	0
7	0	1	1	1	Full	0	1	1	1	0	1
8	0	1	1	1	Full	1	0	0	X	0	0
9	0	1	1	1	Full	1	X	1	X	1	1
10	0	1	1	1	Full	1	1	0	0	0	0
11	0	1	1	1	Full	1	1	0	1	1	0

Note 6.1 If Auto-negotiation is enabled and complete, but the link partner is not Auto-negotiation capable, half-duplex is forced via the parallel detect function.

Note 6.2 For the Port 1 and Port 2 PHYs, these are the bits from the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) and Port x PHY Auto-Negotiation Link Partner Base Page Ability Register (PHY_AN_LP_BASE_ABILITY_x). For the Virtual PHY, these are the local/partner swapped outputs from the bits in the Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV) and Virtual PHY Auto-Negotiation Link Partner Base Page Ability Register (VPHY_AN_LP_BASE_ABILITY). Refer to Section 7.3.1, "Virtual PHY Auto-Negotiation," on page 110 for more information.

Per Table 6.1, the following cases are possible:

- **Case 1** - Auto-negotiation is still in progress. Since the result is not yet established, flow control is disabled.
- **Case 2** - Auto-negotiation is enabled and unsuccessful (link partner not Auto-negotiation capable). The link partner ability is undefined, effectively a don't-care value, in this case. The duplex setting will default to half-duplex in this case. Flow control is determined by the BP_EN_x bit.
- **Case 3** - Auto-negotiation is enabled and successful with half-duplex as a result. The link partner ability is undefined since it only applies to full-duplex operation. Flow control is determined by the BP_EN_x bit.
- **Cases 4-11** -Auto-negotiation is enabled and successful with full-duplex as the result. In these cases, the advertisement registers and the link partner ability controls the RX and TX enables. These cases match IEEE 802.3 Annex 28B.3.
  - **Cases 4,5,6,8,10** - No flow control enabled
  - **Case 7** - Asymmetric pause towards partner (away from switch port)
  - **Case 9** - Symmetric pause
  - **Case 11** - Asymmetric pause from partner (towards switch port)

6.3 10/100 Ethernet MACs

The Switch Fabric contains three 10/100 MAC blocks, one for each switch port (0,1,2). The 10/100 MAC provides the basic 10/100 Ethernet functionality, including transmission deferral and collision back-off/retry, receive/transmit FCS checking and generation, receive/transmit pause flow control, and transmit back pressure. The 10/100 MAC also includes RX and TX FIFOs and per port statistic counters.

6.3.1 Receive MAC

The receive MAC (IEEE 802.3) sublayer decomposes Ethernet packets acquired via the internal MII interface by stripping off the preamble sequence and Start of Frame Delimiter (SFD). The receive MAC checks the FCS, the MAC Control Type, and the byte count against the drop conditions. The packet is stored in the RX FIFO as it is received.

The receive MAC determines the validity of each received packet by checking the Type field, FCS, and oversize or undersize conditions. All bad packets will be either immediately dropped or marked (at the end) as bad packets.

Oversized packets are normally truncated at 1519 or 1523 (VLAN tagged) octets and marked as erroneous. The MAC can be configured to accept packets up to 2048 octets (inclusive), in which case the oversize packets are truncated at 2048 bytes and marked as erroneous.

Undersized packets are defined as packets with a length less than the minimum packet size. The minimum packet size is defined to be 64 bytes, exclusive of preamble sequence and SFD.

The FCS and length/type fields of the frame are checked to detect if the packet has a valid MAC control frame. When the MAC receives a MAC control frame with a valid FCS and determines the operation code is a pause command (Flow Control frame), the MAC will load its internal pause counter with the Number_of_Slots variable from the MAC control frame just received. Anytime the internal pause counter is zero, the transmit MAC will be allowed to transmit (XON). If the internal pause counter is not zero, the receive MAC will not allow the transmit MAC to transmit (XOFF). When the transmit MAC detects an XOFF condition it will continue to transmit the current packet, terminating transmission after the current packet has been transmitted until receiving the XON condition from the receive MAC. The pause counter will begin to decrement at then end of the current transmission, or immediately if no transmission is underway. If another pause command is received while the transmitter is already in pause, the new pause time indicated by the Flow Control packet will be loaded into the pause counter. The pause function is enabled by either Auto-negotiation, or manually as discussed in Section 6.2.3, "Flow Control Enable Logic," on page 70. Pause frames are consumed by the MAC and are not sent to the Switch Engine. Non-pause control frames are optionally filtered or forwarded.

When the receive FIFO is full and additional data continues to be received, an overrun condition occurs and the frame is discarded (FIFO space recovered) or marked as a bad frame.

The receive MAC can be disabled from receiving all frames by clearing the RX Enable bit of the Port x MAC Receive Configuration Register (MAC_RX_CFG_x).

The size of the RX FIFO is 256 bytes. If a bad packet with less than 64 bytes is received, it will be flushed from the FIFO automatically and the FIFO space recovered. Packets equal to or larger than 64 bytes with an error will be marked and reported to the Switch Engine. The Switch Engine will subsequently drop the packet.

6.3.1.1 Receive Counters

The receive MAC gathers statistics on each packet and increments the related counter registers. The following receive counters are supported for each Switch Fabric port. Refer to Table 13.14, “Indirectly Accessible Switch Control and Status Registers,” on page 228 and Section 13.4.2.3 through Section 13.4.2.22 for detailed descriptions of these counters.

- Total undersized packets (Section 13.4.2.3, on page 245)
- Total packets 64 bytes in size (Section 13.4.2.4, on page 246)
- Total packets 65 through 127 bytes in size (Section 13.4.2.5, on page 247)
- Total packets 128 through 255 bytes in size (Section 13.4.2.6, on page 248)
- Total packets 256 through 511 bytes in size (Section 13.4.2.7, on page 249)
- Total packets 512 through 1023 bytes in size (Section 13.4.2.8, on page 250)
- Total packets 1024 through maximum bytes in size (Section 13.4.2.9, on page 251)
- Total oversized packets (Section 13.4.2.10, on page 252)
- Total OK packets (Section 13.4.2.11, on page 253)
- Total packets with CRC errors (Section 13.4.2.12, on page 254)
- Total multicast packets (Section 13.4.2.13, on page 255)
- Total broadcast packets (Section 13.4.2.14, on page 256)
- Total MAC Pause packets (Section 13.4.2.15, on page 257)
- Total fragment packets (Section 13.4.2.16, on page 258)
- Total jabber packets (Section 13.4.2.17, on page 259)
- Total alignment errors (Section 13.4.2.18, on page 260)
- Total bytes received from all packets (Section 13.4.2.19, on page 261)
- Total bytes received from good packets (Section 13.4.2.20, on page 262)
- Total packets with a symbol error (Section 13.4.2.21, on page 263)
- Total MAC control packets (Section 13.4.2.22, on page 264)

6.3.2 Transmit MAC

The transmit MAC generates an Ethernet MAC frame from TX FIFO data. This includes generating the preamble and SFD, calculating and appending the frame checksum value, optionally padding undersize packets to meet the minimum packet requirement size (64 bytes), and maintaining a standard inter-frame gap time during transmit.

The transmit MAC can operate at 10/100Mbps, half- or full-duplex, and with or without flow control depending on the state of the transmission. In half-duplex mode, the transmit MAC meets CSMA/CD IEEE 802.3 requirements. The transmit MAC will re-transmit if collisions occur during the first 64 bytes (normal collisions), or will discard the packet if collisions occur after the first 64 bytes (late collisions). The transmit MAC follows the standard truncated binary exponential back-off algorithm, collision and jamming procedures.

The transmit MAC pre-pends the standard preamble and SFD to every packet from the FIFO. The transmit MAC also follows, as default, the standard Inter-Frame Gap (IFG). The default IFG is 96 bit times and can be adjusted via the IFG Config field of the Port x MAC Transmit Configuration Register (MAC_TX_CFG_x).

Packet padding and cyclic redundant code (FCS) calculation may be optionally performed by the transmit MAC. The auto-padding process automatically adds enough zeros to packets shorter than 64 bytes. The auto-padding and FCS generation is controlled via the TX Pad Enable bit of the Port x MAC Transmit Configuration Register (MAC_TX_CFG_x).

The transmit FIFO acts as a temporary buffer between the transmit MAC and the Switch Engine. The FIFO logic manages the re-transmission for normal collision conditions or discards the frames for late or excessive collisions.

When in full-duplex mode, the transmit MAC uses the flow-control algorithm specified in IEEE 802.3. MAC pause frames are used primarily for flow control packets, which pass signalling information between stations. MAC pause frames have a unique type of 8808h, and a pause op-code of 0001h. The MAC pause frame contains the pause value in the data field. The flow control manager will auto-adapt the procedure based on traffic volume and speed to avoid packet loss and unnecessary pause periods.

When in half-duplex mode, the MAC uses a back pressure algorithm. The back pressure algorithm is based on a forced collision and an aggressive back-off algorithm.

6.3.2.1 Transmit Counters

The transmit MAC gathers statistics on each packet and increments the related counter registers. The following transmit counters are supported for each Switch Fabric port. Refer to Table 13.14, “Indirectly Accessible Switch Control and Status Registers,” on page 228 and Section 13.4.2.25 through Section 13.4.2.42 for detailed descriptions of these counters.

- Total packets deferred (Section 13.4.2.25, on page 267)
- Total pause packets (Section 13.4.2.26, on page 268)
- Total OK packets (Section 13.4.2.27, on page 269)
- Total packets 64 bytes in size (Section 13.4.2.28, on page 270)
- Total packets 65 through 127 bytes in size (Section 13.4.2.29, on page 271)
- Total packets 128 through 255 bytes in size (Section 13.4.2.30, on page 272)
- Total packets 256 through 511 bytes in size (Section 13.4.2.31, on page 273)
- Total packets 512 through 1023 bytes in size (Section 13.4.2.32, on page 274)
- Total packets 1024 through maximum bytes in size (Section 13.4.2.33, on page 275)
- Total undersized packets (Section 13.4.2.34, on page 276)
- Total bytes transmitted from all packets (Section 13.4.2.35, on page 277)

- Total broadcast packets (Section 13.4.2.36, on page 278)
- Total multicast packets (Section 13.4.2.37, on page 279)
- Total packets with a late collision (Section 13.4.2.38, on page 280)
- Total packets with excessive collisions (Section 13.4.2.39, on page 281)
- Total packets with a single collision (Section 13.4.2.40, on page 282)
- Total packets with multiple collisions (Section 13.4.2.41, on page 283)
- Total collision count (Section 13.4.2.42, on page 284)

6.4 Switch Engine (SWE)

The Switch Engine (SWE) is a VLAN layer 2 (link layer) switching engine supporting 3 ports. The SWE supports the following types of frame formats: untagged frames, VLAN tagged frames, and priority tagged frames. The SWE supports both the 802.3 and Ethernet II frame formats.

The SWE provides the control for all forwarding/filtering rules. It handles the address learning and aging, and the destination port resolution based upon the MAC address and VLAN of the packet. The SWE implements the standard bridge port states for spanning tree and provides packet metering for input rate control. It also implements port mirroring, broadcast throttling, and multicast pruning and filtering. Packet priorities are supported based on the IPv4 TOS bits and IPv6 Traffic Class bits using a DIFFSERV Table mapping, the non-DIFFSERV mapped IPv4 precedence bits, VLAN priority using a per port Priority Regeneration Table, DA based static priority, and Traffic Class mapping to one of 4 QoS transmit priority queues.

The following sections detail the various features of the Switch Engine.

6.4.1 MAC Address Lookup Table

The Address Logic Resolution (ALR) maintains a 512 entry MAC Address Table. The ALR searches the table for the destination MAC address. If the search finds a match, the associated data is returned indicating the destination port or ports, whether to filter the packet, the packet's priority (used if enabled), and whether to override the ingress and egress spanning tree port state. Figure 6.3 displays the ALR table entry structure. Refer to the Switch Engine ALR Write Data 0 Register (SWE_ALR_WR_DAT_0) and Switch Engine ALR Write Data 1 Register (SWE_ALR_WR_DAT_1) for detailed descriptions of these bits.

Bit	58	57	56	55	54	53 52 51	50 49 48	47 0
	Valid	Age / Override	Static	Filter	Priority Enable	Priority	Port	MAC Address

Figure 6.3 ALR Table Entry Structure

6.4.1.1 Learning/Aging/Migration

The ALR adds new MAC addresses upon ingress along with the associated receive port.

If the source MAC address already exists, the entry is refreshed. This action serves two purposes. First, if the source port has changed due to a network reconfiguration (migration), it is updated. Second, each instance the entry is refreshed, the aging status bit is set, keeping the entry active. Learning can be disabled per port via the Enable Learning on Ingress field of the Switch Engine Port Ingress Configuration Register (SWE_PORT_INGRSS_CFG).

During each aging period, the ALR scans the learned MAC addresses. For entries which have the aging status bit set, the ALR simply clears the bit. As mentioned above, if a MAC address is subsequently refreshed, the aging bit will be set again and the process would repeat. If a learned entry already had its aging status bit cleared (by a previous scan), the ALR will instead remove the learned entry. Therefore, if two scans occur before a MAC address is refreshed, the entry will be aged and removed. Each aging period is approximately 5 minutes. Therefore an entry will be aged and removed at a minimum of 5 minutes, and a maximum of 10 minutes.

6.4.1.2 Static Entries

If a MAC address entry is manually added by the host CPU, it can be (and typically is) marked as static. Static entries are not subjected to the aging process. Static entries also cannot be changed by the learning process (including migration).

6.4.1.3 Multicast Pruning

The destination port that is returned as a result of a destination MAC address lookup may be a single port or any combination of ports. The latter is used to setup multicast address groups. An entry with a multicast MAC address would be entered manually by the host CPU with the appropriate destination port(s). Typically, the Static bit should also be set to prevent automatic aging of the entry.

6.4.1.4 Address Filtering

Filtering can be performed on a destination MAC address. Such an entry would be entered manually by the host CPU with the Filter bit active. Typically, the Static bit should also be set to prevent automatic aging of the entry.

6.4.1.5 Spanning Tree Port State Override

A special spanning tree port state override setting can be applied to MAC address entries. When the host CPU manually adds an entry with both the Static and Age bits set, packets with a matching destination address will bypass the spanning tree port state (except the Disabled state) and will be forwarded. This feature is typically used to allow the reception of the BPDU packets while a port is in the non-forwarding state. Refer to Section 6.4.5, "Spanning Tree Support," on page 82 for additional details.

6.4.1.6 MAC Destination Address Lookup Priority

If enabled globally in the Switch Engine Global Ingress Configuration Register (SWE_GLOBAL_INGRSS_CFG) and per entry with the Priority Enable bit, the transmit priority for MAC address entries is taken from the associated data of that entry.

6.4.1.7 Host Access

The ALR contains a learning engine that is used by the host CPU to add, delete, and modify the MAC Address Table. This engine is accessed by using the Switch Engine ALR Command Register (SWE_ALR_CMD), Switch Engine ALR Command Status Register (SWE_ALR_CMD_STS), Switch Engine ALR Write Data 0 Register (SWE_ALR_WR_DAT_0), and Switch Engine ALR Write Data 1 Register (SWE_ALR_WR_DAT_1).

The following procedure should be followed in order to add, delete, and modify the ALR entries:

1. Write the Switch Engine ALR Write Data 0 Register (SWE_ALR_WR_DAT_0) and Switch Engine ALR Write Data 1 Register (SWE_ALR_WR_DAT_1) with the desired MAC address and control bits.

   Note: An entry can be deleted by setting the Valid bit to 0.
2. Write the Switch Engine ALR Command Register (SWE_ALR_CMD) register with 0004h (Make Entry).
3. Poll the Make Pending bit in the Switch Engine ALR Command Status Register (SWE_ALR_CMD_STS) until it is cleared.
4. Write the Switch Engine ALR Command Register (SWE_ALR_CMD) with 0000h.

The ALR contains a search engine that is used by the host to read the MAC Address Table. This engine is accessed by using the Switch Engine ALR Command Register (SWE_ALR_CMD), Switch Engine ALR Read Data 0 Register (SWE_ALR_RD_DAT_0), and Switch Engine ALR Read Data 1 Register (SWE_ALR_RD_DAT_1).

Note: The entries read are not necessarily in the same order as they were learned or manually added.

The following procedure should be followed in order to read the ALR entries:

1. Write the Switch Engine ALR Command Register (SWE_ALR_CMD) with 0002h (Get First Entry).
2. Write the Switch Engine ALR Command Register (SWE_ALR_CMD) with 0000h (Clear the Get First Entry Bit).
3. Poll the Valid and End of Table bits in the Switch Engine ALR Read Data 1 Register (SWE_ALR_RD_DAT_1) until either is set.
4. If the Valid bit is set, then the entry is valid and the data from the Switch Engine ALR Read Data 0 Register (SWE_ALR_RD_DAT_0) and Switch Engine ALR Read Data 1 Register (SWE_ALR_RD_DAT_1) can be stored.
5. If the End of Table bit is set, then exit.
6. Write the Switch Engine ALR Command Register (SWE_ALR_CMD) with 0001h (Get Next Entry).
7. Write the Switch Engine ALR Command Register (SWE_ALR_CMD) with 0000h (Clear the Get Next Entry bit).
8. Go to step 3.

Note: Refer to Section 13.4.3.1, on page 287 through Section 13.4.3.6, on page 294 for detailed definitions of these registers.

6.4.2 Forwarding Rules

Upon ingress, packets are filtered or forwarded based on the following rules:

- If the destination port equals the source port (local traffic), the packet is filtered.
- If the source port is in the Disabled state, the packet is filtered.
- If the source port is in the Learning or Listening / Blocking state, the packet is filtered (unless the Spanning Tree Port State Override is in effect).
- If the packet is a multicast packet and it is identified as a IGMP packet and IGMP monitoring is enabled (respectively), the packet is redirected to the IGMP monitor port(s). This check is not done on special tagged packets from the host CPU port when an ALR lookup is not requested. Refer to Section 6.4.10.1, "Packets from the Host CPU," on page 88 for additional information.
- If the destination port is in the disabled state, the packet is filtered. (This rule is for a destination MAC address which is found in the ALR table and the ALR result indicates a single destination port. When there are multiple destination ports or when the MAC address is not found, the packet is sent to only those ports that are in the Forwarding state.)
- If the destination port is in the Learning or Listening / Blocking state, the packet is filtered (unless the Spanning Tree Port State Override is in effect). (This rule is for a destination MAC address which is found in the ALR table and the ALR result indicates a single destination port. When there are multiple destination ports or when the MAC address is not found, the packet is sent to only those ports that are in the Forwarding state.)
- If the Filter bit for the Destination Address is set in the ALR table, the packet is filtered.
- If the packet has a unicast destination MAC address which is not found in the ALR table and the Drop Unknown bit is set, the packet is filtered.
- If the packet has a multicast destination MAC address which is not found in the ALR table and the Filter Multicast bit is set, the packet is filtered.
- If the packet has a broadcast destination MAC address and the Broadcast Storm Control level has been reached, the packet is discarded.
- If Drop on Yellow is set, the packet is colored Yellow, and randomly selected, it is discarded.
- If Drop on Red is set and the packet is colored Red, it is discarded.
- If the destination address was not found in the ALR table (an unknown or a broadcast) and the Broadcast Buffer Level is exceeded, the packet is discarded.
- If there is insufficient buffer space, the packet is discarded.
- If the destination address was not found in the ALR table (an unknown or a broadcast) or the destination address was found in the ALR table with the ALR result indicating multiple destination ports and the port forward states resulted in zero valid destination ports, the packet is filtered.

When the switch is enabled for VLAN support, these following rules also apply:

- If the packet is untagged or priority tagged and the Admit Only VLAN bit for the ingress port is set, the packet is filtered.
- If the packet is tagged and has a VID equal to FFFh, it is filtered.
- If Enable Membership Checking on Ingress is set, Admit Non Member is cleared, and the source port is not a member of the incoming VLAN, the packet is filtered.
- If Enable Membership Checking on Ingress is set and the destination port is not a member of the incoming VLAN, the packet is filtered. (This rule is for a destination MAC address which is found in the ALR table and the ALR result indicates a single destination port. When there are multiple destination ports or when the MAC address is not found, the packet is sent to only those ports that are in the Forwarding state.)
- If the destination address was not found in the ALR table (as unknown or broadcast) or the destination address was found in the ALR table with the ALR result indicating multiple destination

ports and the VLAN broadcast domain containment resulted in zero valid destination ports, the packet is filtered.

Note: For the last three cases, if the VID is not in the VLAN table, the VLAN is considered foreign and the membership result is NULL. A NULL membership will result in the packet being filtered if Enable Membership Checking is set. A NULL membership will also result in the packet being filtered if the destination address is not found in the ALR table (since the packet would have no destinations).

6.4.3 Transmit Priority Queue Selection

The transmit priority queue may be selected from five options. As shown in Figure 6.4, the priority may be based on:

- the static value for the destination address in the ALR table
- the precedence bits in the IPv4 TOS octet
- the DIFFSERV mapping table indexed by the IPv4 TOS octet or the IPv6 Traffic Class octet
- the VLAN tag priority field using the per port Priority Regeneration table
- the port default

All options are sent through the Traffic Class table which maps the selected priority to one of the four output queues.

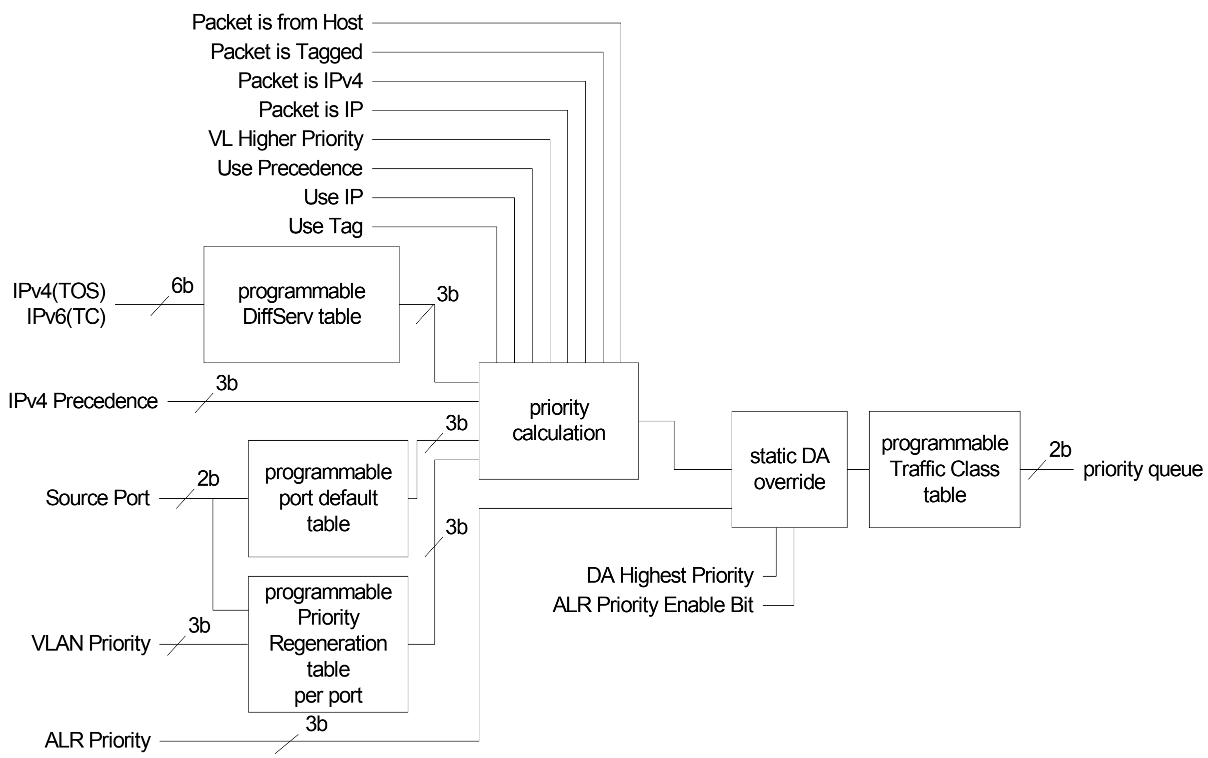


Figure 6.4 Switch Engine Transmit Queue Selection

The transmit queue priority is based on the packet type and device configuration as shown in Figure 6.5. Refer to Section 13.4.3.16, "Switch Engine Global Ingress Configuration Register (SWE_GLOBAL_INGRSS_CFG)," on page 306 for definitions of the configuration bits.

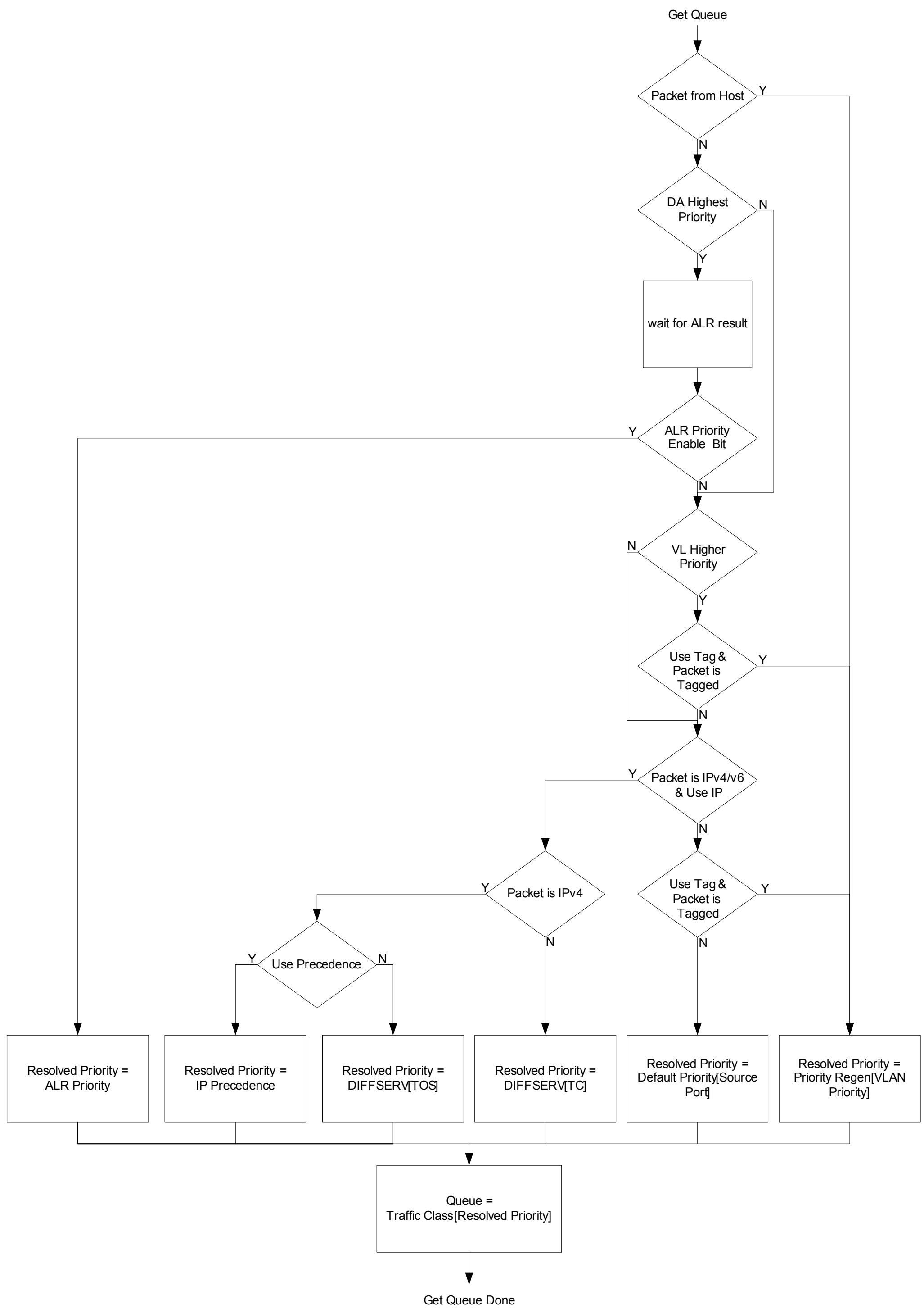


Figure 6.5 Switch Engine Transmit Queue Calculation

6.4.3.1 Port Default Priority

As detailed in Figure 6.5, the default priority is based on the ingress port's priority bits in its port VID value. The PVID table is read and written by using the Switch Engine VLAN Command Register (SWE_VLAN_CMD), Switch Engine VLAN Write Data Register (SWE_VLAN_WR_DATA), Switch Engine VLAN Read Data Register (SWE_VLAN_RD_DATA), and Switch Engine VLAN Command Status Register (SWE_VLAN_CMD_STS). Refer to Section 13.4.3.8, on page 296 through Section 13.4.3.11, on page 301 for detailed VLAN register descriptions.

6.4.3.2 IP Precedence Based Priority

The transmit priority queue can be chosen based on the Precedence bits of the IPv4 TOS octet. This is supported for tagged and non-tagged packets for both type field and length field encapsulations. The Precedence bits are the three most significant bits of the IPv4 TOS octet.

6.4.3.3 DIFFSERV Based Priority

The transmit priority queue can be chosen based on the DIFFSERV usage of the IPv4 TOS or IPv6 Traffic Class octet. This is supported for tagged and non-tagged packets for both type field and length field encapsulations.

The DIFFSERV table is used to determine the packet priority from the 6-bit Differentiated Services (DS) field. The DS field is defined as the six most significant bits of the IPv4 TOS octet or the IPv6 Traffic Class octet and is used as an index into the DIFFSERV table. The output of the DIFFSERV table is then used as the priority. This priority is then passed through the Traffic Class table to select the transmit priority queue.

Note: The DIFFSERV table is not initialized upon reset or power-up. If DIFFSERV is enabled, then the full table must be initialized by the host.

The DIFFSERV table is read and written by using the Switch Engine DIFFSERV Table Command Register (SWE_DIFFSERV_TBL_CFG), Switch Engine DIFFSERV Table Write Data Register (SWE_DIFFSERV_TBL_WR_DATA), Switch Engine DIFFSERV Table Read Data Register (SWE_DIFFSERV_TBL_RD_DATA), and Switch Engine DIFFSERV Table Command Status Register (SWE_DIFFSERV_TBL_CMD_STS). Refer to Section 13.4.3.12, on page 302 through Section 13.4.3.15, on page 305 for detailed DIFFSERV register descriptions.

6.4.3.4 VLAN Priority

As detailed in Figure 6.5, the transmit priority queue can be taken from the priority field of the VLAN tag. The VLAN priority is sent through a per port Priority Regeneration table, which is used to map the VLAN priority into a user defined priority.

The Priority Regeneration table is programmed by using the Switch Engine Port 0 Ingress VLAN Priority Regeneration Table Register (SWE_INGRSS_REGEN_TBL_0), Switch Engine Port 1 Ingress VLAN Priority Regeneration Table Register (SWE_INGRSS_REGEN_TBL_1), and Switch Engine Port 2 Ingress VLAN Priority Regeneration Table Register (SWE_INGRSS_REGEN_TBL_2). Refer to Section 13.4.3.33, on page 325 through Section 13.4.3.35, on page 327 for detailed descriptions of these registers.

6.4.4 VLAN Support

The Switch Engine supports 16 active VLANs out of a possible 4096. The VLAN table contains the 16 active VLAN entries, each consisting of the VID, the port membership, and un-tagging instructions.

17	16	15	14	13	12	11 ... 0
Member Port 2	Un-tag Port 2	Member Port 1	Un-tag Port 1	Member MII	Un-tag MII	VID

Figure 6.6 VLAN Table Entry Structure

On ingress, if a packet has a VLAN tag containing a valid VID (not 000h or FFFh), the VID table is searched. If the VID is found, the VLAN is considered active and the membership and un-tag instruction is used. If the VID is not found, the VLAN is considered foreign and the membership result is NULL. A NULL membership will result in the packet being filtered if Enable Membership Checking is set. A NULL membership will also result in the packet being filtered if the destination address is not found in the ALR table (since the packet would have no destinations).

On ingress, if a packet does not have a VLAN tag or if the VLAN tag contains VID with a value of 0 (priority tag), the packet is assigned a VLAN based on the Port Default VID (PVID) and Priority. The PVID is then used to access the above VLAN table. The usage of the PVID can be forced by setting the 802.1Q VLAN Disable bit, in effect creating port based VLANs.

The VLAN membership of the packet is used for ingress and egress checking and for VLAN broadcast domain containment. The un-tag instructions are used at egress on ports defined as hybrid ports.

Refer to Section 13.4.3.8, on page 296 through Section 13.4.3.11, on page 301 for detailed VLAN register descriptions.

6.4.5 Spanning Tree Support

Hardware support for the Spanning Tree Protocol (STP) and the Rapid Spanning Tree Protocol (RSTP) includes a per port state register as well as the override bit in the MAC Address Table entries (Section 6.4.1.5, on page 76) and the host CPU port special tagging (Section 6.4.10, on page 88).

The Switch Engine Port State Register (SWE_PORT_STATE) is used to place a port into one of the modes as shown in Table 6.2. Normally only Port 1 and Port 2 are placed into modes other than forwarding. Port 0, which is connected to the host CPU, should normally be left in forwarding mode.

Table 6.2 Spanning Tree States

Port State	Hardware Action	Software Action
11 - Disabled	Received packets on the port are always discarded. Transmissions to the port are always blocked. Learning on the port is disabled.	The host CPU may attempt to send packets to the port in this state, but they will not be transmitted.

Table 6.2 Spanning Tree States (continued)

Port State	Hardware Action	Software Action
01 - Blocking	Received packets on the port are discarded unless overridden. Transmissions to the port are blocked unless overridden. Learning on the port is disabled.	The MAC Address Table should be programmed with entries that the host CPU needs to receive (e.g. the BPDU address). The static and override bits should be set. The host CPU may send packets to the port in this state. Only packets with STP override will be transmitted. **Note:** There is no hardware distinction between the Blocking and Listening states.
01 - Listening	Received packets on the port are discarded unless overridden. Transmissions to the port are blocked unless overridden. Learning on the port is disabled.	The MAC Address Table should be programmed with entries that the host CPU needs to receive (e.g. the BPDU address). The static and override bits should be set. The host CPU may send packets to the port in this state. Only packets with STP override will be transmitted.
10 - Learning	Received packets on the port are discarded unless overridden. Transmissions to the port are blocked unless overridden. Learning on the port is enabled.	The MAC Address Table should be programmed with entries that the host CPU needs to receive (e.g. the BPDU address). The static and override bits should be set. The host CPU may send packets to the port in this state. Only packets with STP override will be transmitted.
00 - Forwarding	Received packets on the port are forwarded normally. Transmissions to the port are sent normally. Learning on the port is enabled.	The MAC Address Table should be programmed with entries that the host CPU needs to receive (e.g. the BPDU address). The static and override bits should be set. The host CPU may send packets to the port in this state.

6.4.6 Ingress Flow Metering and Coloring

Hardware ingress rate limiting is supported by metering packet streams and marking packets as either Green, Yellow, or Red according to three traffic parameters: Committed Information Rate (CIR), Committed Burst Size (CBS), and Excess Burst Size (EBS). A packet is marked Green if it does not exceed the CBS, Yellow if it exceeds to CBS but not the EBS, or Red otherwise.

Ingress flow metering and coloring is enabled via the Ingress Rate Enable bit in the Switch Engine Ingress Rate Configuration Register (SWE_INGRSS_RATE_CFG). Once enabled, each incoming packet is classified into a stream. Streams are defined as per port (3 streams), per priority (8 streams), or per port & priority (24 streams) as selected via the Rate Mode bits in the Switch Engine Ingress Rate Configuration Register (SWE_INGRSS_RATE_CFG). Each stream can have a different CIR setting. All streams share common CBS and EBS settings. CIR, CBS, and EBS are programmed via the Switch Engine Ingress Rate Command Register (SWE_INGRSS_RATE_CMD) and Switch Engine Ingress Rate Write Data Register (SWE_INGRSS_RATE_WR_DATA).

Each stream is metered according to RFC 2697. At the rate set by the CIR, two token buckets are credited per stream. First, the Committed Burst bucket is incremented up to the maximum set by the CBS. Once the Committed Burst bucket is full, the Excess Burst bucket is incremented up to the maximum set by the EBS. The CIR rate is specified in time per byte. The value programmed is in approximately 20 nS per byte increments. Typical values are listed in Table 6.3. When a port is receiving at 10Mbps, any setting faster than 39 has the effect of not limiting the rate.

Table 6.3 Typical Ingress Rate Settings

CIR Setting	Time Per Byte	Bandwidth
0-3	80 nS	100 Mbps
4	100 nS	80 Mbps
5	120 nS	67 Mbps
6	140 nS	57 Mbps
7	160 nS	50 Mbps
9	200 nS	40 Mbps
12	260 nS	31 Mbps
19	400 nS	20 Mbps
39	800 nS	10 Mbps
79	1600 nS	5 Mbps
160	3220 nS	2.5 Mbps
402	8060 nS	1 Mbps
804	16100 nS	500 Kbps
1610	32220 nS	250 Kbps
4028	80580 nS	100 Kbps
8056	161140 nS	50 Kbps

After each packet is received, the bucket is decremented. If the Committed Burst bucket has sufficient tokens, it is debited and the packet is colored Green. If the Committed Burst bucket lacks sufficient tokens for the packet, the Excess Burst bucket is checked. If the Excess Burst bucket has sufficient tokens, it is debited, the packet is colored Yellow and is subjected to random discard. If the Excess Burst bucket lacks sufficient tokens for the packet, the packet is colored Red and is discarded.

Note: All of the token buckets are initialized to the default value of 1536. If lower values are programmed into the CBS and EBS parameters, the token buckets will need to be normally depleted below these values before the values have any affect on limiting the maximum value of the token buckets.

Refer to Section 13.4.3.25, on page 316 through Section 13.4.3.29, on page 321 for detailed register descriptions.

6.4.6.1 Ingress Flow Calculation

Based on the flow monitoring mode, an ingress flow definition can include the ingress priority. This is calculated similarly to the transmit queue with the exception that the Traffic Class table is not used. As shown in Figure 6.7, the priority can be based on:

- The static value for the destination address in the ALR table.
- The precedence bits in the IPv4 TOS octet
- The DIFFSERV mapping table indexed by the IPv4 TOS octet or the IPv6 Traffic Class octet
- The VLAN tag priority field using the per port Priority Regeneration table
- The port default

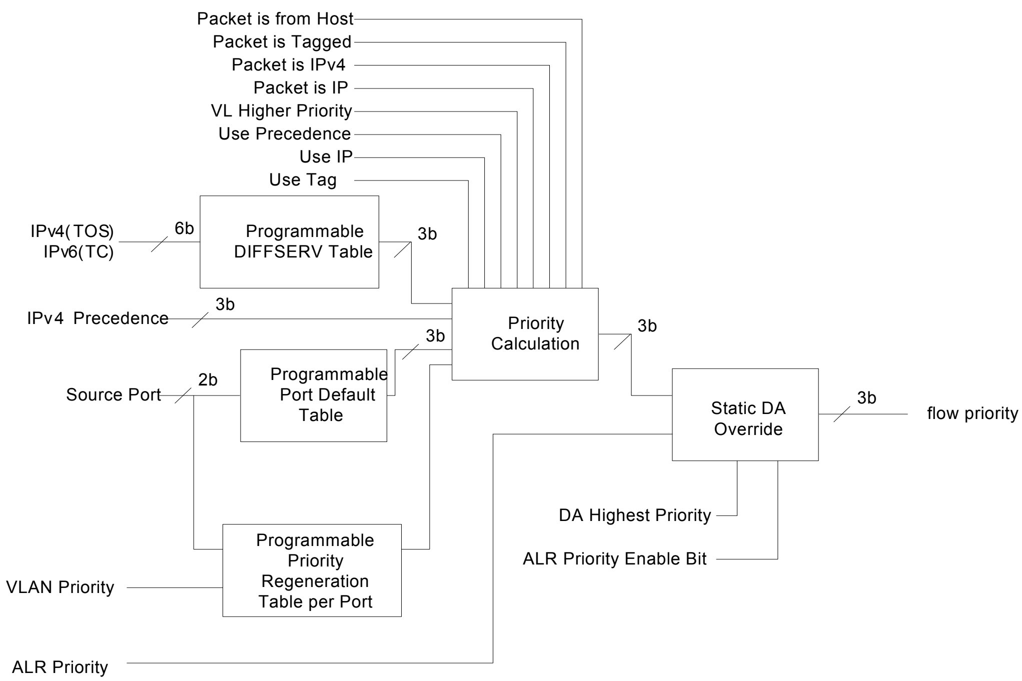


Figure 6.7 Switch Engine Ingress Flow Priority Selection

The ingress flow calculation is based on the packet type and the device configuration as shown in Figure 6.8.

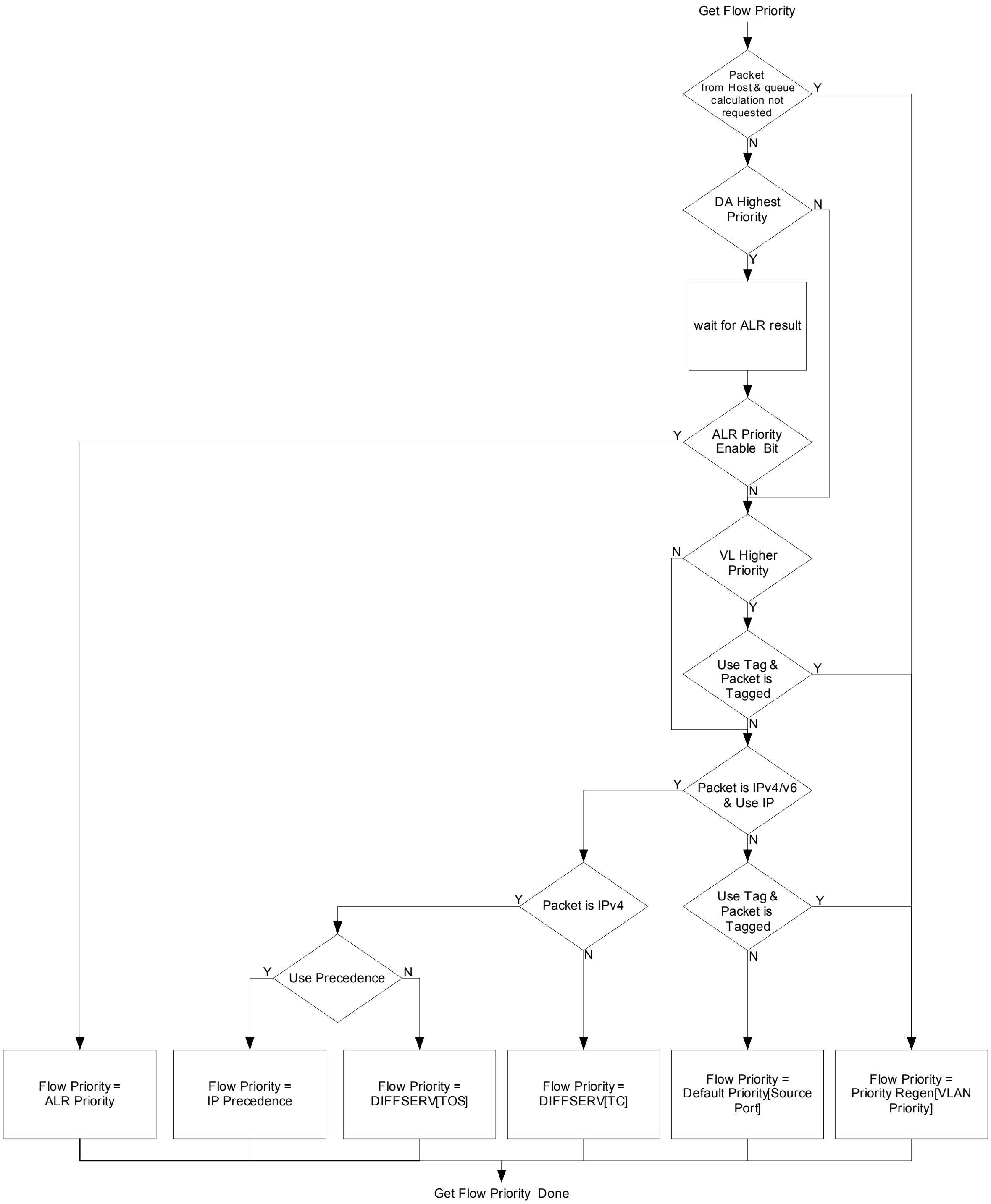


Figure 6.8 Switch Engine Ingress Flow Priority Calculation

6.4.7 Broadcast Storm Control

In addition to ingress rate limiting, the device supports hardware broadcast storm control on a per port basis. This feature is enabled via the Switch Engine Broadcast Throttling Register (SWE_BCST_THROT). The allowed rate per port is specified as the number of bytes multiplied by 64 allowed to be received every 1.72 mS interval. Packets that exceed this limit are dropped. Typical values are listed in Table 6.4. When a port is receiving at 10Mbps, any setting above 34 has the effect of not limiting the rate.

Table 6.4 Typical Broadcast Rate Settings

Broadcast Throttle Level	Bandwidth
252	75 Mbps
168	50 Mbps
134	40 Mbps
67	20 Mbps
34	10 Mbps
17	5 Mbps
8	2.4 Mbps
4	1.2 Mbps
3	900 Kbps
2	600 Kbps
1	300 Kbps

In addition to the rate limit, the Buffer Manager Broadcast Buffer Level Register (BM_BCST_LVL) specifies the maximum number of buffers that can be used by broadcasts, multicasts, and unknown unicasts.

6.4.8 IPv4 IGMP Support

The device provides Internet Group Management Protocol (IGMP) hardware support using two mechanisms: IGMP monitoring and Multicast Pruning.

On ingress, if IGMP packet monitoring is enabled in the Switch Engine Global Ingress Configuration Register (SWE_GLOBAL_INGRSS_CFG), IGMP *multicast* packets are trapped and redirected to the IGMP monitor port (typically set to the port to which the host CPU is connected). IGMP packets are identified as IPv4 packets with a protocol of 2. Both Ethernet and IEEE 802.3 frame formats are supported as are VLAN tagged packets.

Once the IGMP packets are received by the host CPU, the host software can decide which port or ports need to be members of the multicast group. This group is then added to the ALR table as detailed in Section 6.4.1.3, "Multicast Pruning," on page 76. The host software should also forward the original IGMP packet if necessary.

Normally, packets are never transmitted back to the receiving port. For IGMP monitoring, this may optionally be enabled via the Switch Engine Global Ingress Configuration Register (SWE_GLOBAL_INGRSS_CFG). This function would be used if the monitoring port wished to participate in the IGMP group without the need to perform special handling in the transmit portion of the driver software.

Note: Most forwarding rules are skipped when a packet is monitored. However, a packet is still filtered if:

- The source port is in the Disabled state
- The source port is in the Learning or Listening / Blocking state (unless Spanning Tree Port State Override is in effect.
- VLAN's are enabled, the packet is untagged or priority tagged, and the Admit Only VLAN bit for the ingress port is set.
- VLAN's are enabled and the packet is tagged and had a VID equal to FFFh.
- VLAN's are enabled, Enabled Membership Checking on Ingress is set, Admit Non Member is cleared, and the source port is not a member of the incoming VLAN.

6.4.9 Port Mirroring

The device supports port mirroring where packets received or transmitted on a port or ports can also be copied onto another "sniffer" port.

Port mirroring is configured using the Switch Engine Port Mirroring Register (SWE_PORT_MIRROR). Multiple mirrored ports can be defined, but only one sniffer port can be defined.

When receive mirroring is enabled, packets that are forwarded from a port designated as a mirrored port are also transmitted by the sniffer port. For example, Port 2 is setup to be a mirrored port and Port 0 is setup to be the sniffer port. If a packet is received on Port 2 with a destination of Port 1, it is forwarded to both Port 1 and Port 0.

When transmit mirroring is enabled, packets that are forwarded to a port designated as a mirrored port are also transmitted by the sniffer port. For example, Port 2 is setup to be a mirrored port and Port 0 is setup to be the sniffer port. If a packet is received on Port 1 with a destination of Port 2, it is forwarded to both Port 2 and Port 0.

Note: A packet will never be transmitted out of the receiving port. A receive packet is not normally mirrored if it is filtered. This can optionally be enabled.

6.4.10 Host CPU Port Special Tagging

The Switch Engine Ingress Port Type Register (SWE_INGRSS_PORT_TYP) and Buffer Manager Egress Port Type Register (BM_EGRSS_PORT_TYPE) are used to enable a special VLAN tag that is used by the host CPU. This special tag is used to specify the port(s) where packets from the CPU should be sent, and to indicate which port received the packet that was forwarded to the CPU.

6.4.10.1 Packets from the Host CPU

The Switch Engine Ingress Port Type Register (SWE_INGRSS_PORT_TYP) configures the switch to use the special VLAN tag in packets from the host CPU as a destination port indicator. A setting of 11b should be used on the port that is connected to the host CPU (typically Port 0). A setting of 00b should be used on the normal network ports.

The special VLAN tag is a normal VLAN tag where the VID field is used as the destination port indicator.

VID bit 3 indicates a request for an ALR lookup.

If VID bit 3 is zero, then bits 0 and 1 specify the destination port (0, 1, 2) or broadcast (3). Bit 4 is used to specify if the STP port state should be overridden. When set, the packet will be transmitted, even if the destination port(s) is (are) in the Learning or Listening / Blocking state.

If VID bit 3 is one, then the normal ALR lookup is performed and learning is performed on the source address (if enabled in the Switch Engine Port Ingress Configuration Register

(SWE_PORT_INGRSS_CFG) and the port state for the CPU port is set to Forwarding or Learning). The STP port state override is taken from the ALR entry.

VID bit 5 indicates a request to calculate the packet priority (and egress queue) based on the packet contents.

If VID bit 5 is zero, the PRI field from the VLAN tag is used as the packet priority.

If VID bit 5 is one, the packet priority is calculated from the packet contents. The procedure described in Section 6.4.3, "Transmit Priority Queue Selection," on page 79 is followed with the exception that the special tag is skipped and the VLAN priority is taken from the second VLAN tag, if it exists.

VID bit 6 indicates a request to follow VLAN rules.

If VID bit 6 is zero, a default membership of “all ports” is assumed and no VLAN rules are followed.

If VID bit 6 is one, all ingress and egress VLAN rules are followed. The procedure described in Section 6.4.2, "Forwarding Rules," on page 78 is followed with the exception that the special tag is skipped and the VID is taken from the second VLAN tag if it exists.

Upon egress from the destination port(s), the special tag is removed. If a regular VLAN tag needs to be sent as part of the packet, then it should be part of the packet data from the host CPU port or set as an unused bit in the VID field.

Note: When specifying Port 0 as the destination port, the VID will be set to 0. A VID of 0 is normally considered a priority tagged packet. Such a packet will be filtered if Admit Only VLAN is set on the host CPU port. Either avoid setting Admit Only VLAN on the host CPU port or set an unused bit in the VID field.

Note: The maximum size tagged packet that can normally be sent into a switch port (on port 0) is 1522 bytes. Since the special tag consumes four bytes of the packet length, the outgoing packet is limited to 1518 bytes, even if it contains a regular VLAN tag as part of the packet data. If a larger outgoing packet is required, the Jumbo2K bit in the Port x MAC Receive Configuration Register (MAC_RX_CFG_x) of Port 0 should be set.

6.4.10.2 Packets to the Host CPU

The Buffer Manager Egress Port Type Register (BM_EGRSS_PORT_TYPE) configures the switch to add the special VLAN tag in packets to the host CPU as a source port indicator. A setting of 11b should be used only on the port that is connected to the host CPU (typically Port 0). Other settings can be used on the normal network ports as needed.

The special VLAN tag is a normal VLAN tag where:

- The priority field indicates the packet’s priority as classified on receive.
- Bits 0 and 1 of the VID field specify the source port (0, 1, or 2).
- Bit 3 of the VID field indicates the packet was a monitored IGMP packet.
- Bit 4 of the VID field indicates STP override was set (static AND age bits set) in the ALR entry for the packet’s Destination MAC Address.
- Bit 5 of the VID field indicates the static bit was set in the ALR entry for the packet’s Destination MAC address.
- Bit 6 of the VID field indicates priority enable was set in the ALR entry or the packet’s Destination MAC address.
- Bits 7,8, and 9 of the VID field are the priority field in the ALR entry for the packet’s Destination MAC address - these can be used as a tag to identify different packet types (PTP, RSTP, etc.) when the host CPU adds MAC address entries.

Note: Bits 4 through 9 of the VID field will be all zero for Destination MAC Addresses that have been learned (i.e., not added by the host) or are not found in the ALR table (i.e., not learned or added by the host).

Upon egress from the host CPU port, the special tag is added. If a regular VLAN tag already exists, it is not deleted. Instead it will follow the special tag.

6.4.11 Counters

A counter is maintained per port that contains the number of MAC address that were not learned or were overwritten by a different address due to MAC Address Table space limitations. These counters are accessible via the following registers:

- Switch Engine Port 0 Learn Discard Count Register (SWE_LRN_DISCRD_CNT_0)
- Switch Engine Port 1 Learn Discard Count Register (SWE_LRN_DISCRD_CNT_1)
- Switch Engine Port 2 Learn Discard Count Register (SWE_LRN_DISCRD_CNT_2)

A counter is maintained per port that contains the number of packets filtered at ingress. This count includes packets filtered due to broadcast throttling, but does not include packets dropped due to ingress rate limiting. These counters are accessible via the following registers:

- Switch Engine Port 0 Ingress Filtered Count Register (SWE_FILTERED_CNT_0)
- Switch Engine Port 1 Ingress Filtered Count Register (SWE_FILTERED_CNT_1)
- Switch Engine Port 2 Ingress Filtered Count Register (SWE_FILTERED_CNT_2)

6.5 Buffer Manager (BM)

The Buffer Manager (BM) provides control of the free buffer space, the multiple priority transmit queues, transmission scheduling, and packet dropping. VLAN tag insertion and removal is also performed by the Buffer Manager. The following sections detail the various features of the Buffer Manager.

6.5.1 Packet Buffer Allocation

The packet buffer consists of 32KB of RAM that is dynamically allocated in 128 byte blocks as packets are received. Up to 16 blocks may be used per packet, depending on the packet length. The blocks are linked together as the packet is received. If a packet is filtered, dropped, or contains a receive error, the buffers are reclaimed.

6.5.1.1 Buffer Limits and Flow Control Levels

The BM keeps track of the amount of buffers used per each ingress port. These counts are used to generate flow control (half-duplex backpressure or full-duplex pause frames) and to limit the amount of buffer space that can be used by any individual receiver (hard drop limit). The flow control and drop limit thresholds are dynamic and adapt based on the current buffer usage. Based on the number of active receiving ports, the drop level and flow control pause and resume thresholds adjust between fixed settings and two user programmable levels via the Buffer Manager Drop Level Register (BM_DROP_LVL), Buffer Manager Flow Control Pause Level Register (BM_FC_PAUSE_LVL), and Buffer Manager Flow Control Resume Level Register (BM_FC_RESUME_LVL) respectively.

The BM also keeps a count of the number of buffers that are queued for multiple ports (broadcast queue). This count is compared against the Buffer Manager Broadcast Buffer Level Register (BM_BCST_LVL), and if the configured drop level is reached or exceeded, subsequent packets are dropped.

6.5.2 Random Early Discard (RED)

Based on the ingress flow monitoring detailed in Section 6.4.6, "Ingress Flow Metering and Coloring," on page 83, packets are colored as Green, Yellow, or Red. Packets colored Red are always discarded if the Drop on Red bit in the Buffer Manager Configuration Register (BM_CFG) is set. If the Drop on Yellow bit in the Buffer Manager Configuration Register (BM_CFG) is set, packets colored Yellow are randomly discarded based on the moving average number of buffers used by the ingress port.

The probability of a discard is programmable into the Random Discard Weight table via the Buffer Manager Random Discard Table Command Register (BM_RNDM_DSCRD_TBL_CMD), Buffer Manager Random Discard Table Write Data Register (BM_RNDM_DSCRD_TBL_WDATA), and Buffer Manager Random Discard Table Read Data Register (BM_RNDM_DSCRD_TBL_RDATA). The Random Discard Weight table contains sixteen entries, each 10-bits wide. Each entry corresponds to a range of the average number of buffers used by the ingress port. Entry 0 is for 0 to 15 buffers, entry 1 is for 16 to 31 buffers, etc. The probability for each entry us set in 1/1024's. For example, a setting of 1 is 1-in-1024, or approximately 0.1%. A setting of all ones (1023) is 1023-in-1024, or approximately 99.9%.

Refer to Section 13.4.4.10, "Buffer Manager Random Discard Table Command Register (BM_RNDM_DSCRD_TBL_CMD)," on page 343 for additional details on writing and reading the Random Discard Weight table.

6.5.3 Transmit Queues

Once a packet has been completely received, it is queued for transmit. There are four queues per transmit port, one for each level of transmit priority. Each queue is virtual (if there are no packets for that port/priority, the queue is empty), and dynamic (a queue may be any length if there is enough memory space). When a packet is read from the memory and sent out to the corresponding port, the used buffers are released.

6.5.4 Transmit Priority Queue Servicing

When a transmit queue is non-empty, it is serviced and the packet is read from the buffer RAM and sent to the transmit MAC. If there are multiple queues that require servicing, one of two methods may be used: fixed priority ordering, or weighted round-robin ordering. If the Fixed Priority Queue Servicing bit in the Buffer Manager Configuration Register (BM_CFG) is set, a strict order, fixed priority is selected. Transmit queue 3 has the highest priority, followed by 2, 1, and 0. If the Fixed Priority Queue Servicing bit in the Buffer Manager Configuration Register (BM_CFG) is cleared, a weighted round-robin order is followed. Assuming all four queues are non-empty, the service is weighted with a 9:4:2:1 ratio (queue 3,2,1,0). The servicing is blended to avoid burstiness (e.g. queue 3, then queue 2, then queue 3, etc.).

6.5.5 Egress Rate Limiting (Leaky Bucket)

For egress rate limiting, the leaky bucket algorithm is used on each output priority queue. For each output port, the bandwidth that is used by each priority queue can be limited. If any egress queue receives packets faster than the specified egress rate, packets will be accumulated in the packet memory. After the memory is used, packet dropping or flow control will be triggered.

Note: Egress rate limiting occurs before the Transmit Priority Queue Servicing, such that a lower priority queue will be serviced if a higher priority queue is being rate limited.

The egress limiting is enabled per priority queue. After a packet is selected to be sent, its length is recorded. The switch then waits a programmable amount of time, scaled by the packet length, before servicing that queue once again. The amount of time per byte is programmed into the Buffer Manager Egress Rate registers (refer to Section 13.4.4.14 through Section 13.4.4.19 for detailed register definitions). The value programmed is in approximately 20 nS per byte increments. Typical values are listed in Table 6.5. When a port is transmitting at 10 Mbps, any setting above 39 has the effect of not limiting the rate.

Table 6.5 Typical Egress Rate Settings

EGRESS RATE SETTING	TIME PER BYTE	BANDWIDTH @ 64 BYTE PACKET	BANDWIDTH @ 512 BYTE PACKET	BANDWIDTH @ 1518 BYTE PACKET
0-3	80 nS	76 Mbps (Note 6.3)	96 Mbps (Note 6.3)	99 Mbps (Note 6.3)
4	100 nS	66 Mbps	78 Mbps	80 Mbps
5	120 nS	55 Mbps	65 Mbps	67 Mbps
6	140 nS	48 Mbps	56 Mbps	57 Mbps
7	160 nS	42 Mbps	49 Mbps	50 Mbps
9	200 nS	34 Mbps	39 Mbps	40 Mbps
12	260 nS	26 Mbps	30 Mbps	31 Mbps
19	400 nS	17 Mbps	20 Mbps	20 Mbps
39	800 nS	8.6 Mbps	10 Mbps	10 Mbps
78	1580 nS	4.4 Mbps	5 Mbps	5 Mbps
158	3180 nS	2.2 Mbps	2.5 Mbps	2.5 Mbps
396	7940 nS	870 Kbps	990 Kbps	1 Mbps
794	15900 nS	440 Kbps	490 Kbps	500 Kbps
1589	31800 nS	220 Kbps	250 Kbps	250 Kbps
3973	79480 nS	87 Kbps	98 Kbps	100 Kbps
7947	158960 nS	44 Kbps	49 Kbps	50 Kbps

Note 6.3 These are the unlimited max bandwidths when IFG and preamble are taken into account.

6.5.6 Adding, Removing, and Changing VLAN Tags

Based on the port configuration and the received packet formation, a VLAN tag can be added to, removed from, or modified in a packet. There are four received packet type cases: non-tagged, priority-tagged, normal-tagged, and CPU special-tagged. There are also four possible settings for an egress port: dumb, access, hybrid, and CPU. In addition, each VLAN table entry can specify the removal of the VLAN tag (the entry's un-tag bit).

The tagging/un-tagging rules are specified as follows:

- **Dumb Port** - This port type generally does not change the tag.
  When a received packet is non-tagged, priority-tagged, or normal-tagged, the packet passes untouched.
  When a packet is received special-tagged from a CPU port, the special tag is removed.
- **Access Port** - This port type generally does not support tagging.
  When a received packet in non-tagged, the packet passes untouched.
  When a received packet is priority-tagged or normal-tagged, the tag is removed.
  When a received packet is special-tagged from a CPU port, the special tag is removed.
- **CPU Port** - Packets transmitted from this port type generally contain a special tag. Special tags are described in detail in Section 6.4.10, "Host CPU Port Special Tagging," on page 88.
- **Hybrid Port** - Generally, this port type supports a mix of normal-tagged and non-tagged packets. It is the most complex, but most flexible port type.

For clarity, the following details the incoming un-tag instruction. As described in Section 6.4.4, "VLAN Support," on page 82, the un-tag instruction is the three un-tag bits from the applicable entry in the VLAN table. The entry in the VLAN table is either the VLAN from the received packet or the ingress port's default VID.

- When a received packet is non-tagged, a new VLAN tag is added if two conditions are met. First, the Insert Tag bit for the egress port in the Buffer Manager Egress Port Type Register (BM_EGRSS_PORT_TYPE) must be set. Second, the un-tag bit, for the egress port, from the un-tag instruction associated with the ingress port's default VID, must be cleared. The VLAN tag that is added will have a VID taken from either the ingress or egress port's default VID. The priority of the VLAN tag is either the priority calculated on ingress or the egress port's default. The choice of ingress or egress is determined by the egress port's VID/Priority Select bit in the Buffer Manager Egress Port Type Register (BM_EGRSS_PORT_TYPE).
- When a received packet is priority-tagged, either the tag is removed or it is modified.

  If the un-tag bit, for the egress port, from the un-tag instruction associated with the ingress port's default VID is set, then the tag is removed.

  Otherwise, the tag is modified. The VID of the new VLAN tag is changed to either the ingress or egress port's default VID. If the Change Priority bit in the Buffer Manager Egress Port Type Register (BM_EGRSS_PORT_TYPE) for the egress port is set, then the Priority field of the new VLAN tag is also changed. The priority of the VLAN tag is either the priority calculated on ingress or the egress port's default. The choice of ingress or egress is determined by the egress port's VID/Priority Select bit.
- When a received packet is normal-tagged, either the tag is removed, modified, or passed unchanged.

  If the un-tag bit, for the egress port, from the un-tag instruction associated with the VID in the received packet is set, then the tag is removed.

  Else, if the Change Tag bit in the Buffer Manager Egress Port Type Register (BM_EGRSS_PORT_TYPE) for the egress port is clear, the packet passes untouched.

  Else, if both the Change VLAN ID and the Change Priority bits in the Buffer Manager Egress Port Type Register (BM_EGRSS_PORT_TYPE) for the egress port are clear, the packet passes untouched.

  Otherwise, the tag is modified. If the Change VLAN ID bit for the egress port is set, the VID of the new VLAN tag is changed to either the ingress or egress port's default VID. If the Change Priority bit for the egress port is set, the Priority field of the new VLAN tag is changed to either the priority calculated on ingress or the egress port's default. The choice of ingress or egress is determined by the egress port's VID / Priority Select bit.
- When a packet is received special-tagged from a CPU port, the special tag is removed.

Hybrid tagging is summarized in Figure 6.9.

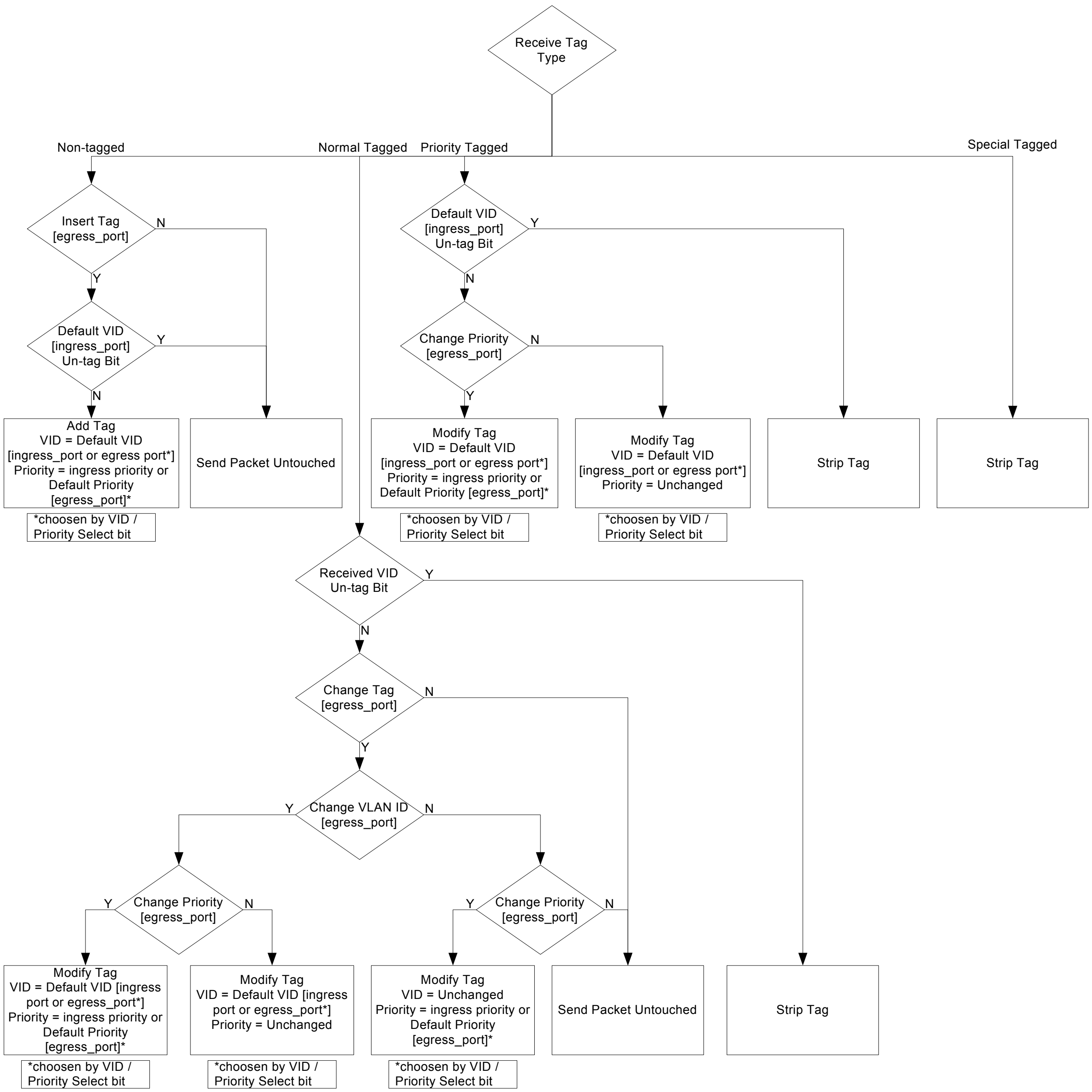


Figure 6.9 Hybrid Port Tagging and Un-tagging

The default VLAN ID and priority of each port may be configured via the following registers:

- Buffer Manager Port 0 Default VLAN ID and Priority Register (BM_VLAN_0)
- Buffer Manager Port 1 Default VLAN ID and Priority Register (BM_VLAN_1)
- Buffer Manager Port 2 Default VLAN ID and Priority Register (BM_VLAN_2)

6.5.7 Counters

A counter is maintained per port that contains the number of packets dropped due to buffer space limits and ingress rate limit discarding (Red and random Yellow dropping). These counters are accessible via the following registers:

- Buffer Manager Port 0 Drop Count Register (BM_DRP_CNT_SRC_0)
- Buffer Manager Port 1 Drop Count Register (BM_DRP_CNT_SRC_1)
- Buffer Manager Port 2 Drop Count Register (BM_DRP_CNT_SRC_2)

A counter is maintained per port that contains the number of packets dropped due solely to ingress rate limit discarding (Red and random Yellow dropping). This count value can be subtracted from the drop counter, as described above, to obtain the drop counts due solely to buffer space limits. The ingress rate drop counters are accessible via the following registers:

- Buffer Manager Port 0 Ingress Rate Drop Count Register (BM_RATE_DRP_CNT_SRC_0)
- Buffer Manager Port 1 Ingress Rate Drop Count Register (BM_RATE_DRP_CNT_SRC_1)
- Buffer Manager Port 2 Ingress Rate Drop Count Register (BM_RATE_DRP_CNT_SRC_2)

6.6 Switch Fabric Interrupts

The Switch Fabric is capable of generating multiple maskable interrupts from the Buffer Manager, Switch Engine, and MACs. These interrupts are detailed in Section 5.2.1, "Switch Fabric Interrupts," on page 64.

Chapter 7 Ethernet PHYs

7.1 Functional Overview

The device contains three PHYs: Port 1 PHY, Port 2 PHY and a Virtual PHY. The Port 1 & 2 PHYs are identical in functionality and each connect their corresponding Ethernet signal pins to the Switch Fabric MAC of their respective port. These PHYs interface with their respective MAC via an internal MII interface. The Virtual PHY provides the virtual functionality of a PHY and allows connection of an external MAC to Port 0 of the Switch Fabric as if it was connected to a single port PHY. The Port 1 PHY may optionally be bypassed for the connection of an external MAC or PHY via the Port 1 MII/RMII interface. All PHYs comply with the IEEE 802.3 Physical Layer for Twisted Pair Ethernet and can be configured for full/half duplex 100 Mbps (100BASE-TX) or 10Mbps (10BASE-T) Ethernet operation. All PHY registers follow the IEEE 802.3 (clause 22.2.4) specified MII management register set and can be configured indirectly via the external MII interface signals, or directly via the memory mapped Virtual PHY registers. In addition, the Port 1 PHY and Port 2 PHY can be configured via the PHY Management Interface (PMI). Refer to Section 13.3, "Ethernet PHY Control and Status Registers" for details on the Ethernet PHY registers.

The Ethernet PHYs are discussed in detail in the following sections:

- Section 7.2, "Port 1 & 2 PHYs," on page 97
- Section 7.3, "Virtual PHY," on page 110

7.1.1 PHY Addressing

Each individual PHY is assigned a unique default PHY address via the phy_addr_sel_strap configuration strap as shown in Table 7.1. In addition, the Port 1 PHY and Port 2 PHY addresses can be changed via the PHY Address (PHYADD) field in the Port x PHY Special Modes Register (PHY_SPECIAL_MODES_x). For proper operation, all PHY addresses must be unique. No check is performed to assure each PHY is set to a different address. Configuration strap values are latched upon the de-assertion of a chip-level reset as described in Section 4.2.4, "Configuration Straps," on page 52.

Table 7.1 Default PHY Serial MII Addressing

phy_addr_sel_strap	VIRTUAL PHY DEFAULT ADDRESS VALUE	PORT 1 PHY DEFAULT ADDRESS VALUE	PORT 2 PHY DEFAULT ADDRESS VALUE
0	0	1	2
1	1	2	3

7.2 Port 1 & 2 PHYs

The Port 1 and Port 2 PHYs are functionally identical. The Port 1 PHY is active when Port 1 is operating in Internal PHY mode. The Port 1 PHY may optionally be bypassed for the connection of an external MAC or PHY via the Port 1 MII/RMII interface. Each PHY can be divided into the following functional sections:

- 100BASE-TX Transmit and 100BASE-TX Receive
- 10BASE-T Transmit and 10BASE-T Receive
- PHY Auto-negotiation
- HP Auto-MDIX
- MII MAC Interface
- PHY Management Control

Note 7.1 Because the Port 1 PHY and Port 2 PHY are functionally identical, this section will describe them as the “Port x PHY”, or simply “PHY”. Wherever a lowercase “x” has been appended to a port or signal name, it can be replaced with “1” or “2” to indicate the Port 1 or Port 2 PHY respectively. All references to “PHY” in this section can be used interchangeably for both the Port 1 & 2 PHYs. This nomenclature excludes the Virtual PHY.

A block diagram of the Port x PHYs main components can be seen in Figure 7.1.

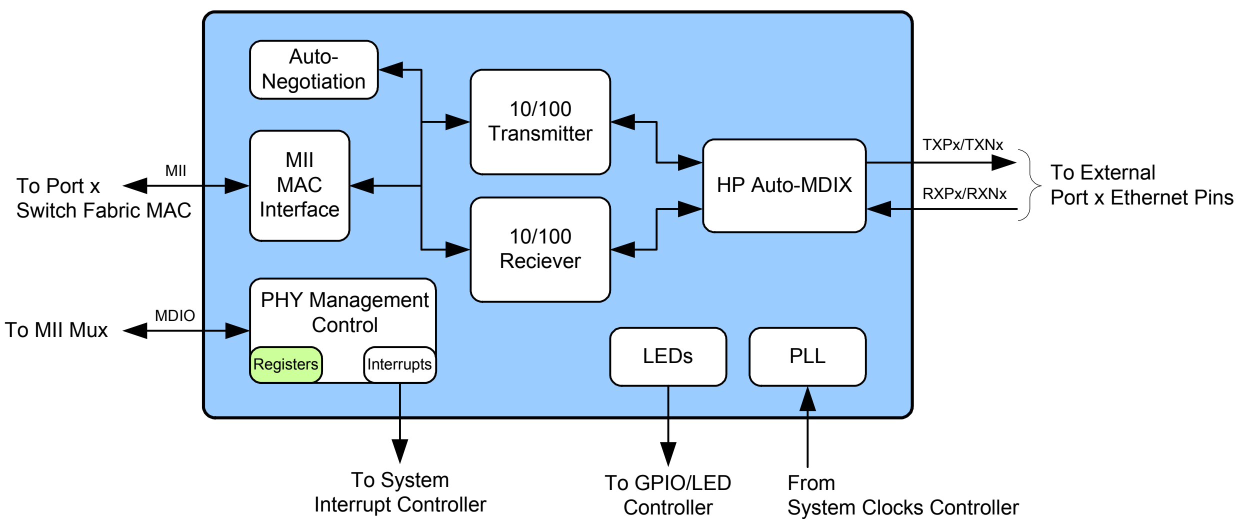


Figure 7.1 Port x PHY Block Diagram

7.2.1 100BASE-TX Transmit

The 100BASE-TX transmit data path is shown in Figure 7.2. Shaded blocks are those which are internal to the PHY. Each major block is explained in the following sections.

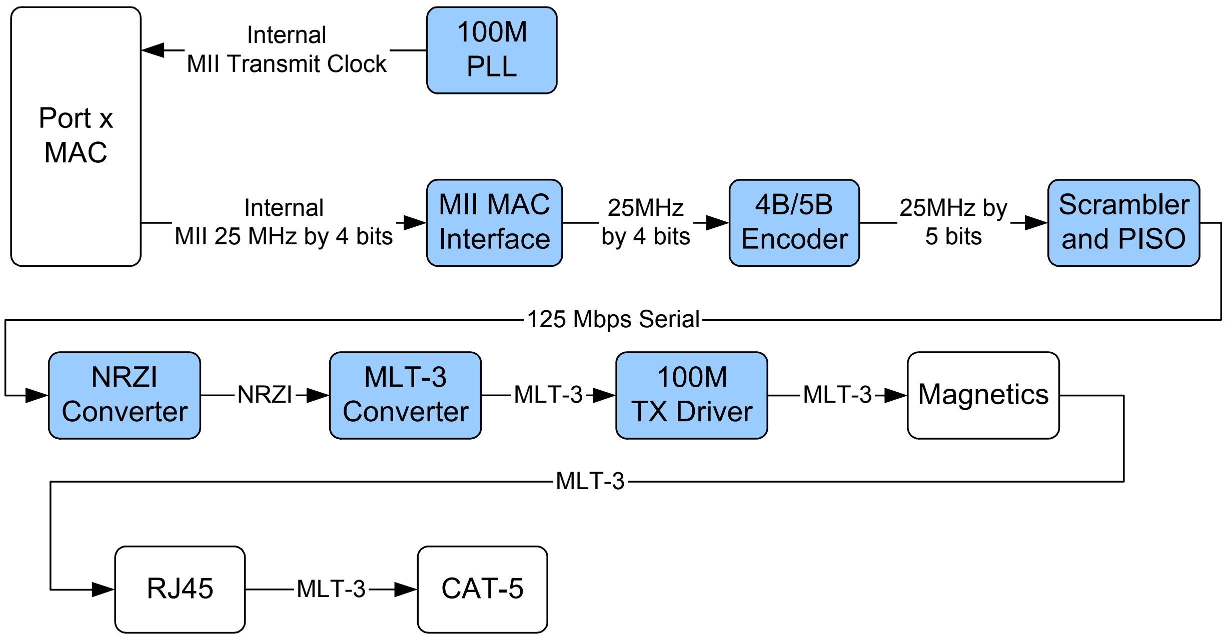


Figure 7.2 100BASE-TX Transmit Data Path

7.2.1.1 MII MAC Interface

For a transmission, the Switch Fabric MAC drives the transmit data to the PHYs MII MAC Interface. The MII MAC Interface is described in detail in Section 7.2.7, "MII MAC Interface".

Note: The PHY is connected to the Switch Fabric MAC via standard MII signals. Refer to the IEEE 802.3 specification for additional details.

7.2.1.2 4B/5B Encoder

The transmit data passes from the MII block to the 4B/5B Encoder. This block encodes the data from 4-bit nibbles to 5-bit symbols (known as “code-groups”) according to Table 7.2. Each 4-bit data-nibble is mapped to 16 of the 32 possible code-groups. The remaining 16 code-groups are either used for control information or are not valid.

The first 16 code-groups are referred to by the hexadecimal values of their corresponding data nibbles, 0 through F. The remaining code-groups are given letter designations with slashes on either side. For example, an IDLE code-group is /I/, a transmit error code-group is /H/, etc.

Table 7.2 4B/5B Code Table

CODE GROUP	SYM	RECEIVER INTERPRETATION			TRANSMITTER INTERPRETATION		
11110	0	0	0000	DATA	0	0000	DATA
01001	1	1	0001		1	0001	
10100	2	2	0010		2	0010	
10101	3	3	0011		3	0011	
01010	4	4	0100		4	0100	
01011	5	5	0101		5	0101	
01110	6	6	0110		6	0110	
01111	7	7	0111		7	0111	
10010	8	8	1000		8	1000	
10011	9	9	1001		9	1001	
10110	A	A	1010		A	1010	
10111	B	B	1011		B	1011	
11010	C	C	1100		C	1100	
11011	D	D	1101		D	1101	
11100	E	E	1110		E	1110	
11101	F	F	1111		F	1111	
11111	/I/	IDLE			Sent after /T/R/ until the MII Transmitter Enable signal (TXEN) is received		
11000	/J/	First nibble of SSD, translated to “0101” following IDLE, else MII Receive Error (RXER)			Sent for rising MII Transmitter Enable signal (TXEN)		
10001	/K/	Second nibble of SSD, translated to “0101” following /J/, else MII Receive Error (RXER)			Sent for rising MII Transmitter Enable signal (TXEN)		
01101	/T/	First nibble of ESD, causes de-assertion of CRS if followed by /R/, else assertion of MII Receive Error (RXER)			Sent for falling MII Transmitter Enable signal (TXEN)		
00111	/R/	Second nibble of ESD, causes de-assertion of CRS if following /T/, else assertion of MII Receive Error (RXER)			Sent for falling MII Transmitter Enable signal (TXEN)		
00100	/H/	Transmit Error Symbol			Sent for rising MII Transmit Error (TXER)		
00110	/V/	INVALID, MII Receive Error (RXER) if during MII Receive Data Valid (RXDV)			INVALID		
11001	/V/	INVALID, MII Receive Error (RXER) if during MII Receive Data Valid (RXDV)			INVALID		
00000	/V/	INVALID, MII Receive Error (RXER) if during MII Receive Data Valid (RXDV)			INVALID		

Table 7.2 4B/5B Code Table (continued)

CODE GROUP	SYM	RECEIVER INTERPRETATION	TRANSMITTER INTERPRETATION
00001	/V/	INVALID, MII Receive Error (RXER) if during MII Receive Data Valid (RXDV)	INVALID
00010	/V/	INVALID, MII Receive Error (RXER) if during MII Receive Data Valid (RXDV)	INVALID
00011	/V/	INVALID, MII Receive Error (RXER) if during MII Receive Data Valid (RXDV)	INVALID
00101	/V/	INVALID, MII Receive Error (RXER) if during MII Receive Data Valid (RXDV)	INVALID
01000	/V/	INVALID, MII Receive Error (RXER) if during MII Receive Data Valid (RXDV)	INVALID
01100	/V/	INVALID, MII Receive Error (RXER) if during MII Receive Data Valid (RXDV)	INVALID
10000	/V/	INVALID, MII Receive Error (RXER) if during MII Receive Data Valid (RXDV)	INVALID

7.2.1.3 Scrambler and PISO

Repeated data patterns (especially the IDLE code-group) can have power spectral densities with large narrow-band peaks. Scrambling the data helps eliminate these peaks and spread the signal power more uniformly over the entire channel bandwidth. This uniform spectral density is required by FCC regulations to prevent excessive EMI from being radiated by the physical wiring. The scrambler also performs the Parallel In Serial Out conversion (PISO) of the data.

The seed for the scrambler is generated from the PHY address, ensuring that each PHY will have its own scrambler sequence. For more information on PHY addressing, refer to Section 7.1.1, "PHY Addressing".

7.2.1.4 NRZI and MLT-3 Encoding

The scrambler block passes the 5-bit wide parallel data to the NRZI converter where it becomes a serial 125MHz NRZI data stream. The NRZI is then encoded to MLT-3. MLT-3 is a tri-level code where a change in the logic level represents a code bit “1” and the logic output remaining at the same level represents a code bit “0”.

7.2.1.5 100M Transmit Driver

The MLT-3 data is then passed to the analog transmitter, which drives the differential MLT-3 signal on output pins TXPx and TXNx (where “x” is replaced with “1” for the Port 1 PHY, or “2” for the Port 2 PHY), to the twisted pair media across a 1:1 ratio isolation transformer. The 10BASE-T and 100BASE-TX signals pass through the same transformer so that common “magnetics” can be used for both. The transmitter drives into the 100Ω impedance of the CAT-5 cable. Cable termination and impedance matching require external components.

7.2.1.6 100M Phase Lock Loop (PLL)

The 100M PLL locks onto the reference clock and generates the 125MHz clock used to drive the 125 MHz logic and the 100BASE-TX Transmitter.

7.2.2 100BASE-TX Receive

The 100BASE-TX receive data path is shown in Figure 7.3. Shaded blocks are those which are internal to the PHY. Each major block is explained in the following sections.

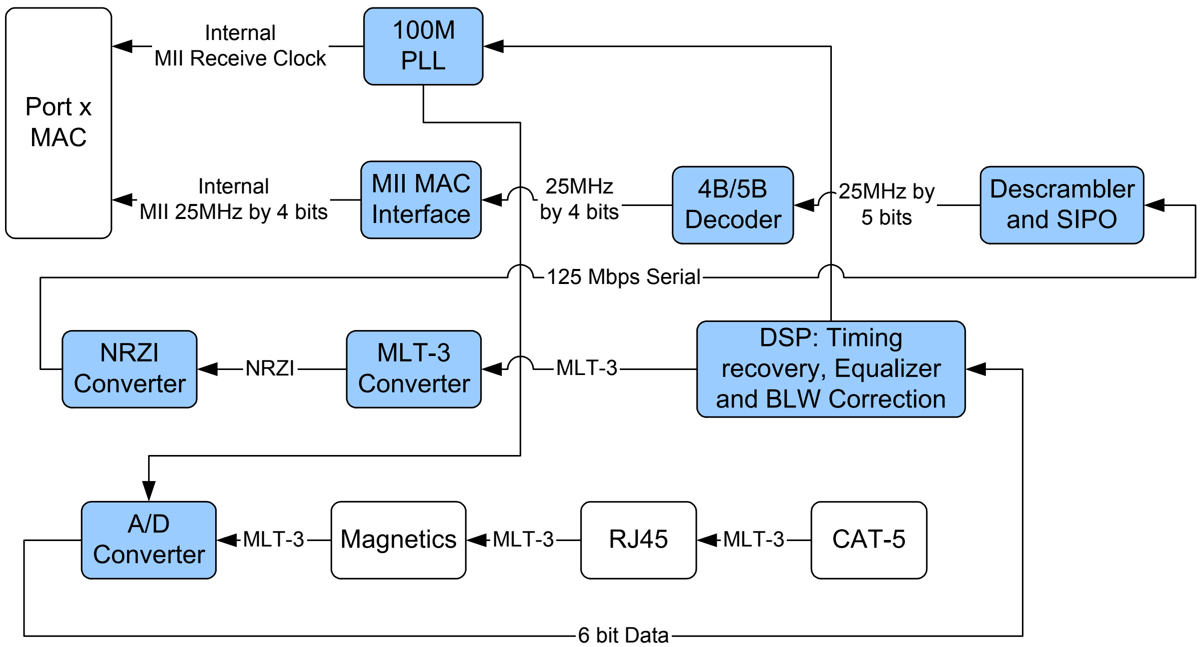


Figure 7.3 100BASE-TX Receive Data Path

7.2.2.1 A/D Converter

The MLT-3 data from the cable is fed into the PHY on inputs RXPx and RXNx (where “x” is replaced with “1” for the Port 1 PHY, or “2” for the Port 2 PHY) via a 1:1 ratio transformer. The ADC samples the incoming differential signal at a rate of 125M samples per second. Using a 64-level quantizer, 6 digital bits are generated to represent each sample. The DSP adjusts the gain of the A/D Converter (ADC) according to the observed signal levels such that the full dynamic range of the ADC can be used.

7.2.2.2 DSP: Equalizer, BLW Correction and Clock/Data Recovery

The 6 bits from the ADC are fed into the DSP block. The equalizer in the DSP section compensates for phase and amplitude distortion caused by the physical channel (magnetics, connectors, and CAT-5 cable). The equalizer can restore the signal for any good-quality CAT-5 cable between 1m and 150m.

If the DC content of the signal is such that the low-frequency components fall below the low frequency pole of the isolation transformer, then the droop characteristics of the transformer will become significant and Baseline Wander (BLW) on the received signal will result. To prevent corruption of the received data, the PHY corrects for BLW and can receive the ANSI X3.263-1995 FDDI TP-PMD defined “killer packet” with no bit errors.

The 100M PLL generates multiple phases of the 125MHz clock. A multiplexer, controlled by the timing unit of the DSP, selects the optimum phase for sampling the data. This is used as the received recovered clock. This clock is used to extract the serial data from the received signal.

7.2.2.3 NRZI and MLT-3 Decoding

The DSP generates the MLT-3 recovered levels that are fed to the MLT-3 converter. The MLT-3 is then converted to an NRZI data stream.

7.2.2.4 Descrambler and SIPO

The descrambler performs an inverse function to the scrambler in the transmitter and also performs the Serial In Parallel Out (SIPO) conversion of the data.

During reception of IDLE (/I/) symbols. the descrambler synchronizes its descrambler key to the incoming stream. Once synchronization is achieved, the descrambler locks on this key and is able to descramble incoming data.

Special logic in the descrambler ensures synchronization with the remote PHY by searching for IDLE symbols within a window of 4000 bytes (40us). This window ensures that a maximum packet size of 1514 bytes, allowed by the IEEE 802.3 standard, can be received with no interference. If no IDLE-symbols are detected within this time-period, receive operation is aborted and the descrambler re-starts the synchronization process.

The de-scrambled signal is then aligned into 5-bit code-groups by recognizing the /J/K/ Start-of-Stream Delimiter (SSD) pair at the start of a packet. Once the code-word alignment is determined, it is stored and utilized until the next start of frame.

7.2.2.5 5B/4B Decoding

The 5-bit code-groups are translated into 4-bit data nibbles according to the 4B/5B table shown in Table 7.2. The translated data is presented on the internal MII RXD[3:0] signal lines to the Switch Fabric MAC. The SSD, /J/K/, is translated to “0101 0101” as the first 2 nibbles of the MAC preamble. Reception of the SSD causes the PHY to assert the RXDV signal, indicating that valid data is available on the RXD bus. Successive valid code-groups are translated to data nibbles. Reception of either the End of Stream Delimiter (ESD) consisting of the /T/R/ symbols, or at least two /I/ symbols causes the PHY to de-assert carrier sense and RXDV. These symbols are not translated into data.

7.2.2.6 Receiver Errors

During a frame, unexpected code-groups are considered receive errors. Expected code groups are the DATA set (0 through F), and the /T/R/ (ESD) symbol pair. When a receive error occurs, the internal MII’s RXER signal is asserted and arbitrary data is driven onto the internal receive data bus (RXD) to the Switch Fabric MAC. Should an error be detected during the time that the /J/K/ delimiter is being decoded (bad SSD error), RXER is asserted and the value 1110b is driven onto the internal receive data bus (RXD) to the Switch Fabric MAC. Note that the internal MII’s data valid signal (RXDV) is not yet asserted when the bad SSD occurs.

7.2.2.7 MII MAC Interface

For reception, the 4-bit data nibbles are sent to the MII MAC Interface block where they are sent via MII to the Switch Fabric MAC. The MII MAC Interface is described in detail in Section 7.2.7, "MII MAC Interface".

Note: The PHY is connected to the Switch Fabric MAC via standard MII signals. Refer to the IEEE 802.3 specification for additional details.

7.2.3 10BASE-T Transmit

Data to be transmitted comes from the Switch Fabric MAC. The 10BASE-T transmitter receives 4-bit nibbles from the internal MII at a rate of 2.5MHz and converts them to a 10Mbps serial data stream. The data stream is then Manchester-encoded and sent to the analog transmitter, which drives a signal onto the twisted pair via the external magnetics.

10BASE-T transmissions use the following blocks:

- MII MAC Interface (digital)
- 10M TX Driver (digital/analog)
- 10M PLL (analog)

7.2.3.1 MII MAC Interface

For a transmission, the Switch Fabric MAC drives the transmit data to the PHYs MII MAC Interface. The MII MAC Interface is described in detail in Section 7.2.7, "MII MAC Interface".

Note: The PHY is connected to the Switch Fabric MAC via standard MII signals. Refer to the IEEE 802.3 specification for additional details.

7.2.3.2 10M TX Driver and PLL

The 4-bit wide data is sent to the 10M TX Driver block. The nibbles are converted to a 10Mbps serial NRZI data stream. The 10M PLL locks onto the external clock or internal oscillator and produces a 20MHz clock. This is used to Manchester encode the NRZ data stream. When no data is being transmitted (TXEN is low), the 10M TX Driver block outputs Normal Link Pulses (NLPs) to maintain communications with the remote link partner. The manchester encoded data is sent to the analog transmitter where it is shaped and filtered before being driven out as a differential signal across the TXPx and TXNx outputs (where “x” is replaced with “1” for the Port 1 PHY, or “2” for the Port 2 PHY).

7.2.4 10BASE-T Receive

The 10BASE-T receiver gets the Manchester-encoded analog signal from the cable via the magnetics. It recovers the receive clock from the signal and uses this clock to recover the NRZI data stream. This 10M serial data is converted to 4-bit data nibbles which are passed to the controller across the internal MII at a rate of 2.5MHz.

10BASE-T reception uses the following blocks:

- Filter and SQUELCH (analog)
- 10M RX (digital/analog)
- MII MAC Interface (digital)
- 10M PLL (analog)

7.2.4.1 Filter and Squelch

The Manchester signal from the cable is fed into the PHY on inputs RXPx and RXNx (where “x” is replaced with “1” for Port 1, or “2” for Port 2) via 1:1 ratio magnetics. It is first filtered to reduce any out-of-band noise. It then passes through a SQUELCH circuit. The SQUELCH is a set of amplitude and timing comparators that normally reject differential voltage levels below 300mV and detect and recognize differential voltages above 585mV.

7.2.4.2 10M RX and PLL

The output of the SQUELCH goes to the 10M RX block where it is validated as Manchester encoded data. The polarity of the signal is also checked. If the polarity is reversed (local RXP is connected to RXN of the remote partner and vice versa), then this is identified and corrected. The reversed condition is indicated by the 10Base-T Polarity State (XPOL) in the Port x PHY Special Control/Status Indication Register (PHY_SPECIAL_CONTROL_STAT_IND_x). The 10M PLL locks onto the received Manchester signal and generates the received 20MHz clock from it. Using this clock, the Manchester encoded data is extracted and converted to a 10MHz NRZI data stream. It is then converted from serial to 4-bit wide parallel data.

The RX10M block also detects valid 10BASE-T IDLE signals - Normal Link Pulses (NLPs) - to maintain the link.

7.2.4.3 MII MAC Interface

For reception, the 4-bit data nibbles are sent to the MII MAC Interface block where they are sent via MII to the Switch Fabric MAC. The MII MAC Interface is described in detail in Section 7.2.7, "MII MAC Interface".

Note: The PHY is connected to the Switch Fabric MAC via standard MII signals. Refer to the IEEE 802.3 specification for additional details.

7.2.4.4 Jabber Detection

Jabber is a condition in which a station transmits for a period of time longer than the maximum permissible packet length, usually due to a fault condition, that results in holding the TXEN input for an extended period of time. Special logic is used to detect the jabber state and abort the transmission to the line, within 45ms. Once TXEN is deasserted, the logic resets the jabber condition.

7.2.5 PHY Auto-negotiation

The purpose of the auto-negotiation function is to automatically configure the PHY to the optimum link parameters based on the capabilities of its link partner. Auto-negotiation is a mechanism for exchanging configuration information between two link-partners and automatically selecting the highest performance mode of operation supported by both sides. Auto-negotiation is fully defined in clause 28 of the IEEE 802.3 specification and is enabled by setting the Auto-Negotiation (PHY_AN) bit of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x).

The advertised capabilities of the PHY are stored in the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x). The PHY contains the ability to advertise 100BASE-TX and 10BASE-T in both full or half-duplex modes. Besides the connection speed, the PHY can advertise remote fault indication and symmetric or asymmetric pause flow control as defined in the IEEE 802.3 specification. “Next Page” capability is not supported. Many of the default advertised capabilities of the PHY are determined via configuration straps as shown in Section 13.3.2.5, "Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x)," on page 214. Refer to Section 4.2.4, "Configuration Straps," on page 52 for additional details on the configuration straps.

Once auto-negotiation has completed, information about the resolved link and the results of the negotiation process are reflected in the speed indication bits in the Port x PHY Special Control/Status Register (PHY_SPECIAL_CONTROL_STATUS_x), as well as the Port x PHY Auto-Negotiation Link Partner Base Page Ability Register (PHY_AN_LP_BASE_ABILITY_x).

The auto-negotiation protocol is a purely physical layer activity and proceeds independently of the MAC controller.

The following blocks are activated during an Auto-negotiation session:

- Auto-negotiation (digital)
- 100M ADC (analog)
- 100M PLL (analog)
- 100M equalizer/BLW/clock recovery (DSP)
- 10M SQUELCH (analog)

- 10M PLL (analog)
- 10M TX Driver (analog)

Auto-negotiation is started by the occurrence of any of the following events:

- Power-On Reset (POR)
- Hardware reset (nRST)
- PHY Software reset (via Reset Control Register (RESET_CTL), or the Reset (PHY_RST) bit of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x))
- PHY Power-down reset (Section 7.2.9, "PHY Power-Down Modes," on page 109)
- PHY Link status down (the Link Status bit of the Port x PHY Basic Status Register (PHY_BASIC_STATUS_x) is cleared)
- Setting the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x), Restart Auto-Negotiation (PHY_RST_AN) bit high
- Digital Reset (via the Digital Reset (DIGITAL_RST) bit of the Reset Control Register (RESET_CTL))
- Issuing an EEPROM Loader RELOAD command (Section 8.4, "EEPROM Loader," on page 121)

Note: Refer to Section 4.2, "Resets," on page 48 for information on these and other system resets.

On detection of one of these events, the PHY begins auto-negotiation by transmitting bursts of Fast Link Pulses (FLP). These are bursts of link pulses from the 10M TX Driver. They are shaped as Normal Link Pulses and can pass uncorrupted down CAT-3 or CAT-5 cable. A Fast Link Pulse Burst consists of up to 33 pulses. The 17 odd-numbered pulses, which are always present, frame the FLP burst. The 16 even-numbered pulses, which may be present or absent, contain the data word being transmitted. Presence of a data pulse represents a “1”, while absence represents a “0”.

The data transmitted by an FLP burst is known as a “Link Code Word.” These are defined fully in IEEE 802.3 clause 28. In summary, the PHY advertises 802.3 compliance in its selector field (the first 5 bits of the Link Code Word). It advertises its technology ability according to the bits set in the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x).

There are 4 possible matches of the technology abilities. In the order of priority these are:

- 100M Full Duplex (highest priority)
- 100M Half Duplex
- 10M Full Duplex
- 10M Half Duplex (lowest priority)

If the full capabilities of the PHY are advertised (100M, full-duplex), and if the link partner is capable of 10M and 100M, then auto-negotiation selects 100M as the highest performance mode. If the link partner is capable of half and full-duplex modes, then auto-negotiation selects full-duplex as the highest performance mode.

Once a speed and duplex match has been determined, the link code words are repeated with the acknowledge bit set. Any difference in the main content of the link code words at this time will cause auto-negotiation to re-start. Auto-negotiation will also re-start if all of the required FLP bursts are not received.

Writing the 10BASE-T Half Duplex, 10BASE-T Full Duplex, 100BASE-X Half Duplex, and 100BASE-X Full Duplex bits of the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) allows software control of the capabilities advertised by the PHY. Writing the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) does not automatically re-start auto-negotiation. The Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x), Restart Auto-Negotiation (PHY_RST_AN) bit must be set before the new abilities will be advertised. Auto-negotiation can also be disabled via software by clearing the Auto-Negotiation (PHY_AN) bit of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x).

7.2.5.1 PHY Pause Flow Control

The Port 1 & 2 PHYs are capable of generating and receiving pause flow control frames per the IEEE 802.3 specification. The PHYs advertised pause flow control abilities are set via the Symmetric Pause and Asymmetric Pause bits of the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x). This allows the PHY to advertise its flow control abilities and auto-negotiate the flow control settings with its link partner. The default values of these bits are determined via configuration straps as defined in Section 13.3.2.5, "Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x)," on page 214.

The pause flow control settings may also be manually set via the manual flow control registers Port 1 Manual Flow Control Register (MANUAL_FC_1) and Port 2 Manual Flow Control Register (MANUAL_FC_2). These registers allow the Switch Fabric ports flow control settings to be manually set when auto-negotiation is disabled or the respective manual flow control select bit is set (Port 1 Full-Duplex Manual Flow Control Select (MANUAL_FC_1) for Port 1, Port 2 Full-Duplex Manual Flow Control Select (MANUAL_FC_2) for Port 2). The currently enabled duplex and flow control settings can also be monitored via these registers. The flow control values in the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) are not affected by the values of the manual flow control register. Refer to Section 6.2.3, "Flow Control Enable Logic," on page 70 for additional information.

7.2.5.2 Parallel Detection

If LAN9303M/LAN9303Mi is connected to a device lacking the ability to auto-negotiate (i.e. no FLPs are detected), it is able to determine the speed of the link based on either 100M MLT-3 symbols or 10M Normal Link Pulses. In this case the link is presumed to be half-duplex per the IEEE 802.3 standard. This ability is known as “Parallel Detection.” This feature ensures interoperability with legacy link partners. If a link is formed via parallel detection, then the Link Partner Auto-Negotiation Able bit in the Port x PHY Auto-Negotiation Expansion Register (PHY_AN_EXP_x) is cleared to indicate that the link partner is not capable of auto-negotiation. If a fault occurs during parallel detection, the Parallel Detection Fault bit of the Port x PHY Auto-Negotiation Expansion Register (PHY_AN_EXP_x) is set.

The Port x PHY Auto-Negotiation Link Partner Base Page Ability Register (PHY_AN_LP_BASE_ABILITY_x) is used to store the Link Partner Ability information, which is coded in the received FLPs. If the link partner is not auto-negotiation capable, then this register is updated after completion of parallel detection to reflect the speed capability of the link partner.

7.2.5.3 Restarting Auto-Negotiation

Auto-negotiation can be re-started at any time by setting the Restart Auto-Negotiation (PHY_RST_AN) bit of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x). Auto-negotiation will also re-start if the link is broken at any time. A broken link is caused by signal loss. This may occur because of a cable break, or because of an interruption in the signal transmitted by the Link Partner. Auto-negotiation resumes in an attempt to determine the new link configuration.

If the management entity re-starts Auto-negotiation by writing to the Restart Auto-Negotiation (PHY_RST_AN) bit of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x), the device will respond by stopping all transmission/receiving operations. Once the internal break link time of approximately 1200ms has passed in the Auto-negotiation state-machine, the auto-negotiation will re-start. In this case, the link partner will have also dropped the link due to lack of a received signal, so it too will resume auto-negotiation.

7.2.5.4 Disabling Auto-Negotiation

Auto-negotiation can be disabled by clearing the Auto-Negotiation (PHY_AN) bit of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x). The PHY will then force its speed of operation to reflect the speed (Speed Select LSB (PHY_SPEED_SEL_LSB)) and duplex (Duplex Mode (PHY_DUPLEX)) of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x). The speed and duplex bits in the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) should be ignored when auto-negotiation is enabled.

7.2.5.5 Half Vs. Full-Duplex

Half-duplex operation relies on the CSMA/CD (Carrier Sense Multiple Access / Collision Detect) protocol to handle network traffic and collisions. In this mode, the carrier sense signal, CRS, responds to both transmit and receive activity. If data is received while the PHY is transmitting, a collision results.

In full-duplex mode, the PHY is able to transmit and receive data simultaneously. In this mode, CRS responds only to receive activity. The CSMA/CD protocol does not apply and collision detection is disabled.

7.2.6 HP Auto-MDIX

HP Auto-MDIX facilitates the use of CAT-3 (10 BASE-T) or CAT-5 (100 BASE-T) media UTP interconnect cable without consideration of interface wiring scheme. If a user plugs in either a direct connect LAN cable or a cross-over patch cable, as shown in Figure 7.4 (See Note 7.1 on page 97), the PHY is capable of configuring the TXPx/TXNx and RXPx/RXNx twisted pair pins for correct transceiver operation.

The internal logic of the device detects the TX and RX pins of the connecting device. Since the RX and TX line pairs are interchangeable, special PCB design considerations are needed to accommodate the symmetrical magnetics and termination of an Auto-MDIX design.

The Auto-MDIX function can be disabled through the Auto-MDIX Control (AMDIXCTRL) bit of the Port x PHY Special Control/Status Indication Register (PHY_SPECIAL_CONTROL_STAT_IND_x). When Auto-MDIX Control (AMDIXCTRL) is cleared, Auto-MDIX can be selected via the Auto-MDIX Enable configuration straps (auto_mdix_strap_1 and auto_mdix_strap_2 for Port 1 and Port 2, respectively). The MDIX can also be configured manually via the Manual MDIX strap (manual_mdix_strap_1 and manual_mdix_strap_2 for Port 1 and Port 2, respectively) if both the Auto-MDIX Control (AMDIXCTRL) bit and the Auto-MDIX Enable configuration strap are low. Refer to Section 3.2, "Pin Descriptions," on page 24 for more information on the configuration straps.

When the Auto-MDIX Control (AMDIXCTRL) bit of the Port x PHY Special Control/Status Indication Register (PHY_SPECIAL_CONTROL_STAT_IND_x) is set to 1, the Auto-MDIX capability is determined by the Auto-MDIX Enable (AMDIXEN) and Auto-MDIX State (AMDIXSTATE) bits of the Port x PHY Special Control/Status Indication Register (PHY_SPECIAL_CONTROL_STAT_IND_x).

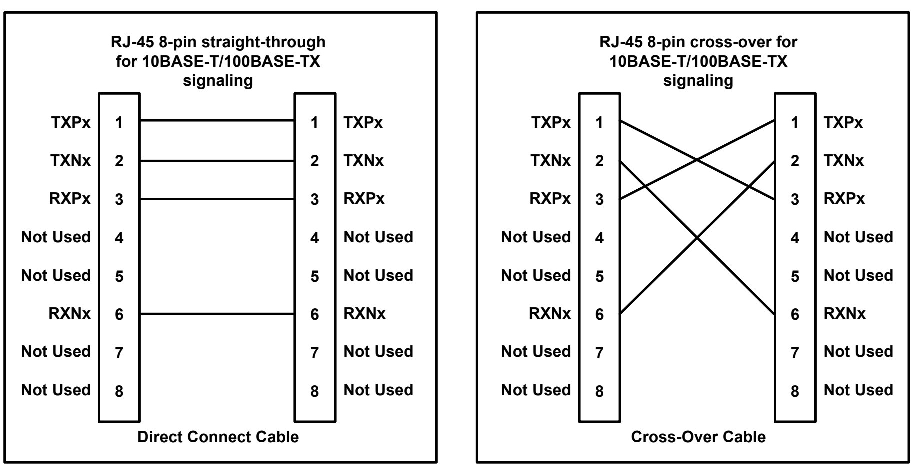


Figure 7.4 Direct Cable Connection vs. Cross-Over Cable Connection

7.2.7 MII MAC Interface

The MII MAC Interface is responsible for the transmission and reception of the Ethernet data to and from the Switch Fabric MAC. The PHY is connected internally to the Switch Fabric MAC via standard MII signals per IEEE 802.3.

For a transmission, the Switch Fabric MAC drives the transmit data onto the internal MII TXD bus and asserts TXEN to indicate valid data. The data is in the form of 4-bit wide data at a rate of 25MHz for 100BASE-TX, or 2.5MHz for 10BASE-T.

For reception, the 4-bit data nibbles are sent to the MII MAC Interface block. These data nibbles are clocked to the controller at a rate of 25MHz for 100BASE-TX, or 2.5MHz for 10BASE-T. RXCLK is the output clock for the internal MII bus. It is recovered from the received data to clock the RXD bus. If there is no received signal, it is derived from the system reference clock.

7.2.8 PHY Management Control

The PHY Management Control block is responsible for the management functions of the PHY, including register access and interrupt generation. A Serial Management Interface (SMI) is used to support registers 0 through 6 as required by the IEEE 802.3 (Clause 22), as well as the vendor specific registers allowed by the specification. The SMI interface consists of the MII Management Data (MDIO) signal and the MII Management Clock (MDC) signal. These signals interface to the MDIO and MDC pins of LAN9303M/LAN9303Mi (or the PMI block in I^2C mode of operation) and allow access to all PHY registers. Refer to Section 13.3.2, "Port 1 & 2 PHY Registers," on page 206 for a list of all supported registers and register descriptions. Non-supported registers will be read as FFFFh.

7.2.8.1 PHY Interrupts

The PHY contains the ability to generate various interrupt events as described in Table 7.3. Reading the Port x PHY Interrupt Source Flags Register (PHY_INTERRUPT_SOURCE_x) shows the source of the interrupt, and clears the interrupt signal. The Port x PHY Interrupt Mask Register (PHY_INTERRUPT_MASK_x) enables or disables each PHY interrupt. The PHY Management Control block aggregates the enabled interrupts status into an internal signal which is sent to the System Interrupt Controller and is reflected via the Interrupt Status Register (INT_STS) bits Port 1 PHY Interrupt Event (PHY_INT1) and Port 2 PHY Interrupt Event (PHY_INT2) for the Port 1 and Port 2 PHYs, respectively. For more information on interrupts, refer to Chapter 5, "System Interrupts," on page 62.

Table 7.3 PHY Interrupt Sources

INTERRUPT SOURCE	PHY_INTERRUPT_MASK_x & PHY_INTERRUPT_SOURCE_x REGISTER BIT #
ENERGYON Activated	7
Auto-Negotiation Complete	6
Remote Fault Detected	5
Link Down (Link Status Negated)	4
Auto-Negotiation LP Acknowledge	3
Parallel Detection Fault	2
Auto-Negotiation Page Received	1

7.2.9 PHY Power-Down Modes

There are two power-down modes for the PHY:

- PHY General Power-Down
- PHY Energy Detect Power-Down

Note: For more information on the various power management features of the device, refer to Section 4.3, "Power Management," on page 61.

Note: The power-down modes of each PHY (Port 1 PHY and Port 2 PHY) are controlled independently.

Note: The PHY power-down modes do not reload or reset the PHY registers.

7.2.9.1 PHY General Power-Down

This power-down mode is controlled by the Power Down (PHY_PWR_DWN) bit of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x). In this mode the entire PHY, except the PHY management control interface, is powered down. The PHY will remain in this power-down state as long as the bit is set. When the bit is cleared, the PHY powers up and is automatically reset.

Note: When the Port 1 external MII/RMII interface is selected, the Port 1 PHY is placed into the general power-down mode.

7.2.9.2 PHY Energy Detect Power-Down

This power-down mode is enabled by setting the Energy Detect Power-Down (EDPWRDOWN) bit of the Port x PHY Mode Control/Status Register (PHY_MODE_CONTROL_STATUS_x). When in this mode, if no energy is detected on the line, the entire PHY is powered down except for the PHY management control interface, the SQUELCH circuit, and the ENERGYON logic. The ENERGYON logic is used to detect the presence of valid energy from 100BASE-TX, 10BASE-T, or auto-negotiation signals and is responsible for driving the ENERGYON signal, whose state is reflected in the Energy On (ENERGYON) bit of the Port x PHY Mode Control/Status Register (PHY_MODE_CONTROL_STATUS_x).

In this mode, when the ENERGYON signal is cleared, the PHY is powered down and no data is transmitted from the PHY. When energy is received, via link pulses or packets, the ENERGYON signal goes high, and the PHY powers up. The PHY automatically resets itself into its previous state prior to power-down, and asserts the INT7 interrupt bit of the Port x PHY Interrupt Source Flags Register (PHY_INTERRUPT_SOURCE_x). The first and possibly second packet to activate ENERGYON may be lost.

When the Energy Detect Power-Down (EDPWRDOWN) bit of the Port x PHY Mode Control/Status Register (PHY_MODE_CONTROL_STATUS_x) is low, energy detect power-down is disabled.

7.2.10 PHY Resets

In addition to the chip-level hardware reset (nRST) and Power-On Reset (POR), the PHY supports three block specific resets. These are discussed in the following sections. For detailed information on all resets and the reset sequence refer to Section 4.2, "Resets," on page 48.

Note: The Digital Reset (DIGITAL_RST) bit in the Reset Control Register (RESET_CTL) does not reset the PHYs. Only a hardware reset (nRST) or an EEPROM RELOAD command will automatically reload the configuration strap values into the PHY registers. For all other PHY resets, these values will need to be manually configured via software.

7.2.10.1 PHY Software Reset via RESET_CTL

The PHY can be reset via the Reset Control Register (RESET_CTL). The Port 1 PHY is reset by setting the Port 1 PHY Reset (PHY1_RST) bit, and the Port 2 PHY is reset by setting the Port 2 PHY Reset (PHY2_RST) bit. These bits are self clearing after approximately 102uS. This reset does not reload the configuration strap values into the PHY registers.

7.2.10.2 PHY Software Reset via PHY_BASIC_CTRL_x

The PHY can also be reset by setting the Reset (PHY_RST) bit of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x). This bit is self clearing and will return to 0 after the reset is complete. This reset does not reload the configuration strap values into the PHY registers.

7.2.10.3 PHY Power-Down Reset

After the PHY has returned from a power-down state, a reset of the PHY is automatically generated. The PHY power-down modes do not reload or reset the PHY registers. Refer to Section 7.2.9, "PHY Power-Down Modes," on page 109 for additional information.

7.2.11 LEDs

Each PHY provides LED indication signals to the GPIO/LED block of the device. This allows external LEDs to be used to indicate various PHY related functions such as TX/RX activity, speed, duplex, or link status. Refer to Chapter 12, "GPIO/LED Controller," on page 144 for additional information on the configuration of these signals.

7.2.12 Required Ethernet Magnetics

The magnetics selected for use with the device should be an Auto-MDIX style magnetic, which is widely available from several vendors. Please review the SMSC Application note 8.13 “Suggested Magnetics” for the latest qualified and suggested magnetics. A list of vendors and part numbers are provided within the application note.

7.3 Virtual PHY

The Virtual PHY provides a basic MII management interface (MDIO) to the MII management pins per the IEEE 802.3 (clause 22) so that a MAC with an unmodified driver can be supported as if the MAC was attached to a single port PHY. This functionality is designed to allow easy and quick integration of the device into designs with minimal driver modifications. The Virtual PHY provides a full bank of registers which comply with the IEEE 802.3 specification. This enables the Virtual PHY to provide various status and control bits similar to those provided by a real PHY. These include the output of speed selection, duplex, loopback, isolate, collision test, and auto-negotiation status. For a list of all Virtual PHY registers and related bit descriptions, refer to Section 13.3.1, "Virtual PHY Registers," on page 206.

7.3.1 Virtual PHY Auto-Negotiation

The purpose of the auto-negotiation function is to automatically configure the Virtual PHY to the optimum link parameters based on the capabilities of its link partner. Because the Virtual PHY has no actual link partner, the auto-negotiation process is emulated with deterministic results.

Auto-negotiation is enabled by setting the Auto-Negotiation (VPHY_AN) bit of the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) and is restarted by the occurrence of any of the following events:

- Power-On Reset (POR)
- Hardware reset (nRST)

- PHY Software reset (via the Virtual PHY Reset (VPHY_RST) bit of the Reset Control Register (RESET_CTL), or the Reset (VPHY_RST) bit of the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL))
- Setting the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL), Restart Auto-Negotiation (VPHY_RST_AN) bit high
- Digital Reset (via the Digital Reset (DIGITAL_RST) bit of the Reset Control Register (RESET_CTL))
- Issuing an EEPROM Loader RELOAD command (Section 8.4, "EEPROM Loader," on page 121)

The emulated auto-negotiation process is much simpler than the real process and can be categorized into three steps:

1. The Auto-Negotiation Complete bit is set in the Virtual PHY Basic Status Register (VPHY_BASIC_STATUS).
2. The Page Received bit is set in the Virtual PHY Auto-Negotiation Expansion Register (VPHY_AN_EXP).
3. The auto-negotiation result (speed, duplex, and pause) is determined and registered.

The auto-negotiation result (speed and duplex) is determined using the Highest Common Denominator (HCD) of the Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV) and Virtual PHY Auto-Negotiation Link Partner Base Page Ability Register (VPHY_AN_LP_BASE_ABILITY) as specified in the IEEE 802.3 standard. The technology ability bits of these registers are ANDed, and if there are multiple bits in common, the priority is determined as follows:

- 100Mbps Full Duplex (highest priority)
- 100Mbps Half Duplex
- 10Mbps Full Duplex
- 10Mbps Half Duplex (lowest priority)

For example, if the full capabilities of the Virtual PHY are advertised (100Mbps, Full Duplex), and if the link partner is capable of 10Mbps and 100Mbps, then auto-negotiation selects 100Mbps as the highest performance mode. If the link partner is capable of half and full-duplex modes, then auto-negotiation selects full-duplex as the highest performance operation. In the event that there are no bits in common, an emulated Parallel Detection is used.

The Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV) defaults to having all four ability bits set. These values can be reconfigured via software. Once the auto-negotiation is complete, any change to the Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV) will not take affect until the auto-negotiation process is re-run. The emulated link partner default advertised abilities in the Virtual PHY Auto-Negotiation Link Partner Base Page Ability Register (VPHY_AN_LP_BASE_ABILITY) are dependant on the P0_DUPLEX pin and the duplex_pol_strap_0 and speed_strap_0 configuration straps as described in Table 13.7 of Section 13.2.6.6, "Virtual PHY Auto-Negotiation Link Partner Base Page Ability Register (VPHY_AN_LP_BASE_ABILITY)," on page 190. Neither the Virtual PHY or the emulated link partner support next page capability, remote faults, or 100BASE-T4.

Note: The P0_DUPLEX, duplex_pol_strap_0, and speed_strap_0 inputs are considered to be static. Auto-negotiation is not automatically re-evaluated if these inputs are changed.

If there is at least one common selection between the emulated link partner and the Virtual PHY advertised abilities, then the auto-negotiation succeeds, the Link Partner Auto-Negotiation Able bit of the Virtual PHY Auto-Negotiation Expansion Register (VPHY_AN_EXP) is set, and the technology ability bits in the Virtual PHY Auto-Negotiation Link Partner Base Page Ability Register (VPHY_AN_LP_BASE_ABILITY) are set to indicate the emulated link partners abilities.

Note: For the Virtual PHY, the auto-negotiation register bits (and management of such) are used by the PMI. So the perception of local and link partner is reversed. The local device is the PMI, while the link partner is the Switch Fabric. This is consistent with the intention of the Virtual PHY.

7.3.1.1 Parallel Detection

In the event that there are no common bits between the advertised ability and the emulated link partners ability, auto-negotiation fails and emulated parallel detect is used. In this case, the Link Partner Auto-Negotiation Able bit of the Virtual PHY Auto-Negotiation Expansion Register (VPHY_AN_EXP) will be cleared, and the communication set to half-duplex. The speed is determined by the speed_strap_0 configuration strap. Only one of the technology ability bits in the Virtual PHY Auto-Negotiation Link Partner Base Page Ability Register (VPHY_AN_LP_BASE_ABILITY) will be set, indicating the emulated parallel detect result.

7.3.1.2 Disabling Auto-Negotiation

Auto-negotiation can be disabled in the Virtual PHY by clearing the Auto-Negotiation (VPHY_AN) bit of the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL). The Virtual PHY will then force its speed of operation to reflect the speed (Speed Select LSB (VPHY_SPEED_SEL_LSB) bit) and duplex (Duplex Mode (VPHY_DUPLEX) bit) of the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL). The speed and duplex bits in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) should be ignored when auto-negotiation is enabled.

7.3.1.3 Virtual PHY Pause Flow Control

The Virtual PHY supports pause flow control per the IEEE 802.3 specification. The Virtual PHYs advertised pause flow control abilities are set via the Symmetric Pause and Asymmetric Pause bits of the Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV). This allows the Virtual PHY to advertise its flow control abilities and auto-negotiate the flow control settings with the emulated link partner. The default values of these bits are as shown in Section 13.2.6.5, "Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV)," on page 188.

The symmetric/asymmetric pause ability of the emulated link partner is based upon the advertised pause flow control abilities of the Virtual PHY as indicated in the Symmetric Pause and Asymmetric Pause bits of the Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV). Thus, the emulated link partner always accommodates the asymmetric/symmetric pause ability settings requested by the Virtual PHY, as shown in Table 13.6, “Emulated Link Partner Pause Flow Control Ability Default Values,” on page 191.

The pause flow control settings may also be manually set via the Port 0 Manual Flow Control Register (MANUAL_FC_0). This register allows the Switch Fabric Port 0 flow control settings to be manually set when auto-negotiation is disabled or the Port 0 Full-Duplex Manual Flow Control Select (MANUAL_FC_0) bit is set. The currently enabled duplex and flow control settings can also be monitored via this register. The flow control values in the Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV) are not affected by the values of the manual flow control register. Refer to Section 6.2.3, "Flow Control Enable Logic," on page 70 for additional information.

7.3.2 Virtual PHY in MAC Mode

In the MAC mode of operation, an external PHY is connected to the MII interface of the device. Because there is an external PHY present, the Virtual PHY is not needed for external configuration. However, the Port 0 Switch Fabric MAC still requires the proper duplex setting. Therefore, in MAC mode, if the Auto-Negotiation (VPHY_AN) bit of the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) is set, the duplex is based on the P0_DUPLEX pin and duplex_pol_strap_0 configuration strap. If these signals are equal, the Port 0 Switch Fabric MAC is configured for full-duplex, otherwise it is set for half-duplex. The P0_DUPLEX pin is typically connected to the duplex indication of the external PHY. The duplex is not latched since the auto-negotiation process is not used. The duplex can be manually selected by clearing the Auto-Negotiation (VPHY_AN) bit and controlling the Duplex Mode (VPHY_DUPLEX) bit in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).

Note: In MAC mode, the Virtual PHY registers are accessible through their memory mapped registers via the SMI or I^2C serial management interfaces only. The Virtual PHY registers are not accessible through MII management.

7.3.2.1 Full-Duplex Flow Control

In the MAC mode of operation, the Virtual PHY is not applicable. Therefore, full-duplex flow control should be controlled manually by the host via the Port 0 Manual Flow Control Register (MANUAL_FC_0), based on the external PHYs auto-negotiation results.

7.3.3 Virtual PHY Resets

In addition to the chip-level hardware reset (nRST) and Power-On Reset (POR), the Virtual PHY supports two block specific resets. These are is discussed in the following sections. For detailed information on all resets, refer to Section 4.2, "Resets," on page 48.

7.3.3.1 Virtual PHY Software Reset via RESET_CTL

The Virtual PHY can be reset via the Reset Control Register (RESET_CTL) by setting the Virtual PHY Reset (VPHY_RST) bit. This bit is self clearing after approximately 102uS.

7.3.3.2 Virtual PHY Software Reset via VPHY_BASIC_CTRL

The Virtual PHY can also be reset by setting the Reset (VPHY_RST) bit of the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL). This bit is self clearing and will return to 0 after the reset is complete.

Chapter 8 Serial Management

8.1 Functional Overview

This chapter details the serial management functionality provided by the device, which includes the EEPROM I^2C master, EEPROM Loader, and I^2C slave controller.

The I^2C EEPROM controller is an I^2C master module which interfaces an optional external EEPROM with the system register bus and the EEPROM Loader. Multiple sizes of external EEPROMs are supported. Configuration of the EEPROM size is accomplished via the eeprom_size_strap configuration strap. Various commands are supported for EEPROM access, allowing for the storage and retrieval of static data. The I^2C interface conforms to the NXP *I^2C-Bus Specification*.

The EEPROM Loader provides the automatic loading of configuration settings from the EEPROM into the device at reset. The EEPROM Loader module interfaces to the EEPROM Controller, Ethernet PHYs, and the system CSRs.

The I^2C slave controller can be used for CPU serial management and allow CPU access to all system CSRs. The I^2C slave controller implements the low level I^2C slave serial interface (start and stop condition detection, data bit transmission/reception, and acknowledge generation/reception), handles the slave command protocol, and performs system register reads and writes. The I^2C slave controller conforms to the NXP *I^2C-Bus Specification*.

8.2 I^2C Overview

I^2C is a bi-directional 2-wire data protocol. A device that sends data is defined as a transmitter and a device that receives data is defined as a receiver. The bus is controlled by a master which generates the EE_SCL clock, controls bus access, and generates the start and stop conditions. Either the master or slave may operate as a transmitter or receiver as determined by the master.

The device implements an I^2C master for accessing an external EEPROM and an I^2C slave for control by a management master. Both the clock and data signals have digital input filters that reject pulses that are less than 100nS. The I^2C Master and the I^2C Slave Serial interfaces share common pins. The data pin is driven low when either interface sends a low, emulating the wired-AND function of the I^2C bus. Since the slave interface never drives the clock pin, the wired-AND is not necessary.

The following bus states exist:

- **Idle:** Both EE_SDA/SDA and EE_SCL/SCL are high when the bus is idle.
- **Start & Stop Conditions:** A start condition is defined as a high to low transition on the EE_ SDA line while EE_ SCL is high. A stop condition is defined as a low to high transition on the EE_SDA line while EE_SCL is high. The bus is considered to be busy following a start condition and is considered free 4.7uS/1.3uS (for 100KHz and 400KHz operation, respectively) following a stop condition. The bus stays busy following a repeated start condition (instead of a stop condition). Starts and repeated starts are otherwise functionally equivalent.
- **Data Valid:** Data is valid, following the start condition, when EE_SDA is stable while EE_SCL is high. Data can only be changed while the clock is low. There is one valid bit per clock pulse. Every byte must be 8 bits long and is transmitted msb first.
- **Acknowledge:** Each byte of data is followed by an acknowledge bit. The master generates a ninth clock pulse for the acknowledge bit. The transmitter releases EE_SDA/SDA (high). The receiver drives EE_SDA/SDA low so that it remains valid during the high period of the clock, taking into account the setup and hold times. The receiver may be the master or the slave depending on the direction of the data. Typically the receiver acknowledges each byte. If the master is the receiver, it does not generate an acknowledge on the last byte of a transfer. This informs the slave to not drive the next byte of data so that the master may generate a stop or repeated start condition.

Figure 8.1 displays the various bus states of a typical I^2C cycle.

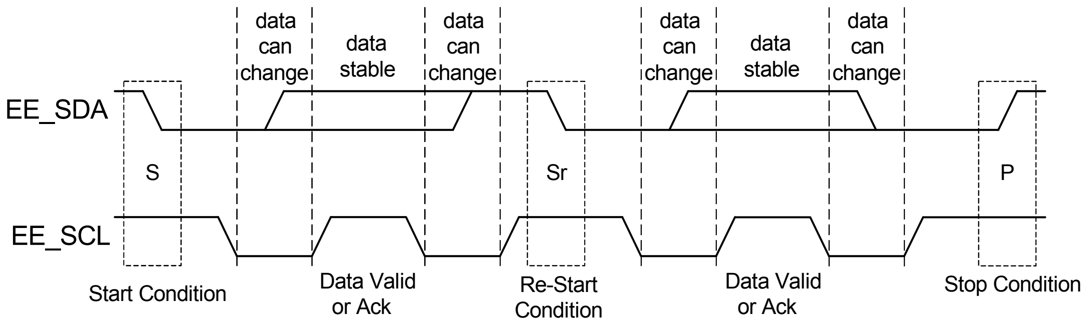


Figure 8.1 I^2C Cycle

8.3 I^2C Master EEPROM Controller

The I^2C EEPROM controller supports I^2C compatible EEPROMs.

Note: When the EEPROM Loader is running, it has exclusive use of the I^2C EEPROM controller. Refer to Section 8.4, "EEPROM Loader" for more information.

The I^2C master implements a low level serial interface (start and stop condition generation, data bit transmission and reception, acknowledge generation and reception) for connection to I2C EEPROMs, and consists of a data wire (EE_SDA) and a serial clock (EE_SCL). The serial clock is driven by the master, while the data wire is bi-directional. Both signals are open-drain and require external pull-upresistors.

The I^2C master interface runs at the standard-mode rate of 100KHz and is fully compliant with the NXP I^2*C-Bus Specification*. Refer to the he NXP I^2*C-Bus Specification* for detailed timing information.

Based on the eeprom_size_strap configuration strap, various sized I^2C EEPROMs are supported. The varying size ranges are supported by additional bits in the EEPROM Controller Address (EPC_ADDRESS) field of the EEPROM Command Register (E2P_CMD). Within each size range, the largest EEPROM uses all the address bits, while the smaller EEPROMs treat the upper address bits as don't cares. The EEPROM controller drives all the address bits as requested regardless of the actual size of the EEPROM. The supported size ranges for I^2C operation are shown in Table 8.1.

Table 8.1 I^2C EEPROM Size Ranges

eeprom_size_strap	# OF ADDRESS BYTES	EEPROM SIZE	EEPROM TYPES
0	1 (Note 8.1)	16 x 8 through 2048 x 8	24xx00, 24xx01, 24xx02, 24xx04, 24xx08, 24xx16
1	2	4096 x 8 through 65536 x 8	24xx32, 24xx64, 24xx128, 24xx256, 24xx512

Note 8.1 Bits in the control byte are used as the upper address bits.

8.3.1 I²C EEPROM Device Addressing

The I²C EEPROM is addressed for a read or write operation by first sending a control byte followed by the address byte or bytes. The control byte is preceded by a start condition. The control byte and address byte(s) are each acknowledged by the EEPROM slave. If the EEPROM slave fails to send an acknowledge, then the sequence is aborted and the EEPROM Controller Timeout (EPC_TIMEOUT) bit of the EEPROM Command Register (E2P_CMD) is set.

The control byte consists of a 4-bit control code, 3-bits of chip/block select and one direction bit. The control code is 1010b. For single byte addressing EEPROMs, the chip/block select bits are used for address bits 10, 9, and 8. For double byte addressing EEPROMs, the chip/block select bits are set low. The direction bit is set low to indicate the address is being written.

Figure 8.2 illustrates typical I²C EEPROM addressing bit order for single and double byte addressing.

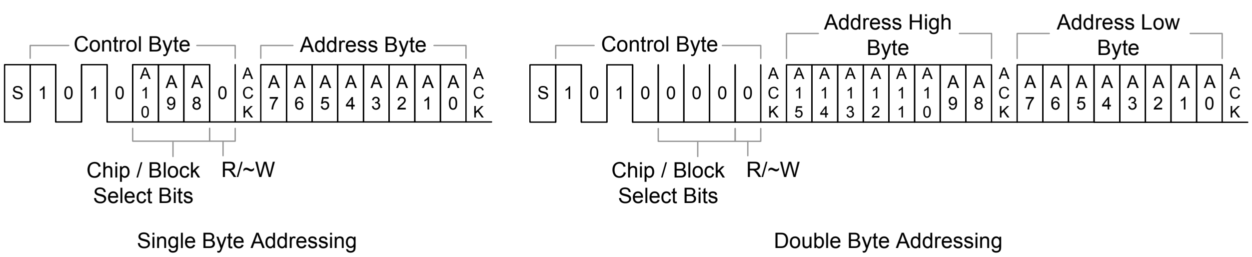


Figure 8.2 I²C EEPROM Addressing

8.3.2 I²C EEPROM Byte Read

Following the device addressing, a data byte may be read from the EEPROM by outputting a start condition and control byte with a control code of 1010b, chip/block select bits as described in Section 8.3.1, and the R/~W bit high. The EEPROM will respond with an acknowledge, followed by 8-bits of data. If the EEPROM slave fails to send an acknowledge, then the sequence is aborted and the EEPROM Controller Timeout (EPC_TIMEOUT) bit in the EEPROM Command Register (E2P_CMD) is set. The I²C master then sends a no-acknowledge, followed by a stop condition.

Figure 8.3 illustrates typical I²C EEPROM byte read for single and double byte addressing.

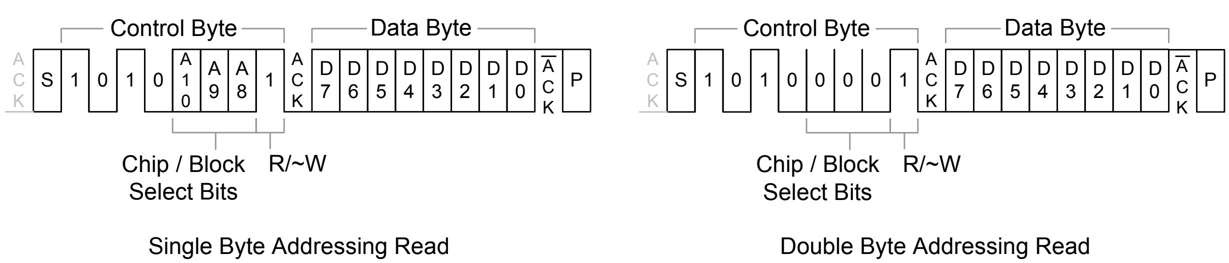


Figure 8.3 I²C EEPROM Byte Read

For a register level description of a read operation, refer to Section 8.3.7, "I2C Master EEPROM Controller Operation," on page 119.

8.3.3 I²C EEPROM Sequential Byte Reads

Following the device addressing, data bytes may be read sequentially from the EEPROM by outputting a start condition and control byte with a control code of 1010b, chip/block select bits as described in Section 8.3.1, and the R/~W bit high. The EEPROM will respond with an acknowledge, followed by 8-bits of data. If the EEPROM slave fails to send an acknowledge, then the sequence is aborted and the EEPROM Controller Timeout (EPC_TIMEOUT) bit in the EEPROM Command Register (E2P_CMD) is set. The I²C master then sends an acknowledge, and the EEPROM responds with the next 8-bits of data. This continues until the last desired byte is read, at which point the I²C master sends a no-acknowledge, followed by a stop condition.

Figure 8.3 illustrates typical I²C EEPROM sequential byte reads for single and double byte addressing.

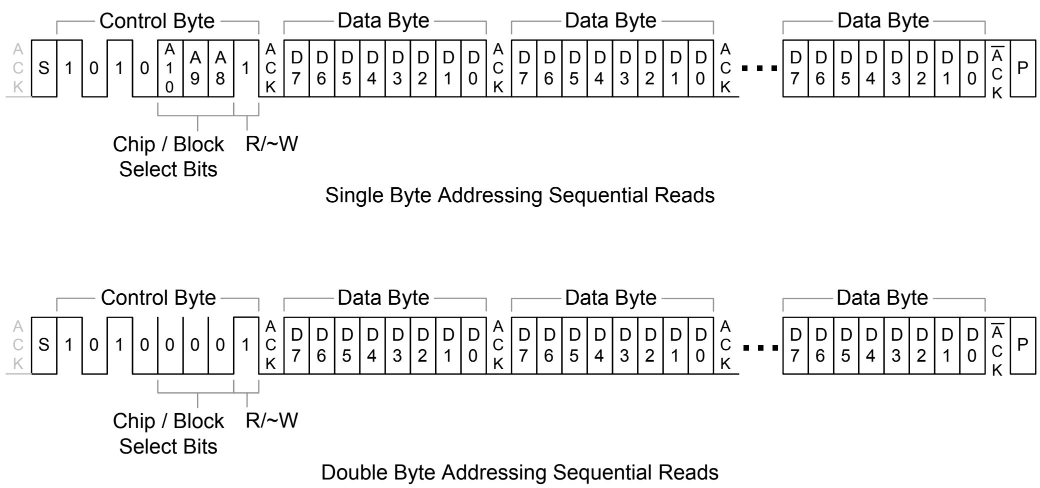


Figure 8.4 I²C EEPROM Sequential Byte Reads

Sequential reads are used by the EEPROM Loader. Refer to Section 8.4, "EEPROM Loader" for additional information.

For a register level description of a read operation, refer to Section 8.3.7, "I2C Master EEPROM Controller Operation," on page 119.

8.3.4 I²C EEPROM Byte Writes

Following the device addressing, a data byte may be written to the EEPROM by outputting the data after receiving the acknowledge from the EEPROM. The data byte is acknowledged by the EEPROM slave and the I²C master finishes the write cycle with a stop condition. If the EEPROM slave fails to send an acknowledge, then the sequence is aborted and the EEPROM Controller Timeout (EPC_TIMEOUT) bit in the EEPROM Command Register (E2P_CMD) is set.

Following the data byte write cycle, the I²C master will poll the EEPROM to determine when the byte write is finished. After meeting the minimum bus free time, a start condition is sent followed by a control byte with a control code of 1010b, chip/block select bits low, and the R/~W bit low. If the EEPROM is finished with the byte write, it will respond with an acknowledge. Otherwise, it will respond with a no-acknowledge and the I²C master will issue a stop and repeat the poll. If the acknowledge does not occur within 30mS, a time-out occurs. The check for timeout is only performed following each no-acknowledge, since it may be possible that the EEPROM write finished before the timeout but the 30mS expired before the poll was performed (due to the bus being used by another master).

Once the I²C master receives the acknowledge, it concludes by sending a start condition, followed by a stop condition, which will place the EEPROM into standby.

Figure 8.3 illustrates typical I^2C EEPROM byte write.

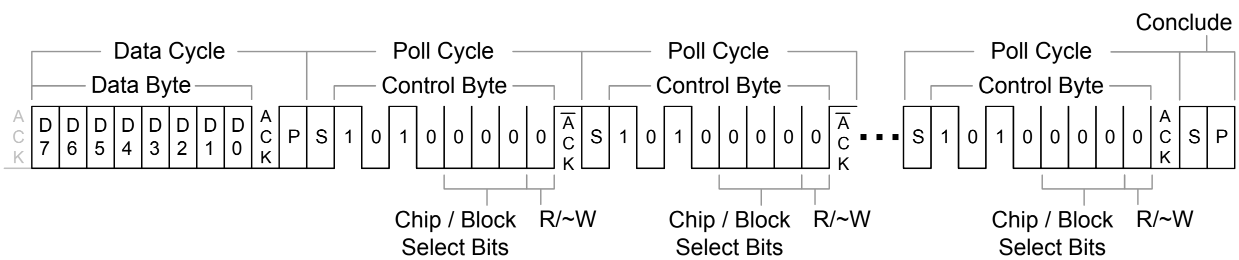


Figure 8.5 I^2C EEPROM Byte Write

For a register level description of a write operation, refer to Section 8.3.7, "I2C Master EEPROM Controller Operation," on page 119.

8.3.5 Wait State Generation

The serial clock is also used as an input as it can be held low by the slave device in order to wait-state the data cycle. Once the slave has data available or is ready to receive, it will release the clock. Assuming the masters clock low time is also expired, the clock will rise and the cycle will continue. If the slave device holds the clock low for more than 30mS, the current command sequence is aborted and the EEPROM Controller Timeout (EPC_TIMEOUT) bit in the EEPROM Command Register (E2P_CMD) is set.

8.3.6 I_2C Bus Arbitration and Clock Synchronization

Since the I^2C Master and the I^2C Slave Serial interfaces share common pins, there are at least two master I^2C devices on the bus (the device and the Host). There exists the potential that both masters try to access the bus at the same time. The I^2C specification handles this situation with three mechanisms: bus busy, clock synchronization and bus arbitration.

Note: The timing parameters referred to in the following subsections refer to the detailed timing information presented in the NXP *I^2C-Bus Specification*.

8.3.6.1 Bus Busy

A master may start a transfer only if the bus is not busy. The bus is considered to be busy after the START condition and is considered to be free again t_{buf} time after the STOP condition. The standard mode value of 4.7us is used for t_{buf} since the EEPROM master runs at the standard mode rate. Following reset, it is unknown if the bus is actually busy, since the START condition may have been missed. Therefore, following reset, the bus is initially considered busy and is considered free t_{buf} time after the STOP condition or if clock and data are seen high for 4mS. In order to speed up device configuration, if the management mode is not I^2C, this check is not performed (the bus is initially considered free).

8.3.6.2 Clock Synchronization

Clock synchronization is used, since both masters may be generating different clock frequencies. When the clock is driven low by one master, each other active master will restart its low timer and also drive the clock low. Each master will drive the clock low for its minimum low time and then release it. The clock line will not go high until all masters have released it. The slowest master therefore determines the actual low time. Devices with shorter low timers will wait. Once the clock goes high, each master will start its high timer. The first master to reach its high time will once again drive the clock low. The fastest master therefore determines the actual high time. The process then repeats. Clock synchronization is similar to the cycle stretching that can be done by a slave device, with the exception that a slave device can only extend the low time of the clock. It can not cause the falling edge of the clock.

8.3.6.3 Arbitration

Arbitration involves testing the input data vs. the output data, when the clock goes high, to see if they match. Since the data line is wired-AND'ed, a master transmitting a high value will see a mismatch if another master is transmitting a low value. The comparison is not done when receiving bits from the slave. Arbitration starts with the control byte and, if both masters are accessing the same slave, can continue into address and data bits (for writes) or acknowledge bits (for reads). If desired, a master that loses arbitration can continue to generate clock pulses until the end of the loosing byte (note that the ACK on a read is considered the end of the byte) but the losing master may no longer drive any data bits. It is not permitted for another master to access the EEPROM while the device is using it during startup or due to an EEPROM command. The other master should wait sufficient time or poll the device to determine when the EEPROM is available. This restriction simplifies the arbitration and access process since arbitration will always be resolved when transmitting the 8 control bits during the Device Addressing or during the Poll Cycles. If arbitration is lost during the Device Addressing, the I^2C Master will return to the beginning of the Device Addressing sequence and wait for the bus to become free. If arbitration is lost during a Poll Cycle, the I^2C Master will return to the beginning of the Poll Cycle sequence and wait for the bus to become free. Note that in this case the 30mS time out counter should not be reset. If the 30mS timeout should expire while waiting for the bus to become free, the sequence should not abort without first completing a final poll (with the exception of the busy / arbitration timeout described in Section 8.3.6.4).

8.3.6.4 Timeout Due to Busy or Arbitration

It is possible for another master to monopolize the bus (due to a continual bus busy or more successful arbitration). If successful arbitration is not achieved within 1.92 seconds from the start of the read or write request or from the start of the Poll cycle, the command sequence or Poll cycle is aborted and the EEPROM Controller Timeout (EPC_TIMEOUT) bit in the EEPROM Command Register (E2P_CMD) is set. Note that this is a total timeout value and not the timeout for any one portion of the sequence.

8.3.7 I^2C Master EEPROM Controller Operation

I^2C master EEPROM operations are performed using the EEPROM Command Register (E2P_CMD) and EEPROM Data Register (E2P_DATA).

The following operations are supported:

- READ (Read Location)
- WRITE (Write Location)
- RELOAD (EEPROM Loader Reload - See Section 8.4, "EEPROM Loader")

Note: The EEPROM Loader uses the READ command only.

The supported commands are detailed in Section 13.2.3.1, "EEPROM Command Register (E2P_CMD)," on page 160. Details specific to each operational mode are explained in Section 8.2, "I2C Overview" and Section 8.4, "EEPROM Loader", respectively.

When issuing a WRITE command, the desired data must first be written into the EEPROM Data Register (E2P_DATA). The WRITE command may then be issued by setting the EEPROM Controller Command (EPC_COMMAND) field of the EEPROM Command Register (E2P_CMD) to the desired command value. If the operation is a WRITE, the EEPROM Controller Address (EPC_ADDRESS) field in the EEPROM Command Register (E2P_CMD) must also be set to the desired location. The command is executed when the EEPROM Controller Busy (EPC_BUSY) bit of the EEPROM Command Register (E2P_CMD) is set. The completion of the operation is indicated when the EEPROM Controller Busy (EPC_BUSY) bit is cleared.

When issuing a READ command, the EEPROM Controller Command (EPC_COMMAND) and EEPROM Controller Address (EPC_ADDRESS) fields of the EEPROM Command Register (E2P_CMD) must be configured with the desired command value and the read address, respectively. The READ command is executed by setting the EEPROM Controller Busy (EPC_BUSY) bit of the EEPROM Command Register (E2P_CMD). The completion of the operation is indicated when the EEPROM Controller Busy (EPC_BUSY) bit is cleared, at which time the data from the EEPROM may be read from the EEPROM Data Register (E2P_DATA).

The RELOAD operation is performed by writing the RELOAD command into the EEPROM Controller Command (EPC_COMMAND) field of the EEPROM Command Register (E2P_CMD). The command is executed by setting the EEPROM Controller Busy (EPC_BUSY) bit of the EEPROM Command Register (E2P_CMD). In all cases, the software must wait for the EEPROM Controller Busy (EPC_BUSY) bit to clear before modifying the EEPROM Command Register (E2P_CMD).

If an operation is attempted and the EEPROM device does not respond within 30mS, the device will time-out, and the EEPROM Controller Timeout (EPC_TIMEOUT) bit of the EEPROM Command Register (E2P_CMD) will be set.

Figure 8.6 illustrates the process required to perform an EEPROM read or write operation.

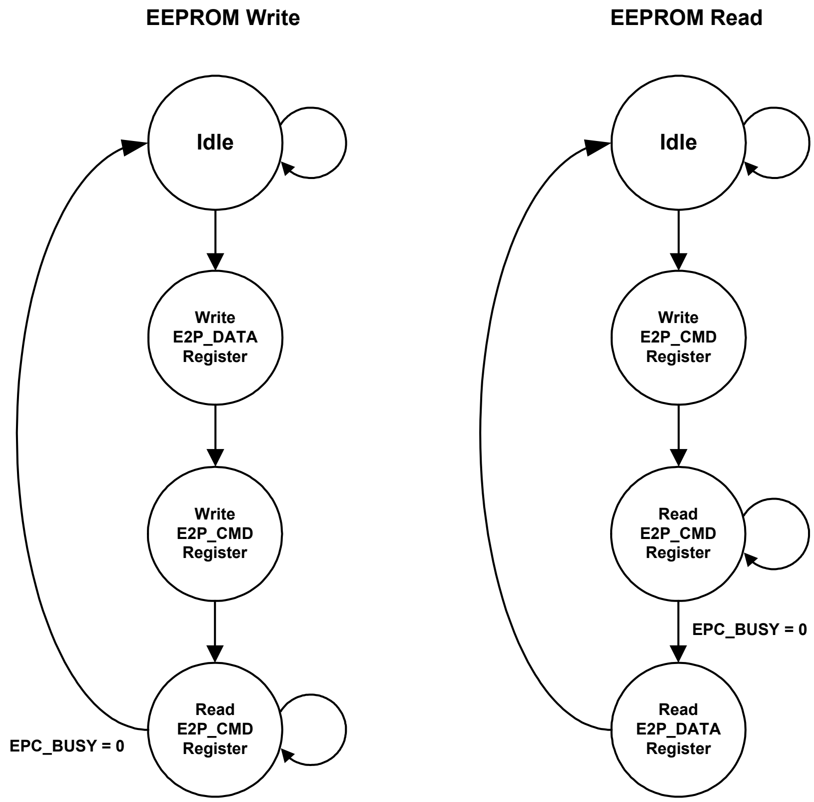


Figure 8.6 EEPROM Access Flow Diagram

8.4 EEPROM Loader

The EEPROM Loader interfaces to the I^2C EEPROM controller, the PHYs, and to the system CSRs (via the Register Access MUX). All system CSRs are accessible to the EEPROM Loader.

The EEPROM Loader runs upon a pin reset (nRST), power-on reset (POR), digital reset (Digital Reset (DIGITAL_RST) bit in the Reset Control Register (RESET_CTL)), or upon the issuance of a RELOAD command via the EEPROM Command Register (E2P_CMD). Refer to Section 4.2, "Resets," on page 48 for additional information on resets.

The EEPROM contents must be loaded in a specific format for use with the EEPROM Loader. An overview of the EEPROM content format is shown in Table 8.2. Each section of EEPROM contents is discussed in detail in the following sections.

Table 8.2 EEPROM Contents Format Overview

EEPROM ADDRESS	DESCRIPTION	VALUE
0	EEPROM Valid Flag	A5h
1	MAC Address Low Word [7:0]	1st Byte on the Network
2	MAC Address Low Word [15:8]	2nd Byte on the Network
3	MAC Address Low Word [23:16]	3rd Byte on the Network
4	MAC Address Low Word [31:24]	4th Byte on the Network
5	MAC Address High Word [7:0]	5th Byte on the Network
6	MAC Address High Word [15:8]	6th Byte on the Network
7	Configuration Strap Values Valid Flag	A5h
8 - 11	Configuration Strap Values	See Table 8.3
12	Burst Sequence Valid Flag	A5h
13	Number of Bursts	See Section 8.4.5, "Register Data"
14 and above	Burst Data	See Section 8.4.5, "Register Data"

8.4.1 EEPROM Loader Operation

Upon a pin reset (nRST), power-on reset (POR), digital reset (Digital Reset (DIGITAL_RST) bit in the Reset Control Register (RESET_CTL)), or upon the issuance of a RELOAD command via the EEPROM Command Register (E2P_CMD), the EEPROM Controller Busy (EPC_BUSY) bit in the EEPROM Command Register (E2P_CMD) will be set. While the EEPROM Loader is active, the Device Ready (READY) bit of the Hardware Configuration Register (HW_CFG) is cleared and no writes to the device should be attempted. The operational flow of the EEPROM Loader can be seen in Figure 8.7.

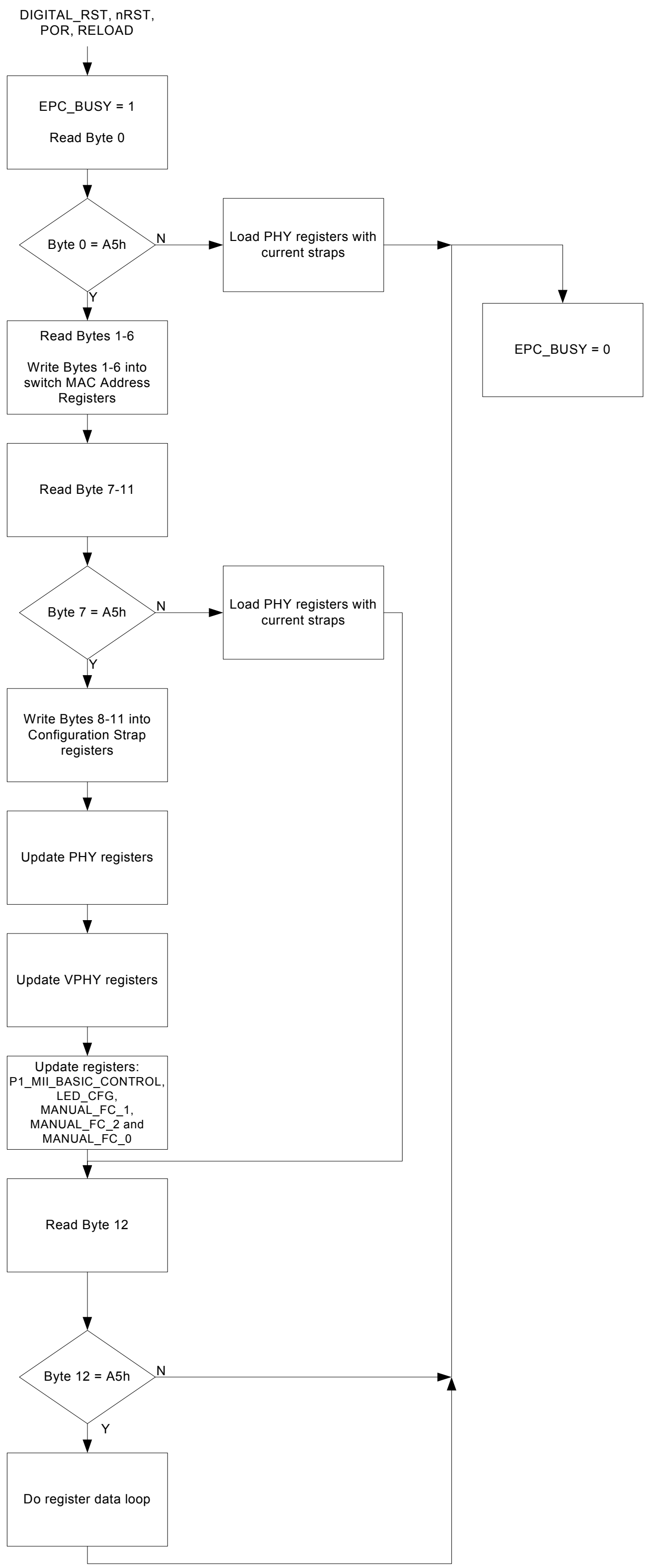


Figure 8.7 EEPROM Loader Flow Diagram

8.4.2 EEPROM Valid Flag

Following the release of nRST, POR, DIGITAL_RST, or a RELOAD command, the EEPROM Loader starts by reading the first byte of data from the EEPROM. If the value of A5h is not read from the first byte, the EEPROM Loader will load the current configuration strap values into the PHY registers (see Section 8.4.4.1) and then terminate, clearing the EEPROM Controller Busy (EPC_BUSY) bit in the EEPROM Command Register (E2P_CMD). Otherwise, the EEPROM Loader will continue reading sequential bytes from the EEPROM.

8.4.3 MAC Address

The next six bytes in the EEPROM, after the EEPROM Valid Flag, are written into the Switch Fabric MAC Address High Register (SWITCH_MAC_ADDRH) and Switch Fabric MAC Address Low Register (SWITCH_MAC_ADDRL). The EEPROM bytes are written into the MAC address registers in the order specified in Table 8.2.

8.4.4 Soft-Straps

The 7th byte of data to be read from the EEPROM is the Configuration Strap Values Valid Flag. If this byte has a value of A5h, the next 4 bytes of data (8-11) are written into the configuration strap registers per the assignments detailed in Table 8.3. If the flag byte is not A5h, these next 4 bytes are skipped (they are still read to maintain the data burst, but are discarded). However, the current configuration strap values are still loaded into the PHY registers (see Section 8.4.4.1). Refer to Section 4.2.4, "Configuration Straps," on page 52 for more information on configuration straps.

Table 8.3 EEPROM Configuration Bits

BYTE/BIT	7	6	5	4	3	2	1	0
Byte 8	BP_EN_strap_1	FD_FC_strap_1	manual_FC_strap_1	manual_mdix_strap_1	auto_mdix_strap_1	speed_strap_1	duplex_strap_1 / duplex_pol_strap_1	autoneg_strap_1/ SQE_test_disable_strap_1
Byte 9	BP_EN_strap_2	FD_FC_strap_2	manual_FC_strap_2	manual_mdix_strap_2	auto_mdix_strap_2	speed_strap_2	duplex_strap_2	autoneg_strap_2
Byte 10	unused		BP_EN_strap_0	FD_FC_strap_0	manual_FC_strap_0	speed_strap_0	duplex_pol_strap_0	SQE_test_disable_strap_0
Byte 11	LED_fun_strap[1:0]		LED_en_strap[5:0]					

8.4.4.1 PHY Registers Synchronization

Some PHY register defaults are based on configuration straps. In order to maintain consistency between the updated configuration strap registers and the PHY registers, the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x), Port x PHY Special Modes Register (PHY_SPECIAL_MODES_x), and Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) are written when the EEPROM Loader is run.

The Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) is written with the new defaults as detailed in Section 13.3.2.5, "Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x)," on page 214.

The Port x PHY Special Modes Register (PHY_SPECIAL_MODES_x) is written with the new defaults as detailed in Section 13.3.2.9, "Port x PHY Special Modes Register (PHY_SPECIAL_MODES_x)," on page 221.

The Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) is written with the new defaults as detailed in Section 13.3.2.1, "Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x)," on page 208. Additionally, the Restart Auto-Negotiation (PHY_RST_AN) bit is set in these registers. This re-runs the Auto-negotiation using the new default values of the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) register to determine the new Auto-negotiation results.

Note: Each of these PHY registers is written in its entirety, overwriting any previously changed bits.

Note: When any external MII mode is selected, the PHY registers for Port 1 are not updated.

Following the writes to the PHY registers, the PMI registers are reset back to their default values.

8.4.4.2 Virtual PHY Registers Synchronization

Some PHY register defaults are based on configuration straps. In order to maintain consistency between the updated configuration strap registers and the Virtual PHY registers, the Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV), Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS), and Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) are written when the EEPROM Loader is run.

The Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV) is written with the new defaults as detailed in Section 13.2.6.5, "Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV)," on page 188.

The Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS) is written with the new defaults as detailed in Section 13.2.6.8, "Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS)," on page 194.

The Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) is written with the new defaults as detailed in Section 13.2.6.1, "Virtual PHY Basic Control Register (VPHY_BASIC_CTRL)," on page 182. Additionally, the Restart Auto-Negotiation (PHY_RST_AN) bit is set in this register. This re-runs the Auto-negotiation using the new default values of the Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV) register to determine the new Auto-negotiation results.

Note: Each of these VPHY registers is written in its entirety, overwriting any previously changed bits.

8.4.4.3 Port 1 MII Basic Control Register Synchronization

Some of the defaults of the Port 1 MII Basic Control Register are based on configuration straps. In order to maintain consistency between the updated Configuration Strap registers and the register, it is written with the new defaults as detailed in Section 13.2.7.7, "Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL)," on page 202.

Note: The register is written in its entirety, overwriting any previously changed bits.

8.4.4.4 LED and Manual Flow Control Register Synchronization

Since the defaults of the LED Configuration Register (LED_CFG), Port 1 Manual Flow Control Register (MANUAL_FC_1), Port 2 Manual Flow Control Register (MANUAL_FC_2), and Port 0 Manual Flow Control Register (MANUAL_FC_0) are based on configuration straps, the EEPROM Loader reloads these registers with their new default values.

8.4.5 Register Data

Optionally following the configuration strap values, the EEPROM data may be formatted to allow access to the device's parallel, directly writable registers. Access to indirectly accessible registers (e.g. Switch Engine registers, etc.) is achievable with an appropriate sequence of writes (at the cost of EEPROM space).

This data is first preceded with a Burst Sequence Valid Flag (EEPROM byte 12). If this byte has a value of A5h, the data that follows is recognized as a sequence of bursts. Otherwise, the EEPROM Loader is finished, will go into a wait state, and clear the EEPROM Controller Busy (EPC_BUSY) bit in the EEPROM Command Register (E2P_CMD). This can optionally generate an interrupt.

The data at EEPROM byte 13 and above should be formatted in a sequence of bursts. The first byte is the total number of bursts. Following this is a series of bursts, each consisting of a starting address, count, and the count x 4 bytes of data. This results in the following formula for formatting register data:

8-bits number_of_bursts

repeat (number_of_bursts)

    16-bits {starting_address[9:2] / count[7:0]}

    repeat (count)

        8-bits data[31:24], 8-bits data[23:16], 8-bits data[15:8], 8-bits data[7:0]

Note: The starting address is a DWORD address. Appending two 0 bits will form the register address.

As an example, the following is a 3 burst sequence, with 1, 2, and 3 DWORDs starting at register addresses 40h, 80h, and C0h respectively:

A5h, (Burst Sequence Valid Flag)

3h, (number_of_bursts)

16{10h, 1h}, (starting_address1 divided by 4 / count1)

11h, 12h, 13h, 14h, (4 x count1 of data)

16{20h, 2h}, (starting_address2 divided by 4 / count2)

21h, 22h, 23h, 24h, 25h, 26h, 27h, 28h, (4 x count2 of data)

16{30h, 3h}, (starting_address3 divided by 4 / count3)

31h, 32h, 33h, 34h, 35h, 36h, 37h, 38h, 39h, 3Ah, 3Bh, 3Ch (4 x count3 of data)

In order to avoid overwriting the Switch CSR register interface or the PHY Management Interface (PMI), the EEPROM Loader waits until the CSR Busy (CSR_BUSY) bit of the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD) and the MII Busy (MIIBZY) bit of the PHY Management Interface Access Register (PMI_ACCESS) are cleared before performing any register write.

The EEPROM Loader checks that the EEPROM address space is not exceeded. If so, it will stop and set the EEPROM Loader Address Overflow (LOADER_OVERFLOW) bit in the EEPROM Command Register (E2P_CMD). The address limit is based on the eeprom_size_strap which specifies a range of sizes. The address limit is set to the largest value of the specified range.

8.4.6 EEPROM Loader Finished Wait-State

Once finished with the last burst, the EEPROM Loader will go into a wait-state and the EEPROM Controller Busy (EPC_BUSY) bit of the EEPROM Command Register (E2P_CMD) will be cleared.

8.4.7 Reset Sequence and EEPROM Loader

In order to allow the EEPROM Loader to change the Port 1/2 PHYs and Virtual PHY strap inputs and maintain consistency with the PHY and Virtual PHY registers, the following sequence is used:

1. After power-up or upon a hardware reset (nRST), the straps are sampled into the device as specified in Section 14.5.2, "Reset and Configuration Strap Timing," on page 368.
2. After the PLL is stable, the main chip reset is released and the EEPROM Loader reads the EEPROM and configures (overrides) the strap inputs.

3. The EEPROM Loader writes select Port 1/2 and Virtual PHY registers, as specified in Section 8.4.4.1 and Section 8.4.4.2, respectively.

Note: Step 3 is also performed in the case of a RELOAD command or digital reset.

8.5 I²C Slave Operation

When in MAC/PHY I²C managed mode, the I²C slave interface is used for CPU management of the device. All system CSRs are accessible to the CPU in these modes. I²C mode is selected when the mngt_mode_strap[1:0] configuration straps are set to 10b, respectively. The I²C slave controller implements the low level I²C slave serial interface (start and stop condition detection, data bit transmission and reception, and acknowledge generation and reception), handles the slave command protocol, and performs system register reads and writes. The I²C slave controller conforms to the NXP *I²C-Bus Specification*.

The I²C slave serial interface consists of a data wire (SDA) and a serial clock (SCL). The serial clock is driven by the master, while the data wire is bi-directional. Both signals are open-drain and require external pull-up resistors.

The I²C slave serial interface supports the standard-mode speed of up to 100KHz and the fast-mode speed of 400KHz. Refer to the NXP *I²C-Bus Specification* for detailed I²C timing information.

8.5.1 I²C Slave Command Format

The I²C slave serial interface supports single register and multiple register read and write commands. A read or write command is started by the master first sending a start condition, followed by a control byte. The control byte consists of a 7-bit slave address and a 1-bit read/write indication (R/~W). The slave address used by the device is 0001010b, written as SA6 (first bit on the wire) through SA0 (last bit on the wire). Assuming the slave address in the control byte matches this address, the control byte is acknowledged by the device. Otherwise, the entire sequence is ignored until the next start condition. The I²C command format can be seen in Figure 8.8.

If the read/write indication (R/~W) in the control byte is a 0 (indicating a potential write), the next byte sent by the master is the register address. After the address byte is acknowledged by the device, the master may either send data bytes to be written, or it may send another start condition (to start the reading of data), or a stop condition. The latter two will terminate the current write (without writing any data), but will have the affect of setting the internal register address which will be used for subsequent reads.

If the read/write indication in the control byte is a 1 (indicating a read), the device will start sending data following the control byte acknowledgement.

Note: All registers are accessed as DWORDs. Appending two 0 bits to the address field will form the register address. Addresses and data are transferred msb first. Data is transferred MSB first (little endian).

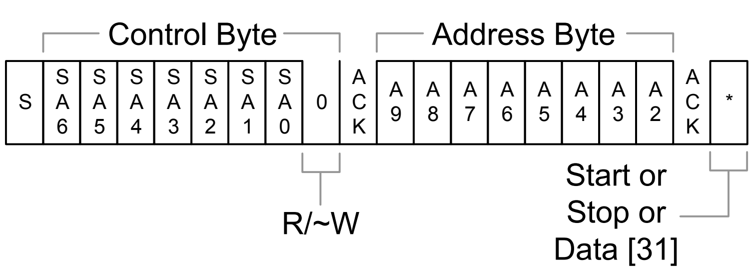


Figure 8.8 I²C Slave Addressing

8.5.2 I^{2}C Slave Read Sequence

Following the device addressing, as detailed in Section 8.5.1, a register is read from the device when the master sends a start condition and control byte with the R/~W bit set. Assuming the slave address in the control byte matches the device address, the control byte is acknowledged by the device. Otherwise, the entire sequence is ignored until the next start condition. Following the acknowledge, the device sends 4 bytes of data. The first 3 bytes are acknowledged by the master and on the fourth, the master sends a no-acknowledge followed by the stop condition. The no-acknowledge informs the device not to send the next 4 bytes (as it would in the case of a multiple read). The internal register address is unchanged following the single read.

Multiple reads are performed when the master sends an acknowledge on the fourth byte. The internal address is incremented and the next register is shifted out. Once the internal address reaches its maximum, it rolls over to 0. The multiple read is concluded when the master sends a no-acknowledge followed by a stop condition. The no-acknowledge informs the device not to send the next 4 bytes. The internal register address in incremented for each read including the final.

For both single and multiple reads, in the case that the master sends a no-acknowledge on any of the first three bytes of the register, the device will stop sending subsequent bytes. If the master sends an unexpected start or stop condition, the device will stop sending immediately and will respond to the next sequence as needed.

Since data is read serially, register values are latched (registered) at the beginning of each 32-bit read to prevent the host from reading an intermediate value. The latching occurs multiple times in a multiple read sequence. In addition, any register that is affected by a read operation (e.g. a clear on read bit) is not cleared until after all 32-bits are output. In the event that 32-bits are not read (master sends a no-acknowledge on one of the first three bytes or a start or stop condition occurs unexpectedly), the read is considered invalid and the register is not affected. Multiple registers may be cleared in a multiple read cycle, each one being cleared as it is read. I^{2}C reads from unused register addresses return all zeros.

Figure 8.9 illustrates a typical single and multiple register read.

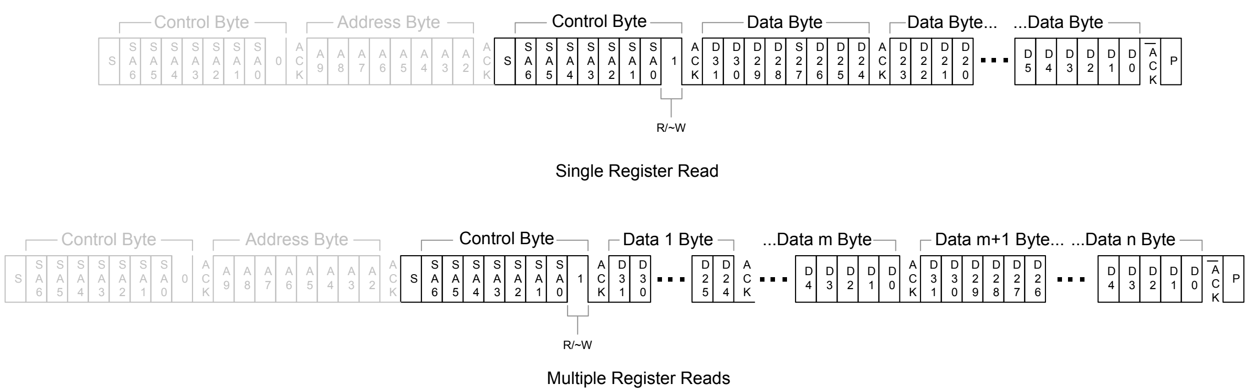


Figure 8.9 I^{2}C Slave Reads

8.5.2.1 I^{2}C Slave Read Polling for Reset Complete

During reset, the I^{2}C slave interface will not return valid data. To determine when the reset condition is complete, the Byte Order Test Register (BYTE_TEST) should be polled. Once the correct pattern is read, the interface can be considered functional. At this point, the Device Ready (READY) bit in the Hardware Configuration Register (HW_CFG) can be polled to determine when the device initialization is complete. Refer to Section 4.2, "Resets," on page 48 for additional information.

8.5.3 I²C Slave Write Sequence

Following the device addressing, as detailed in Section 8.5.1, a register is written to the device when the master continues to send data bytes. Each byte is acknowledged by the device. Following the fourth byte of the sequence, the master may either send another start condition or halt the sequence with a stop condition. The internal register address is unchanged following a single write.

Multiple writes are performed when the master sends additional bytes following the fourth acknowledge. The internal address is automatically incremented and the next register is written. once the internal address reaches it maximum value, it rolls over to 0. The multiple write is concluded when the master sends another start condition or stop condition. The internal register address is incremented for each write including the final. This is not relevant for subsequent writes, since a new register address would be included on a new write cycle. However, this does affect the internal register address if it were to be used for reads without first resetting the register address.

For both single and multiple writes, if the master sends an unexpected start or stop condition, the device will stop immediately and will respond to the next sequence as needed.

The data write to the register occurs after the 32-bits are input. In the event that 32-bits are not written (master sends a start, or a stop condition occurs unexpectedly), the write is considered invalid and the register is not affected. Multiple registers may be written in a multiple write cycle, each one being written after 32-bits. I²C writes must not be performed to unused register addresses.

Figure 8.10 illustrates a typical single and multiple register write.

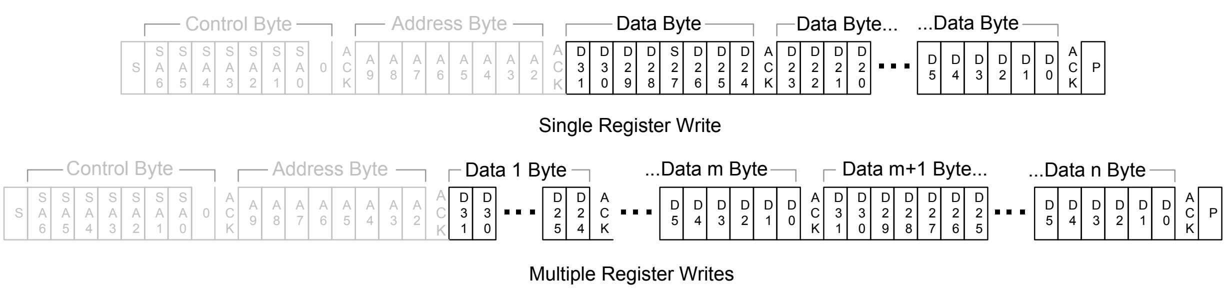


Figure 8.10 I²C Slave Writes

Chapter 9 MII Data Interfaces

9.1 Port 0 MII Data Path

The MII Data Path is used to connect the Switch Engine port to the external MII pins, to emulate an RMII/MII PHY, and to select between PHY and MAC modes.

9.1.1 Port 0 MII MAC Mode

When operating in MII MAC mode, the Switch Fabric MAC output signals are routed directly to the device's MII output pins (P0_OUTD[3:0] and P0_OUTDV). The Switch Fabric MAC inputs are sourced from the MII input pins (P0_IND[3:0], P0_INDV, P0_INER, P0_COL, P0_CRS, P0_OUTCLK, and P0_INCLK). MII MAC mode can operate at up to 200Mbps.

9.1.2 Port 0 MII PHY Mode

When operating in MII PHY mode, the MII Data Path supplies the RX and TX clocks, creates the CRS and COL signals and optionally loops back the MII or Switch Engine's transmissions. It also provides the collision test function for the external MII pins or Switch Engine. MII PHY mode can operate at up to 200Mbps (Turbo mode).

The MII pins P0_INCLK, P0_OUTCLK, P0_COL, and P0_CRS, which are inputs when in MII MAC mode, are outputs when in MII PHY mode. When in MII PHY mode, if the Isolate (VPHY_ISO) bit of the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) is set, MII data path output pins are three-stated, the pull-ups and pull-downs are disabled and the MII data path input pins are ignored (disabled into the non-active state and powered down). Note that setting the Isolate (VPHY_ISO) bit does not cause isolation of the MII management pins and does not affect MII MAC mode.

9.1.2.1 Turbo Operation

Turbo (200Mbps) operation is facilitated in MII PHY mode via the Turbo MII Enable bit of the Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS). When set, this bit changes the data rate of the MII PHY from 100Mbps to 200Mbps. The Speed Select LSB (VPHY_SPEED_SEL_LSB) bit of the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) toggles between 10 and 200 Mbps operation when Turbo MII Enable is set.

9.1.2.2 Clock Drive Strength

When operating at 200Mbps (Turbo mode), the drive strength of P0_INCLK and P0_OUTCLK pins is selected based on the setting of the RMII/Turbo MII Clock Strength bit of the Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS). A low selects 12ma, a high selects 16ma. When operating at 10 or 100Mbps, the drive strength is fixed at 12ma.

9.1.2.3 Signal Quality Error (SQE) Heartbeat Test

The SQE_HEARTBEAT signal, observable on the P0_COL pin, is generated in 10Mbit half duplex mode in response to a transmission from the external MAC. At 0.6uS to 1.6uS (1.0uS nominal) following the de-assertion of P0_INDV, SQE_HEARTBEAT is set active for 0.5uS to 1.5uS (5 to 15 bit times) (1.0uS nominal). This test is disabled via the SQEOFF bit of the Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS).

9.1.2.4 Collision Test

Two forms of collision testing are available: External MAC collision testing and Switch Engine collision testing.

External MAC collision testing is enabled when the Collision Test (VPHY_COL_TEST) bit of the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) is set. In this test mode, any transmissions from the external MAC will result in collision signaling to the external MAC via the P0_COL pin.

Switch Engine collision testing is enabled when the Switch Collision Test Port 0 bit of the Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS) is set. In this test mode, any transmissions from the Switch Engine will result in the assertion of the internal collision signal to the Switch Fabric Port 0. Switch Engine collision testing occurs regardless of the setting of the Isolate (VPHY_ISO) bit.

9.1.2.5 Loopback

Two forms of loopback testing are available: External MAC loopback and Switch Engine loopback.

External MAC loopback is enabled when the Loopback (VPHY_LOOPBACK) bit of the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) is set. Transmissions from the external MAC are not sent to the Switch Engine and are not used for purposes of signaling data valid, collision or carrier sense to the Switch Engine. Instead, they are looped back onto the receive path. Transmissions from the Switch Engine are ignored and are not used for purposes of signaling data valid, collision or carrier sense on the MII pins. The collision output to the external MAC (via P0_COL) is not generated unless the Collision Test (VPHY_COL_TEST) bit is set. The SQE_HEARTBEAT signal does not drive the collision output (via P0_COL) during External MAC loopback but can drive it during Switch Engine loopback. The carrier sense output on the P0_CRS pin is only based on the transmit enable from the external MAC (via the P0_INDV pin).

Switch Engine loopback is enabled when the Switch Looopback Port 0 bit of the Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS) is set. Transmissions from the Switch Engine are not sent to the external MAC and are not used for purposes of signaling data valid, collision or carrier sense to the MII pins. Instead, they are looped back internally onto the receive path. Transmissions from the external MAC are ignored and are not used for purposes of data valid, collision or carrier sense to the Switch Engine. The collision signal to the Switch Engine is not generated unless the Switch Collision Test Port 0 bit is set. The carrier sense signal is only based on the transmit enable from the Switch Engine. Switch Engine loopback occurs regardless of the setting of the Isolate (VPHY_ISO) bit.

9.1.3 Port 0 RMII PHY Mode

Port 0 RMII PHY mode is used when interfacing Port 0 to an external MAC that does not support the full MII interface. The RMII interface uses a subset of the MII pins. The P0_OUTD[1:0], P0_OUTDV, P0_IND[1:0], P0_INDV, and P0_OUTCLK pins are the only MII pins used to communicate with the external MAC in this mode. This mode provides collision testing for the Switch Engine, as well as loopback test capabilities.

Note: The RMII standard does not support external MAC collision testing.

When in RMII PHY mode, if the Isolate (VPHY_ISO) bit of the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) is set, MII data path output pins are three-stated, the pull-ups and pull-downs are disabled and the MII data path input pins are ignored (disabled into the non-active state and powered down). Note that setting the Isolate (VPHY_ISO) bit does not cause isolation of the MII management pins and does not affect MII MAC mode.

9.1.3.1 Reference Clock Selection

The 50MHz RMII reference clock can be selected from either the P0_OUTCLK pin input or the internal 50MHz clock. The choice is based on the setting of the RMII Clock Direction bit of the Virtual PHY

Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS). A low selects P0_OUTCLK and a high selects the internal 50MHz clock. The high setting also enables P0_OUTCLK as an output to be used as the system reference clock.

9.1.3.2 Clock Drive Strength

When P0_OUTCLK is configured as an output via the RMII Clock Direction bit of the Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS), its drive strength is based on the setting of the RMII/Turbo MII Clock Strength bit of the Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS). A low selects 12ma, a high selects 16ma.

9.1.3.3 Signal Quality Error (SQE) Heartbeat Test

The SQE_HEARTBEAT signal is not generated when operating in RMII PHY mode. The SQEOFF bit of the Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS) has no effect when operating in RMII PHY mode.

9.1.3.4 Collision Test

External MAC collision testing is not available when operating in the RMII PHY mode. The Collision Test (VPHY_COL_TEST) bit of the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) has no effect on system operation in RMII PHY mode.

Switch Engine collision testing is available and is enabled when the Switch Collision Test Port 0 bit of the Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS) is set. In this test mode, any transmissions from the Switch Engine will result in the assertion of an internal collision signal to the Switch Fabric Port 0. Switch Engine collision test occurs regardless of the setting of the Isolate (VPHY_ISO) bit.

9.1.3.5 Loopback Mode

Two forms of loopback testing are available: External MAC loopback and Switch Engine loopback.

External MAC loopback is enabled when the Loopback (VPHY_LOOPBACK) bit of the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) is set. Transmissions from the external MAC are not sent to the Switch Engine. Instead, they are looped back onto the receive path. Transmissions from the Switch Engine are ignored.

Switch Engine loopback is enabled when the Switch Looopback Port 0 bit of the Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS) is set. Transmissions from the Switch Engine are not sent to the external MAC. Instead, they are looped back internally onto the receive path. Transmissions from the external MAC are ignored. An internal collision signal to the Switch Engine is available and is asserted when the Switch Collision Test Port 0 bit is set. Switch Engine loopback occurs regardless of the setting of the Isolate (VPHY_ISO) bit.

9.2 Port 1 MII MUX/Data Path

The MII MUX/Data Path is used to connect the Switch Engine port to the external MII pins, to emulate an RMII/MII PHY, and to select between PHY and MAC modes.

9.2.1 Port 1 Internal Mode

When operating in Internal mode, the Switch Fabric MAC outputs are directly connected to the internal PHY. Similarly, the Switch Fabric Mac inputs are sourced from the internal PHY.

9.2.2 Port 1 MII MAC Mode

When operating in MII MAC mode, the Switch Fabric MAC output signals are routed directly to the device's MII output pins (P1_OUTD[3:0] and P1_OUTDV). The Switch Fabric MAC inputs are sourced from the MII input pins (P1_IND[3:0], P1_INDV, P1_INER, P1_COL, P1_CRS, P1_OUTCLK, and P1_INCLK). MII MAC mode can operate at up to 200Mbps.

9.2.3 Port 1 MII PHY Mode

When operating in MII PHY mode, the MII Data Path supplies the RX and TX clocks, creates the CRS and COL signals and optionally loops back the MII or Switch Engine's transmissions. It also provides the collision test function for the external MII pins or Switch Engine. MII PHY mode can operate at up to 200Mbps (Turbo mode).

The MII pins P1_INCLK, P1_OUTCLK, P1_COL, and P1_CRS, which are inputs when in MII MAC mode, are outputs when in MII PHY mode. When in MII PHY mode, if the Isolate bit of the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL) is set, MII data path output pins are three-stated, the pull-ups and pull-downs are disabled and the MII data path input pins are ignored (disabled into the non-active state and powered down). Note that setting the Isolate bit does not cause isolation of the MII management pins and does not affect MII MAC mode.

9.2.3.1 Turbo Operation

Turbo (200Mbps) operation is facilitated in MII PHY mode via the Turbo MII Enable bit of the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL). When set, this bit changes the data rate of the MII PHY from 100Mbps to 200Mbps. The Speed Select LSB bit of the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL) toggles between 10 and 200 Mbps operation when Turbo MII Enable is set.

9.2.3.2 Clock Drive Strength

When operating at 200Mbps (Turbo mode), the drive strength of P1_INCLK and P1_OUTCLK pins is selected based on the setting of the RMII/Turbo MII Clock Strength bit of the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL). A low selects 12ma, a high selects 16ma. When operating at 10 or 100Mbps, the drive strength is fixed at 12ma.

9.2.3.3 Signal Quality Error (SQE) Heartbeat Test

The SQE_HEARTBEAT signal, observable on the P1_COL pin, is generated in 10Mbit half duplex mode in response to a transmission from the external MAC. At 0.6uS to 1.6uS (1.0uS nominal) following the de-assertion of P1_INDV, SQE_HEARTBEAT is set active for 0.5uS to 1.5uS (5 to 15 bit times) (1.0uS nominal). This test is disabled via the SQEOFF bit of the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL).

9.2.3.4 Collision Test

Two forms of collision testing are available: External MAC collision testing and Switch Engine collision testing.

External MAC collision testing is enabled when the Collision Test bit of the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL) is set. In this test mode, any transmissions from the external MAC will result in collision signaling to the external MAC via the P1_COL pin.

Switch Engine collision testing is enabled when the Switch Collision Test Port 1 bit of the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL) is set. In this test mode, any transmissions from the Switch Engine will result in the assertion of the internal collision signal to the Switch Fabric Port 1. Switch Engine collision testing occurs regardless of the setting of the Isolate bit.

9.2.3.5 Loopback

Two forms of loopback testing are available: External MAC loopback and Switch Engine loopback.

External MAC loopback is enabled when the Loopback bit of the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL) is set. Transmissions from the external MAC are not sent to the Switch Engine and are not used for purposes of signaling data valid, collision or carrier sense to the Switch Engine. Instead, they are looped back onto the receive path. Transmissions from the Switch Engine are ignored and are not used for purposes of signaling data valid, collision or carrier sense on the MII pins. The collision output to the external MAC (via P1_COL) is not generated unless the Collision Test bit is set. The SQE_HEARTBEAT signal does not drive the collision output (via P1_COL) during External MAC loopback but can drive it during Switch Engine loopback. The carrier sense output on the P1_CRS pin is only based on the transmit enable from the external MAC (via the P1_INDV pin).

Switch Engine loopback is enabled when the Switch Looopback Port 1 bit of the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL) is set. Transmissions from the Switch Engine are not sent to the external MAC and are not used for purposes of signaling data valid, collision or carrier sense to the MII pins. Instead, they are looped back internally onto the receive path. Transmissions from the external MAC are ignored and are not used for purposes of data valid, collision or carrier sense to the Switch Engine. The collision signal to the Switch Engine is not generated unless the Switch Collision Test Port 1 bit is set. The carrier sense signal is only based on the transmit enable from the Switch Engine. Switch Engine loopback occurs regardless of the setting of the Isolate bit.

9.2.4 Port 1 RMII PHY Mode

Port 1 RMII PHY mode is used when interfacing Port 1 to an external MAC that does not support the full MII interface. The RMII interface uses a subset of the MII pins. The P1_OUTD[1:0], P1_OUTDV, P1_IND[1:0], P1_INDV, and P1_OUTCLK pins are the only MII pins used to communicate with the external MAC in this mode. This mode provides collision testing for the Switch Engine, as well as loopback test capabilities.

Note: The RMII standard does not support external MAC collision testing.

When in RMII PHY mode, if the Isolate bit of the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL) is set, MII data path output pins are three-stated, the pull-ups and pull-downs are disabled and the MII data path input pins are ignored (disabled into the non-active state and powered down). Note that setting the Isolate bit does not cause isolation of the MII management pins and does not affect MII MAC mode.

9.2.4.1 Reference Clock Selection

The 50MHz RMII reference clock can be selected from either the P1_OUTCLK pin input or the internal 50MHz clock. The choice is based on the setting of the RMII Clock Direction bit of the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL). A low selects P1_OUTCLK and a high selects the internal 50MHz clock. The high setting also enables P1_OUTCLK as an output to be used as the system reference clock.

9.2.4.2 Clock Drive Strength

When P1_OUTCLK is configured as an output via the RMII Clock Direction bit of the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL), its drive strength is based on the setting of the RMII/Turbo MII Clock Strength bit of the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL). A low selects 12ma, a high selects 16ma.

9.2.4.3 Signal Quality Error (SQE) Heartbeat Test

The SQE_HEARTBEAT signal is not generated when operating in RMII PHY mode. The SQEOFF bit of the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL) has no effect when operating in RMII PHY mode.

9.2.4.4 Collision Test

External MAC collision testing is not available when operating in the RMII PHY mode. The Collision Test bit of the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL) has no effect on system operation in RMII PHY mode.

Switch Engine collision testing is available and is enabled when the Switch Collision Test Port 1 bit of the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL) is set. In this test mode, any transmissions from the Switch Engine will result in the assertion of an internal collision signal to the Switch Fabric Port 1. Switch Engine collision test occurs regardless of the setting of the Isolate bit.

9.2.4.5 Loopback Mode

Two forms of loopback testing are available: External MAC loopback and Switch Engine loopback.

External MAC loopback is enabled when the Loopback bit of the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL) is set. Transmissions from the external MAC are not sent to the Switch Engine. Instead, they are looped back onto the receive path. Transmissions from the Switch Engine are ignored.

Switch Engine loopback is enabled when the Switch Looopback Port 1 bit of the Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL) is set. Transmissions from the Switch Engine are not sent to the external MAC. Instead, they are looped back internally onto the receive path. Transmissions from the external MAC are ignored. An internal collision signal to the Switch Engine is available and is asserted when the Switch Collision Test Port 1 bit is set. Switch Engine loopback occurs regardless of the setting of the Isolate bit.

Chapter 10 MII Management

10.1 Functional Overview

This chapter details the MII management functionality provided by the device, which includes the SMI Slave Controller, PHY Management Interface (PMI), and the MII Mode Multiplexer. The SMI Slave Controller is used for CPU management of the device via the MII pins, and allows CPU access to all system CSRs. The PHY Management Interface (PMI) is used to access the internal PHYs and optional external PHY, dependant on the management mode. The PMI implements the IEEE 802.3 management protocol. The MII Mode Multiplexer is used to direct the connections of the MII data path and MII management path based on the selected mode of the device.

10.2 SMI Slave Controller

The SMI slave controller uses the same pins and protocol as the IEEE 802.3 MII management function, and differs only in that SMI provides access to all internal registers by using a non-standard extended addressing map. The SMI protocol co-exists with the MII management protocol by using the upper half of the PHY address space (16 through 31). All direct and indirect registers can be accessed. The SMI management mode is selected when the mngt_mode_strap[1:0] inputs are set to 01b. A list of management modes and their configuration settings are discussed in Section 2.3, "Modes of Operation," on page 19.

The MII management protocol is limited to 16-bit data accesses. The protocol is also limited to 5 PHY address bits and 5 register address bits. The SMI frame format can be seen in Table 10.1. The device uses the PHY Address field bits 3:0 as the system register address bits 9:6, and the Register Address field as the system register address bits 5:1. Therefore, Register Address field bit 0 is used as the upper/lower word select. The device requires two back-to-back accesses to each register (with alternate settings of Register Address field bit 0) which are combined to form a 32-bit access. The access may be performed in any order.

Note: When accessing the device, the pair of cycles must be atomic. In this case, the first host SMI cycle is performed to the low/high word and the second host SMI cycle is performed to the high/low word, forming a 32-bit transaction with no cycles to the device in between. With the exception of Register Address field bit 0, all address and control bits must be the same for both 16-bit cycles of a 32-bit transaction.

Input data on the MDIO pin is sampled on the rising edge of the MDC input clock. Output data is sourced on the MDIO pin with the rising edge of the clock. The MDIO pin is three-stated unless actively driving read data.

A read or a write is performed using the frame format shown in Table 10.1. All addresses and data are transferred msb first. Data bytes are transferred little endian. When Register Address bit 0 is 1, bytes

3 & 2 are selected with byte 3 occurring first. When Register Address bit 0 is 0, bytes 1 & 0 are selected with byte 1 occurring first.

Table 10.1 SMI Frame Format

	PREAMBLE	START	OP CODE	PHY ADDRESS Note 10.1	REGISTER ADDRESS Note 10.1	TURN-AROUND TIME Note 10.2	DATA	IDLE Note 10.3
READ	32 1's	01	10	1AAAA 9876	AAAAA 54321	Z0	DDDDDDDDDDDDDDDD 1111110000000000 5432109876543210	Z
WRITE	32 1's	01	01	1AAAA 9876	AAAAA 54321	10	DDDDDDDDDDDDDDDD 1111110000000000 5432109876543210	Z

Note 10.1 PHY Address bit 4 is 1 for SMI commands. PHY Address 3:0 form system register address bits 9:6. The Register Address field forms the system register address bits 5:1

Note 10.2 The turn-around time (TA) is used to avoid contention during a read cycle. For a read, the device drives the second bit of the turn-around time to 0, and then drives the msb of the read data in the following clock cycle. For a write, the external host drives the first bit of the turn-around time to 1, the second bit of the turn-around time to 0, and then the msb of the write data in the following clock cycle.

Note 10.3 In the IDLE condition, the MDIO output is three-stated and pulled high externally.

Note: The SMI interface supports up to a 2.5MHz input clock. The MII/SMI timing adheres to the IEEE 802.3 specification. Refer to the IEEE 802.3 specification for detailed MII timing information.

10.2.1 Read Sequence

In a read sequence, the host sends the 32-bit preamble, 2-bit start of frame, 2-bit op-code, 5-bit PHY Address, and the 5-bit Register Address. The next clock is the first bit of the turnaround time in which the device continues to three-state MDIO. On the next rising edge of MDC, the device drives MDIO low. For the next 16 rising edges, the device drives the output data. On the final clock, the device once again three-states MDIO.

The host processor is required to perform two consecutive 16-bit reads to complete a single DWORD transfer. No ordering requirements exist. The processor can access either the low or high word first, as long as the next read is performed from the other word. If a read to the same word is performed, the combined data read pair is invalid and should be re-read. This is not a fatal error. The device will simply reset the read counters, and restart a new cycle on the next read.

Note: Select registers are readable as 16-bit registers, as noted in their register descriptions. For these registers, only one 16-bit read may be performed without the need to read the other word.

Register values are latched (registered) at the beginning of each 16-bit read to prevent the host from reading an intermediate value. In addition, any register that is affected by a read operation, such as a clear on read bit, is not cleared until after the end of the second read. In the event that 32-bits are not read, the read in considered invalid and the register is not affected.

Any register that may change between two consecutive host read cycles and spans across two WORDs, such as a counter, is latched (registered) at the beginning of the first read and held until after the second read has completed. This prevents the host from reading inconsistent data from the first and second half of a register. For example, if a counters value is 01FFh, the first half will be read as

01h. If the counter then changes to 0200h, the host would read 00h, resulting an the incorrect value of 0100h instead of either 01FFh or 0200h.

Note: SMI reads from unused register addresses return all zeros. This differs from unused PHY registers which leave MDIO un-driven.

10.2.1.1 SMI Read Polling for Reset Complete

During reset, the SMI slave interface will not return valid data. To determine when the reset condition is complete, the Byte Order Test Register (BYTE_TEST) should be polled. Once the correct pattern is read, the interface can be considered functional. At this point, the Device Ready (READY) bit in the Hardware Configuration Register (HW_CFG) can be polled to determine when the device initialization is complete. Refer to Section 4.2, "Resets," on page 48 for additional information.

Note: In the event that a reset condition terminates between halves of 16-bit read pair, the device will not expect another 16-bit read to complete the DWORD cycle. Only specific registers may be read during a reset. Refer to Section 4.2, "Resets," on page 48 for additional information.

10.2.2 Write Sequence

In a write sequence, the host sends the 32-bit preamble, 2-bit start of frame, 2-bit op-code, 5-bit PHY Address, 5-bit Register Address, 2-bit turn-around time, and finally the 16-bits of data. The MDIO pin is three-stated throughout the write sequence.

The host processor is required to perform two contiguous 16-bit writes to complete a single DWORD transfer. No ordering requirement exists. The host may access either the low or high word first, as long as the next write is performed to the opposite word. If a write to the same word is performed, the device disregards the transfer.

Note: SMI writes must not be performed to unused register addresses.

10.3 PHY Management Interface (PMI)

The PHY Management Interface (PMI) is used to access the internal PHYs as well as the external PHY on the MII pins (in MAC modes only). The PMI operates at 2.5MHz, and implements the IEEE 802.3 management protocol, providing read/write commands for PHY configuration.

A read or write is performed using the frame format shown in Table 10.2. All addresses and data are transferred msb first. Data bytes are transferred little endian.

Table 10.2 MII Management Frame Format

	PREAMBLE	START	OP CODE	PHY ADDRESS	REGISTER ADDRESS	TURN-AROUND TIME Note 10.4	DATA	IDLE Note 10.5
READ	32 1's	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
WRITE	32 1's	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

Note 10.4 The turn-around time (TA) is used to avoid bus contention during a read cycle. For a read, the external PHY drives the second bit of the turn-around time to 0, and then drives the msb of the read data in the following cycle. For a write, the device drives the first bit of the turnaround time to 1, the second bit of the turnaround time to 0, and then the msb of the write data in the following clock cycle.

Note 10.5 In the IDLE condition, the MDIO output is three-stated and pulled high externally.

The internal PHYs and optional external PHY (in MAC modes) are accessed via the PHY Management Interface Access Register (PMI_ACCESS) and PHY Management Interface Data Register (PMI_DATA). These registers allow read and write operations to all PHY registers. Refer to Section 13.2.5, "PHY Management Interface (PMI)," on page 179 for detailed information on these registers.

10.3.1 EEPROM Loader PHY Register Access

The PMI is also used by the EEPROM Loader to load the PHY registers with various configuration strap values. The PHY Management Interface Access Register (PMI_ACCESS) and PHY Management Interface Data Register (PMI_DATA) are also accessible as part of the Register Data burst sequence of the EEPROM Loader. Refer to Section 8.4, "EEPROM Loader," on page 121 for additional information.

10.4 MII Mode Multiplexer

The MII mode multiplexer is used to direct the MII data/management path connections. One master (MAC via the MII pins, or PMI) is connected to the slaves (PHY via MII pins, Port 1/2 PHYs, Virtual PHY, and SMI slave) dependant on the selected management mode of the device. The MII mode multiplexer also performs the multiplexing of the read data signals from the slaves and controls the output enable of the MII pins.

The following sections detail the operation of the MII mode multiplexer in each management mode. A list of management modes and their configuration settings are discussed in Section 2.3, "Modes of Operation," on page 19.

10.4.1 Port 0 MAC Mode SMI Managed

In Port 0 MAC mode SMI managed, the internal PHYs and SMI slave block are accessed via the MII management pins. The Virtual PHY and PMI are not used in this mode.

The Virtual PHY interface is accessible via the SMI slave or the EEPROM Loader. Refer to Section 10.2, "SMI Slave Controller," on page 135 and Section 8.4, "EEPROM Loader," on page 121 for additional information.

Figure 10.1 details the MII multiplexer management path connections for this mode.

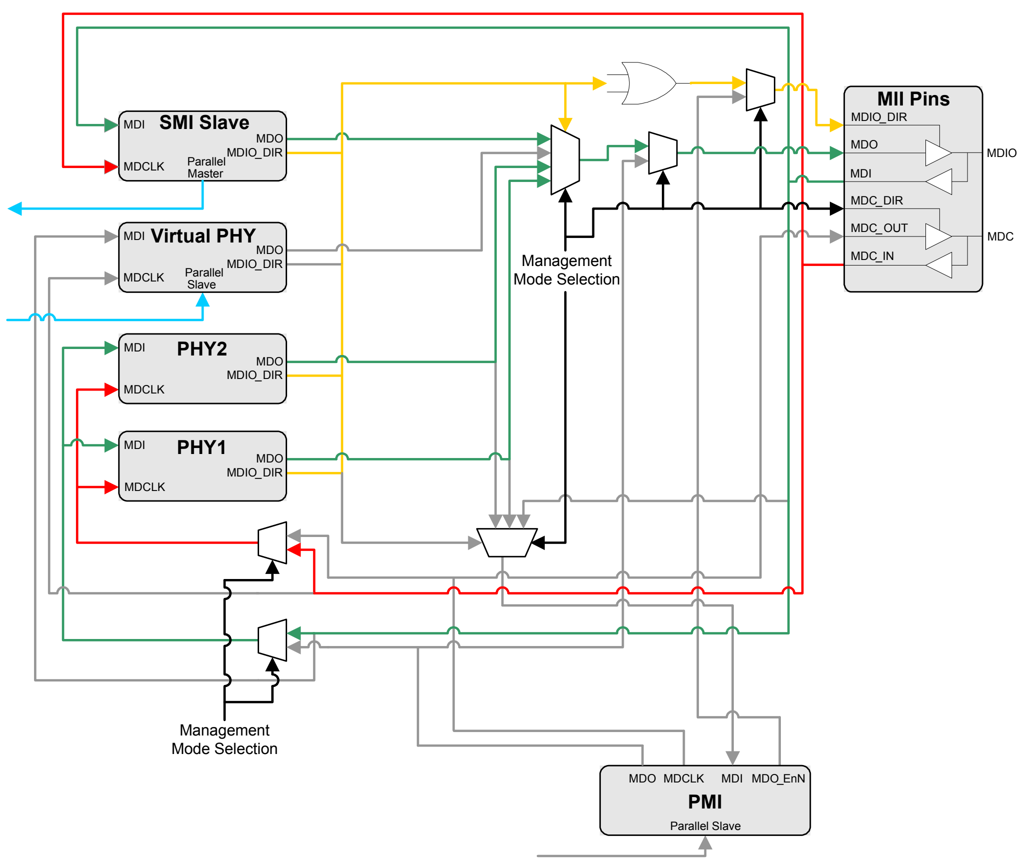


Figure 10.1 MII Mux Management Path Connections - MAC Mode SMI Managed

10.4.2 Port 0 MAC Mode I²C Managed

In MAC mode I²C managed, the internal PHYs and the external PHY are accessed via the PMI. The SMI slave and the Virtual PHY are not used in this mode.

The Virtual PHY and PMI interfaces are accessible via the I²C slave interface or the EEPROM Loader. Refer to Section 8.4, "EEPROM Loader," on page 121 for additional information.

Figure 10.2 details the MII multiplexer management path connections for this mode.

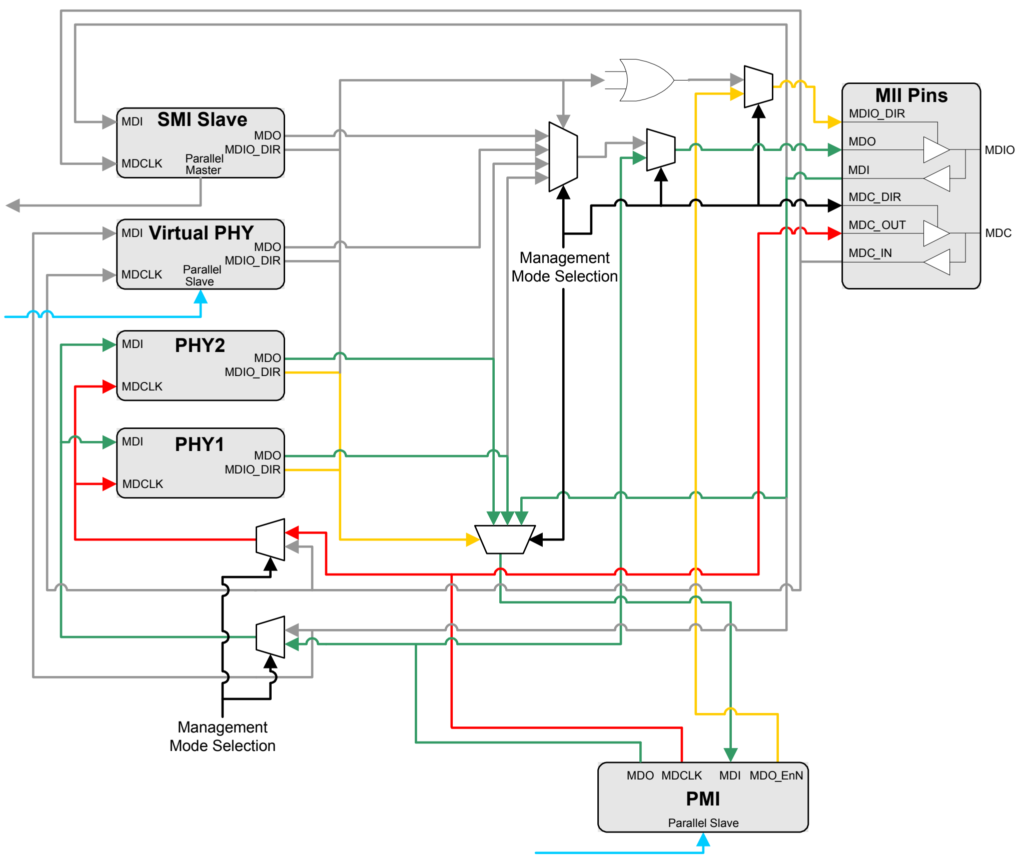


Figure 10.2 MII Mux Management Path Connections - MAC Mode I²C Managed

10.4.3 Port 0 PHY Mode SMI Managed

In PHY mode SMI managed, the internal PHYs, Virtual PHY, and SMI slave block are accessed via the MII management pins. The PMI is not used in this mode.

The Virtual PHY interface is accessible via the SMI slave or the EEPROM Loader. Refer to Section 10.2, "SMI Slave Controller," on page 135 and Section 8.4, "EEPROM Loader," on page 121 for additional information.

Figure 10.1 details the MII multiplexer management path connections for this mode.

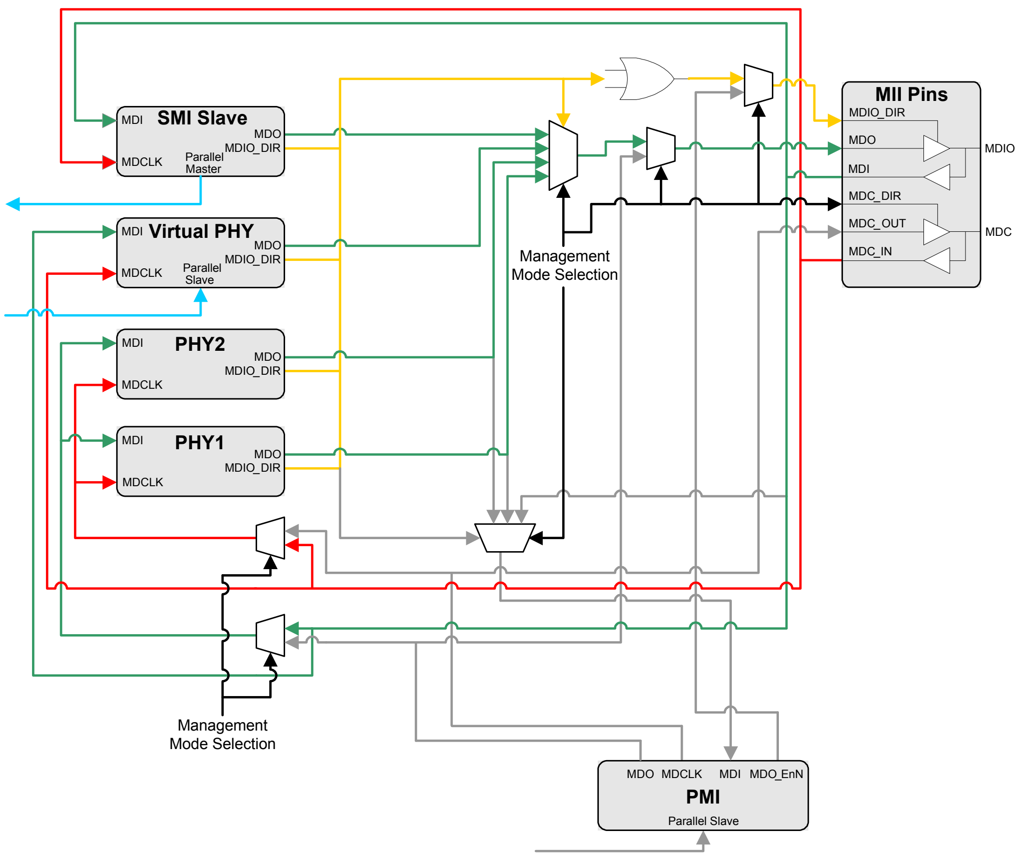


Figure 10.3 MII Mux Management Path Connections - PHY Mode SMI Managed

10.4.4 Port 0 PHY Mode I^{2}C Managed

In PHY mode I^{2}C managed, the Port 1/2 PHYs are accessed via the PMI, and the Virtual PHY is accessed via the external MII management pins. The SMI slave is not used in this mode.

The Virtual PHY and PMI parallel interfaces are accessible via the I^{2}C slave interface or the EEPROM Loader. Refer to Section 8.4, "EEPROM Loader," on page 121 for additional information.

Figure 10.2 details the MII multiplexer management path connections for this mode.

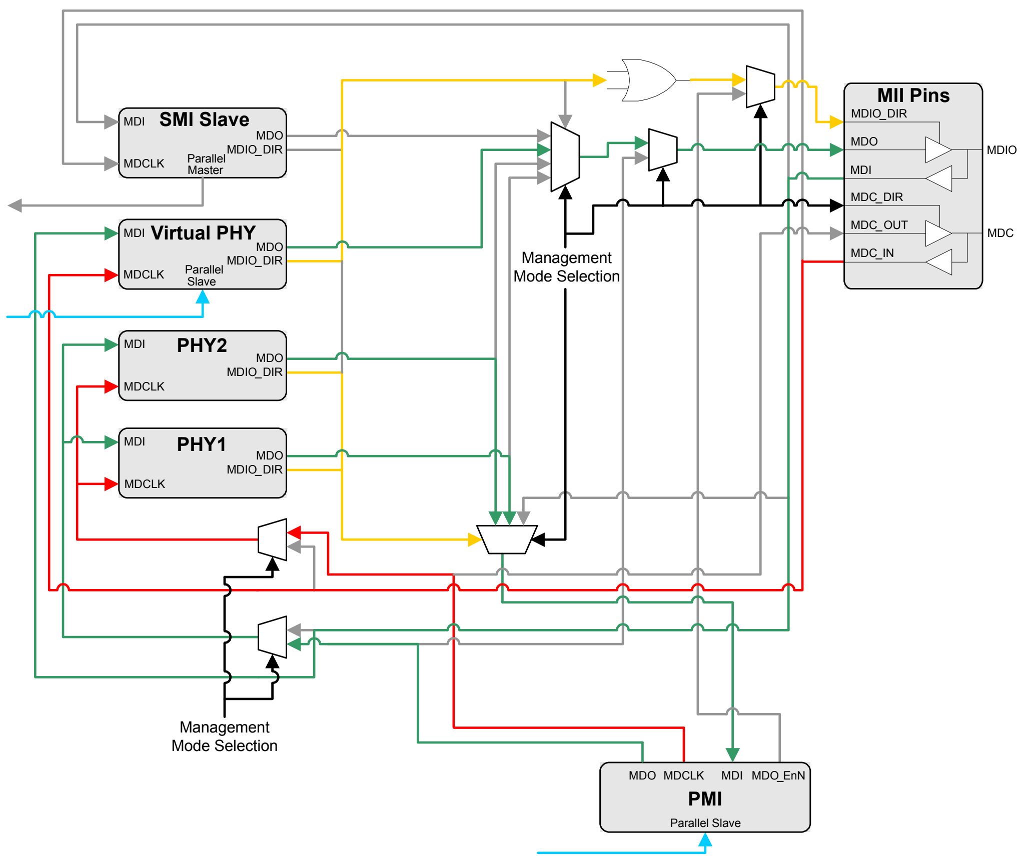


Figure 10.4 MII Mux Management Path Connections - PHY Mode I^{2}C Managed

Chapter 11 General Purpose Timer & Free-Running Clock

This chapter details the General Purpose Timer (GPT) and the Free-Running Clock.

11.1 General Purpose Timer

The device provides a 16-bit programmable General Purpose Timer that can be used to generate periodic system interrupts. The resolution of this timer is 100uS.

The GPT loads the General Purpose Timer Count Register (GPT_CNT) with the value in the General Purpose Timer Pre-Load (GPT_LOAD) field of the General Purpose Timer Configuration Register (GPT_CFG) when the General Purpose Timer Enable (TIMER_EN) bit of the General Purpose Timer Configuration Register (GPT_CFG) is asserted (1). On a chip-level reset, or when the General Purpose Timer Enable (TIMER_EN) bit changes from asserted (1) to de-asserted (0), the General Purpose Timer Pre-Load (GPT_LOAD) field is initialized to FFFFh. The General Purpose Timer Count Register (GPT_CNT) is also initialized to FFFFh on reset. Software can write a pre-load value into the General Purpose Timer Pre-Load (GPT_LOAD) field at any time (e.g. before or after the General Purpose Timer Enable (TIMER_EN) bit is asserted).

Once enabled, the GPT counts down until it reaches 0000h, or until a new pre-load value is written to the General Purpose Timer Pre-Load (GPT_LOAD) field. At 0000h, the counter wraps around to FFFFh, asserts the GP Timer (GPT_INT) interrupt status bit in the Interrupt Status Register (INT_STS), asserts the IRQ interrupt (if GP Timer Interrupt Enable (GPT_INT_EN) is set in the Interrupt Status Register (INT_STS)), and continues counting. GP Timer (GPT_INT) is a sticky bit. Once this bit is asserted, it can only be cleared by writing a 1 to the bit. Refer to Section 5.2.4, "General Purpose Timer Interrupt," on page 65 for additional information on the GPT interrupt.

11.2 Free-Running Clock

The Free-Running Clock (FRC) is a simple 32-bit up-counter that operates from a fixed 25MHz clock. The current FRC value can be read via the Free Running 25MHz Counter Register (FREE_RUN). On assertion of a chip-level reset, this counter is cleared to zero. On de-assertion of a reset, the counter is incremented once for every 25MHz clock cycle. When the maximum count has been reached, the counter rolls over to zeros. The FRC does not generate interrupts.

Note: The free running counter can take up to 160nS to clear after a reset event.

Chapter 12 GPIO/LED Controller

12.1 Functional Overview

The GPIO/LED Controller provides 6 configurable general purpose input/output pins, GPIO[5:0]. These pins can be individually configured to function as inputs, push-pull outputs, or open drain outputs and each is capable of interrupt generation with configurable polarity. Alternatively, all 6 GPIO pins can be configured as LED outputs, enabling these pins to drive Ethernet status LEDs for external indication of various attributes of the switch ports.

GPIO and LED functionality is configured via the GPIO/LED System Control and Status Registers (CSRs). These registers are defined in Section 13.2.2, "GPIO/LED," on page 156.

12.2 GPIO Operation

The GPIO controller is comprised of 6 programmable input/output pins. These pins are individually configurable via the GPIO CSRs. On application of a chip-level reset:

- All GPIOs are set as inputs (GPIO Direction 5-0 (GPDIR[5:0]) cleared in General Purpose I/O Data & Direction Register (GPIO_DATA_DIR))
- All GPIO interrupts are disabled (GPIO Interrupt Enable[5:0] (GPIO[5:0]_INT_EN) cleared in General Purpose I/O Interrupt Status and Enable Register (GPIO_INT_STS_EN)
- All GPIO interrupts are configured to low logic level triggering (GPIO Interrupt Polarity 5-0 (GPIO_INT_POL[5:0]) cleared in General Purpose I/O Configuration Register (GPIO_CFG))

Note: GPIO[5:0] may be configured as LED outputs by default, dependant on the LED_en_strap[5:0] configuration straps. Refer to Section 12.3, "LED Operation" for additional information.

The direction and buffer type of all 6 GPIOs are configured via the General Purpose I/O Configuration Register (GPIO_CFG) and General Purpose I/O Data & Direction Register (GPIO_DATA_DIR). The direction of each GPIO, input or output, should be configured first via its respective GPIO Direction 5-0 (GPDIR[5:0]) bit in the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR). When configured as an output, the output buffer type for each GPIO is selected by the GPIO Buffer Type 5-0 (GPIOBUF[5:0]) bits in the General Purpose I/O Configuration Register (GPIO_CFG). Push/pull and open-drain output buffers are supported for each GPIO. When functioning as an open-drain driver, the GPIO output pin is driven low when the corresponding GPIO Data 5-0 (GPIOD[5:0]) bit in the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR) is cleared to 0, and is not driven when set to 1.

When a GPIO is enabled as a push/pull output, the value output to the GPIO pin is set via the corresponding GPIO Data 5-0 (GPIOD[5:0]) bit in the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR). For GPIOs configured as inputs, the corresponding GPIO Data 5-0 (GPIOD[5:0]) bit reflects the current state of the GPIO input.

12.2.1 GPIO Interrupts

Each GPIO provides the ability to trigger a unique GPIO interrupt in the General Purpose I/O Interrupt Status and Enable Register (GPIO_INT_STS_EN). Reading the GPIO Interrupt[5:0] (GPIO[5:0]_INT) bits of this register provides the current status of the corresponding interrupt, and each interrupt is enabled by setting the corresponding GPIO Interrupt Enable[5:0] (GPIO[5:0]_INT_EN) bit. The GPIO/LED Controller aggregates the enabled interrupt values into an internal signal that is sent to the System Interrupt Controller and is reflected via the Interrupt Status Register (INT_STS) GPIO Interrupt Event (GPIO) bit. For more information on interrupts, refer to Chapter 5, "System Interrupts," on page 62.

12.2.1.1 GPIO Interrupt Polarity

The interrupt polarity can be set for each individual GPIO via the GPIO Interrupt Polarity 5-0 (GPIO_INT_POL[5:0]) bits in the General Purpose I/O Configuration Register (GPIO_CFG). When set, a high logic level on the GPIO pin will set the corresponding interrupt bit in the General Purpose I/O Interrupt Status and Enable Register (GPIO_INT_STS_EN). When cleared, a low logic level on the GPIO pin will set the corresponding interrupt bit.

12.3 LED Operation

Each GPIO can be individually selected to function as a LED. These pins are configured as LED outputs by setting the corresponding LED Enable 5-0 (LED_EN[5:0]) bit in the LED Configuration Register (LED_CFG). When configured as a LED, the pin is either a push-pull or open-drain / open-source output and the GPIO related input buffer and pull-up are disabled. The default configuration, including polarity, is determined by input straps or EEPROM entries. Refer to Configuration Straps on page 52 for additional information.

The functions associated with each LED pin are configurable via the LED Function 1-0 (LED_FUN[1:0]) bits of the LED Configuration Register (LED_CFG). These bits allow the configuration of each LED pin to indicate various port related functions. These functions are described in Table 12.1, followed by a detailed definition of each indication type.

The default values of the LED Function 1-0 (LED_FUN[1:0]) and LED Enable 5-0 (LED_EN[5:0]) bits of the LED Configuration Register (LED_CFG) are determined by the LED_fun_strap[1:0] and LED_en_strap[5:0] configuration straps. For more information on the LED Configuration Register (LED_CFG) and its related straps, refer to Section 13.2.2.4, "LED Configuration Register (LED_CFG)," on page 159.

Table 12.1 LED Operation as a Function of LED_FUN[1:0]

	00b	01b	10b	11b
LED5 (GPIO5)	Link / Activity Port 2	100Link / Activity Port 2	TX Port 0	TX_EN Port 0
LED4 (GPIO4)	Full-duplex / Collision Port 2	Full-duplex / Collision Port 2	Link / Activity Port 2	TX_EN Port 2
LED3 (GPIO3)	Speed Port 2	10Link / Activity Port 2	Speed Port 2	RX_DV Port 2
LED2 (GPIO2)	Link / Activity Port 1 (if Port 1 internal PHY enabled) Activity Port 1 (if Port 1 internal PHY disabled)	100Link / Activity Port 1 (if Port 1 internal PHY enabled) Activity Port 1 (if Port 1 internal PHY disabled)	RX Port 0	RX_DV Port 0

Table 12.1 LED Operation as a Function of LED_FUN[1:0] (continued)

	00b	**01b**	**10b**	**11b**
LED1 (GPIO1)	Full-duplex / Collision Port 1 (if Port 1 internal PHY enabled) Inactive (if Port 1 internal PHY disabled)	Full-duplex / Collision Port 1 (if Port 1 internal PHY enabled) Inactive (if Port 1 internal PHY disabled)	Link / Activity Port 1 (if Port 1 internal PHY enabled) TX Port 1 (if Port 1 internal PHY disabled)	TX_EN Port 1
LED0 (GPIO0)	Speed Port 1 (if Port 1 internal PHY enabled) Activity Port 0 (if Port 1 internal PHY disabled)	10Link / Activity Port 1 (if Port 1 internal PHY enabled) Activity Port 0 (if Port 1 internal PHY disabled)	Speed Port 1 (if Port 1 internal PHY enabled) RX Port 1 (if Port 1 internal PHY disabled)	RX_DV Port 1

The various LED indication functions shown in Table 12.1 are described in the following sections.

12.3.1 LED Function Definitions when LED_FUN[1:0] = 00b, 01b, or 10b

When LED Function 1-0 (LED_FUN[1:0]) is 00b, 01b, or 10b, the following LED rules apply:

- "Active" is defined as the pin being driven to the opposite value latched at reset on the led_pol_strap[5:0] LED polarity hard-straps. LED polarity is determined by these hard-straps as detailed in Section 4.2.4, "Configuration Straps," on page 52. The LED polarity cannot be modified via soft-straps.
- "Inactive" is defined as the pin not being driven.
- The input buffers and pull-ups are disabled on the shared GPIO/LED pins.

When LED Function 1-0 (LED_FUN[1:0]) is 00b, 01b, or 10b, the following LED function definitions apply:

- **TX Port 0/1 -** The signal is pulsed active for 80mS to indicate activity from the Switch Fabric to the external MII pins. This signal is then made inactive for a minimum of 80mS, after which the process will repeat if TX activity is again detected.
  Note: Link indication does not affect this function.
- **RX Port 0/1 -** The signal is pulsed active for 80mS to indicate activity from the external MII pins to the Switch Fabric. This signal is then made inactive for a minimum of 80mS, after which the process will repeat if RX activity is again detected.
  Note: Link indication does not affect this function.
- **Activity Port 0/1 -** The signal is pulsed active for 80mS to indicate transmit or receive activity on the port. The signal is then made inactive for a minimum of 80mS, after which the process will repeat if RX or TX activity is again detected.
  Note: The idle condition is *inactive* in contrast to that of the Link / Activity function.
  Note: Link indication does not affect this function.

- **Link / Activity Port 1/2 -** A steady active output indicates that the port has a valid link, while a steady inactive output indicates no link on the port. The signal is pulsed inactive for 80mS to indicate transmit or receive activity on the port. The signal is then made active for a minimum of 80mS, after which the process will repeat if RX or TX activity is again detected.
- **Full-duplex / Collision Port 1/2 -** A steady active output indicates the port is in full-duplex mode. In half-duplex mode, the signal is pulsed active for 80mS to indicate a network collision. The signal is then made inactive for a minimum of 80mS, after which the process will repeat if another collision is detected. The signal will be held inactive if the port does not have a valid link.
- **Speed Port 1/2 -** A steady active output indicates a valid link with a speed of 100Mbps. A steady inactive output indicates a speed of 10Mbps. The signal will be held inactive if the port does not have a valid link.
- **100Link / Activity Port 1/2 -** A steady active output indicates the port has a valid link and the speed is 100Mbps. The signal is pulsed inactive for 80mS to indicate TX or RX activity on the port. The signal is then driven active for a minimum of 80mS, after which the process will repeat if RX or TX activity is again detected. The signal will be held inactive if the port does not have a valid link or the speed is not 100Mbps.
- **10Link / Activity Port 1/2 -** A steady active output indicates the port has a valid link and the speed is 10Mbps. The signal is pulsed inactive for 80mS to indicate transmit or receive activity on the port. The signal is then driven active for a minimum of 80mS, after which the process will repeat if RX or TX activity is again detected. This signal will be held inactive if the port does not have a valid link or the speed is not 10Mbps.

12.3.2 LED Function Definitions when LED_FUN[1:0] = 11b

When LED Function 1-0 (LED_FUN[1:0]) is 11b, the following LED rules apply:

- The LED pins are push-pull drivers.
- The LED polarity does not depend upon the led_pol_strap[5:0] LED polarity hard-straps. The LED pin is driven high when the function signal is high, and is driven low when the function signal is low.
- The input buffers and pull-ups are disabled on the shared GPIO/LED pins.

When LED Function 1-0 (LED_FUN[1:0]) is 11b, the following LED function definitions apply:

- **TX_EN Port 0 -** Non-stretched TX_EN signal from the Switch Fabric to the external MII pins.
  Note: Link indication does not affect this function.
- **RX_DV Port 0 -** Non-stretched RX_DV signal from the external MII pins to the Switch Fabric.
  Note: Link indication does not affect this function.
- **TX_EN Port 1 -** Non-stretched TX_EN signal from the Switch Fabric to the PHY or external MII pins.
  Note: Link indication does not affect this function.
- **RX_DV Port 1 -** Non-stretched RX_DV signal from the PHY or external MII pins to the Switch Fabric.
  Note: Link indication does not affect this function.
- **TX_EN Port 2 -** Non-stretched TX_EN signal from the Switch Fabric to the PHY.
  Note: Link indication does not affect this function.
- **RX_DV Port 2 -** Non-stretched RX_DV signal from the PHY to the Switch Fabric.
  Note: Link indication does not affect this function.

Chapter 13 Register Descriptions

This section describes the various control and status registers (CSR's). These registers are broken into 3 categories. The following sections detail the functionality and accessibility of all the registers within each category:

- Section 13.2, "System Control and Status Registers," on page 150
- Section 13.3, "Ethernet PHY Control and Status Registers," on page 206
- Section 13.4, "Switch Fabric Control and Status Registers," on page 228

Figure 13.1 contains an overall base register memory map of the device. This memory map is not drawn to scale, and should be used for general reference only.

Note: Not all registers are memory mapped or directly addressable. For details on the accessibility of the various registers, refer the register sub-sections listed above.

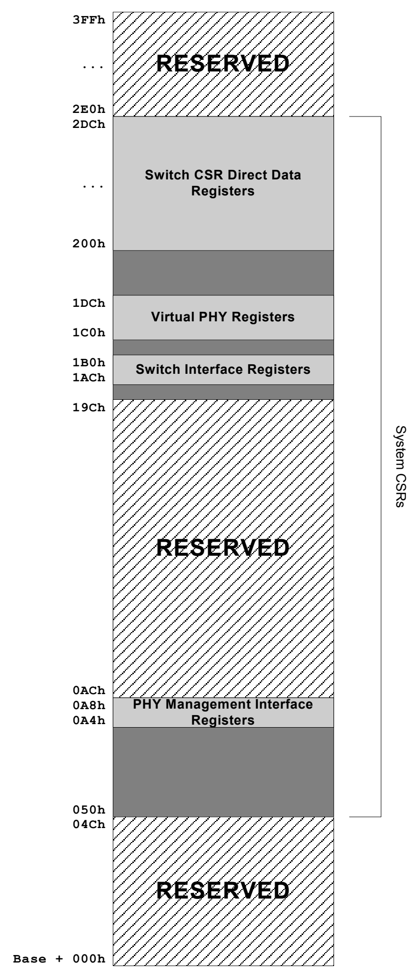


Figure 13.1 Base Register Memory Map

13.1 Register Nomenclature

Table 13.1 describes the register bit attribute notation used throughout this document.

Table 13.1 Register Bit Types

REGISTER BIT TYPE NOTATION	REGISTER BIT DESCRIPTION
R	**Read:** A register or bit with this attribute can be read.
W	**Read:** A register or bit with this attribute can be written.
RO	**Read only:** Read only. Writes have no effect.
WO	**Write only:** If a register or bit is write-only, reads will return unspecified data.
WC	**Write One to Clear:** writing a one clears the value. Writing a zero has no effect
WAC	**Write Anything to Clear:** writing anything clears the value.
RC	**Read to Clear:** Contents is cleared after the read. Writes have no effect.
LL	**Latch Low:** Clear on read of register.
LH	**Latch High:** Clear on read of register.
SC	**Self-Clearing:** Contents are self-cleared after the being set. Writes of zero have no effect. Contents can be read.
SS	**Self-Setting:** Contents are self-setting after being cleared. Writes of one have no effect. Contents can be read.
RO/LH	**Read Only, Latch High:** Bits with this attribute will stay high until the bit is read. After it is read, the bit will either remain high if the high condition remains, or will go low if the high condition has been removed. If the bit has not been read, the bit will remain high regardless of a change to the high condition. This mode is used in some Ethernet PHY registers.
NASR	**Not Affected by Software Reset.** The state of NASR bits do not change on assertion of a software reset.
RESERVED	**Reserved Field:** Reserved fields must be written with zeros to ensure future compatibility. The value of reserved bits is not guaranteed on a read.

Many of these register bit notations can be combined. Some examples of this are shown below:

- **R/W:** Can be written. Will return current setting on a read.
- **R/WAC:** Will return current setting on a read. Writing anything clears the bit.

13.2 System Control and Status Registers

The System CSR's are directly addressable memory mapped registers with a base address offset range of 050h to 2DCh. These registers are accessed through the I^{2}C serial interface or the MIIM/SMI serial interface. For more information on the various modes and their corresponding address configurations, see Section 2.3, "Modes of Operation," on page 19.

Table 13.2 lists the System CSR's and their corresponding addresses in order. All system CSR's are reset to their default value on the assertion of a chip-level reset.

The System CSR's can be divided into 7 sub-categories. Each of these sub-categories contains the System CSR descriptions of the associated registers. The register descriptions are categorized as follows:

- Section 13.2.1, "Interrupts," on page 152
- Section 13.2.2, "GPIO/LED," on page 156
- Section 13.2.3, "EEPROM," on page 160
- Section 13.2.4, "Switch Fabric," on page 164
- Section 13.2.5, "PHY Management Interface (PMI)," on page 179
- Section 13.2.6, "Virtual PHY," on page 181
- Section 13.2.7, "Miscellaneous," on page 196

Table 13.2 System Control and Status Registers

ADDRESS OFFSET	SYMBOL	REGISTER NAME
000h - 04Ch	RESERVED	Reserved for Future Use
050h	ID_REV	Chip ID and Revision Register, Section 13.2.7.1
054h	IRQ_CFG	Interrupt Configuration Register, Section 13.2.1.1
058h	INT_STS	Interrupt Status Register, Section 13.2.1.2
05Ch	INT_EN	Interrupt Enable Register, Section 13.2.1.3
060h	RESERVED	Reserved for Future Use
064h	BYTE_TEST	Byte Order Test Register, Section 13.2.7.2
068h - 070h	RESERVED	Reserved for Future Use
074h	HW_CFG	Hardware Configuration Register, Section 13.2.7.3
078h - 088h	RESERVED	Reserved for Future Use
08Ch	GPT_CFG	General Purpose Timer Configuration Register, Section 13.2.7.4
090h	GPT_CNT	General Purpose Timer Count Register, Section 13.2.7.5
094h - 098h	RESERVED	Reserved for Future Use
09Ch	FREE_RUN	Free Running Counter Register, Section 13.2.7.6
0A0h	RESERVED	Reserved for Future Use
0A4h	PMI_DATA	PHY Management Interface Data Register, Section 13.2.5.1
0A8h	PMI_ACCESS	PHY Management Interface Access Register, Section 13.2.5.2

Table 13.2 System Control and Status Registers (continued)

ADDRESS OFFSET	SYMBOL	REGISTER NAME
0ACh - 19Ch	RESERVED	Reserved for Future Use
1A0h	MANUAL_FC_1	Port 1 Manual Flow Control Register, Section 13.2.4.1
1A4h	MANUAL_FC_2	Port 2 Manual Flow Control Register, Section 13.2.4.2
1A8h	MANUAL_FC_0	Port 0 Manual Flow Control Register, Section 13.2.4.3
1ACh	SWITCH_CSR_DATA	Switch Fabric CSR Interface Data Register, Section 13.2.4.4
1B0h	SWITCH_CSR_CMD	Switch Fabric CSR Interface Command Register, Section 13.2.4.5
1B4h	E2P_CMD	EEPROM Command Register, Section 13.2.3.1
1B8h	E2P_DATA	EEPROM Data Register, Section 13.2.3.2
1BCh	LED_CFG	LED Configuration Register, Section 13.2.2.4
1C0h	VPHY_BASIC_CTRL	Virtual PHY Basic Control Register, Section 13.2.6.1
1C4h	VPHY_BASIC_STATUS	Virtual PHY Basic Status Register, Section 13.2.6.2
1C8h	VPHY_ID_MSB	Virtual PHY Identification MSB Register, Section 13.2.6.3
1CCh	VPHY_ID_LSB	Virtual PHY Identification LSB Register, Section 13.2.6.4
1D0h	VPHY_AN_ADV	Virtual PHY Auto-Negotiation Advertisement Register, Section 13.2.6.5
1D4h	VPHY_AN_LP_BASE_ABILITY	Virtual PHY Auto-Negotiation Link Partner Base Page Ability Register, Section 13.2.6.6
1D8h	VPHY_AN_EXP	Virtual PHY Auto-Negotiation Expansion Register, Section 13.2.6.7
1DCh	VPHY_SPECIAL_CONTROL_STATUS	Virtual PHY Special Control/Status Register, Section 13.2.6.8
1E0h	GPIO_CFG	General Purpose I/O Configuration Register, Section 13.2.2.1
1E4h	GPIO_DATA_DIR	General Purpose I/O Data & Direction Register, Section 13.2.2.2
1E8h	GPIO_INT_STS_EN	General Purpose I/O Interrupt Status and Enable Register, Section 13.2.2.3
1ECh	P1_MII_BASIC_CONTROL	Port 1 MII Basic Control Register, Section 13.2.7.7
1F0h	SWITCH_MAC_ADDRH	Switch MAC Address High Register, Section 13.2.4.6
1F4h	SWITCH_MAC_ADDRL	Switch MAC Address Low Register, Section 13.2.4.7
1F8h	RESET_CTL	Reset Control Register, Section 13.2.7.8
1FCh	RESERVED	Reserved for Future Use
200h-2DCh	SWITCH_CSR_DIRECT_DATA	Switch Engine CSR Interface Direct Data Register, Section 13.2.4.8
2E0h-3FFh	RESERVED	Reserved for Future Use

13.2.1 Interrupts

This section details the interrupt related System CSR's. These registers control, configure, and monitor the IRQ interrupt output pin and the various interrupt sources. For more information on interrupts, refer to Chapter 5, "System Interrupts," on page 62.

13.2.1.1 Interrupt Configuration Register (IRQ_CFG)

Offset:	054h	Size:	32 bits

This read/write register configures and indicates the state of the IRQ signal.

BITS	DESCRIPTION	TYPE	DEFAULT
31:24	**Interrupt De-assertion Interval (INT_DEAS)** This field determines the Interrupt Request De-assertion Interval in multiples of 10 microseconds. Setting this field to zero causes the device to disable the INT_DEAS Interval, reset the interval counter and issue any pending interrupts. If a new, non-zero value is written to this field, any subsequent interrupts will obey the new setting.	R/W	00h
23:15	**RESERVED**	RO	-
14	**Interrupt De-assertion Interval Clear (INT_DEAS_CLR)** Writing a 1 to this register clears the de-assertion counter in the Interrupt Controller, thus causing a new de-assertion interval to begin (regardless of whether or not the Interrupt Controller is currently in an active de-assertion interval). **0: Normal operation** **1: Clear de-assertion counter**	R/W SC	0h
13	**Interrupt De-assertion Status (INT_DEAS_STS)** When set, this bit indicates that interrupts are currently in a de-assertion interval, and will not be sent to the IRQ pin. When this bit is clear, interrupts are not currently in a de-assertion interval, and will be sent to the IRQ pin. **0: No interrupts in de-assertion interval** **1: Interrupts in de-assertion interval**	RO SC	0b
12	**Master Interrupt (IRQ_INT)** This read-only bit indicates the state of the internal IRQ line, regardless of the setting of the IRQ_EN bit, or the state of the interrupt de-assertion function. When this bit is set, one of the enabled interrupts is currently active. **0: No enabled interrupts active** **1: One or more enabled interrupts active**	RO	0b
11:9	**RESERVED**	RO	-
8	**IRQ Enable (IRQ_EN)** This bit controls the final interrupt output to the IRQ pin. When clear, the IRQ output is disabled and permanently de-asserted. This bit has no effect on any internal interrupt status bits. **0: Disable output on IRQ pin** **1: Enable output on IRQ pin**	R/W	0b
7:5	**RESERVED**	RO	-

BITS	DESCRIPTION	TYPE	DEFAULT
4	**IRQ Polarity (IRQ_POL)** When cleared, this bit enables the IRQ line to function as an active low output. When set, the IRQ output is active high. When the IRQ is configured as an open-drain output (via the IRQ_TYPE bit), this bit is ignored, and the interrupt is always active low. **0: IRQ active low output** **1: IRQ active high output**	R/W NASR Note 13.1	0b
3:1	**RESERVED**	RO	-
0	**IRQ Buffer Type (IRQ_TYPE)** When this bit is cleared, the IRQ pin functions as an open-drain output for use in a wired-or interrupt configuration. When set, the IRQ is a push-pull driver. **Note:** When configured as an open-drain output, the IRQ_POL bit is ignored and the interrupt output is always active low. **0: IRQ pin open-drain output** **1: IRQ pin push-pull driver**	R/W NASR Note 13.1	0b

Note 13.1 Register bits designated as NASR are not reset when the Digital Reset (DIGITAL_RST) bit in the Reset Control Register (RESET_CTL) is set.

13.2.1.2 Interrupt Status Register (INT_STS)

Offset:	058h	Size:	32 bits

This register contains the current status of the generated interrupts. A value of 1 indicates the corresponding interrupt conditions have been met, while a value of 0 indicates the interrupt conditions have not been met. The bits of this register reflect the status of the interrupt source regardless of whether the source has been enabled as an interrupt in the Interrupt Enable Register (INT_EN). Where indicated as R/WC, writing a 1 to the corresponding bits acknowledges and clears the interrupt.

BITS	DESCRIPTION	TYPE	DEFAULT
31	**Software Interrupt (SW_INT)** This interrupt is generated when the Software Interrupt Enable (SW_INT_EN) bit of the Interrupt Enable Register (INT_EN) is set high. Writing a one clears this interrupt.	R/WC	0b
30	**Device Ready (READY)** This interrupt indicates that the device is ready to be accessed after a power-up or reset condition.	R/WC	0b
29	**RESERVED**	RO	-
28	**Switch Fabric Interrupt Event (SWITCH_INT)** This bit indicates an interrupt event from the Switch Fabric. This bit should be used in conjunction with the Switch Global Interrupt Pending Register (SW_IPR) to determine the source of the interrupt event within the Switch Fabric.	RO	0b
27	**Port 2 PHY Interrupt Event (PHY_INT2)** This bit indicates an interrupt event from the Port 2 PHY. The source of the interrupt can be determined by polling the Port x PHY Interrupt Source Flags Register (PHY_INTERRUPT_SOURCE_x).	RO	0b
26	**Port 1 PHY Interrupt Event (PHY_INT1)** This bit indicates an interrupt event from the Port 1 PHY. The source of the interrupt can be determined by polling the Port x PHY Interrupt Source Flags Register (PHY_INTERRUPT_SOURCE_x).	RO	0b
25:20	**RESERVED**	RO	-
19	**GP Timer (GPT_INT)** This interrupt is issued when the General Purpose Timer Count Register (GPT_CNT) wraps past zero to FFFFh.	R/WC	0b
18:13	**RESERVED**	RO	-
12	**GPIO Interrupt Event (GPIO)** This bit indicates an interrupt event from the General Purpose I/O. The source of the interrupt can be determined by polling the General Purpose I/O Interrupt Status and Enable Register (GPIO_INT_STS_EN)	RO	0b
11:0	**RESERVED**	RO	-

13.2.1.3 Interrupt Enable Register (INT_EN)

Offset:	05Ch	Size:	32 bits

This register contains the interrupt enables for the IRQ output pin. Writing 1 to any of the bits enables the corresponding interrupt as a source for IRQ. Bits in the Interrupt Status Register (INT_STS) register will still reflect the status of the interrupt source regardless of whether the source is enabled as an interrupt in this register (with the exception of Software Interrupt Enable (SW_INT_EN)). For descriptions of each interrupt, refer to the Interrupt Status Register (INT_STS) bits, which mimic the layout of this register.

BITS	DESCRIPTION	TYPE	DEFAULT
31	**Software Interrupt Enable (SW_INT_EN)**	R/W	0b
30	**Device Ready Enable (READY_EN)**	R/W	0b
29	**RESERVED**	RO	-
28	**Switch Fabric Interrupt Event Enable (SWITCH_INT_EN)**	R/W	0b
27	**Port 2 PHY Interrupt Event Enable (PHY_INT2_EN)**	R/W	0b
26	**Port 1 PHY Interrupt Event Enable (PHY_INT1_EN)**	R/W	0b
25:20	**RESERVED**	RO	-
19	**GP Timer Interrupt Enable (GPT_INT_EN)**	R/W	0b
18:13	**RESERVED**	RO	-
12	**GPIO Interrupt Event Enable (GPIO_EN)**	R/W	0b
11:0	**RESERVED**	RO	-

13.2.2 GPIO/LED

This section details the General Purpose I/O (GPIO) and LED related System CSR's.

13.2.2.1 General Purpose I/O Configuration Register (GPIO_CFG)

Offset:	1E0h	Size:	32 bits

This read/write register configures the GPIO input and output pins. The polarity of the GPIO pins is configured here.

BITS	DESCRIPTION	TYPE	DEFAULT
31:22	**RESERVED**	RO	-
21:16	**GPIO Interrupt Polarity 5-0 (GPIO_INT_POL[5:0])** These bits set the interrupt polarity of the GPIO pins. The configured level (high/low) will set the corresponding GPIO_INT bit in the General Purpose I/O Interrupt Status and Enable Register (GPIO_INT_STS_EN). **0: Sets low logic level trigger on corresponding GPIO pin** **1: Sets high logic level trigger on corresponding GPIO pin**	R/W	0h
15:6	**RESERVED**	RO	-
5:0	**GPIO Buffer Type 5-0 (GPIOBUF[5:0])** This field sets the buffer types of the GPIO pins. **0: Corresponding GPIO pin configured as an open-drain driver** **1: Corresponding GPIO pin configured as a push/pull driver** As an open-drain driver, the output pin is driven low when the corresponding data register is cleared, and is not driven when the corresponding data register is set.	R/W	0h

13.2.2.2 General Purpose I/O Data & Direction Register (GPIO_DATA_DIR)

Offset:	1E4h	Size:	32 bits

This read/write register configures the direction of the GPIO pins and contains the GPIO input and output data bits.

BITS	DESCRIPTION	TYPE	DEFAULT
31:22	**RESERVED**	RO	-
21:16	**GPIO Direction 5-0 (GPDIR[5:0])** These bits set the input/output direction of the GPIO pins. **0: GPIO pin is configured as an input** **1: GPIO pin is configured as an output**	R/W	0h
15:6	**RESERVED**	RO	-
5:0	**GPIO Data 5-0 (GPIOD[5:0])** When a GPIO pin is enabled as an output, the value written to this field is output on the corresponding GPIO pin. Upon a read, the value returned depends on the current direction of the pin. If the pin is an input, the data reflects the current state of the corresponding GPIO pin. If the pin is an output, the data is the value that was last written into this register. The pin direction is determined by the GPDIR bits of this register.	R/W	0h

13.2.2.3 General Purpose I/O Interrupt Status and Enable Register (GPIO_INT_STS_EN)

Offset: 1E8h Size: 32 bits

This read/write register contains the GPIO interrupt status bits.

Writing a 1 to any of the interrupt status bits acknowledges and clears the interrupt. If enabled, these interrupt bits are cascaded into the GPIO Interrupt Event (GPIO) bit of the Interrupt Status Register (INT_STS). Writing a 1 to any of the interrupt enable bits will enable the corresponding interrupt as a source. Status bits will still reflect the status of the interrupt source regardless of whether the source is enabled as an interrupt in this register. The GPIO Interrupt Event Enable (GPIO_EN) bit of the Interrupt Enable Register (INT_EN) must also be set in order for an actual system level interrupt to occur. Refer to Chapter 5, "System Interrupts," on page 62 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:22	**RESERVED**	RO	-
21:16	**GPIO Interrupt Enable[5:0] (GPIO[5:0]_INT_EN)** When set, these bits enable the corresponding GPIO interrupt. **Note:** The GPIO interrupts must also be enabled via the GPIO Interrupt Event Enable (GPIO_EN) bit of the Interrupt Enable Register (INT_EN), in order to cause the interrupt pin (IRQ) to be asserted.	R/W	0h
15:6	**RESERVED**	RO	-
5:0	**GPIO Interrupt[5:0] (GPIO[5:0]_INT)** These signals reflect the interrupt status as generated by the GPIOs. These interrupts are configured through the General Purpose I/O Configuration Register (GPIO_CFG). **Note:** As GPIO interrupts, GPIO inputs are level sensitive and must be active greater than 40 nS to be recognized as interrupt inputs.	R/WC	0h

13.2.2.4 LED Configuration Register (LED_CFG)

Offset:	1BCh	Size:	32 bits

This read/write register configures the GPIO[5:0] pins as LED[5:0] pins and sets their functionality.

BITS	DESCRIPTION	TYPE	DEFAULT
31:10	**RESERVED**	RO	-
9:8	**LED Function 1-0 (LED_FUN[1:0])** These bits control the function associated with each LED pin as shown in Table 12.1 of Section 12.3, "LED Operation," on page 145. **Note:** In order for these assignments to be valid, the particular pin must be enabled as an LED output pin via the LED_EN[5:0] bits of this register.	R/W	Note 13.2
7:6	**RESERVED**	RO	-
5:0	**LED Enable 5-0 (LED_EN[5:0])** This field toggles the functionality of the GPIO[5:0] pins between GPIO and LED. **0: Enables the associated pin as a GPIO signal** **1: Enables the associated pin as a LED output** When configured as LED outputs, the pins are either push-pull or open-drain/open-source outputs and the pull-ups and input buffers are disabled. Push-pull is selected when LED_FUN[1:0] = 11b, otherwise, they are open-drain/open-source. When open-drain/open-source, the polarity of the pins depends upon the strap value sampled at reset. If a high is sampled at reset, then this signal is active low. **Note:** The polarity is determined by the strap value sampled on reset (a hard-strap) and not the soft-strap value (of the shared strap) set via EEPROM. When configured as a GPIO output, the pins are configured per the General Purpose I/O Configuration Register (GPIO_CFG) and the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR). The polarity of the pins does not depend upon the strap value sampled at reset.	R/W	Note 13.3

Note 13.2 The default value of this field is determined by the configuration strap LED_fun_strap[1:0]. Configuration strap values are latched on power-on reset or nRST de-assertion. Some configuration straps can be overridden by values from the EEPROM Loader. Refer to Section 4.2.4, "Configuration Straps," on page 52 for more information.

Note 13.3 The default value of this field is determined by the configuration strap LED_en_strap[5:0]. Configuration strap values are latched on power-on reset or nRST de-assertion. Some configuration straps can be overridden by values from the EEPROM Loader. Refer to Section 4.2.4, "Configuration Straps," on page 52 for more information.

13.2.3 EEPROM

This section details the EEPROM related System CSR's. These registers should only be used if an EEPROM has been connected to the device. Refer to chapter Section 8.3, "I2C Master EEPROM Controller," on page 115 for additional information.

13.2.3.1 EEPROM Command Register (E2P_CMD)

Offset:	1B4h	Size:	32 bits

This read/write register is used to control the read and write operations of the serial EEPROM.

BITS	DESCRIPTION	TYPE	DEFAULT
31	**EEPROM Controller Busy (EPC_BUSY)** When a 1 is written into this bit, the operation specified in the EPC_COMMAND field of this register is performed at the specified EEPROM address. This bit will remain set until the selected operation is complete. In the case of a read, this indicates that the Host can read valid data from the EEPROM Data Register (E2P_DATA). The E2P_CMD and E2P_DATA registers should not be modified until this bit is cleared. In the case where a write is attempted and an EEPROM is not present, the EPC_BUSY bit remains set until the EEPROM Controller Timeout (EPC_TIMEOUT) bit is set. At this time the EPC_BUSY bit is cleared. **Note:** EPC_BUSY is set immediately following power-up, or pin reset, or Digital Reset (DIGITAL_RST). After the EEPROM Loader has finished loading, the EPC_BUSY bit is cleared. Refer to chapter Section 8.4, "EEPROM Loader," on page 121 for more information.	R/W SC	0b

<table>
<tr><th>BITS</th><th>DESCRIPTION</th><th>TYPE</th><th>DEFAULT</th></tr>
<tr><td>30:28</td><td>EEPROM Controller Command (EPC_COMMAND)
This field is used to issue commands to the EEPROM controller. The EEPROM controller will execute a command when the EPC_BUSY bit is set. A new command must not be issued until the previous command completes. The field is encoded as follows:
<table>
<tr><th>[30]</th><th>[29]</th><th>[28]</th><th>Operation</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>READ</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>RESERVED</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>RESERVED</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>WRITE</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>RESERVED</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>RESERVED</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>RESERVED</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>RELOAD</td></tr>
</table>
Note: Only the READ, WRITE and RELOAD commands are valid for I^2C mode. If an unsupported command is attempted, the EPC_BUSY bit will be cleared and EPC_TIMEOUT will be set.
The EEPROM operations are defined as follows:

READ (Read Location)
This command will cause a read of the EEPROM location pointed to by the EPC_ADDRESS bit field. The result of the read is available in the EEPROM Data Register (E2P_DATA).

WRITE (Write Location)
If erase/write operations are enabled in the EEPROM, this command will cause the contents of the EEPROM Data Register (E2P_DATA) to be written to the EEPROM location selected by the EPC_ADDRESS field.

RELOAD (EEPROM Loader Reload)
Instructs the EEPROM Loader to reload the device from the EEPROM. If a value of A5h is not found in the first address of the EEPROM, the EEPROM is assumed to be un-programmed and the RELOAD operation will fail. The CFG_LOADED bit indicates a successful load. Following this command, the device will enter the not ready state. The Device Ready (READY) bit in the Hardware Configuration Register (HW_CFG) should be polled to determine when the RELOAD is complete.</td><td>R/W</td><td>000b</td></tr>
<tr><td>27:19</td><td>RESERVED</td><td>RO</td><td>-</td></tr>
<tr><td>18</td><td>EEPROM Loader Address Overflow (LOADER_OVERFLOW)
This bit indicates that the EEPROM Loader tried to read past the end of the EEPROM address space. This indicates misconfigured EEPROM data.

This bit is cleared when the EEPROM Loader is restarted with a RELOAD command, or a Digital Reset (DIGITAL_RST).</td><td>RO</td><td>0b</td></tr>
<tr><td>17</td><td>EEPROM Controller Timeout (EPC_TIMEOUT)
This bit is set when a timeout occurs, indicating the last operation was unsuccessful. If an EEPROM WRITE operation is performed, and no response is received from the EEPROM within 30mS, the EEPROM controller will timeout and return to its idle state.

The bit is also set if the EEPROM fails to respond with the appropriate ACKs, if the EEPROM slave device holds the clock low for more than 30mS, if the I^2C bus is not acquired within 1.92 seconds, or if an unsupported EPC_COMMAND is attempted.

This bit is cleared when written high.</td><td>R/WC</td><td>0b</td></tr>
</table>

BITS	DESCRIPTION	TYPE	DEFAULT
16	**Configuration Loaded (CFG_LOADED)** When set, this bit indicates that a valid EEPROM was found and the EEPROM Loader completed normally. This bit is set upon a successful load. It is cleared on power-up, pin and Digital Reset (DIGITAL_RST) resets, or at the start of a RELOAD. This bit is cleared when written high.	RO	0b
15:0	**EEPROM Controller Address (EPC_ADDRESS)** This field is used by the EEPROM Controller to address a specific memory location in the serial EEPROM. This address must be byte aligned.	R/W	0000h

13.2.3.2 EEPROM Data Register (E2P_DATA)

Offset: 1B8h Size: 32 bits

This read/write register is used in conjunction with the EEPROM Command Register (E2P_CMD) to perform read and write operations with the serial EEPROM.

BITS	DESCRIPTION	TYPE	DEFAULT
31:8	**RESERVED**	RO	-
7:0	**EEPROM Data (EEPROM_DATA)** This field contains the data read from or written to the EEPROM.	R/W	00h

13.2.4 Switch Fabric

This section details the memory mapped System CSR's which are related to the Switch Fabric. The flow control of all three ports of the Switch Fabric can be configured via the memory mapped System CSR's MANUAL_FC_1, MANUAL_FC_2 and MANUAL_FC_0. The MAC address used by the switch for Pause frames is configured via the SWITCH_MAC_ADDRH and SWITCH_MAC_ADDRL registers. In addition, the SWITCH_CSR_CMD, SWITCH_CSR_DATA and SWITCH_CSR_DIRECT_DATA registers serve as a memory mapped accessible interface to the full range of otherwise inaccessible switch control and status registers. A list of all the Switch Fabric CSRs can be seen in Table 13.14. For additional information on the Switch Fabric, including a full explanation on how to use the Switch Fabric CSR interface registers, refer to Chapter 6, "Switch Fabric," on page 67. For detailed descriptions of the Switch Fabric CSR's that are accessible via these interface registers, refer to section Section 13.4, "Switch Fabric Control and Status Registers".

13.2.4.1 Port 1 Manual Flow Control Register (MANUAL_FC_1)

Offset:	1A0h	Size:	32 bits

This read/write register allows for the manual configuration of the switch Port 1 flow control. This register also provides read back of the currently enabled flow control settings, whether set manually or Auto-Negotiated. Refer to Section 6.2.3, "Flow Control Enable Logic," on page 70 for additional information.

Note: The flow control values in the PHY_AN_ADV_1 register (see Section 13.3.2.5, on page 214) within the PHY are not affected by the values of this register.

BITS	DESCRIPTION	TYPE	DEFAULT
31:7	**RESERVED**	RO	-
6	**Port 1 Backpressure Enable (BP_EN_1)** This bit enables/disables the generation of half-duplex backpressure on switch Port 1. **0: Disable backpressure** **1: Enable backpressure**	R/W	Note 13.4
5	**Port 1 Current Duplex (CUR_DUP_1)** This bit indicates the actual duplex setting of switch Port 1. **0: Full-Duplex** **1: Half-Duplex**	RO	Note 13.5
4	**Port 1 Current Receive Flow Control Enable (CUR_RX_FC_1)** This bit indicates the actual receive flow setting of switch Port 1. **0: Flow control receive is currently disabled** **1: Flow control receive is currently enabled**	RO	Note 13.5
3	**Port 1 Current Transmit Flow Control Enable (CUR_TX_FC_1)** This bit indicates the actual transmit flow setting of switch Port 1. **0: Flow control transmit is currently disabled** **1: Flow control transmit is currently enabled**	RO	Note 13.5

BITS	DESCRIPTION	TYPE	DEFAULT
2	**Port 1 Full-Duplex Receive Flow Control Enable (RX_FC_1)** When the MANUAL_FC_1 bit is set, or Auto-Negotiation is disabled, this bit enables/disables the detection of full-duplex Pause packets on switch Port 1. **0: Disable flow control receive** **1: Enable flow control receive**	R/W	Note 13.6
1	**Port 1 Full-Duplex Transmit Flow Control Enable (TX_FC_1)** When the MANUAL_FC_1 bit is set, or Auto-Negotiation is disabled, this bit enables/disables full-duplex Pause packets to be generated on switch Port 1. **0: Disable flow control transmit** **1: Enable flow control transmit**	R/W	Note 13.6
0	**Port 1 Full-Duplex Manual Flow Control Select (MANUAL_FC_1)** This bit toggles flow control selection between manual and auto-negotiation. **0: If auto-negotiation is enabled, the auto-negotiation function determines the flow control of switch Port 1 (RX_FC_1 and TX_FC_1 values ignored). If auto-negotiation is disabled, the RX_FC_1 and TX_FC_1 values are used.** **1: TX_FC_1 and RX_FC_1 bits determine the flow control of switch Port 1 when in full-duplex mode.** **Note:** In Port 1 MII PHY, RMII PHY, or MII MAC mode, this bit is forced high. There is no auto-negotiation capability. Full-duplex flow control should be controlled manually by the host, if desired.	Note 13.7	Note 13.8

Note 13.4 The default value of this field is determined by the BP_EN_strap_1 configuration strap. The strap values are loaded during reset and can be re-written by the EEPROM Loader. Once the EEPROM Loader re-writes the values, this register is updated with the new values. See Section 4.2.4, "Configuration Straps," on page 52 for more information.

Note 13.5 The default value of this bit is determined by multiple strap settings. The strap values are loaded during reset and can be re-written by the EEPROM Loader. Once the EEPROM Loader re-writes the values, this register is updated with the new values. Refer to Section 6.2.3, "Flow Control Enable Logic," on page 70 for additional information.

Note 13.6 The default value of this field is determined by the FD_FC_strap_1 configuration strap. The strap values are loaded during reset and can be re-written by the EEPROM Loader. Once the EEPROM Loader re-writes the values, this register is updated with the new values. See Section 4.2.4, "Configuration Straps," on page 52 for more information.

Note 13.7 The type is determined by the operating mode. In Port 1 MII PHY, RMII PHY, or MII MAC mode, the type is RO. It is R/W for all other modes.

Note 13.8 The default value of this field is determined by the operating mode. In Port 1 MII PHY, RMII PHY, or MII MAC mode, it is 1, and the bit is not re-written by the EEPROM Loader. For all other operating modes, the default value is determined by the manual_FC_strap_1 configuration strap. The strap values are loaded during reset and can be re-written by the EEPROM Loader. Once the EEPROM Loader re-writes the values, this register is updated with the new values. See Section 4.2.4, "Configuration Straps," on page 52 for more information.

13.2.4.2 Port 2 Manual Flow Control Register (MANUAL_FC_2)

Offset:	1A4h	Size:	32 bits

This read/write register allows for the manual configuration of the switch Port 2 flow control. This register also provides read back of the currently enabled flow control settings, whether set manually or Auto-Negotiated. Refer to Section 6.2.3, "Flow Control Enable Logic," on page 70 for additional information.

Note: The flow control values in the PHY_AN_ADV_2 register (see Section 13.3.2.5, on page 214) within the PHY are not affected by the values of this register.

BITS	DESCRIPTION	TYPE	DEFAULT
31:7	**RESERVED**	RO	-
6	**Port 2 Backpressure Enable (BP_EN_2)** This bit enables/disables the generation of half-duplex backpressure on switch Port 2. **0: Disable backpressure** **1: Enable backpressure**	R/W	Note 13.9
5	**Port 2 Current Duplex (CUR_DUP_2)** This bit indicates the actual duplex setting of switch Port 2. **0: Full-Duplex** **1: Half-Duplex**	RO	Note 13.10
4	**Port 2 Current Receive Flow Control Enable (CUR_RX_FC_2)** This bit indicates the actual receive flow setting of switch Port 2. **0: Flow control receive is currently disabled** **1: Flow control receive is currently enabled**	RO	Note 13.10
3	**Port 2 Current Transmit Flow Control Enable (CUR_TX_FC_2)** This bit indicates the actual transmit flow setting of switch Port 2. **0: Flow control transmit is currently disabled** **1: Flow control transmit is currently enabled**	RO	Note 13.10
2	**Port 2 Full-Duplex Receive Flow Control Enable (RX_FC_2)** When the MANUAL_FC_2 bit is set, or Auto-Negotiation is disabled, this bit enables/disables the detection of full-duplex Pause packets on switch Port 2. **0: Disable flow control receive** **1: Enable flow control receive**	R/W	Note 13.11
1	**Port 2 Full-Duplex Transmit Flow Control Enable (TX_FC_2)** When the MANUAL_FC_2 bit is set, or Auto-Negotiation is disabled, this bit enables/disables full-duplex Pause packets to be generated on switch Port 2. **0: Disable flow control transmit** **1: Enable flow control transmit**	R/W	Note 13.11

BITS	DESCRIPTION	TYPE	DEFAULT
0	**Port 2 Full-Duplex Manual Flow Control Select (MANUAL_FC_2)** This bit toggles flow control selection between manual and auto-negotiation. **0: If auto-negotiation is enabled, the auto-negotiation function determines the flow control of switch Port 2 (RX_FC_2 and TX_FC_2 values ignored). If auto-negotiation is disabled, the RX_FC_2 and TX_FC_2 values are used.** **1: TX_FC_2 and RX_FC_2 bits determine the flow control of switch Port 2 when in full-duplex mode**	R/W	Note 13.12

Note 13.9 The default value of this field is determined by the BP_EN_strap_2 configuration strap. The strap values are loaded during reset and can be re-written by the EEPROM Loader. Once the EEPROM Loader re-writes the values, this register is updated with the new values. See Section 4.2.4, "Configuration Straps," on page 52 for more information.

Note 13.10 The default value of this bit is determined by multiple strap settings. The strap values are loaded during reset and can be re-written by the EEPROM Loader. Once the EEPROM Loader re-writes the values, this register is updated with the new values. Refer to Section 6.2.3, "Flow Control Enable Logic," on page 70 for additional information.

Note 13.11 The default value of this field is determined by the FD_FC_strap_2 configuration strap. The strap values are loaded during reset and can be re-written by the EEPROM Loader. Once the EEPROM Loader re-writes the values, this register is updated with the new values. See Section 4.2.4, "Configuration Straps," on page 52 for more information.

Note 13.12 The default value of this field is determined by the manual_FC_strap_2 configuration strap. The strap values are loaded during reset and can be re-written by the EEPROM Loader. Once the EEPROM Loader re-writes the values, this register is updated with the new values. See Section 4.2.4, "Configuration Straps," on page 52 for more information.

13.2.4.3 Port 0 Manual Flow Control Register (MANUAL_FC_0)

Offset:	1A8h	Size:	32 bits

This read/write register allows for the manual configuration of the switch Port 0 flow control. This register also provides read back of the currently enabled flow control settings, whether set manually or Auto-Negotiated. Refer to Section 6.2.3, "Flow Control Enable Logic," on page 70 for additional information.

Note: The flow control values in the Section 13.2.6.5, "Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV)," on page 188 are not affected by the values of this register.

BITS	DESCRIPTION	TYPE	DEFAULT
31:7	**RESERVED**	RO	-
6	**Port 0 Backpressure Enable (BP_EN_0)** This bit enables/disables the generation of half-duplex backpressure on switch Port 0. **0: Disable backpressure** **1: Enable backpressure**	R/W	Note 13.13
5	**Port 0 Current Duplex (CUR_DUP_0)** This bit indicates the actual duplex setting of switch Port 0. **0: Full-Duplex** **1: Half-Duplex**	RO	Note 13.14
4	**Port 0 Current Receive Flow Control Enable (CUR_RX_0)** This bit indicates the actual receive flow setting of switch Port 0 **0: Flow control receive is currently disabled** **1: Flow control receive is currently enabled**	RO	Note 13.14
3	**Port 0 Current Transmit Flow Control Enable (CUR_TX_FC_0)** This bit indicates the actual transmit flow setting of switch Port 0. **0: Flow control transmit is currently disabled** **1: Flow control transmit is currently enabled**	RO	Note 13.14
2	**Port 0 Receive Flow Control Enable (RX_FC_0)** When the MANUAL_FC_0 bit is set, or Virtual Auto-Negotiation is disabled, this bit enables/disables the detection of full-duplex Pause packets on switch Port 0. **0: Disable flow control receive** **1: Enable flow control receive**	R/W	Note 13.15
1	**Port 0 Transmit Flow Control Enable (TX_FC_0)** When the MANUAL_FC_0 bit is set, or Virtual Auto-Negotiation is disabled, this bit enables/disables full-duplex Pause packets to be generated on switch Port 0. **0: Disable flow control transmit** **1: Enable flow control transmit**	R/W	Note 13.15

BITS	DESCRIPTION	TYPE	DEFAULT
0	**Port 0 Full-Duplex Manual Flow Control Select (MANUAL_FC_0)** This bit toggles flow control selection between manual and auto-negotiation. **0: If auto-negotiation is enabled, the auto-negotiation function determines the flow control of switch Port 0 (RX_FC_0 and TX_FC_0 values ignored). If auto-negotiation is disabled, the RX_FC_0 and TX_FC_0 values are used.** **1: TX_FC_0 and RX_FC_0 bits determine the flow control of switch Port 0 when in full-duplex mode** **Note:** In MAC mode, this bit is forced high. The Virtual PHY is not applicable in this mode and full-duplex flow control should be controlled manually by the host based on the external PHYs Auto-Negotiation results.	R/W Note 13.16	Note 13.17

Note 13.13 The default value of this field is determined by the BP_EN_strap_0 configuration strap. The strap value is loaded during reset and can be re-written by the EEPROM Loader. Once the EEPROM Loader re-writes the value, this register is updated with the new values. See Section 4.2.4, "Configuration Straps," on page 52 for more information.

Note 13.14 The default value of this bit is determined by multiple strap settings. The strap values are loaded during reset and can be re-written by the EEPROM Loader. Once the EEPROM Loader re-writes the values, this register is updated with the new values. Refer to Section 6.2.3, "Flow Control Enable Logic," on page 70 for additional information.

Note 13.15 The default value of this field is determined by the FD_FC_strap_0 configuration strap. The strap value is loaded during reset and can be re-written by the EEPROM Loader. Once the EEPROM Loader re-writes the value, this register is updated with the new values. See Section 4.2.4, "Configuration Straps," on page 52 for more information.

Note 13.16 This bit is RO when in MAC mode.

Note 13.17 The default value of this field is determined by the manual_FC_strap_0 configuration strap. The strap value is loaded during reset and can be re-written by the EEPROM Loader. Once the EEPROM Loader re-writes the value, this register is updated with the new values. In MAC mode, this bit is not re-written by the EEPROM Loader and has a default value of “1”. See Section 4.2.4, "Configuration Straps," on page 52 for more information.

13.2.4.4 Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA)

Offset:	1ACh	Size:	32 bits

This read/write register is used in conjunction with the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD) to perform read and write operations with the Switch Fabric CSR's. Refer to Section 13.4, "Switch Fabric Control and Status Registers," on page 228 for details on the registers indirectly accessible via this register.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Switch CSR Data (CSR_DATA)** This field contains the value read from or written to the Switch Fabric CSR. The Switch Fabric CSR is selected via the CSR Address (CSR_ADDR[15:0]) bits of the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD). Upon a read, the value returned depends on the Read/Write (R_nW) bit in the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD). If Read/Write (R_nW) is set, the data is from the switch fabric. If Read/Write (R_nW) is cleared, the data is the value that was last written into this register.	R/W	00000000h

13.2.4.5 Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD)

Offset:	1B0h	Size:	32 bits

This read/write register is used in conjunction with the Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA) to control the read and write operations to the various Switch Fabric CSR's. Refer to Section 13.4, "Switch Fabric Control and Status Registers," on page 228 for details on the registers indirectly accessible via this register.

BITS	DESCRIPTION	TYPE	DEFAULT
31	**CSR Busy (CSR_BUSY)** When a 1 is written to this bit, the read or write operation (as determined by the R_nW bit) is performed to the specified Switch Fabric CSR in CSR Address (CSR_ADDR[15:0]). This bit will remain set until the operation is complete, at which time the bit will clear. In the case of a read, the clearing of this bit indicates to the Host that valid data can be read from the Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA). The SWITCH_CSR_CMD and SWITCH_CSR_DATA registers should not be modified until this bit is cleared.	R/W SC	0b
30	**Read/Write (R_nW)** This bit determines whether a read or write operation is performed by the Host to the specified Switch Engine CSR. **0: Write** **1: Read**	R/W	0b
29	**Auto Increment (AUTO_INC)** This bit enables/disables the auto increment feature. When this bit is set, a write to the Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA) register will automatically set the CSR Busy (CSR_BUSY) bit. Once the write command is finished, the CSR Address (CSR_ADDR[15:0]) will automatically increment. When this bit is set, a read from the Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA) will automatically increment the CSR Address (CSR_ADDR[15:0]) and set the CSR Busy (CSR_BUSY) bit. This bit should be cleared by software before the last read from the SWITCH_CSR_DATA register. **0: Disable Auto Increment** **1: Enable Auto Increment** **Note:** This bit has precedence over the Auto Decrement (AUTO_DEC) bit	R/W	0b
28	**Auto Decrement (AUTO_DEC)** This bit enables/disables the auto decrement feature. When this bit is set, a write to the Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA) will automatically set the CSR Busy (CSR_BUSY) bit. Once the write command is finished, the CSR Address (CSR_ADDR[15:0]) will automatically decrement. When this bit is set, a read from the Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA) will automatically decrement the CSR Address (CSR_ADDR[15:0]) and set the CSR Busy (CSR_BUSY) bit. This bit should be cleared by software before the last read from the SWITCH_CSR_DATA register. **0: Disable Auto Decrement** **1: Enable Auto Decrement**	R/W	0b
27:20	**RESERVED**	RO	-

BITS	DESCRIPTION	TYPE	DEFAULT
19:16	**CSR Byte Enable (CSR_BE[3:0])** This field is a 4-bit byte enable used for selection of valid bytes during write operations. Bytes which are not selected will not be written to the corresponding Switch Engine CSR. CSR_BE[3] corresponds to register data bits [31:24] CSR_BE[2] corresponds to register data bits [23:16] CSR_BE[1] corresponds to register data bits [15:8] CSR_BE[0] corresponds to register data bits [7:0] Typically all four byte enables should be set for auto increment and auto decrement operations.	R/W	0h
15:0	**CSR Address (CSR_ADDR[15:0])** This field selects the 16-bit address of the Switch Fabric CSR that will be accessed with a read or write operation. Refer to Table 13.14, "Indirectly Accessible Switch Control and Status Registers," on page 228 for a list of Switch Fabric CSR addresses.	R/W	00h

13.2.4.6 Switch Fabric MAC Address High Register (SWITCH_MAC_ADDRH)

Offset:	1F0h	Size:	32 bits

This register contains the upper 16-bits of the MAC address used by the switch for Pause frames. This register is used in conjunction with Switch Fabric MAC Address Low Register (SWITCH_MAC_ADDRL). The contents of this register are optionally loaded from the EEPROM at power-on through the EEPROM Loader if a programmed EEPROM is detected. The least significant byte of this register (bits [7:0]) is loaded from address 05h of the EEPROM. The second byte (bits [15:8]) is loaded from address 06h of the EEPROM. The Host can update the contents of this field after the initialization process has completed.

Refer to Section 13.2.4.7, "Switch Fabric MAC Address Low Register (SWITCH_MAC_ADDRL)" for information on how this address is loaded by the EEPROM Loader. Section 8.4, "EEPROM Loader," on page 121 contains additional details on using the EEPROM Loader.

BITS	DESCRIPTION	TYPE	DEFAULT
31:23	**RESERVED**	RO	-
22	**DiffPauseAddr** When set, each port may have a unique MAC address.	R/W	0b
21:20	**Port 2 Physical Address [41:40]** When DiffPauseAddr is set, these bits are used as bits 41 and 40 of the MAC Address for Port 2.	R/W	10b
19:18	**Port 1 Physical Address [41:40]** When DiffPauseAddr is set, these bits are used as bits 41 and 40 of the MAC Address for Port 1.	R/W	01b
17:16	**Port 0 Physical Address [41:40]** When DiffPauseAddr is set, these bits are used as bits 41 and 40 of the MAC Address for Port 0.	R/W	00b
15:0	**Physical Address[47:32]** This field contains the upper 16-bits (47:32) of the physical address of the Switch Fabric MACs. Bits 41 and 10 are ignored if DiffPauseAddr is set.	R/W	FFFFh

13.2.4.7 Switch Fabric MAC Address Low Register (SWITCH_MAC_ADDRL)

Offset: 1F4h Size: 32 bits

This register contains the lower 32-bits of the MAC address used by the switch for Pause frames. This register is used in conjunction with Switch Fabric MAC Address High Register (SWITCH_MAC_ADDRH). The contents of this register are optionally loaded from the EEPROM at power-on through the EEPROM Loader if a programmed EEPROM is detected. The least significant byte of this register (bits [7:0]) is loaded from address 01h of the EEPROM. The most significant byte (bits [31:24]) is loaded from address 04h of the EEPROM. The Host can update the contents of this field after the initialization process has completed.

Refer to Section 8.4, "EEPROM Loader," on page 121 for information on using the EEPROM Loader.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Physical Address[31:0]** This field contains the lower 32-bits (31:0) of the physical address of the Switch Fabric MACs.	R/W	FF0F8000h

Table 13.3 illustrates the byte ordering of the SWITCH_MAC_ADDRL and SWITCH_MAC_ADDRH registers with respect to the reception of the Ethernet physical address. Also shown is the correlation between the EEPROM addresses and the SWITCH_MAC_ADDRL and SWITCH_MAC_ADDRH registers.

Table 13.3 SWITCH_MAC_ADDRL, SWITCH_MAC_ADDRH, and EEPROM Byte Ordering

EEPROM Address	Register Location Written	Order of Reception on Ethernet
01h	SWITCH_MAC_ADDRL[7:0]	1st
02h	SWITCH_MAC_ADDRL[15:8]	2nd
03h	SWITCH_MAC_ADDRL[23:16]	3rd
04h	SWITCH_MAC_ADDRL[31:24]	4th
05h	SWITCH_MAC_ADDRH[7:0]	5th
06h	SWITCH_MAC_ADDRH[15:8]	6th

For example, if the desired Ethernet physical address is 12-34-56-78-9A-BC, the SWITCH_MAC_ADDRL and SWITCH_MAC_ADDRH registers would be programmed as shown in Figure 13.2. The values required to automatically load this configuration from the EEPROM are also shown.

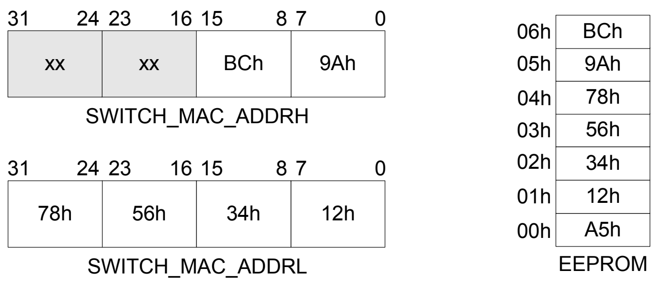


Figure 13.2 Example SWITCH_MAC_ADDRL, SWITCH_MAC_ADDRH, and EEPROM Setup

Note: By convention, the right nibble of the left most byte of the Ethernet address (in this example, the 2 of the 12h) is the most significant nibble and is transmitted/received first.

13.2.4.8 Switch Fabric CSR Interface Direct Data Registers (SWITCH_CSR_DIRECT_DATA)

Offset:	200h - 2DCh	Size:	32 bits

This write-only register set is used to perform directly addressed write operations to the Switch Fabric CSR's. Using this set of registers, writes can be directly addressed to select Switch Fabric registers, as specified in Table 13.4.

Writes within the Switch Fabric CSR Interface Direct Data Registers (SWITCH_CSR_DIRECT_DATA) address range automatically set the appropriate CSR Address (CSR_ADDR[15:0]), set the four CSR Byte Enable (CSR_BE[3:0]) bits, clear the Read/Write (R_nW) bit and set the CSR Busy (CSR_BUSY) bit in the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD). The completion of the write cycle is indicated when the CSR Busy (CSR_BUSY) bit is cleared. The address that is set in the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD) is mapped via Table 13.4. For more information on this method of writing to the Switch Fabric CSR's, refer to Section 6.2.3, "Flow Control Enable Logic," on page 70.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Switch CSR Data (CSR_DATA)** This field contains the value to be written to the corresponding Switch Fabric register.	WO	00000000h

Note: This set of registers is for write operations only. Reads can be performed via the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD) and Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA) registers only.

Table 13.4 Switch Fabric CSR to SWITCH_CSR_DIRECT_DATA Address Range Map

REGISTER NAME	SWITCH FABRIC CSR REGISTER #	SWITCH_CSR_DIRECT_DATA ADDRESS
General Switch CSRs		
SW_RESET	0001h	200h
SW_IMR	0004h	204h
Switch Port 0 CSRs		
MAC_RX_CFG_0	0401h	208h
MAC_TX_CFG_0	0440h	20Ch
MAC_TX_FC_SETTINGS_0	0441h	210h
MAC_IMR_0	0480h	214h
Switch Port 1 CSRs		
MAC_RX_CFG_1	0801h	218h
MAC_TX_CFG_1	0840h	21Ch
MAC_TX_FC_SETTINGS_1	0841h	220h
MAC_IMR_1	0880h	224h

Table 13.4 Switch Fabric CSR to SWITCH_CSR_DIRECT_DATA Address Range Map (continued)

REGISTER NAME	SWITCH FABRIC CSR REGISTER #	SWITCH_CSR_DIRECT_DATA ADDRESS
Switch Port 2 CSRs		
MAC_RX_CFG_2	0C01h	228h
MAC_TX_CFG_2	0C40h	22Ch
MAC_TX_FC_SETTINGS_2	0C41h	230h
MAC_IMR_2	0C80h	234h
Switch Engine CSRs		
SWE_ALR_CMD	1800h	238h
SWE_ALR_WR_DAT_0	1801h	23Ch
SWE_ALR_WR_DAT_1	1802h	240h
SWE_ALR_CFG	1809h	244h
SWE_VLAN_CMD	180Bh	248h
SWE_VLAN_WR_DATA	180Ch	24Ch
SWE_DIFFSERV_TBL_CMD	1811h	250h
SWE_DIFFSERV_TBL_WR_DATA	1812h	254h
SWE_GLB_INGRESS_CFG	1840h	258h
SWE_PORT_INGRESS_CFG	1841h	25Ch
SWE_ADMT_ONLY_VLAN	1842h	260h
SWE_PORT_STATE	1843h	264h
SWE_PRI_TO_QUE	1845h	268h
SWE_PORT_MIRROR	1846h	26Ch
SWE_INGRESS_PORT_TYP	1847h	270h
SWE_BCST_THROT	1848h	274h
SWE_ADMT_N_MEMBER	1849h	278h
SWE_INGRESS_RATE_CFG	184Ah	27Ch
SWE_INGRESS_RATE_CMD	184Bh	280h
SWE_INGRESS_RATE_WR_DATA	184Dh	284h
SWE_INGRESS_REGEN_TBL_0	1855h	288h
SWE_INGRESS_REGEN_TBL_1	1856h	28Ch
SWE_INGRESS_REGEN_TBL_2	1857h	290h
SWE_IMR	1880h	294h
Buffer Manager (BM) CSRs		

Table 13.4 Switch Fabric CSR to SWITCH_CSR_DIRECT_DATA Address Range Map (continued)

REGISTER NAME	SWITCH FABRIC CSR REGISTER #	SWITCH_CSR_DIRECT_DATA ADDRESS
BM_CFG	1C00h	298h
BM_DROP_LVL	1C01h	29Ch
BM_FC_PAUSE_LVL	1C02h	2A0h
BM_FC_RESUME_LVL	1C03h	2A4h
BM_BCST_LVL	1C04h	2A8h
BM_RNDM_DSCRD_TBL_CMD	1C09h	2ACh
BM_RNDM_DSCRD_TBL_WDATA	1C0Ah	2B0h
BM_EGRSS_PORT_TYPE	1C0Ch	2B4h
BM_EGRSS_RATE_00_01	1C0Dh	2B8h
BM_EGRSS_RATE_02_03	1C0Eh	2BCh
BM_EGRSS_RATE_10_11	1C0Fh	2C0h
BM_EGRSS_RATE_12_13	1C10h	2C4h
BM_EGRSS_RATE_20_21	1C11h	2C8h
BM_EGRSS_RATE_22_23	1C12h	2CCh
BM_VLAN_0	1C13h	2D0h
BM_VLAN_1	1C14h	2D4h
BM_VLAN_2	1C15h	2D8h
BM_IMR	1C20h	2DCh

13.2.5 PHY Management Interface (PMI)

The PMI registers are used to indirectly access the PHY registers. Refer to Section 13.3, "Ethernet PHY Control and Status Registers," on page 206 for additional information on the PHY registers. Refer to Section 10.3, "PHY Management Interface (PMI)," on page 137 for information on the PMI.

Note: The Virtual PHY registers are *NOT* accessible via these registers.

13.2.5.1 PHY Management Interface Data Register (PMI_DATA)

Offset:	0A4h	Size:	32 bits

This register is used in conjunction with the PHY Management Interface Access Register (PMI_ACCESS) to perform read and write operations to the PHYs.

Note: The Virtual PHY registers are *NOT* accessible via these registers.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:0	**MII Data** This field contains the value read from or written to the PHYs. For a write operation, this register should be first written with the desired data. For a read operation, the PMI_ACCESS register is first written and once the command is finished, this register will contain the return data. **Note:** Upon a read, the value returned depends on the MII Write (MIIWnR) bit in the PHY Management Interface Access Register (PMI_ACCESS). If MII Write (MIIWnR) is 0, the data is from the PHY. If MII Write (MIIWnR) is 1, the data is the value that was last written into this register.	R/W	0000h

13.2.5.2 PHY Management Interface Access Register (PMI_ACCESS)

Offset: 0A8h Size: 32 bits

This register is used to control the management cycles to the PHYs. A PHY access is initiated when this register is written. This register is used in conjunction with the PHY Management Interface Data Register (PMI_DATA) to perform read and write operations to the PHYs.

Note: The Virtual PHY registers are *NOT* accessible via these registers.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:11	**PHY Address (PHY_ADDR)** These bits select the PHY device being accessed. Refer to Section 7.1.1, "PHY Addressing," on page 96 for information on PHY address assignments.	R/W	00000b
10:6	**MII Register Index (MIIRINDA)** These bits select the desired MII register in the PHY. Refer to Section 13.3, "Ethernet PHY Control and Status Registers," on page 206 for detailed descriptions on all PHY registers.	R/W	00000b
5:2	**RESERVED**	RO	-
1	**MII Write (MIIWnR)** Setting this bit informs the PHY that the access will be a write operation using the PHY Management Interface Data Register (PMI_DATA). If this bit is cleared, the access will be a read operation, returning data into the PHY Management Interface Data Register (PMI_DATA).	R/W	0b
0	**MII Busy (MIIBZY)** This bit must be read as 0 before writing to the PHY Management Interface Data Register (PMI_DATA) or PHY Management Interface Access Register (PMI_ACCESS) registers. This bit is automatically set when this register is written. During a PHY register access, this bit will be set, signifying a read or write access is in progress. This is a self-clearing (SC) bit that will return to 0 when the PHY register access has completed. During a PHY register write, the PHY Management Interface Data Register (PMI_DATA) must be kept valid until this bit is cleared. During a PHY register read, the PHY Management Interface Data Register (PMI_DATA) register is invalid until the MAC has cleared this bit.	RO SC	0b

13.2.6 Virtual PHY

This section details the Virtual PHY System CSR's. These registers provide status and control information similar to that of a real PHY while maintaining IEEE 802.3 compatibility. The Virtual PHY registers are addressable via the memory map, as described in Table 13.2, as well as serially via the MII management protocol (IEEE 802.3 clause 22). When accessed serially, these registers are accessed through the MII management pins (in PHY modes only) via the MII serial management protocol specified in IEEE 802.3 clause 22. See Section 2.3, "Modes of Operation," on page 19 for a detailed description of the various device modes. When being accessed serially, the Virtual PHY will respond when the PHY address equals the address assigned by the phy_addr_sel_strap configuration strap, as defined in Section 7.1.1, "PHY Addressing," on page 96. A list of all Virtual PHY register indexes for serial access can be seen in Table 13.5. For more information on the Virtual PHY access modes, refer to section Section 13.3. For Virtual PHY functionality and operation information, see Section 7.3, "Virtual PHY," on page 110.

Note: All Virtual PHY registers follow the IEEE 802.3 (clause 22.2.4) specified MII management register set. All functionality and bit definitions comply with these standards. The IEEE 802.3 specified register index (in decimal) is included under the memory mapped offset of each Virtual PHY register as a reference. For additional information, refer to the IEEE 802.3 Specification.

Note: When serially accessed, the Virtual PHY registers are only 16-bits wide, as is standard for MII management of PHY's.

Table 13.5 Virtual PHY MII Serially Adressable Register Index

INDEX #	SYMBOL	REGISTER NAME
0	VPHY_BASIC_CTRL	Virtual PHY Basic Control Register, Section 13.2.6.1
1	VPHY_BASIC_STATUS	Virtual PHY Basic Status Register, Section 13.2.6.2
2	VPHY_ID_MSB	Virtual PHY Identification MSB Register, Section 13.2.6.3
3	VPHY_ID_LSB	Virtual PHY Identification LSB Register, Section 13.2.6.4
4	VPHY_AN_ADV	Virtual PHY Auto-Negotiation Advertisement Register, Section 13.2.6.5
5	VPHY_AN_LP_BASE_ABILITY	Virtual PHY Auto-Negotiation Link Partner Base Page Ability Register, Section 13.2.6.6
6	VPHY_AN_EXP	Virtual PHY Auto-Negotiation Expansion Register, Section 13.2.6.7
31	VPHY_SPEC_CTRL_STATUS	Virtual PHY Special Control/Status Register, Section 13.2.6.8

13.2.6.1 Virtual PHY Basic Control Register (VPHY_BASIC_CTRL)

Offset: 1C0h Size: 32 bits
Index (decimal): 0

This read/write register is used to configure the Virtual PHY.

Note: This register is re-written in its entirety by the EEPROM Loader following the release or reset or a RELOAD command. Refer to Section 8.4, "EEPROM Loader," on page 121 for more information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED** (See Note 13.18)	RO	-
15	**Reset (VPHY_RST)** When set, this bit resets all the Virtual PHY registers to their default state. This bit is self clearing. **0: Normal Operation** **1: Reset**	R/W SC	0b
14	**Loopback (VPHY_LOOPBACK)** This bit enables/disables the loopback mode. When enabled, transmissions from the external MAC are not sent to the Switch Fabric. Instead, they are looped back onto the receive path. **0: Loopback mode disabled (normal operation)** **1: Loopback mode enabled**	R/W	0b
13	**Speed Select LSB (VPHY_SPEED_SEL_LSB)** This bit is used to set the speed of the Virtual PHY when the Auto-Negotiation (VPHY_AN) bit is disabled. **0: 10 Mbps** **1: 100/200 Mbps**	R/W	0b
12	**Auto-Negotiation (VPHY_AN)** This bit enables/disables Auto-Negotiation. When enabled, the Speed Select LSB (VPHY_SPEED_SEL_LSB) and Duplex Mode (VPHY_DUPLEX) bits are overridden. **0: Auto-Negotiation disabled** **1: Auto-Negotiation enabled**	R/W	1b
11	**Power Down (VPHY_PWR_DWN)** This bit is not used by the Virtual PHY and has no effect.	R/W	0b
10	**Isolate (VPHY_ISO)** This bit controls the MII input/output pins. When set and in MII/RMII PHY mode, the MII output pins are not driven, MII pull-ups and pull-downs are disabled and the input pins are ignored. When in MAC mode, this bit is ignored and has no effect. (Note 13.19) **0: Non-Isolated (Normal operation)** **1: Isolated**	R/W	0b
9	**Restart Auto-Negotiation (VPHY_RST_AN)** When set, this bit updates the emulated Auto-Negotiation results. **0: Normal operation** **1: Auto-Negotiation restarted**	R/W SC	0b

BITS	DESCRIPTION	TYPE	DEFAULT
8	**Duplex Mode (VPHY_DUPLEX)** This bit is used to set the duplex when the Auto-Negotiation (VPHY_AN) bit is disabled. **0: Half Duplex** **1: Full Duplex**	R/W	0b
7	**Collision Test (VPHY_COL_TEST)** This bit enables/disables the collision test mode. When set, the collision signal to the external MAC is active during transmission from the external MAC. **Note:** It is recommended that this bit be used only when in loopback mode. **0: Collision test mode disabled** **1: Collision test mode enabled**	R/W	0b
6	**Speed Select MSB (VPHY_SPEED_SEL_MSB)** This bit is not used by the Virtual PHY and has no effect. The value returned is always 0.	RO	0b
5:0	**RESERVED**	RO	-

Note 13.18 The reserved bits 31-16 are used to pad the register to 32-bits so that each register is on a DWORD boundary. When accessed serially (through the MII management protocol), the register is 16-bits wide.

Note 13.19 The isolation does not apply to the MII management pins (MDIO).

13.2.6.2 Virtual PHY Basic Status Register (VPHY_BASIC_STATUS)

Offset:	1C4h	Size:	32 bits
Index (decimal):	1		

This register is used to monitor the status of the Virtual PHY.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED** (See Note 13.20)	RO	-
15	**100BASE-T4** This bit displays the status of 100BASE-T4 compatibility. **0: PHY not able to perform 100BASE-T4** **1: PHY able to perform 100BASE-T4**	RO	0b Note 13.21
14	**100BASE-X Full Duplex** This bit displays the status of 100BASE-X full duplex compatibility. **0: PHY not able to perform 100BASE-X full duplex** **1: PHY able to perform 100BASE-X full duplex**	RO	1b
13	**100BASE-X Half Duplex** This bit displays the status of 100BASE-X half duplex compatibility. **0: PHY not able to perform 100BASE-X half duplex** **1: PHY able to perform 100BASE-X half duplex**	RO	1b
12	**10BASE-T Full Duplex** This bit displays the status of 10BASE-T full duplex compatibility. **0: PHY not able to perform 10BASE-T full duplex** **1: PHY able to perform 10BASE-T full duplex**	RO	1b
11	**10BASE-T Half Duplex** This bit displays the status of 10BASE-T half duplex compatibility. **0: PHY not able to perform 10BASE-T half duplex** **1: PHY able to perform 10BASE-T half duplex**	RO	1b
10	**100BASE-T2 Full Duplex** This bit displays the status of 100BASE-T2 full duplex compatibility. **0: PHY not able to perform 100BASE-T2 full duplex** **1: PHY able to perform 100BASE-T2 full duplex**	RO	0b Note 13.21
9	**100BASE-T2 Half Duplex** This bit displays the status of 100BASE-T2 half duplex compatibility. **0: PHY not able to perform 100BASE-T2 half duplex** **1: PHY able to perform 100BASE-T2 half duplex**	RO	0b Note 13.21
8	**Extended Status** This bit displays whether extended status information is in register 15 (per IEEE 802.3 clause 22.2.4). **0: No extended status information in Register 15** **1: Extended status information in Register 15**	RO	0b Note 13.22
7	**RESERVED**	RO	-

BITS	DESCRIPTION	TYPE	DEFAULT
6	**MF Preamble Suppression** This bit indicates whether the Virtual PHY accepts management frames with the preamble suppressed. **0: Management frames with preamble suppressed not accepted** **1: Management frames with preamble suppressed accepted**	RO	0b
5	**Auto-Negotiation Complete** This bit indicates the status of the Auto-Negotiation process. **0: Auto-Negotiation process not completed** **1: Auto-Negotiation process completed**	RO	1b Note 13.23
4	**Remote Fault** This bit indicates if a remote fault condition has been detected. **0: No remote fault condition detected** **1: Remote fault condition detected**	RO	0b Note 13.24
3	**Auto-Negotiation Ability** This bit indicates the status of the Virtual PHY's auto-negotiation. **0: Virtual PHY is unable to perform auto-negotiation** **1: Virtual PHY is able to perform auto-negotiation**	RO	1b
2	**Link Status** This bit indicates the status of the link. **0: Link is down** **1: Link is up**	RO	1b Note 13.24
1	**Jabber Detect** This bit indicates the status of the jabber condition. **0: No jabber condition detected** **1: Jabber condition detected**	RO	0b Note 13.24
0	**Extended Capability** This bit indicates whether extended register capability is supported. **0: Basic register set capabilities only** **1: Extended register set capabilities**	RO	1b Note 13.25

Note 13.20 The reserved bits 31-16 are used to pad the register to 32-bits so that each register is on a DWORD boundary. When accessed serially (through the MII management protocol), the register is 16-bits wide.

Note 13.21 The Virtual PHY supports 100BASE-X (half and full duplex) and 10BASE-T (half and full duplex) only. All other modes will always return as 0 (unable to perform).

Note 13.22 The Virtual PHY does not support Register 15 or 1000 Mb/s operation. Thus this bit is always returned as 0.

Note 13.23 The Auto-Negotiation Complete bit is first cleared on a reset, but set shortly after (when the Auto-Negotiation process is run). Refer to Section 7.3.1, "Virtual PHY Auto-Negotiation," on page 110 for additional details.

Note 13.24 The Virtual PHY never has remote faults, its link is always up, and does not detect jabber.

Note 13.25 The VIrtual PHY supports basic and some extended register capability. The Virtual PHY supports Registers 0-6 (per the IEEE 802.3 specification).

13.2.6.3 Virtual PHY Identification MSB Register (VPHY_ID_MSB)

Offset:	1C8h	Size:	32 bits
Index (decimal):	2		

This read/write register contains the MSB of the Virtual PHY Organizationally Unique Identifier (OUI). The LSB of the Virtual PHY OUI is contained in the Virtual PHY Identification LSB Register (VPHY_ID_LSB).

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED** (See Note 13.26)	RO	-
15:0	**PHY ID** This field contains the MSB of the Virtual PHY OUI (Note 13.27).	R/W	0000h

Note 13.26 The reserved bits 31-16 are used to pad the register to 32-bits so that each register is on a DWORD boundary. When accessed serially (through the MII management protocol), the register is 16-bits wide.

Note 13.27 IEEE allows a value of zero in each of the 32-bits of the PHY Identifier.

13.2.6.4 Virtual PHY Identification LSB Register (VPHY_ID_LSB)

Offset:	1CCh	Size:	32 bits
Index (decimal):	3		

This read/write register contains the LSB of the Virtual PHY Organizationally Unique Identifier (OUI). The MSB of the Virtual PHY OUI is contained in the Virtual PHY Identification MSB Register (VPHY_ID_MSB).

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED** (See Note 13.28)	RO	-
15:10	**PHY ID** This field contains the lower 6-bits of the Virtual PHY OUI (Note 13.29).	R/W	000000b
9:4	**Model Number** This field contains the 6-bit manufacturer's model number of the Virtual PHY (Note 13.29).	R/W	000000b
3:0	**Revision Number** This field contain the 4-bit manufacturer's revision number of the Virtual PHY (Note 13.29).	R/W	0000b

Note 13.28 The reserved bits 31-16 are used to pad the register to 32-bits so that each register is on a DWORD boundary. When accessed serially (through the MII management protocol), the register is 16-bits wide.

Note 13.29 IEEE allows a value of zero in each of the 32-bits of the PHY Identifier.

13.2.6.5 Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV)

Offset: 1D0h Size: 32 bits
Index (decimal): 4

This read/write register contains the advertised ability of the Virtual PHY and is used in the Auto-Negotiation process with the link partner.

Note: This register is re-written in its entirety by the EEPROM Loader following the release or reset or a RELOAD command. Refer to Section 8.4, "EEPROM Loader," on page 121 for more information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED** (See Note 13.30)	RO	-
15	**Next Page** This bit determines the advertised next page capability and is always 0. **0: Virtual PHY does not advertise next page capability** **1: Virtual PHY advertises next page capability**	RO	0b Note 13.31
14	**RESERVED**	RO	-
13	**Remote Fault** This bit is not used since there is no physical link partner.	RO	0b Note 13.32
12	**RESERVED**	RO	-
11	**Asymmetric Pause** This bit determines the advertised asymmetric pause capability. **0: No Asymmetric PAUSE toward link partner advertised** **1: Asymmetric PAUSE toward link partner advertised**	R/W	Note 13.33
10	**Symmetric Pause** This bit determines the advertised symmetric pause capability. **0: No Symmetric PAUSE toward link partner advertised** **1: Symmetric PAUSE toward link partner advertised**	R/W	Note 13.33
9	**100BASE-T4** This bit determines the advertised 100BASE-T4 capability and is always 0. **0: 100BASE-T4 ability not advertised** **1: 100BASE-T4 ability advertised**	RO	0b Note 13.34
8	**100BASE-X Full Duplex** This bit determines the advertised 100BASE-X full duplex capability. **0: 100BASE-X full duplex ability not advertised** **1: 100BASE-X full duplex ability advertised**	R/W	1b
7	**100BASE-X Half Duplex** This bit determines the advertised 100BASE-X half duplex capability. **0: 100BASE-X half duplex ability not advertised** **1: 100BASE-X half duplex ability advertised**	R/W	1b

BITS	DESCRIPTION	TYPE	DEFAULT
6	**10BASE-T Full Duplex** This bit determines the advertised 10BASE-T full duplex capability. **0: 10BASE-T full duplex ability not advertised** **1: 10BASE-T full duplex ability advertised**	R/W	1b
5	**10BASE-T Half Duplex** This bit determines the advertised 10BASE-T half duplex capability. **0: 10BASE-T half duplex ability not advertised** **1: 10BASE-T half duplex ability advertised**	R/W	1b
4:0	**Selector Field** This field identifies the type of message being sent by Auto-Negotiation. **00001: IEEE 802.3**	R/W	00001b Note 13.35

Note 13.30 The reserved bits 31-16 are used to pad the register to 32-bits so that each register is on a DWORD boundary. When accessed serially (through the MII management protocol), the register is 16-bits wide.

Note 13.31 The Virtual PHY does not support next page capability. This bit value will always be 0.

Note 13.32 The Remote Fault bit is not useful since there is no actual link partner to send a fault to.

Note 13.33 The Symmetric Pause and Asymmetric Pause bits default to 1 if the manual_FC_strap_0 strap is low (both Symmetric and Asymmetric are advertised), and 0 if the manual_FC_strap_0 strap is high (neither Symmetric and Asymmetric are advertised). Configuration strap values are latched upon the de-assertion of a chip-level reset as described in Section 4.2.4, "Configuration Straps," on page 52.

Note 13.34 Virtual 100BASE-T4 is not supported.

Note 13.35 The Virtual PHY supports only IEEE 802.3. Only a value of 00001b should be used in this field.

13.2.6.6 Virtual PHY Auto-Negotiation Link Partner Base Page Ability Register (VPHY_AN_LP_BASE_ABILITY)

Offset:	1D4h	Size:	32 bits
Index (decimal):	5		

This read-only register contains the advertised ability of the link partner's PHY and is used in the Auto-Negotiation process with the Virtual PHY. Because the Virtual PHY does not physically connect to an actual link partner, the values in this register are emulated as described below.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED** (See Note 13.36)	RO	-
15	**Next Page** This bit indicates the emulated link partner PHY next page capability and is always 0. **0: Link partner PHY does not advertise next page capability** **1: Link partner PHY advertises next page capability**	RO	0b Note 13.37
14	**Acknowledge** This bit indicates whether the link code word has been received from the partner and is always 1. **0: Link code word not yet received from partner** **1: Link code word received from partner**	RO	1b Note 13.37
13	**Remote Fault** Since there is no physical link partner, this bit is not used and is always returned as 0.	RO	0b Note 13.37
12	**RESERVED**	RO	-
11	**Asymmetric Pause** This bit indicates the emulated link partner PHY asymmetric pause capability. **0: No Asymmetric PAUSE toward link partner** **1: Asymmetric PAUSE toward link partner**	RO	Note 13.38
10	**Pause** This bit indicates the emulated link partner PHY symmetric pause capability. **0: No Symmetric PAUSE toward link partner** **1: Symmetric PAUSE toward link partner**	RO	Note 13.38
9	**100BASE-T4** This bit indicates the emulated link partner PHY 100BASE-T4 capability. This bit is always 0. **0: 100BASE-T4 ability not supported** **1: 100BASE-T4 ability supported**	RO	0b Note 13.37
8	**100BASE-X Full Duplex** This bit indicates the emulated link partner PHY 100BASE-X full duplex capability. **0: 100BASE-X full duplex ability not supported** **1: 100BASE-X full duplex ability supported**	RO	Note 13.39

BITS	DESCRIPTION	TYPE	DEFAULT
7	**100BASE-X Half Duplex** This bit indicates the emulated link partner PHY 100BASE-X half duplex capability. **0: 100BASE-X half duplex ability not supported** **1: 100BASE-X half duplex ability supported**	RO	Note 13.39
6	**10BASE-T Full Duplex** This bit indicates the emulated link partner PHY 10BASE-T full duplex capability. **0: 10BASE-T full duplex ability not supported** **1: 10BASE-T full duplex ability supported**	RO	Note 13.39
5	**10BASE-T Half Duplex** This bit indicates the emulated link partner PHY 10BASE-T half duplex capability. **0: 10BASE-T half duplex ability not supported** **1: 10BASE-T half duplex ability supported**	RO	Note 13.39
4:0	**Selector Field** This field identifies the type of message being sent by Auto-Negotiation. **00001: IEEE 802.3**	RO	00001b

Note 13.36 The reserved bits 31-16 are used to pad the register to 32-bits so that each register is on a DWORD boundary. When accessed serially (through the MII management protocol), the register is 16-bits wide.

Note 13.37 The emulated link partner does not support next page, always instantly sends its link code word, never sends a fault, and does not support 100BASE-T4.

Note 13.38 The emulated link partner's asymmetric/symmetric pause ability is based upon the values of the Asymmetric Pause and Symmetric Pause bits of the Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV). Thus the emulated link partner always accommodates the request of the Virtual PHY, as shown in Table 13.6.

The link partner pause ability bits are determined when Auto-Negotiation is complete. Changing the Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV) will have no affect until the Auto-Negotiation process is re-run. If the local device advertises both Symmetric and Asymmetric pause, the result is determined based on the FD_FC_strap_0 configuration strap. This allows the user the choice of network emulation. If FD_FC_strap_0 = 1, then the result is Symmetrical, else Asymmetrical. See Section 7.3.1, "Virtual PHY Auto-Negotiation," on page 110 for additional information.

Table 13.6 Emulated Link Partner Pause Flow Control Ability Default Values

	VPHY SYMMETRIC PAUSE (REGISTER 4.10)	VPHY ASYMMETRIC PAUSE (REGISTER 4.11)	FD_FC_strap_0	LINK PARTNER SYMMETRIC PAUSE (REGISTER 5.10)	LINK PARTNER ASYMMETRIC PAUSE (REGISTER 5.11)
No Flow Control Enabled	0	0	x	0	0
Symmetric Pause	1	0	x	1	0
Asymmetric Pause Towards Switch	0	1	x	1	1

Table 13.6 Emulated Link Partner Pause Flow Control Ability Default Values

	VPHY SYMMETRIC PAUSE (REGISTER 4.10)	VPHY ASYMMETRIC PAUSE (REGISTER 4.11)	FD_FC_strap_0	LINK PARTNER SYMMETRIC PAUSE (REGISTER 5.10)	LINK PARTNER ASYMMETRIC PAUSE (REGISTER 5.11)
Asymmetric Pause Towards MAC	1	1	0	0	1
Symmetric Pause	1	1	1	1	1

Note 13.39 The emulated link partner's ability is based on the P0_DUPLEX pin, duplex_pol_strap_0, and speed_strap_0, as well as on the Auto-Negotiation success. Table 13.7 defines the default capabilities of the emulated link partner as a function of these signals. Configuration strap values are latched upon the de-assertion of a chip-level reset as described in Section 4.2.4, "Configuration Straps," on page 52. For more information on the Virtual PHY auto-negotiation, see Section 7.3.1, "Virtual PHY Auto-Negotiation," on page 110.

Table 13.7 Emulated Link Partner Default Advertised Ability

	speed_strap_0	ADVERTISED LINK PARTNER ABILITY (BITS 8,7,6,5)
P0_DUPLEX = duplex_pol_strap_0	0	10BASE-T Full-Duplex (0010)
	1	100BASE-X Full-Duplex (1000)
P0_DUPLEX != duplex_pol_strap_0	0	10BASE-T Half-Duplex (0001)
	1	100BASE-X Half-Duplex (0100)

13.2.6.7 Virtual PHY Auto-Negotiation Expansion Register (VPHY_AN_EXP)

Offset:	1D8h	Size:	32 bits
Index (decimal):	6		

This register is used in the Auto-Negotiation process.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED** (See Note 13.40)	RO	-
15:5	**RESERVED**	RO	-
4	**Parallel Detection Fault** This bit indicates whether a Parallel Detection Fault has been detected. This bit is always 0. **0: A fault hasn't been detected via the Parallel Detection function** **1: A fault has been detected via the Parallel Detection function**	RO	0b Note 13.41
3	**Link Partner Next Page Able** This bit indicates whether the link partner has next page ability. This bit is always 0. **0: Link partner does not contain next page capability** **1: Link partner contains next page capability**	RO	0b Note 13.42
2	**Local Device Next Page Able** This bit indicates whether the local device has next page ability. This bit is always 0. **0: Local device does not contain next page capability** **1: Local device contains next page capability**	RO	0b Note 13.42
1	**Page Received** This bit indicates the reception of a new page. **0: A new page has not been received** **1: A new page has been received**	RO/LH	1b Note 13.43
0	**Link Partner Auto-Negotiation Able** This bit indicates the Auto-negotiation ability of the link partner. **0: Link partner is not Auto-Negotiation able** **1: Link partner is Auto-Negotiation able**	RO	1b Note 13.44

Note 13.40 The reserved bits 31-16 are used to pad the register to 32-bits so that each register is on a DWORD boundary. When accessed serially (through the MII management protocol), the register is 16-bits wide.

Note 13.41 Since the Virtual PHY link partner is emulated, there is never a Parallel Detection Fault and this bit is always 0.

Note 13.42 Next page ability is not supported by the Virtual PHY or emulated link partner.

Note 13.43 The Page Received bit is clear when read. It is first cleared on reset, but set shortly thereafter when the Auto-Negotiation process is run.

Note 13.44 The emulated link partner will show Auto-Negotiation able unless Auto-Negotiation fails (no common bits between the advertised ability and the link partner ability).

13.2.6.8 Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS)

Offset:	1DCh	Size:	32 bits
Index (decimal):	31		

This read/write register contains a current link speed/duplex indicator and SQE control.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED** (See Note 13.45)	RO	-
15	**RESERVED**	RO	-
14	**Switch Looopback Port 0** When set, transmissions from the Switch Fabric Port 0 are not sent to the External MAC. Instead, they are looped back into the Switch Engine. From the MAC viewpoint, this is effectively a FAR LOOPBACK. If loopback is enabled during half-duplex operation, then the Enable Receive Own Transmit bit in the Port x MAC Receive Configuration Register (MAC_RX_CFG_x) must be set for this port. Otherwise, the Switch Fabric will ignore receive activity when transmitting in half-duplex mode. **Note:** This mode works even if the Isolate (VPHY_ISO) bit of the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) is set.	R/W	0b
13:11	**RESERVED**	RO	-
10	**Turbo MII Enable** When set, this bit changes the data rate of the MII PHY 100Mbps mode to 200Mbps. The normal Virtual PHY selection mechanism that chooses between 10 and 100Mbps will instead choose between 10Mbps and 200Mbps. **Note:** When operating at 200Mbps, the drive strength of the MII output clocks is selected using the RMII/Turbo MII Clock Strength bit. When at 100 Mbps or 10 Mbps, the drive strength is fixed at 12 mA.	R/W	Note 13.46
9:8	**Mode** This field indicates the operating mode of port 0. **00: MII MAC mode** **01: MII PHY mode** **10: RMII PHY mode** **11: RESERVED**	RO	Note 13.47
7	**Switch Collision Test Port 0** When set, the collision signal to the Switch Fabric Port 0 is active during transmission from the Switch Engine. **Note:** It is recommended that this bit be used only when using loopback mode.	R/W	0b
6	**RMII Clock Direction** **0: Selects P0_OUTCLK as an Input** **1: Selects P0_OUTCLK as an Output**	R/W NASR Note 13.51	Note 13.48
5	**RMII/Turbo MII Clock Strength** For RMII and 200 Mbps MII PHY modes, a low selects 12 mA drive while a high selects a 16 mA drive. For 100 Mbps and 10 Mbps MII PHY modes, the drive strength is fixed at 12mA.	R/W NASR Note 13.51	Note 13.49

<table>
<tr><th>BITS</th><th>DESCRIPTION</th><th>TYPE</th><th>DEFAULT</th></tr>
<tr><td>4:2</td><td>Current Speed/Duplex Indication
This field indicates the current speed and duplex of the Virtual PHY link.
<table>
<tr><th>[4]</th><th>[3]</th><th>[2]</th><th>Speed</th><th>Duplex</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td colspan="2">RESERVED</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>10Mbps</td><td>half-duplex</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>100/200Mbps</td><td>half-duplex</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td colspan="2">RESERVED</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td colspan="2">RESERVED</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>10Mbps</td><td>full-duplex</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>100/200Mbps</td><td>full-duplex</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td colspan="2">RESERVED</td></tr>
</table></td><td>RO</td><td>Note 13.50</td></tr>
<tr><td>1</td><td>RESERVED</td><td>RO</td><td>-</td></tr>
<tr><td>0</td><td>SQEOFF
This bit enables/disables the Signal Quality Error (Heartbeat) test.

0: SQE test enabled
1: SQE test disabled
Note: This bit is used when Port 0 is in MII PHY mode. It is not usable in RMII PHY or MII MAC modes.</td><td>R/W
NASR
Note 13.51</td><td>Note 13.52</td></tr>
</table>

Note 13.45 The reserved bits 31-16 are used to pad the register to 32-bits so that each register is on a DWORD boundary. When accessed serially (through the MII management protocol), the register is 16-bits wide.

Note 13.46 The default value of this field is determined via the turbo_mii_enable_strap_0 configuration strap. Refer to Section 4.2.4, "Configuration Straps," on page 52 for additional information.

Note 13.47 The default value of this field is determined via the P0_mode_strap[1:0] configuration straps. Refer to Section 4.2.4, "Configuration Straps," on page 52 for additional information.

Note 13.48 The default value of this field is determined via the P0_rmii_clock_dir_strap configuration strap. Refer to Section 4.2.4, "Configuration Straps," on page 52 for additional information.

Note 13.49 The default value of this field is determined via the P0_clock_strength_strap configuration strap. Refer to Section 4.2.4, "Configuration Straps," on page 52 for additional information.

Note 13.50 The default value of this field is the result of the Auto-Negotiation process if the Auto-Negotiation (VPHY_AN) bit of the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) is set. Otherwise, this field reflects the Speed Select LSB (VPHY_SPEED_SEL_LSB) and Duplex Mode (VPHY_DUPLEX) bit settings of the VPHY_BASIC_CTRL register. Refer to Section 7.3.1, "Virtual PHY Auto-Negotiation," on page 110 for information on the Auto-Negotiation determination process of the Virtual PHY.

Note 13.51 Register bits designated as NASR are reset when the Virtual PHY Reset is generated via the Reset Control Register (RESET_CTL). The NASR designation is only applicable when the Reset (VPHY_RST) bit of the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) is set.

Note 13.52 The default value of this field is determined via the SQE_test_disable_strap_0 configuration strap. Refer to Section 4.2.4, "Configuration Straps," on page 52 for additional information.

13.2.7 Miscellaneous

This section details the remainder of the System CSR's. These registers allow for monitoring and configuration of various functions such as the Chip ID/revision, byte order testing, hardware configuration, general purpose timer, and free running counter.

13.2.7.1 Chip ID and Revision (ID_REV)

Offset:	050h	Size:	32 bits

This read-only register contains the ID and Revision fields for the device.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**Chip ID** This field indicates the chip ID.	RO	9303h
15:0	**Chip Revision** This field indicates the design revision.	RO	Note 13.53

Note 13.53 Default value is dependent on device revision.

13.2.7.2 Byte Order Test Register (BYTE_TEST)

Offset: 064h Size: 32 bits

This read-only register can be used to determine the byte ordering of the current configuration.

Note: This register can be read while the device is in the not ready state. This register can also be polled while the device is in the reset state without causing any damaging effects. The returned data will be invalid since the serial interfaces are also in the reset state at this time. However, the returned data will not match the normal valid data pattern during reset.

Note: In SMI mode, either half of this register can be read without the need to read the other half.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Byte Test (BYTE_TEST)** This field reflects the current byte ordering	RO	87654321h

13.2.7.3 Hardware Configuration Register (HW_CFG)

Offset:	074h	Size:	32 bits

This register allows the configuration of various hardware features.

Note: This register can be polled while the device is in the reset or not ready state (Device Ready (READY) bit is cleared). Returned data will be invalid during the reset state since the serial interfaces are also in reset at this time.

Note: In SMI mode, either half of this register can be read without the need to read the other half.

BITS	DESCRIPTION	TYPE	DEFAULT
31:28	**RESERVED**	RO	-
27	**Device Ready (READY)** When set, this bit indicates that the device is ready to be accessed. Upon power-up, nRST reset, or digital reset, the host processor may interrogate this field as an indication that the device has stabilized and is fully active. This bit can cause an interrupt if enabled. **Note:** With the exception of the HW_CFG, BYTE_TEST, and RESET_CTL registers, read access to any internal resources is forbidden while the READY bit is cleared. Writes to any address are invalid until this bit is set.	RO	0b
26	**AMDIX_EN Strap State Port 2** This bit reflects the state of the auto_mdix_strap_2 strap that connects to the PHY. The strap value is loaded with the level of the auto_mdix_strap_2 during reset and can be re-written by the EEPROM Loader. The strap value can be overridden by the Auto-MDIX Control (AMDIXCTRL) and Auto-MDIX State (AMDIXSTATE) bits of the Port 2 PHY Special Control/Status Indication Register (Section 13.3.2.10).	RO	Note 13.54
25	**AMDIX_EN Strap State Port 1** This bit reflects the state of the auto_mdix_strap_1 strap that connects to the PHY. The strap value is loaded with the level of the auto_mdix_strap_1 during reset and can be re-written by the EEPROM Loader. The strap value can be overridden by the Auto-MDIX Control (AMDIXCTRL) and Auto-MDIX State (AMDIXSTATE) bits of the Port 1 PHY Special Control/Status Indication Register (Section 13.3.2.10).	RO	Note 13.55
24:0	**RESERVED**	RO	-

Note 13.54 The default value of this field is determined by the configuration strap auto_mdix_strap_2. See Section 4.2.4, "Configuration Straps," on page 52 for more information.

Note 13.55 The default value of this field is determined by the configuration strap auto_mdix_strap_1. See Section 4.2.4, "Configuration Straps," on page 52 for more information.

13.2.7.4 General Purpose Timer Configuration Register (GPT_CFG)

Offset:	08Ch	Size:	32 bits

This read/write register configures the General Purpose Timer (GPT). The GPT can be configured to generate host interrupts at the interval defined in this register. The current value of the GPT can be monitored via the General Purpose Timer Count Register (GPT_CNT). Refer to Section 11.1, "General Purpose Timer," on page 143 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:30	**RESERVED**	RO	-
29	**General Purpose Timer Enable (TIMER_EN)** This bit enables the GPT. When set, the GPT enters the run state. When cleared, the GPT is halted. On the 1 to 0 transition of this bit, the GPT_LOAD field of this register will be preset to FFFFh. **0: GPT Disabled** **1: GPT Enabled**	R/W	0b
28:16	**RESERVED**	RO	-
15:0	**General Purpose Timer Pre-Load (GPT_LOAD)** This value is pre-loaded into the GPT. This is the starting value of the GPT. The timer will begin decrementing from this value when enabled.	R/W	FFFFh

13.2.7.5 General Purpose Timer Count Register (GPT_CNT)

Offset:	090h	Size:	32 bits

This read-only register reflects the current general purpose timer (GPT) value. The register should be used in conjunction with the General Purpose Timer Configuration Register (GPT_CFG) to configure and monitor the GPT. Refer to Section 11.1, "General Purpose Timer," on page 143 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:0	**General Purpose Timer Current Count (GPT_CNT)** This 16-bit field represents the current value of the GPT.	RO	FFFFh

13.2.7.6 Free Running 25MHz Counter Register (FREE_RUN)

Offset: 09Ch Size: 32 bits

This read-only register reflects the current value of the free-running 25MHz counter. Refer to Section 11.2, "Free-Running Clock," on page 143 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Free Running Counter (FR_CNT)** This field reflects the current value of the free-running 32-bit counter. At reset, the counter starts at zero and is incremented by one every 25MHz cycle. When the maximum count has been reached, the counter will rollover to zero and continue counting. **Note:** The free running counter can take up to 160nS to clear after a reset event.	RO	00000000h

13.2.7.7 Port 1 MII Basic Control Register (P1_MII_BASIC_CONTROL)

Offset: 1ECh Size: 32 bits

This register is re-written in its entirety by the EEPROM Loader following the release of reset or a RELOAD command. Refer to Section 8.4, "EEPROM Loader," on page 121 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31	**RESERVED**	RO	-
30	**Switch Looopback Port 1** When set, transmissions from the Switch Fabric Port 1 are not sent to the External MAC. Instead, they are looped back into the Switch Engine. From the MAC viewpoint, this is effectively a FAR LOOPBACK. If loopback is enabled during half-duplex operation, then the Enable Receive Own Transmit bit in the (x=1) Port x MAC Receive Configuration Register (MAC_RX_CFG_x) must be set for this port. Otherwise, the Switch Fabric will ignore receive activity when transmitting in half-duplex mode. **Note:** This mode works even if the Isolate bit is set. **Note:** This bit is used when Port 1 is in MII or RMII PHY mode. It is not usable in internal PHY or MII MAC modes.	R/W	0b
29	**RESERVED**	RO	-
28	**Manual Duplex** When set, the duplex is based on the Duplex Mode bit. When clear, the duplex is based on the P1_DUPLEX input and duplex_pol_strap_1. **Note:** This bit is used when Port 1 is in the MII MAC mode. It is not usable in internal PHY or MII or RMII PHY modes.	R/W	0b
27	**RESERVED**	RO	-
26	**Turbo MII Enable** This bit, along with the Speed Select LSB bit, determines the speed of the MII PHY mode. When set, the Speed Select LSB bit selects between 200Mbps and 10 Mbps. When cleared, the Speed Select LSB bit selects between 100Mbps and 10 Mbps. **Note:** When operating at 200Mbps, the drive strength of the MII output clock is selected using the RMII/Turbo MII Clock Strength bit. When at 100 Mbps or 10 Mbps, the drive strength is fixed at 12 mA.	R/W	Note 13.56
25:24	**Mode** This field indicates the operating mode of port 1. **00: MII MAC mode** **01: MII PHY mode** **10: RMII PHY mode** **11: Internal PHY mode**	RO	Note 13.57

BITS	DESCRIPTION	TYPE	DEFAULT
23	**Switch Collision Test Port 1** When set, the collision signal to the Switch Fabric Port 1 is active during transmission from the Switch Engine. **Note:** This bit is used when Port 1 is in the MII or RMII PHY mode. It is not usable in the internal PHY or MII MAC modes. **Note:** It is recommended that this bit be used only when using loopback mode.	R/W	0b
22	**RMII Clock Direction** **0: Selects P1_OUTCLK as an Input** **1: Selects P1_OUTCLK as an Output**	R/W	Note 13.58
21	**RMII/Turbo MII Clock Strength** For RMII and 200 Mbps MII PHY modes, a low selects 12 mA drive while a high selects a 16 mA drive. For 100 Mbps and 10 Mbps MII PHY modes, the drive strength is fixed at 12mA.	R/W	Note 13.59
20:17	**RESERVED**	RO	-
16	**SQEOFF** This bit enables/disables the Signal Quality Error (Heartbeat) test. **0: SQE test enabled** **1: SQE test disabled** **Note:** This bit is used when Port 1 is in MII PHY mode. It is not usable in internal PHY, RMII PHY, or MII MAC modes.	R/W	Note 13.60
15	**RESERVED**	RO	-
14	**Loopback** When set, transmissions from the external MAC are not sent to the Switch Engine. Instead, they are looped back onto the receive path. **Note:** This bit is used when Port 1 is in MII or RMII PHY mode. It is not usable in internal PHY or MII MAC modes.	R/W	0b
13	**Speed Select LSB** This bit is used, along with the Turbo MII Enable bit, to set the speed. **0: 10 Mbps** **1: 200 or 100 Mbps** **Note:** This bit is used when Port 1 is in MII or RMII PHY mode. It is not usable in internal PHY or MII MAC modes.	R/W	Note 13.61
12:11	**RESERVED**	RO	-
10	**Isolate** When set and in PHY mode, the MII output pins are not driven, the MII pull-ups and pull-downs are disabled, and the input pins are ignored. **Note:** This bit is used when Port 1 is in MII or RMII PHY mode. It is not usable in internal PHY or MII MAC modes.	R/W	0b
9	**RESERVED**	RO	-
8	**Duplex Mode** In MII and RMII PHY modes, this bit is used to set the duplex. In MII MAC mode, this bit is used to set the duplex when the Manual Duplex bit is set. **0: Half duplex** **1: Full duplex** **Note:** This bit is used when Port 1 is in MII PHY, RMII PHY, or MII MAC mode. It is not usable in internal PHY mode.	R/W	Note 13.62

BITS	DESCRIPTION	TYPE	DEFAULT
7	**Collision Test** This bit enables/disables the collision test mode. When set, the collision signal to the external MAC is active during transmission from the external MAC. **Note:** It is recommended that this bit be used only when in loopback mode. **0: Collision test mode disabled** **1: Collision test mode enabled** **Note:** This bit is used when Port 1 is in MII PHY mode. It is not usable in internal PHY, RMII PHY, or MII MAC mode.	R/W	0b
6:0	**RESERVED**	RO	-

Note 13.56 The default value of this field is determined via the turbo_mii_enable_strap_1 configuration strap. Refer to Section 4.2.4, "Configuration Straps," on page 52 for additional information.

Note 13.57 The default value of this field is determined via the P1_mode_strap[1:0] configuration straps. Refer to Section 4.2.4, "Configuration Straps," on page 52 for additional information.

Note 13.58 The default value of this field is determined via the P1_rmii_clock_dir_strap configuration strap. Refer to Section 4.2.4, "Configuration Straps," on page 52 for additional information.

Note 13.59 The default value of this field is determined via the P1_clock_strength_strap configuration strap. Refer to Section 4.2.4, "Configuration Straps," on page 52 for additional information.

Note 13.60 The default value of this field is determined via the SQE_test_disable_strap_1 configuration strap. Refer to Section 4.2.4, "Configuration Straps," on page 52 for additional information.

Note 13.61 The default value of this field is determined via the speed_strap_1 configuration strap. Refer to Section 4.2.4, "Configuration Straps," on page 52 for additional information.

Note 13.62 The default value of this field is determined as follows:
1 if duplex_pol_strap_1 = P1_DUPLEX
0 if duplex_pol_strap_1 != P1_DUPLEX.

13.2.7.8 Reset Control Register (RESET_CTL)

Offset:	1F8h	Size:	32 bits

This register contains software controlled resets.

Note: This register can be read while the device is in the not ready state. This register can also be polled while the device is in the reset state without causing any damaging effects. However, the returned data will be invalid since the serial interfaces are also in the reset state at this time.

Note: In SMI mode, either half of this register can be read without the need to read the other half.

BITS	DESCRIPTION	TYPE	DEFAULT
31:4	**RESERVED**	RO	-
3	**Virtual PHY Reset (VPHY_RST)** Setting this bit resets the Virtual PHY. When the Virtual PHY is released from reset, this bit is automatically cleared. All writes to this bit are ignored while this bit is set. **Note:** This bit is not accessible via the EEPROM Loader.	R/W SC	0b
2	**Port 2 PHY Reset (PHY2_RST)** Setting this bit resets the Port 2 PHY. The internal logic automatically holds the PHY reset for a minimum of 102uS. When the Port 2 PHY is released from reset, this bit is automatically cleared. All writes to this bit are ignored while this bit is set. **Note:** This bit is not accessible via the EEPROM Loader.	R/W SC	0b
1	**Port 1 PHY Reset (PHY1_RST)** Setting this bit resets the Port 1 PHY. The internal logic automatically holds the PHY reset for a minimum of 102uS. When the Port 1 PHY is released from reset, this bit is automatically cleared. All writes to this bit are ignored while this bit is set. **Note:** This bit is not accessible via the EEPROM Loader.	R/W SC	0b
0	**Digital Reset (DIGITAL_RST)** Setting this bit resets the complete chip except the PLL, Virtual PHY, Port 1 PHY, and Port 2 PHY. The EEPROM Loader will automatically reload the configuration following this reset, but will not reset the Virtual PHY, Port 1 PHY, or Port 2 PHY. If desired, the above PHY resets can be issued once the device is configured. All system CSRs are reset except for any NASR type bits. Any in progress EEPROM commands (including RELOAD) are terminated. When the chip is released from reset, this bit is automatically cleared. The Byte Order Test Register (BYTE_TEST) should be polled to determine when the reset is complete. All writes to this bit are ignored while this bit is set. **Note:** This bit is not accessible via the EEPROM Loader.	R/W SC	0b

13.3 Ethernet PHY Control and Status Registers

This section details the various Ethernet PHY control and status registers. The device contains three PHY's: Port 1 PHY, Port 2 PHY and a Virtual PHY. All PHY registers follow the IEEE 802.3 (clause 22.2.4) specified MII management register set. All functionality and bit definitions comply with these standards. The IEEE 802.3 specified register index (in decimal) is included with each register definition, allowing for addressing of these registers via the MII serial management protocol. For additional information on the MII management protocol, refer to the IEEE 802.3 Specification.

Each individual PHY is assigned a unique PHY address as detailed in Section 7.1.1, "PHY Addressing," on page 96.

13.3.1 Virtual PHY Registers

The Virtual PHY provides a basic MII management interface for communication with an standard external MAC as if it was attached to a single port PHY. The Virtual PHY registers differ from the Port 1 & 2 PHY registers in that they are addressable via the memory map, as described in Table 13.2, as well as serially. These modes of access are described in Section 13.2.6, "Virtual PHY," on page 181.

Because the Virtual PHY registers are also memory mapped, their definitions have been included in the System Control and Status Registers Section 13.2.6, "Virtual PHY," on page 181. A list of the Virtual PHY MII addressable registers and their corresponding register index numbers is also included in Table 13.5.

Note: When serially accessed, the Virtual PHY registers are only 16-bits wide, as is standard for MII management of PHY's.

13.3.2 Port 1 & 2 PHY Registers

The Port 1 and Port 2 PHY's are comparable in functionality and have an identical set of non-memory mapped registers. The Port 1 and Port 2 PHY registers are not memory mapped. These registers are indirectly accessed through the PHY Management Interface Access Register (PMI_ACCESS) and PHY Management Interface Data Register (PMI_DATA) registers (in MAC or PHY I^2C modes only) or through the MII management pins (in MAC or PHY SMI modes only) via the MII serial management protocol specified in IEEE 802.3 clause 22. See Section 2.3, "Modes of Operation," on page 19 for a details on the various device modes. Because the Port 1 & 2 PHY registers are functionally identical, their register descriptions have been consolidated. A lowercase "x" has been appended to the end of each PHY register name in this section, where "x" should be replaced with "1" or "2" for the Port 1 PHY or the Port 2 PHY registers respectively. A list of the Port 1 & 2 PHY MII addressable registers and their corresponding register index numbers is included in Table 13.8. Each individual PHY is assigned a unique PHY address as detailed in Section 7.1.1, "PHY Addressing," on page 96.

Table 13.8 Port 1 & 2 PHY MII Serially Adressable Registers

INDEX #	SYMBOL	REGISTER NAME
0	PHY_BASIC_CONTROL_x	Port x PHY Basic Control Register, Section 13.3.2.1
1	PHY_BASIC_STATUS_x	Port x PHY Basic Status Register, Section 13.3.2.2
2	PHY_ID_MSB_x	Port x PHY Identification MSB Register, Section 13.3.2.3
3	PHY_ID_LSB_x	Port x PHY Identification LSB Register, Section 13.3.2.4
4	PHY_AN_ADV_x	Port x PHY Auto-Negotiation Advertisement Register, Section 13.3.2.5
5	PHY_AN_LP_BASE_ABILITY_x	Port x PHY Auto-Negotiation Link Partner Base Page Ability Register, Section 13.3.2.6

Table 13.8 Port 1 & 2 PHY MII Serially Adressable Registers (continued)

INDEX #	SYMBOL	REGISTER NAME
6	PHY_AN_EXP_x	Port x PHY Auto-Negotiation Expansion Register, Section 13.3.2.7
17	PHY_MODE_CONTROL_STATUS_x	Port x PHY Mode Control/Status Register, Section 13.3.2.8
18	PHY_SPECIAL_MODES_x	Port x PHY Special Modes Register, Section 13.3.2.9
27	PHY_SPECIAL_CONTROL_STAT_IND_x	Port x PHY Special Control/Status Indication Register, Section 13.3.2.10
29	PHY_INTERRUPT_SOURCE_x	Port x PHY Interrupt Source Flags Register, Section 13.3.2.11
30	PHY_INTERRUPT_MASK_x	Port x PHY Interrupt Mask Register, Section 13.3.2.12
31	PHY_SPECIAL_CONTROL_STATUS_x	Port x PHY Special Control/Status Register, Section 13.3.2.13

13.3.2.1 Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x)

Index (decimal): 0 Size: 16 bits

This read/write register is used to configure the Port x PHY.

Note: This register is re-written in its entirety by the EEPROM Loader following the release of reset or a RELOAD command. Refer to Section 8.4, "EEPROM Loader," on page 121 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
15	**Reset (PHY_RST)** When set, this bit resets all the Port x PHY registers to their default state, except those marked as NASR type. This bit is self clearing. **0: Normal operation** **1: Reset**	R/W SC	0b
14	**Loopback (PHY_LOOPBACK)** This bit enables/disables the loopback mode. When enabled, transmissions from the Switch Fabric are not sent to network. Instead, they are looped back into the Switch Fabric. **Note:** If loopback is enabled during half-duplex operation, then the Enable Receive Own Transmit bit in the Port x MAC Receive Configuration Register (MAC_RX_CFG_x) must be set for the specified port. Otherwise, the Switch Fabric will ignore receive activity when transmitting in half-duplex mode. **0: Loopback mode disabled (normal operation)** **1: Loopback mode enabled**	R/W	0b
13	**Speed Select LSB (PHY_SPEED_SEL_LSB)** This bit is used to set the speed of the Port x PHY when the Auto-Negotiation (PHY_AN) bit is disabled. **0: 10 Mbps** **1: 100 Mbps**	R/W	Note 13.63
12	**Auto-Negotiation (PHY_AN)** This bit enables/disables Auto-Negotiation. When enabled, the Speed Select LSB (PHY_SPEED_SEL_LSB) and Duplex Mode (PHY_DUPLEX) bits are overridden. **0: Auto-Negotiation disabled** **1: Auto-Negotiation enabled**	R/W	Note 13.64
11	**Power Down (PHY_PWR_DWN)** This bit controls the power down mode of the Port x PHY. After this bit is cleared the PHY may auto-negotiate with it's partner station. This process can take up to a few seconds to complete. Once Auto-Negotiation is complete, the Auto-Negotiation Complete bit of the Port x PHY Basic Status Register (PHY_BASIC_STATUS_x) will be set. **Note:** The PHY_AN bit of this register must be cleared before setting this bit. **0: Normal operation** **1: General power down mode**	R/W	0b
10	**RESERVED**	RO	-

BITS	DESCRIPTION	TYPE	DEFAULT
9	**Restart Auto-Negotiation (PHY_RST_AN)** When set, this bit restarts the Auto-Negotiation process. **0: Normal operation** **1: Auto-Negotiation restarted**	R/W SC	0b
8	**Duplex Mode (PHY_DUPLEX)** This bit is used to set the duplex when the Auto-Negotiation (PHY_AN) bit is disabled. **0: Half Duplex** **1: Full Duplex**	R/W	Note 13.65
7	**Collision Test Mode (PHY_COL_TEST)** This bit enables/disables the collision test mode of the Port x PHY. When set, the collision signal is active during transmission. It is recommended that this feature be used only in loopback mode. **0: Collision test mode disabled** **1: Collision test mode enabled**	R/W	0b
6:0	**RESERVED**	RO	-

Note 13.63 For Port 1 operating in an external mode (MII PHY, RMII PHY, or MII MAC mode), the default value of this bit is 1 and is independent of any strap. For Port 1 operating in Internal PHY mode and for all operating modes of Port 2, the default value of this bit is determined by the logical OR of the Auto-Negotiation strap (autoneg_strap_1 for Port 1 PHY, autoneg_strap_2 for Port 2 PHY) and the Speed Select strap (speed_strap_1 for Port 1 PHY, speed_strap_2 for Port 2 PHY). Essentially, if the Auto-Negotiation strap is set, the default value is 1, otherwise the default is determined by the value of the Speed Select strap. Refer to Section 4.2.4, "Configuration Straps," on page 52 for more information.

Note 13.64 For Port 1 operating in an external mode (MII PHY, RMII PHY, or MII MAC mode), the default value of this bit is 0 and is independent of any strap. For Port 1 operating in Internal PHY mode and for all operating modes of Port 2, the default value of this bit is the value of the Auto-Negotiation strap (autoneg_strap_1 for Port 1 PHY, autoneg_strap_2 for Port 2 PHY). Refer to Section 4.2.4, "Configuration Straps," on page 52 for more information.

Note 13.65 For Port 1 operating in an external mode (MII PHY, RMII PHY, or MII MAC mode), the default value of this bit is 0 and is independent of any strap. For Port 1 operating in Internal PHY mode and for all operating modes of Port 2, the default value of this bit is determined by the logical AND of the negation of the Auto-Negotiation strap (autoneg_strap_1 for Port 1 PHY, autoneg_strap_2 for Port 2 PHY) and the Duplex Select strap (duplex_strap_1 for Port 1 PHY, duplex_strap_2 for Port 2 PHY). Essentially, if the Auto-Negotiation strap is set, the default value is 0, otherwise the default is determined by the value of the Duplex Select strap. Refer to Section 4.2.4, "Configuration Straps," on page 52 for more information.

13.3.2.2 Port x PHY Basic Status Register (PHY_BASIC_STATUS_x)

Index (decimal): 1 Size: 16 bits

This register is used to monitor the status of the Port x PHY.

BITS	DESCRIPTION	TYPE	DEFAULT
15	**100BASE-T4** This bit displays the status of 100BASE-T4 compatibility. **0: PHY not able to perform 100BASE-T4** **1: PHY able to perform 100BASE-T4**	RO	0b Note 13.66
14	**100BASE-X Full Duplex** This bit displays the status of 100BASE-X full duplex compatibility. **0: PHY not able to perform 100BASE-X full duplex** **1: PHY able to perform 100BASE-X full duplex**	RO	1b
13	**100BASE-X Half Duplex** This bit displays the status of 100BASE-X half duplex compatibility. **0: PHY not able to perform 100BASE-X half duplex** **1: PHY able to perform 100BASE-X half duplex**	RO	1b
12	**10BASE-T Full Duplex** This bit displays the status of 10BASE-T full duplex compatibility. **0: PHY not able to perform 10BASE-T full duplex** **1: PHY able to perform 10BASE-T full duplex**	RO	1b
11	**10BASE-T Half Duplex** This bit displays the status of 10BASE-T half duplex compatibility. **0: PHY not able to perform 10BASE-T half duplex** **1: PHY able to perform 10BASE-T half duplex**	RO	1b
10	**100BASE-T2 Full Duplex** This bit displays the status of 100BASE-T2 full duplex compatibility. **0: PHY not able to perform 100BASE-T2 full duplex** **1: PHY able to perform 100BASE-T2 full duplex**	RO	0b Note 13.66
9	**100BASE-T2 Half Duplex** This bit displays the status of 100BASE-T2 half duplex compatibility. **0: PHY not able to perform 100BASE-T2 half duplex** **1: PHY able to perform 100BASE-T2 half duplex**	RO	0b Note 13.66
8:6	**RESERVED**	RO	-
5	**Auto-Negotiation Complete** This bit indicates the status of the Auto-Negotiation process. **0: Auto-Negotiation process not completed** **1: Auto-Negotiation process completed**	RO	0b
4	**Remote Fault** This bit indicates if a remote fault condition has been detected. **0: No remote fault condition detected** **1: Remote fault condition detected**	RO/LH	0b

BITS	DESCRIPTION	TYPE	DEFAULT
3	**Auto-Negotiation Ability** This bit indicates the status of the PHY's auto-negotiation. **0: PHY is unable to perform auto-negotiation** **1: PHY is able to perform auto-negotiation**	RO	1b
2	**Link Status** This bit indicates the status of the link. **0: Link is down** **1: Link is up**	RO/LL	0b
1	**Jabber Detect** This bit indicates the status of the jabber condition. **0: No jabber condition detected** **1: Jabber condition detected**	RO/LH	0b
0	**Extended Capability** This bit indicates whether extended register capability is supported. **0: Basic register set capabilities only** **1: Extended register set capabilities**	RO	1b

Note 13.66 The PHY supports 100BASE-TX (half and full duplex) and 10BASE-T (half and full duplex) only. All other modes will always return as 0 (unable to perform).

13.3.2.3 Port x PHY Identification MSB Register (PHY_ID_MSB_x)

Index (decimal): 2 Size: 16 bits

This read/write register contains the MSB of the Organizationally Unique Identifier (OUI) for the Port x PHY. The LSB of the PHY OUI is contained in the Port x PHY Identification LSB Register (PHY_ID_LSB_x).

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**PHY ID** This field is assigned to the 3rd through 18th bits of the OUI, respectively (OUI = 00800Fh).	R/W	0007h

13.3.2.4 Port x PHY Identification LSB Register (PHY_ID_LSB_x)

Index (decimal): 3 Size: 16 bits

This read/write register contains the LSB of the Organizationally Unique Identifier (OUI) for the Port x PHY. The MSB of the PHY OUI is contained in the Port x PHY Identification MSB Register (PHY_ID_MSB_x).

BITS	DESCRIPTION	TYPE	DEFAULT
15:10	**PHY ID** This field is assigned to the 19th through 24th bits of the PHY OUI, respectively. (OUI = 00800Fh).	R/W	110000b
9:4	**Model Number** This field contains the 6-bit manufacturer's model number of the PHY.	R/W	001101b
3:0	**Revision Number** This field contain the 4-bit manufacturer's revision number of the PHY.	R/W	0001b

13.3.2.5 Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x)

Index (decimal): 4 Size: 16 bits

This read/write register contains the advertised ability of the Port x PHY and is used in the Auto-Negotiation process with the link partner.

Note: This register is re-written by the EEPROM Loader following the release of reset or a RELOAD command. Refer to Section 8.4, "EEPROM Loader," on page 121 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
15:14	**RESERVED**	RO	-
13	**Remote Fault** This bit determines if remote fault indication will be advertised to the link partner. **0: Remote fault indication not advertised** **1: Remote fault indication advertised**	R/W	0b
12	**RESERVED** **Note:** This bit should be written as 0.	R/W	0b
11	**Asymmetric Pause** This bit determines the advertised asymmetric pause capability. **0: No Asymmetric PAUSE toward link partner advertised** **1: Asymmetric PAUSE toward link partner advertised**	R/W	Note 13.67
10	**Symmetric Pause** This bit determines the advertised symmetric pause capability. **0: No Symmetric PAUSE toward link partner advertised** **1: Symmetric PAUSE toward link partner advertised**	R/W	Note 13.67
9	**RESERVED**	RO	-
8	**100BASE-X Full Duplex** This bit determines the advertised 100BASE-X full duplex capability. **0: 100BASE-X full duplex ability not advertised** **1: 100BASE-X full duplex ability advertised**	R/W	Note 13.68
7	**100BASE-X Half Duplex** This bit determines the advertised 100BASE-X half duplex capability. **0: 100BASE-X half duplex ability not advertised** **1: 100BASE-X half duplex ability advertised**	R/W	1b
6	**10BASE-T Full Duplex** This bit determines the advertised 10BASE-T full duplex capability. **0: 10BASE-T full duplex ability not advertised** **1: 10BASE-T full duplex ability advertised**	R/W	Note 13.69 Table 13.9

BITS	DESCRIPTION	TYPE	DEFAULT
5	**10BASE-T Half Duplex** This bit determines the advertised 10BASE-T half duplex capability. **0: 10BASE-T half duplex ability not advertised** **1: 10BASE-T half duplex ability advertised**	R/W	Note 13.70 Table 13.10
4:0	**Selector Field** This field identifies the type of message being sent by Auto-Negotiation. **00001: IEEE 802.3**	R/W	00001b

Note 13.67 The Asymmetric Pause and Symmetric Pause bits are loaded into the PHY registers by the EEPROM Loader. For Port 1 operating in an external mode (MII PHY, RMII PHY, or MII MAC mode), the default value of both these bits is 0 and is independent of any strap. For Port 1 operating in Internal PHY mode and for all operating modes of Port 2, the default values of the Asymmetric Pause and Symmetric Pause bits are determined by the Manual Flow Control Enable Strap (manual_FC_strap_1 for Port 1 PHY, manual_FC_strap_2 for Port 2 PHY). When the Manual Flow Control Enable Strap is 0, the Symmetric Pause bit defaults to 1 and the Asymmetric Pause bit defaults to the setting of the Full Duplex Flow Control Enable Strap (FD_FC_strap_1 for Port 1 PHY, FD_FC_strap_2 for Port 2 PHY). When the Manual Flow Control Enable Strap is 1, both bits default to 0. Configuration strap values are latched upon the de-assertion of a chip-level reset as described in Section 4.2.4, "Configuration Straps," on page 52. Refer to Section 4.2.4, "Configuration Straps," on page 52 for configuration strap definitions.

Note 13.68 For Port 1 operating in an external mode (MII PHY, RMII PHY, or MII MAC mode), the default value of this bit is 0. For Port 1 operating in Internal PHY mode and for all operating modes of Port 2, the default value is 1.

Note 13.69 For Port 1 operating in an external mode (MII PHY, RMII PHY, or MII MAC mode), the default value of this bit is 1 and is independent of any strap. For Port 1 operating in Internal PHY mode and for all operating modes of Port 2, the default value of this bit is determined by the logical OR of the Auto-Negotiation Enable strap (autoneg_strap_1 for Port 1 PHY, autoneg_strap_2 for Port 2 PHY) with the logical AND of the negated Speed Select strap (speed_strap_1 for Port 1 PHY, speed_strap_2 for Port 2 PHY) and the Duplex Select Strap (duplex_strap_1 for Port 1 PHY, duplex_strap_2 for Port 2 PHY). Table 13.9 defines the default behavior of this bit. Configuration strap values are latched upon the de-assertion of a chip-level reset as described in Section 4.2.4, "Configuration Straps," on page 52. Refer to Section 4.2.4, "Configuration Straps," on page 52 for configuration strap definitions.

Table 13.9 10BASE-T Full Duplex Advertisement Default Value

autoneg_strap_x	speed_strap_x	duplex_strap_x	Default 10BASE-T Full Duplex Value
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Note 13.70 For Port 1 operating in an external mode (MII PHY, RMII PHY, or MII MAC mode), the default value of this bit is 1 and is independent of any strap. For Port 1 operating in Internal PHY mode and for all operating modes of Port 2, the default value of this bit is determined by the logical OR of the Auto-Negotiation Enable strap (autoneg_strap_1 for Port 1 PHY, autoneg_strap_2 for Port 2 PHY) and the negated Speed Select strap (speed_strap_1 for Port 1 PHY, speed_strap_2 for Port 2 PHY). Table 13.10 defines the default behavior of this bit. Configuration strap values are latched upon the de-assertion of a chip-level reset as described in Section 4.2.4, "Configuration Straps," on page 52. Refer to Section 4.2.4, "Configuration Straps," on page 52 for configuration strap definitions.

Table 13.10 10BASE-T Half Duplex Advertisement Bit Default Value

autoneg_strap_x	speed_strap_x	Default 10BASE-T Half Duplex Value
0	0	1
0	1	0
1	0	1
1	1	1

13.3.2.6 Port x PHY Auto-Negotiation Link Partner Base Page Ability Register (PHY_AN_LP_BASE_ABILITY_x)

Index (decimal): 5 Size: 16 bits

This read-only register contains the advertised ability of the link partner's PHY and is used in the Auto-Negotiation process between the link partner and the Port x PHY.

BITS	DESCRIPTION	TYPE	DEFAULT
15	**Next Page** This bit indicates the link partner PHY page capability. **0: Link partner PHY does not advertise next page capability** **1: Link partner PHY advertises next page capability**	RO	0b
14	**Acknowledge** This bit indicates whether the link code word has been received from the partner. **0: Link code word not yet received from partner** **1: Link code word received from partner**	RO	0b
13	**Remote Fault** This bit indicates whether a remote fault has been detected. **0: No remote fault** **1: Remote fault detected**	RO	0b
12	**RESERVED**	RO	-
11	**Asymmetric Pause** This bit indicates the link partner PHY asymmetric pause capability. **0: No Asymmetric PAUSE toward link partner** **1: Asymmetric PAUSE toward link partner**	RO	0b
10	**Pause** This bit indicates the link partner PHY symmetric pause capability. **0: No Symmetric PAUSE toward link partner** **1: Symmetric PAUSE toward link partner**	RO	0b
9	**100BASE-T4** This bit indicates the link partner PHY 100BASE-T4 capability. **0: 100BASE-T4 ability not supported** **1: 100BASE-T4 ability supported**	RO	0b
8	**100BASE-X Full Duplex** This bit indicates the link partner PHY 100BASE-X full duplex capability. **0: 100BASE-X full duplex ability not supported** **1: 100BASE-X full duplex ability supported**	RO	0b
7	**100BASE-X Half Duplex** This bit indicates the link partner PHY 100BASE-X half duplex capability. **0: 100BASE-X half duplex ability not supported** **1: 100BASE-X half duplex ability supported**	RO	0b

BITS	DESCRIPTION	TYPE	DEFAULT
6	**10BASE-T Full Duplex** This bit indicates the link partner PHY 10BASE-T full duplex capability. **0: 10BASE-T full duplex ability not supported** **1: 10BASE-T full duplex ability supported**	RO	0b
5	**10BASE-T Half Duplex** This bit indicates the link partner PHY 10BASE-T half duplex capability. **0: 10BASE-T half duplex ability not supported** **1: 10BASE-T half duplex ability supported**	RO	0b
4:0	**Selector Field** This field identifies the type of message being sent by Auto-Negotiation. **00001: IEEE 802.3**	RO	00001b Note 13.71

Note 13.71 The Port 1 & 2 PHY's support only IEEE 802.3.

13.3.2.7 Port x PHY Auto-Negotiation Expansion Register (PHY_AN_EXP_x)

Index (decimal): 6 Size: 16 bits

This read/write register is used in the Auto-Negotiation process between the link partner and the Port x PHY.

BITS	DESCRIPTION	TYPE	DEFAULT
15:5	**RESERVED**	RO	-
4	**Parallel Detection Fault** This bit indicates whether a Parallel Detection Fault has been detected. **0: A fault hasn't been detected via the Parallel Detection function** **1: A fault has been detected via the Parallel Detection function**	RO/LH	0b
3	**Link Partner Next Page Able** This bit indicates whether the link partner has next page ability. **0: Link partner does not contain next page capability** **1: Link partner contains next page capability**	RO	0b
2	**Local Device Next Page Able** This bit indicates whether the local device has next page ability. **0: Local device does not contain next page capability** **1: Local device contains next page capability**	RO	0b
1	**Page Received** This bit indicates the reception of a new page. **0: A new page has not been received** **1: A new page has been received**	RO/LH	0b
0	**Link Partner Auto-Negotiation Able** This bit indicates the Auto-negotiation ability of the link partner. **0: Link partner is not Auto-Negotiation able** **1: Link partner is Auto-Negotiation able**	RO	0b

13.3.2.8 Port x PHY Mode Control/Status Register (PHY_MODE_CONTROL_STATUS_x)

Index (decimal): 17 Size: 16 bits

This read/write register is used to control and monitor various Port x PHY configuration options.

BITS	DESCRIPTION	TYPE	DEFAULT
15:14	**RESERVED**	RO	-
13	**Energy Detect Power-Down (EDPWRDOWN)** This bit controls the Energy Detect Power-Down mode. **0: Energy Detect Power-Down is disabled** **1: Energy Detect Power-Down is enabled**	R/W	0b
12:2	**RESERVED**	RO	-
1	**Energy On (ENERGYON)** This bit indicates whether energy is detected on the line. It is cleared if no valid energy is detected within 256ms. This bit is unaffected by a software reset and is reset to 1 by a hardware reset. **0: No valid energy detected on the line** **1: Energy detected on the line**	RO	1b
0	**RESERVED**	R/W	0b

13.3.2.9 Port x PHY Special Modes Register (PHY_SPECIAL_MODES_x)

Index (decimal): 18 Size: 16 bits

This read/write register is used to control the special modes of the Port x PHY.

Note: This register is re-written by the EEPROM Loader following the release of reset or a RELOAD command. Refer to Section 8.4, "EEPROM Loader," on page 121 for more information.

BITS	DESCRIPTION	TYPE	DEFAULT
15:8	**RESERVED**	RO	-
7:5	**PHY Mode (MODE[2:0])** This field reflects the default PHY mode of operation. Refer to Table 13.11 for a definition of each mode.	R/W NASR Note 13.72	Note 13.73
4:0	**PHY Address (PHYADD)** The PHY Address field determines the MMI address to which the PHY will respond and is also used for initialization of the cipher (scrambler) key. Each PHY must have a unique address. Refer to Section 7.1.1, "PHY Addressing," on page 96 for additional information. **Note:** No check is performed to ensure this address is unique from the other PHY addresses (Port 1 PHY, Port 2 PHY, and Virtual PHY).	R/W NASR Note 13.72	Note 13.74

Note 13.72 Register bits designated as NASR are reset when the Port x PHY Reset is generated via the Reset Control Register (RESET_CTL). The NASR designation is only applicable when the Reset (PHY_RST) bit of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) is set.

Note 13.73 For Port 1 operating in an external mode (MII PHY, RMII PHY, or MII MAC mode), the default value of this field is 110b and is independent of any strap. For Port 1 operating in Internal PHY mode and for all operating modes of Port 2, the default value of this field is determined by a combination of the configuration straps autoneg_strap_x, speed_strap_x, and duplex_strap_x. If the autoneg_strap_x is 1, then the default MODE[2:0] value is 111b. Else, the default value of this field is determined by the remaining straps. MODE[2]=0, MODE[1]=(speed_strap_1 for Port 1 PHY, speed_strap_2 for Port 2 PHY), and MODE[0]=(duplex_strap_1 for Port 1 PHY, duplex_strap_2 for Port 2 PHY). Configuration strap values are latched upon the de-assertion of a chip-level reset as described in Section 4.2.4, "Configuration Straps," on page 52. Refer to Section 4.2.4, "Configuration Straps," on page 52 for strap definitions.

Note 13.74 The default value of this field is determined by the phy_addr_sel_strap configuration strap. Refer to Section 7.1.1, "PHY Addressing," on page 96 for additional information.

Table 13.11 MODE[2:0] Definitions

MODE[2:0]	MODE DEFINITIONS
000	10BASE-T Half Duplex. Auto-negotiation disabled.
001	10BASE-T Full Duplex. Auto-negotiation disabled.
010	100BASE-TX Half Duplex. Auto-negotiation disabled. CRS is active during Transmit & Receive.
011	100BASE-TX Full Duplex. Auto-negotiation disabled. CRS is active during Receive.
100	RESERVED
101	RESERVED
110	Power Down mode.
111	All capable. Auto-negotiation enabled.

13.3.2.10 Port x PHY Special Control/Status Indication Register (PHY_SPECIAL_CONTROL_STAT_IND_x)

Index (decimal): 27 Size: 16 bits

This read/write register is used to control various options of the Port x PHY.

BITS	DESCRIPTION	TYPE	DEFAULT
15	**Auto-MDIX Control (AMDIXCTRL)** This bit is responsible for determining the source of Auto-MDIX control for Port x. When set, the Manual MDIX and Auto MDIX straps (manual_mdix_strap_1/auto_mdix_strap_1 for Port 1 PHY, manual_mdix_strap_2/auto_mdix_strap_2 for Port 2 PHY) are overridden, and Auto-MDIX functions are controlled using the AMDIXEN and AMDIXSTATE bits of this register. When cleared, Auto-MDIX functionality is controlled by the Manual MDIX and Auto MDIX straps by default. Refer to Section 4.2.4, "Configuration Straps," on page 52 for configuration strap definitions. **0: Port x Auto-MDIX determined by strap inputs (Table 13.13)** **1: Port x Auto-MDIX determined by bits AMDIXEN and AMDIXSTATE bits** **Note:** The values of auto_mdix_strap_1 and auto_mdix_strap_2 are indicated in the AMDIX_EN Strap State Port 1 and the AMDIX_EN Strap State Port 2 bits of the Hardware Configuration Register (HW_CFG).	R/W NASR Note 13.75	0b
14	**Auto-MDIX Enable (AMDIXEN)** When the AMDIXCTRL bit of this register is set, this bit is used in conjunction with the AMDIXSTATE bit to control the Port x Auto-MDIX functionality as shown in Table 13.12.	R/W NASR Note 13.75	0b
13	**Auto-MDIX State (AMDIXSTATE)** When the AMDIXCTRL bit of this register is set, this bit is used in conjunction with the AMDIXEN bit to control the Port x Auto-MDIX functionality as shown in Table 13.12.	R/W NASR Note 13.75	0b
12	**RESERVED**	RO	-
11	**SQE Test Disable (SQEOFF)** This bit controls the disabling of the SQE test (Heartbeat). SQE test is enabled by default. **0: SQE test enabled** **1: SQE test disabled**	R/W NASR Note 13.75	0b
10	**Receive PLL Lock Control (VCOOFF_LP)** This bit controls the locking of the receive PLL. Setting this bit to 1 forces the receive PLL 10M to lock on the reference clock at all times. When in this mode, 10M data packets cannot be received. **0: Receive PLL 10M can lock on reference or line as needed (normal operation)** **1: Receive PLL 10M locked onto reference clock at all times**	R/W NASR Note 13.75	0b
9:5	**RESERVED**	RO	-
4	**10Base-T Polarity State (XPOL)** This bit shows the polarity state of the 10Base-T. **0: Normal Polarity** **1: Reversed Polarity**	RO	0b
3:0	**RESERVED**	RO	-

Note 13.75 Register bits designated as NASR are reset when the Port x PHY Reset is generated via the Reset Control Register (RESET_CTL). The NASR designation is only applicable when the Reset (PHY_RST) bit of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) is set.

Table 13.12 Auto-MDIX Enable and Auto-MDIX State Bit Functionality

Auto-MDIX Enable	Auto-MDIX State	MODE
0	0	Manual mode, no crossover
0	1	Manual mode, crossover
1	0	Auto-MDIX mode
1	1	RESERVED (do not use this state)

Table 13.13 MDIX Strap Functionality

auto_mdix_strap_x	manual_mdix_strap_x	MODE
0	0	Manual mode, no crossover
0	1	Manual mode, crossover
1	x	Auto-MDIX mode

13.3.2.11 Port x PHY Interrupt Source Flags Register (PHY_INTERRUPT_SOURCE_x)

Index (decimal): 29 Size: 16 bits

This read-only register is used to determine to source of various Port x PHY interrupts. All interrupt source bits in this register are read-only and latch high upon detection of the corresponding interrupt (if enabled). A read of this register clears the interrupts. These interrupts are enabled or masked via the Port x PHY Interrupt Mask Register (PHY_INTERRUPT_MASK_x).

BITS	DESCRIPTION	TYPE	DEFAULT
15:8	**RESERVED**	RO	-
7	**INT7** This interrupt source bit indicates when the Energy On (ENERGYON) bit of the Port x PHY Mode Control/Status Register (PHY_MODE_CONTROL_STATUS_x) has been set. **0: Not source of interrupt** **1: ENERGYON generated**	RO/LH	0b
6	**INT6** This interrupt source bit indicates Auto-Negotiation is complete. **0: Not source of interrupt** **1: Auto-Negotiation complete**	RO/LH	0b
5	**INT5** This interrupt source bit indicates a remote fault has been detected. **0: Not source of interrupt** **1: Remote fault detected**	RO/LH	0b
4	**INT4** This interrupt source bit indicates a Link Down (link status negated). **0: Not source of interrupt** **1: Link Down (link status negated)**	RO/LH	0b
3	**INT3** This interrupt source bit indicates an Auto-Negotiation LP acknowledge. **0: Not source of interrupt** **1: Auto-Negotiation LP acknowledge**	RO/LH	0b
2	**INT2** This interrupt source bit indicates a Parallel Detection fault. **0: Not source of interrupt** **1: Parallel Detection fault**	RO/LH	0b
1	**INT1** This interrupt source bit indicates an Auto-Negotiation page received. **0: Not source of interrupt** **1: Auto-Negotiation page received**	RO/LH	0b
0	**RESERVED**	RO	-

13.3.2.12 Port x PHY Interrupt Mask Register (PHY_INTERRUPT_MASK_x)

Index (decimal): 30 Size: 16 bits

This read/write register is used to enable or mask the various Port x PHY interrupts and is used in conjunction with the Port x PHY Interrupt Source Flags Register (PHY_INTERRUPT_SOURCE_x).

BITS	DESCRIPTION	TYPE	DEFAULT
15:8	**RESERVED**	RO	-
7	**INT7_MASK** This interrupt mask bit enables/masks the ENERGYON interrupt. **0: Interrupt source is masked** **1: Interrupt source is enabled**	R/W	0b
6	**INT6_MASK** This interrupt mask bit enables/masks the Auto-Negotiation interrupt. **0: Interrupt source is masked** **1: Interrupt source is enabled**	R/W	0b
5	**INT5_MASK** This interrupt mask bit enables/masks the remote fault interrupt. **0: Interrupt source is masked** **1: Interrupt source is enabled**	R/W	0b
4	**INT4_MASK** This interrupt mask bit enables/masks the Link Down (link status negated) interrupt. **0: Interrupt source is masked** **1: Interrupt source is enabled**	R/W	0b
3	**INT3_MASK** This interrupt mask bit enables/masks the Auto-Negotiation LP acknowledge interrupt. **0: Interrupt source is masked** **1: Interrupt source is enabled**	R/W	0b
2	**INT2_MASK** This interrupt mask bit enables/masks the Parallel Detection fault interrupt. **0: Interrupt source is masked** **1: Interrupt source is enabled**	R/W	0b
1	**INT1_MASK** This interrupt mask bit enables/masks the Auto-Negotiation page received interrupt. **0: Interrupt source is masked** **1: Interrupt source is enabled**	R/W	0b
0	**RESERVED**	RO	-

13.3.2.13 Port x PHY Special Control/Status Register (PHY_SPECIAL_CONTROL_STATUS_x)

Index (decimal): 31 Size: 16 bits

This read/write register is used to control and monitor various options of the Port x PHY.

BITS	DESCRIPTION	TYPE	DEFAULT
15:13	**RESERVED**	RO	-
12	**Autodone** This bit indicates the status of the Auto-Negotiation on the Port x PHY. **0: Auto-Negotiation is not completed, is disabled, or is not active** **1: Auto-Negotiation is completed**	RO	0b
11:5	**RESERVED - Write as 0000010b, ignore on read**	R/W	0000010b
4:2	**Speed Indication** This field indicates the current Port x speed configuration. STATE / DESCRIPTION: 000 RESERVED 001 10BASE-T Half-duplex 010 100BASE-TX Half-duplex 011 RESERVED 100 RESERVED 101 10BASE-T Full-duplex 110 100BASE-TX Full-duplex 111 RESERVED	RO	Note 13.76
1:0	**RESERVED**	R/W	0b

Note 13.76 Default value is 010b if any external MII mode is selected, else 000b.

13.4 Switch Fabric Control and Status Registers

This section details the various switch control and status registers that reside within the Switch Fabric. The switch control and status registers allow configuration of each individual switch port, the Switch Engine, and Buffer Manager. Switch Fabric related interrupts and resets are also controlled and monitored via the switch CSRs.

The switch CSRs are not memory mapped. All switch CSRs are accessed indirectly via the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD), Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA), and Switch Fabric CSR Interface Direct Data Registers (SWITCH_CSR_DIRECT_DATA) in the system CSR memory mapped address space. All accesses to the switch CSRs must be performed through these registers. Refer to Section 13.2.4, "Switch Fabric" for additional information.

Note: The flow control settings of the switch ports are configured via the Switch Fabric registers: Port 1 Manual Flow Control Register (MANUAL_FC_1), Port 2 Manual Flow Control Register (MANUAL_FC_2), and Port 0 Manual Flow Control Register (MANUAL_FC_0) located in the system CSR address space.

Table 13.14 lists the Switch CSRs and their corresponding addresses in order. The Switch Fabric registers can be categorized into the following sub-sections:

- Section 13.4.1, "General Switch CSRs," on page 239
- Section 13.4.2, "Switch Port 0, Port 1, and Port 2 CSRs," on page 243
- Section 13.4.3, "Switch Engine CSRs," on page 287
- Section 13.4.4, "Buffer Manager CSRs," on page 334

Table 13.14 Indirectly Accessible Switch Control and Status Registers

REGISTER #	SYMBOL	REGISTER NAME
General Switch CSRs		
0000h	SW_DEV_ID	Switch Device ID Register, Section 13.4.1.1
0001h	SW_RESET	Switch Reset Register, Section 13.4.1.2
0002h-0003h	RESERVED	Reserved for Future Use
0004h	SW_IMR	Switch Global Interrupt Mask Register, Section 13.4.1.3
0005h	SW_IPR	Switch Global Interrupt Pending Register, Section 13.4.1.4
0006h-03FFh	RESERVED	Reserved for Future Use
Switch Port 0 CSRs		
0400h	MAC_VER_ID_0	Port 0 MAC Version ID Register, Section 13.4.2.1
0401h	MAC_RX_CFG_0	Port 0 MAC Receive Configuration Register, Section 13.4.2.2
0402h-040Fh	RESERVED	Reserved for Future Use
0410h	MAC_RX_UNDSZE_CNT_0	Port 0 MAC Receive Undersize Count Register, Section 13.4.2.3
0411h	MAC_RX_64_CNT_0	Port 0 MAC Receive 64 Byte Count Register, Section 13.4.2.4
0412h	MAC_RX_65_TO_127_CNT_0	Port 0 MAC Receive 65 to 127 Byte Count Register, Section 13.4.2.5

Table 13.14 Indirectly Accessible Switch Control and Status Registers (continued)

REGISTER #	SYMBOL	REGISTER NAME
0413h	MAC_RX_128_TO_255_CNT_0	Port 0 MAC Receive 128 to 255 Byte Count Register, Section 13.4.2.6
0414h	MAC_RX_256_TO_511_CNT_0	Port 0 MAC Receive 256 to 511 Byte Count Register, Section 13.4.2.7
0415h	MAC_RX_512_TO_1023_CNT_0	Port 0 MAC Receive 512 to 1023 Byte Count Register, Section 13.4.2.8
0416h	MAC_RX_1024_TO_MAX_CNT_0	Port 0 MAC Receive 1024 to Max Byte Count Register, Section 13.4.2.9
0417h	MAC_RX_OVRSZE_CNT_0	Port 0 MAC Receive Oversize Count Register, Section 13.4.2.10
0418h	MAC_RX_PKTOK_CNT_0	Port 0 MAC Receive OK Count Register, Section 13.4.2.11
0419h	MAC_RX_CRCERR_CNT_0	Port 0 MAC Receive CRC Error Count Register, Section 13.4.2.12
041Ah	MAC_RX_MULCST_CNT_0	Port 0 MAC Receive Multicast Count Register, Section 13.4.2.13
041Bh	MAC_RX_BRDCST_CNT_0	Port 0 MAC Receive Broadcast Count Register, Section 13.4.2.14
041Ch	MAC_RX_PAUSE_CNT_0	Port 0 MAC Receive Pause Frame Count Register, Section 13.4.2.15
041Dh	MAC_RX_FRAG_CNT_0	Port 0 MAC Receive Fragment Error Count Register, Section 13.4.2.16
041Eh	MAC_RX_JABB_CNT_0	Port 0 MAC Receive Jabber Error Count Register, Section 13.4.2.17
041Fh	MAC_RX_ALIGN_CNT_0	Port 0 MAC Receive Alignment Error Count Register, Section 13.4.2.18
0420h	MAC_RX_PKTLEN_CNT_0	Port 0 MAC Receive Packet Length Count Register, Section 13.4.2.19
0421h	MAC_RX_GOODPKTLEN_CNT_0	Port 0 MAC Receive Good Packet Length Count Register, Section 13.4.2.20
0422h	MAC_RX_SYMBL_CNT_0	Port 0 MAC Receive Symbol Error Count Register, Section 13.4.2.21
0423h	MAC_RX_CTLFRM_CNT_0	Port 0 MAC Receive Control Frame Count Register, Section 13.4.2.22
0424h-043Fh	RESERVED	Reserved for Future Use
0440h	MAC_TX_CFG_0	Port 0 MAC Transmit Configuration Register, Section 13.4.2.23
0441h	MAC_TX_FC_SETTINGS_0	Port 0 MAC Transmit Flow Control Settings Register, Section 13.4.2.24
0442h-0450h	RESERVED	Reserved for Future Use
0451h	MAC_TX_DEFER_CNT_0I	Port 0 MAC Transmit Deferred Count Register, Section 13.4.2.25
0452h	MAC_TX_PAUSE_CNT_0	Port 0 MAC Transmit Pause Count Register, Section 13.4.2.26

Table 13.14 Indirectly Accessible Switch Control and Status Registers (continued)

REGISTER #	SYMBOL	REGISTER NAME
0453h	MAC_TX_PKTOK_CNT_0	Port 0 MAC Transmit OK Count Register, Section 13.4.2.27
0454h	MAC_TX_64_CNT_0	Port 0 MAC Transmit 64 Byte Count Register, Section 13.4.2.28
0455h	MAC_TX_65_TO_127_CNT_0	Port 0 MAC Transmit 65 to 127 Byte Count Register, Section 13.4.2.29
0456h	MAC_TX_128_TO_255_CNT_0	Port 0 MAC Transmit 128 to 255 Byte Count Register, Section 13.4.2.30
0457h	MAC_TX_256_TO_511_CNT_0	Port 0 MAC Transmit 256 to 511 Byte Count Register, Section 13.4.2.31
0458h	MAC_TX_512_TO_1023_CNT_0	Port 0 MAC Transmit 512 to 1023 Byte Count Register, Section 13.4.2.32
0459h	MAC_TX_1024_TO_MAX_CNT_0	Port 0 MAC Transmit 1024 to Max Byte Count Register, Section 13.4.2.33
045Ah	MAC_TX_UNDSZE_CNT_0	Port 0 MAC Transmit Undersize Count Register, Section 13.4.2.34
045Bh	RESERVED	Reserved for Future Use
045Ch	MAC_TX_PKTLEN_CNT_0	Port 0 MAC Transmit Packet Length Count Register, Section 13.4.2.35
045Dh	MAC_TX_BRDCST_CNT_0	Port 0 MAC Transmit Broadcast Count Register, Section 13.4.2.36
045Eh	MAC_TX_MULCST_CNT_0	Port 0 MAC Transmit Multicast Count Register, Section 13.4.2.37
045Fh	MAC_TX_LATECOL_0	Port 0 MAC Transmit Late Collision Count Register, Section 13.4.2.38
0460h	MAC_TX_EXCOL_CNT_0	Port 0 MAC Transmit Excessive Collision Count Register, Section 13.4.2.39
0461h	MAC_TX_SNGLECOL_CNT_0	Port 0 MAC Transmit Single Collision Count Register, Section 13.4.2.40
0462h	MAC_TX_MULTICOL_CNT_0	Port 0 MAC Transmit Multiple Collision Count Register, Section 13.4.2.41
0463h	MAC_TX_TOTALCOL_CNT_0	Port 0 MAC Transmit Total Collision Count Register, Section 13.4.2.42
0464-047Fh	RESERVED	Reserved for Future Use
0480h	MAC_IMR_0	Port 0 MAC Interrupt Mask Register, Section 13.4.2.43
0481h	MAC_IPR_0	Port 0 MAC Interrupt Pending Register, Section 13.4.2.44
0482h-07FFh	RESERVED	Reserved for Future Use
Switch Port 1 CSRs		
0800h	MAC_VER_ID_1	Port 1 MAC Version ID Register, Section 13.4.2.1
0801h	MAC_RX_CFG_1	Port 1 MAC Receive Configuration Register, Section 13.4.2.2
0802h-080Fh	RESERVED	Reserved for Future Use

Table 13.14 Indirectly Accessible Switch Control and Status Registers (continued)

REGISTER #	SYMBOL	REGISTER NAME
0810h	MAC_RX_UNDSZE_CNT_1	Port 1 MAC Receive Undersize Count Register, Section 13.4.2.3
0811h	MAC_RX_64_CNT_1	Port 1 MAC Receive 64 Byte Count Register, Section 13.4.2.4
0812h	MAC_RX_65_TO_127_CNT_1	Port 1 MAC Receive 65 to 127 Byte Count Register, Section 13.4.2.5
0813h	MAC_RX_128_TO_255_CNT_1	Port 1 MAC Receive 128 to 255 Byte Count Register, Section 13.4.2.6
0814h	MAC_RX_256_TO_511_CNT_1	Port 1 MAC Receive 256 to 511 Byte Count Register, Section 13.4.2.7
0815h	MAC_RX_512_TO_1023_CNT_1	Port 1 MAC Receive 512 to 1023 Byte Count Register, Section 13.4.2.8
0816h	MAC_RX_1024_TO_MAX_CNT_1	Port 1 MAC Receive 1024 to Max Byte Count Register, Section 13.4.2.9
0817h	MAC_RX_OVRSZE_CNT_1	Port 1 MAC Receive Oversize Count Register, Section 13.4.2.10
0818h	MAC_RX_PKTOK_CNT_1	Port 1 MAC Receive OK Count Register, Section 13.4.2.11
0819h	MAC_RX_CRCERR_CNT_1	Port 1 MAC Receive CRC Error Count Register, Section 13.4.2.12
081Ah	MAC_RX_MULCST_CNT_1	Port 1 MAC Receive Multicast Count Register, Section 13.4.2.13
081Bh	MAC_RX_BRDCST_CNT_1	Port 1 MAC Receive Broadcast Count Register, Section 13.4.2.14
081Ch	MAC_RX_PAUSE_CNT_1	Port 1 MAC Receive Pause Frame Count Register, Section 13.4.2.15
081Dh	MAC_RX_FRAG_CNT_1	Port 1 MAC Receive Fragment Error Count Register, Section 13.4.2.16
081Eh	MAC_RX_JABB_CNT_1	Port 1 MAC Receive Jabber Error Count Register, Section 13.4.2.17
081Fh	MAC_RX_ALIGN_CNT_1	Port 1 MAC Receive Alignment Error Count Register, Section 13.4.2.18
0820h	MAC_RX_PKTLEN_CNT_1	Port 1 MAC Receive Packet Length Count Register, Section 13.4.2.19
0821h	MAC_RX_GOODPKTLEN_CNT_1	Port 1 MAC Receive Good Packet Length Count Register, Section 13.4.2.20
0822h	MAC_RX_SYMBL_CNT_1	Port 1 MAC Receive Symbol Error Count Register, Section 13.4.2.21
0823h	MAC_RX_CTLFRM_CNT_1	Port 1 MAC Receive Control Frame Count Register, Section 13.4.2.22
0824h-083Fh	RESERVED	Reserved for Future Use
0840h	MAC_TX_CFG_1	Port 1 MAC Transmit Configuration Register, Section 13.4.2.23
0841h	MAC_TX_FC_SETTINGS_1	Port 1 MAC Transmit Flow Control Settings Register, Section 13.4.2.24

Table 13.14 Indirectly Accessible Switch Control and Status Registers (continued)

REGISTER #	SYMBOL	REGISTER NAME
0842h-0850h	RESERVED	Reserved for Future Use
0851h	MAC_TX_DEFER_CNT_1	Port 1 MAC Transmit Deferred Count Register, Section 13.4.2.25
0852h	MAC_TX_PAUSE_CNT_1	Port 1 MAC Transmit Pause Count Register, Section 13.4.2.26
0853h	MAC_TX_PKTOK_CNT_1	Port 1 MAC Transmit OK Count Register, Section 13.4.2.27
0854h	MAC_RX_64_CNT_1	Port 1 MAC Transmit 64 Byte Count Register, Section 13.4.2.28
0855h	MAC_TX_65_TO_127_CNT_1	Port 1 MAC Transmit 65 to 127 Byte Count Register, Section 13.4.2.29
0856h	MAC_TX_128_TO_255_CNT_1	Port 1 MAC Transmit 128 to 255 Byte Count Register, Section 13.4.2.30
0857h	MAC_TX_256_TO_511_CNT_1	Port 1 MAC Transmit 256 to 511 Byte Count Register, Section 13.4.2.31
0858h	MAC_TX_512_TO_1023_CNT_1	Port 1 MAC Transmit 512 to 1023 Byte Count Register, Section 13.4.2.32
0859h	MAC_TX_1024_TO_MAX_CNT_1	Port 1 MAC Transmit 1024 to Max Byte Count Register, Section 13.4.2.33
085Ah	MAC_TX_UNDSZE_CNT_1	Port 1 MAC Transmit Undersize Count Register, Section 13.4.2.34
085Bh	RESERVED	Reserved for Future Use
085Ch	MAC_TX_PKTLEN_CNT_1	Port 1 MAC Transmit Packet Length Count Register, Section 13.4.2.35
085Dh	MAC_TX_BRDCST_CNT_1	Port 1 MAC Transmit Broadcast Count Register, Section 13.4.2.36
085Eh	MAC_TX_MULCST_CNT_1	Port 1 MAC Transmit Multicast Count Register, Section 13.4.2.37
085Fh	MAC_TX_LATECOL_1	Port 1 MAC Transmit Late Collision Count Register, Section 13.4.2.38
0860h	MAC_TX_EXCOL_CNT_1	Port 1 MAC Transmit Excessive Collision Count Register, Section 13.4.2.39
0861h	MAC_TX_SNGLECOL_CNT_1	Port 1 MAC Transmit Single Collision Count Register, Section 13.4.2.40
0862h	MAC_TX_MULTICOL_CNT_1	Port 1 MAC Transmit Multiple Collision Count Register, Section 13.4.2.41
0863h	MAC_TX_TOTALCOL_CNT_1	Port 1 MAC Transmit Total Collision Count Register, Section 13.4.2.42
0864-087Fh	RESERVED	Reserved for Future Use
0880h	MAC_IMR_1	Port 1 MAC Interrupt Mask Register, Section 13.4.2.43
0881h	MAC_IPR_1	Port 1 MAC Interrupt Pending Register, Section 13.4.2.44
0882h-0BFFh	RESERVED	Reserved for Future Use
Switch Port 2 CSRs		

Table 13.14 Indirectly Accessible Switch Control and Status Registers (continued)

REGISTER #	SYMBOL	REGISTER NAME
0C00h	MAC_VER_ID_2	Port 2 MAC Version ID Register, Section 13.4.2.1
0C01h	MAC_RX_CFG_2	Port 2 MAC Receive Configuration Register, Section 13.4.2.2
0C02h-0C0Fh	RESERVED	Reserved for Future Use
0C10h	MAC_RX_UNDSZE_CNT_2	Port 2 MAC Receive Undersize Count Register, Section 13.4.2.3
0C11h	MAC_RX_64_CNT_2	Port 2 MAC Receive 64 Byte Count Register, Section 13.4.2.4
0C12h	MAC_RX_65_TO_127_CNT_2	Port 2 MAC Receive 65 to 127 Byte Count Register, Section 13.4.2.5
0C13h	MAC_RX_128_TO_255_CNT_2	Port 2 MAC Receive 128 to 255 Byte Count Register, Section 13.4.2.6
0C14h	MAC_RX_256_TO_511_CNT_2	Port 2 MAC Receive 256 to 511 Byte Count Register, Section 13.4.2.7
0C15h	MAC_RX_512_TO_1023_CNT_2	Port 2 MAC Receive 512 to 1023 Byte Count Register, Section 13.4.2.8
0C16h	MAC_RX_1024_TO_MAX_CNT_2	Port 2 MAC Receive 1024 to Max Byte Count Register, Section 13.4.2.9
0C17h	MAC_RX_OVRSZE_CNT_2	Port 2 MAC Receive Oversize Count Register, Section 13.4.2.10
0C18h	MAC_RX_PKTOK_CNT_2	Port 2 MAC Receive OK Count Register, Section 13.4.2.11
0C19h	MAC_RX_CRCERR_CNT_2	Port 2 MAC Receive CRC Error Count Register, Section 13.4.2.12
0C1Ah	MAC_RX_MULCST_CNT_2	Port 2 MAC Receive Multicast Count Register, Section 13.4.2.13
0C1Bh	MAC_RX_BRDCST_CNT_2	Port 2 MAC Receive Broadcast Count Register, Section 13.4.2.14
0C1Ch	MAC_RX_PAUSE_CNT_2	Port 2 MAC Receive Pause Frame Count Register, Section 13.4.2.15
0C1Dh	MAC_RX_FRAG_CNT_2	Port 2 MAC Receive Fragment Error Count Register, Section 13.4.2.16
0C1Eh	MAC_RX_JABB_CNT_2	Port 2 MAC Receive Jabber Error Count Register, Section 13.4.2.17
0C1Fh	MAC_RX_ALIGN_CNT_2	Port 2 MAC Receive Alignment Error Count Register, Section 13.4.2.18
0C20h	MAC_RX_PKTLEN_CNT_2	Port 2 MAC Receive Packet Length Count Register, Section 13.4.2.19
0C21h	MAC_RX_GOODPKTLEN_CNT_2	Port 2 MAC Receive Good Packet Length Count Register, Section 13.4.2.20
0C22h	MAC_RX_SYMBL_CNT_2	Port 2 MAC Receive Symbol Error Count Register, Section 13.4.2.21
0C23h	MAC_RX_CTLFRM_CNT_2	Port 2 MAC Receive Control Frame Count Register, Section 13.4.2.22

Table 13.14 Indirectly Accessible Switch Control and Status Registers (continued)

REGISTER #	SYMBOL	REGISTER NAME
0C24h-0C3Fh	RESERVED	Reserved for Future Use
0C40h	MAC_TX_CFG_2	Port 2 MAC Transmit Configuration Register, Section 13.4.2.23
0C41h	MAC_TX_FC_SETTINGS_2	Port 2 MAC Transmit Flow Control Settings Register, Section 13.4.2.24
0C42h-0C50h	RESERVED	Reserved for Future Use
0C51h	MAC_TX_DEFER_CNT_2	Port 2 MAC Transmit Deferred Count Register, Section 13.4.2.25
0C52h	MAC_TX_PAUSE_CNT_2	Port 2 MAC Transmit Pause Count Register, Section 13.4.2.26
0C53h	MAC_TX_PKTOK_CNT_2	Port 2 MAC Transmit OK Count Register, Section 13.4.2.27
0C54h	MAC_RX_64_CNT_2	Port 2 MAC Transmit 64 Byte Count Register, Section 13.4.2.28
0C55h	MAC_TX_65_TO_127_CNT_2	Port 2 MAC Transmit 65 to 127 Byte Count Register, Section 13.4.2.29
0C56h	MAC_TX_128_TO_255_CNT_2	Port 2 MAC Transmit 128 to 255 Byte Count Register, Section 13.4.2.30
0C57h	MAC_TX_256_TO_511_CNT_2	Port 2 MAC Transmit 256 to 511 Byte Count Register, Section 13.4.2.31
0C58h	MAC_TX_512_TO_1023_CNT_2	Port 2 MAC Transmit 512 to 1023 Byte Count Register, Section 13.4.2.32
0C59h	MAC_TX_1024_TO_MAX_CNT_2	Port 2 MAC Transmit 1024 to Max Byte Count Register, Section 13.4.2.33
0C5Ah	MAC_TX_UNDSZE_CNT_2	Port 2 MAC Transmit Undersize Count Register, Section 13.4.2.34
0C5Bh	RESERVED	Reserved for Future Use
0C5Ch	MAC_TX_PKTLEN_CNT_2	Port 2 MAC Transmit Packet Length Count Register, Section 13.4.2.35
0C5Dh	MAC_TX_BRDCST_CNT_2	Port 2 MAC Transmit Broadcast Count Register, Section 13.4.2.36
0C5Eh	MAC_TX_MULCST_CNT_2	Port 2 MAC Transmit Multicast Count Register, Section 13.4.2.37
0C5Fh	MAC_TX_LATECOL_2	Port 2 MAC Transmit Late Collision Count Register, Section 13.4.2.38
0C60h	MAC_TX_EXCOL_CNT_2	Port 2 MAC Transmit Excessive Collision Count Register, Section 13.4.2.39
0C61h	MAC_TX_SNGLECOL_CNT_2	Port 2 MAC Transmit Single Collision Count Register, Section 13.4.2.40
0C62h	MAC_TX_MULTICOL_CNT_2	Port 2 MAC Transmit Multiple Collision Count Register, Section 13.4.2.41
0C63h	MAC_TX_TOTALCOL_CNT_2	Port 2 MAC Transmit Total Collision Count Register, Section 13.4.2.42
0C64-0C7Fh	RESERVED	Reserved for Future Use

Table 13.14 Indirectly Accessible Switch Control and Status Registers (continued)

REGISTER #	SYMBOL	REGISTER NAME
0C80h	MAC_IMR_2	Port 2 MAC Interrupt Mask Register, Section 13.4.2.43
0C81h	MAC_IPR_2	Port 2 MAC Interrupt Pending Register, Section 13.4.2.44
0C82h-17FFh	RESERVED	Reserved for Future Use
Switch Engine CSRs		
1800h	SWE_ALR_CMD	Switch Engine ALR Command Register, Section 13.4.3.1
1801h	SWE_ALR_WR_DAT_0	Switch Engine ALR Write Data 0 Register, Section 13.4.3.2
1802h	SWE_ALR_WR_DAT_1	Switch Engine ALR Write Data 1 Register, Section 13.4.3.3
1803h-1804h	RESERVED	Reserved for Future Use
1805h	SWE_ALR_RD_DAT_0	Switch Engine ALR Read Data 0 Register, Section 13.4.3.4
1806h	SWE_ALR_RD_DAT_1	Switch Engine ALR Read Data 1 Register, Section 13.4.3.5
1807h	RESERVED	Reserved for Future Use
1808h	SWE_ALR_CMD_STS	Switch Engine ALR Command Status Register, Section 13.4.3.6
1809h	SWE_ALR_CFG	Switch Engine ALR Configuration Register, Section 13.4.3.7
180Ah	RESERVED	Reserved for Future Use
180Bh	SWE_VLAN_CMD	Switch Engine VLAN Command Register, Section 13.4.3.8
180Ch	SWE_VLAN_WR_DATA	Switch Engine VLAN Write Data Register, Section 13.4.3.9
180Dh	RESERVED	Reserved for Future Use
180Eh	SWE_VLAN_RD_DATA	Switch Engine VLAN Read Data Register, Section 13.4.3.10
180Fh	RESERVED	Reserved for Future Use
1810h	SWE_VLAN_CMD_STS	Switch Engine VLAN Command Status Register, Section 13.4.3.11
1811h	SWE_DIFFSERV_TBL_CMD	Switch Engine DIFSERV Table Command Register, Section 13.4.3.12
1812h	SWE_DIFFSERV_TBL_WR_DATA	Switch Engine DIFFSERV Table Write Data Register, Section 13.4.3.13
1813h	SWE_DIFFSERV_TBL_RD_DATA	Switch Engine DIFFSERV Table Read Data Register, Section 13.4.3.14
1814h	SWE_DIFFSERV_TBL_CMD_STS	Switch Engine DIFFSERV Table Command Status Register, Section 13.4.3.15
1815h-183Fh	RESERVED	Reserved for Future Use
1840h	SWE_GLB_INGRESS_CFG	Switch Engine Global Ingress Configuration Register, Section 13.4.3.16
1841h	SWE_PORT_INGRESS_CFG	Switch Engine Port Ingress Configuration Register, Section 13.4.3.17
1842h	SWE_ADMT_ONLY_VLAN	Switch Engine Admit Only VLAN Register, Section 13.4.3.18

Table 13.14 Indirectly Accessible Switch Control and Status Registers (continued)

REGISTER #	SYMBOL	REGISTER NAME
1843h	SWE_PORT_STATE	Switch Engine Port State Register, Section 13.4.3.19
1844h	RESERVED	Reserved for Future Use
1845h	SWE_PRI_TO_QUE	Switch Engine Priority to Queue Register, Section 13.4.3.20
1846h	SWE_PORT_MIRROR	Switch Engine Port Mirroring Register, Section 13.4.3.21
1847h	SWE_INGRESS_PORT_TYP	Switch Engine Ingress Port Type Register, Section 13.4.3.22
1848h	SWE_BCST_THROT	Switch Engine Broadcast Throttling Register, Section 13.4.3.23
1849h	SWE_ADMT_N_MEMBER	Switch Engine Admit Non Member Register, Section 13.4.3.24
184Ah	SWE_INGRESS_RATE_CFG	Switch Engine Ingress Rate Configuration Register, Section 13.4.3.25
184Bh	SWE_INGRESS_RATE_CMD	Switch Engine Ingress Rate Command Register, Section 13.4.3.26
184Ch	SWE_INGRESS_RATE_CMD_STS	Switch Engine Ingress Rate Command Status Register, Section 13.4.3.27
184Dh	SWE_INGRESS_RATE_WR_DATA	Switch Engine Ingress Rate Write Data Register, Section 13.4.3.28
184Eh	SWE_INGRESS_RATE_RD_DATA	Switch Engine Ingress Rate Read Data Register, Section 13.4.3.29
184Fh	RESERVED	Reserved for Future Use
1850h	SWE_FILTERED_CNT_0	Switch Engine Port 0 Ingress Filtered Count Register, Section 13.4.3.30
1851h	SWE_FILTERED_CNT_1	Switch Engine Port 1 Ingress Filtered Count Register, Section 13.4.3.31
1852h	SWE_FILTERED_CNT_2	Switch Engine Port 2 Ingress Filtered Count Register, Section 13.4.3.32
1853h-1854h	RESERVED	Reserved for Future Use
1855h	SWE_INGRESS_REGEN_TBL_0	Switch Engine Port 0 Ingress VLAN Priority Regeneration Register, Section 13.4.3.33
1856h	SWE_INGRESS_REGEN_TBL_1	Switch Engine Port 1 Ingress VLAN Priority Regeneration Register, Section 13.4.3.34
1857h	SWE_INGRESS_REGEN_TBL_2	Switch Engine Port 2 Ingress VLAN Priority Regeneration Register, Section 13.4.3.35
1858h	SWE_LRN_DISCRD_CNT_0	Switch Engine Port 0 Learn Discard Count Register, Section 13.4.3.36
1859h	SWE_LRN_DISCRD_CNT_1	Switch Engine Port 1 Learn Discard Count Register, Section 13.4.3.37
185Ah	SWE_LRN_DISCRD_CNT_2	Switch Engine Port 2 Learn Discard Count Register, Section 13.4.3.38
185Bh-187Fh	RESERVED	Reserved for Future Use
1880h	SWE_IMR	Switch Engine Interrupt Mask Register, Section 13.4.3.39

Table 13.14 Indirectly Accessible Switch Control and Status Registers (continued)

REGISTER #	SYMBOL	REGISTER NAME
1881h	SWE_IPR	Switch Engine Interrupt Pending Register, Section 13.4.3.40
1882h-1BFFh	RESERVED	Reserved for Future Use
Buffer Manager (BM) CSRs		
1C00h	BM_CFG	Buffer Manager Configuration Register, Section 13.4.4.1
1C01h	BM_DROP_LVL	Buffer Manager Drop Level Register, Section 13.4.4.2
1C02h	BM_FC_PAUSE_LVL	Buffer Manager Flow Control Pause Level Register, Section 13.4.4.3
1C03h	BM_FC_RESUME_LVL	Buffer Manager Flow Control Resume Level Register, Section 13.4.4.4
1C04h	BM_BCST_LVL	Buffer Manager Broadcast Buffer Level Register, Section 13.4.4.5
1C05h	BM_DRP_CNT_SRC_0	Buffer Manager Port 0 Drop Count Register, Section 13.4.4.6
1C06h	BM_DRP_CNT_SRC_1	Buffer Manager Port 1 Drop Count Register, Section 13.4.4.7
1C07h	BM_DRP_CNT_SRC_2	Buffer Manager Port 2 Drop Count Register, Section 13.4.4.8
1C08h	BM_RST_STS	Buffer Manager Reset Status Register, Section 13.4.4.9
1C09h	BM_RNDM_DSCRD_TBL_CMD	Buffer Manager Random Discard Table Command Register, Section 13.4.4.10
1C0Ah	BM_RNDM_DSCRD_TBL_WDATA	Buffer Manager Random Discard Table Write Data Register, Section 13.4.4.11
1C0Bh	BM_RNDM_DSCRD_TBL_RDATA	Buffer Manager Random Discard Table Read Data Register, Section 13.4.4.12
1C0Ch	BM_EGRSS_PORT_TYPE	Buffer Manager Egress Port Type Register, Section 13.4.4.13
1C0Dh	BM_EGRSS_RATE_00_01	Buffer Manager Port 0 Egress Rate Priority Queue 0/1 Register, Section 13.4.4.14
1C0Eh	BM_EGRSS_RATE_02_03	Buffer Manager Port 0 Egress Rate Priority Queue 2/3 Register, Section 13.4.4.15
1C0Fh	BM_EGRSS_RATE_10_11	Buffer Manager Port 1 Egress Rate Priority Queue 0/1 Register, Section 13.4.4.16
1C10h	BM_EGRSS_RATE_12_13	Buffer Manager Port 1 Egress Rate Priority Queue 2/3 Register, Section 13.4.4.17
1C11h	BM_EGRSS_RATE_20_21	Buffer Manager Port 2 Egress Rate Priority Queue 0/1 Register, Section 13.4.4.18
1C12h	BM_EGRSS_RATE_22_23	Buffer Manager Port 2 Egress Rate Priority Queue 2/3 Register, Section 13.4.4.19
1C13h	BM_VLAN_0	Buffer Manager Port 0 Default VLAN ID and Priority Register, Section 13.4.4.20
1C14h	BM_VLAN_1	Buffer Manager Port 1 Default VLAN ID and Priority Register, Section 13.4.4.21
1C15h	BM_VLAN_2	Buffer Manager Port 2 Default VLAN ID and Priority Register, Section 13.4.4.22

Table 13.14 Indirectly Accessible Switch Control and Status Registers (continued)

REGISTER #	SYMBOL	REGISTER NAME
1C16h	BM_RATE_DRP_CNT_SRC_0	Buffer Manager Port 0 Ingress Rate Drop Count Register, Section 13.4.4.23
1C17h	BM_RATE_DRP_CNT_SRC_1	Buffer Manager Port 1 Ingress Rate Drop Count Register, Section 13.4.4.24
1C18h	BM_RATE_DRP_CNT_SRC_2	Buffer Manager Port 2 Ingress Rate Drop Count Register, Section 13.4.4.25
1C19h-1C1Fh	RESERVED	Reserved for Future Use
1C20h	BM_IMR	Buffer Manager Interrupt Mask Register, Section 13.4.4.26
1C21h	BM_IPR	Buffer Manager Interrupt Pending Register, Section 13.4.4.27
1C22h-FFFFh	RESERVED	Reserved for Future Use

13.4.1 General Switch CSRs

This section details the general Switch Fabric CSRs. These registers control the main reset and interrupt functions of the Switch Fabric. A list of the general switch CSRs and their corresponding register numbers is included in Table 13.14.

13.4.1.1 Switch Device ID Register (SW_DEV_ID)

Register #:	0000h	Size:	32 bits

This read-only register contains switch device ID information, including the device type, chip version and revision codes.

BITS	DESCRIPTION	TYPE	DEFAULT
31:24	**RESERVED**	RO	-
23:16	**Device Type Code (DEVICE_TYPE)**	RO	03h
15:8	**Chip Version Code (CHIP_VERSION)**	RO	04h
7:0	**Revision Code (REVISION)**	RO	07h

13.4.1.2 Switch Reset Register (SW_RESET)

Register #: 0001h Size: 32 bits

This register contains the Switch Fabric global reset. Refer to Section 4.2, "Resets," on page 48 for more information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:1	**RESERVED**	RO	-
0	**Switch Fabric Reset (SW_RESET)** This bit is the global switch fabric reset. All switch fabric blocks are affected. This bit must be manually cleared.	WO	0b

13.4.1.3 Switch Global Interrupt Mask Register (SW_IMR)

Register #:	0004h	Size:	32 bits

This read/write register contains the global interrupt mask for the Switch Fabric interrupts. All switch related interrupts in the Switch Global Interrupt Pending Register (SW_IPR) may be masked via this register. An interrupt is masked by setting the corresponding bit of this register. Clearing a bit will unmask the interrupt. When an unmasked Switch Fabric interrupt is generated in the Switch Global Interrupt Pending Register (SW_IPR), the interrupt will trigger the Switch Fabric Interrupt Event (SWITCH_INT) bit in the Interrupt Status Register (INT_STS). Refer to Chapter 5, "System Interrupts," on page 62 for more information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:9	**RESERVED**	RO	-
8:7	**RESERVED** **Note:** These bits must be written as 11b	R/W	11b
6	**Buffer Manager Interrupt Mask (BM)** When set, prevents the generation of Switch Fabric interrupts due to the Buffer Manager via the Buffer Manager Interrupt Pending Register (BM_IPR). The status bits in the Switch Global Interrupt Pending Register (SW_IPR) register are not affected.	R/W	1b
5	**Switch Engine Interrupt Mask (SWE)** When set, prevents the generation of Switch Fabric interrupts due to the Switch Engine via the Switch Engine Interrupt Pending Register (SWE_IPR). The status bits in the Switch Global Interrupt Pending Register (SW_IPR) register are not affected.	R/W	1b
4:3	**RESERVED** **Note:** These bits must be written as 11b	R/W	11b
2	**Port 2 MAC Interrupt Mask (MAC_2)** When set, prevents the generation of Switch Fabric interrupts due to the Port 2 MAC via the MAC_IPR_2 register (see Section 13.4.2.44, on page 286). The status bits in the Switch Global Interrupt Pending Register (SW_IPR) register are not affected.	R/W	1b
1	**Port 1 MAC Interrupt Mask (MAC_1)** When set, prevents the generation of Switch Fabric interrupts due to the Port 1 MAC via the MAC_IPR_1 register (see Section 13.4.2.44, on page 286). The status bits in the Switch Global Interrupt Pending Register (SW_IPR) register are not affected.	R/W	1b
0	**Port 0 MAC Interrupt Mask (MAC_0)** When set, prevents the generation of Switch Fabric interrupts due to the Port 0 MAC via the MAC_IPR_0 register (see Section 13.4.2.44, on page 286). The status bits in the Switch Global Interrupt Pending Register (SW_IPR) register are not affected.	R/W	1b

13.4.1.4 Switch Global Interrupt Pending Register (SW_IPR)

Register #: 0005h Size: 32 bits

This read-only register contains the pending global interrupts for the Switch Fabric. A set bit indicates an unmasked bit in the corresponding Switch Fabric sub-system has been triggered. All switch related interrupts in this register may be masked via the Switch Global Interrupt Mask Register (SW_IMR) register. When an unmasked Switch Fabric interrupt is generated in this register, the interrupt will trigger the Switch Fabric Interrupt Event (SWITCH_INT) bit in the Interrupt Status Register (INT_STS). Refer to Chapter 5, "System Interrupts," on page 62 for more information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:7	**RESERVED**	RO	-
6	**Buffer Manager Interrupt (BM)** Set when any unmasked bit in the Buffer Manager Interrupt Pending Register (BM_IPR) is triggered. This bit is cleared upon a read.	RC	0b
5	**Switch Engine Interrupt (SWE)** Set when any unmasked bit in the Switch Engine Interrupt Pending Register (SWE_IPR) is triggered. This bit is cleared upon a read.	RC	0b
4:3	**RESERVED**	RO	-
2	**Port 2 MAC Interrupt (MAC_2)** Set when any unmasked bit in the MAC_IPR_2 register (see Section 13.4.2.44, on page 286) is triggered. This bit is cleared upon a read.	RC	0b
1	**Port 1 MAC Interrupt (MAC_1)** Set when any unmasked bit in the MAC_IPR_1 register (see Section 13.4.2.44, on page 286) is triggered. This bit is cleared upon a read.	RC	0b
0	**Port 0 MAC Interrupt (MAC_0)** Set when any unmasked bit in the MAC_IPR_0 register (see Section 13.4.2.44, on page 286) is triggered. This bit is cleared upon a read.	RC	0b

13.4.2 Switch Port 0, Port 1, and Port 2 CSRs

This section details the switch Port 0, Port 1, and Port 2 CSRs. Each port provides a functionally identical set of registers which allow for the configuration of port settings, interrupts, and the monitoring of the various packet counters.

Because the Port 0, Port 1, and Port 2 CSRs are functionally identical, their register descriptions have been consolidated. A lowercase "x" has been appended to the end of each switch port register name in this section, where "x" should be replaced with "0", "1", or "2" for the Port 0, Port 1, or Port 2 registers respectively. A list of the Switch Port 0, Port 1, and Port 2 registers and their corresponding register numbers is included in Table 13.14.

13.4.2.1 Port x MAC Version ID Register (MAC_VER_ID_x)

Register #:	Port0: 0400h Port1: 0800h Port2: 0C00h	Size:	32 bits

This read-only register contains switch device ID information, including the device type, chip version and revision codes.

BITS	DESCRIPTION	TYPE	DEFAULT
31:12	**RESERVED**	RO	-
11:8	**Device Type Code (DEVICE_TYPE)**	RO	5h
7:4	**Chip Version Code (CHIP_VERSION)**	RO	8h
3:0	**Revision Code (REVISION)**	RO	3h

13.4.2.2 Port x MAC Receive Configuration Register (MAC_RX_CFG_x)

Register #: Port0: 0401h Size: 32 bits
Port1: 0801h
Port2: 0C01h

This read/write register configures the packet type passing parameters of the port.

BITS	DESCRIPTION	TYPE	DEFAULT
31:8	**RESERVED**	RO	-
7	**RESERVED** **Note:** This bit must always be written as 0.	R/W	0b
6	**RESERVED**	RO	-
5	**Enable Receive Own Transmit** When set, the switch port will receive its own transmission if it is looped back from the PHY. Normally, this function is only used in Half Duplex PHY loopback.	R/W	0b
4	**RESERVED**	RO	-
3	**Jumbo2K** When set, the maximum packet size accepted is 2048 bytes. Statistics boundaries are also adjusted.	R/W	0b
2	**RESERVED**	RO	-
1	**Reject MAC Types** When set, MAC control frames (packets with a type field of 8808h) are filtered. When cleared, MAC Control frames, other than MAC Control Pause frames, are sent to the forwarding process. MAC Control Pause frames are always consumed by the switch.	R/W	1b
0	**RX Enable** When set, the receive port is enabled. When cleared, the receive port is disabled.	R/W	1b

13.4.2.3 Port x MAC Receive Undersize Count Register (MAC_RX_UNDSZE_CNT_x)

Register #:	Port0: 0410h Port1: 0810h Port2: 0C10h	Size:	32 bits

This register provides a counter of undersized packets received by the port. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX Undersize** Count of packets that have less than 64 byte and a valid FCS. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 115 hours.	RC	00000000h

13.4.2.4 Port x MAC Receive 64 Byte Count Register (MAC_RX_64_CNT_x)

Register #:	Port0: 0411h Port1: 0811h Port2: 0C11h	Size:	32 bits

This register provides a counter of 64 byte packets received by the port. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX 64 Bytes** Count of packets (including bad packets) that have exactly 64 bytes. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

Note: A bad packet is defined as a packet that has an FCS or Symbol error. For this counter, a packet that is not an integral number of bytes is rounded down to the nearest byte.

13.4.2.5 Port x MAC Receive 65 to 127 Byte Count Register (MAC_RX_65_TO_127_CNT_x)

Register #:	Port0: 0412h Port1: 0812h Port2: 0C12h	Size:	32 bits

This register provides a counter of received packets between the size of 65 to 127 bytes. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX 65 to 127 Bytes** Count of packets (including bad packets) that have between 65 and 127 bytes. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 487 hours.	RC	00000000h

Note: A bad packet is defined as a packet that has an FCS or Symbol error. For this counter, a packet that is not an integral number of bytes is rounded down to the nearest byte.

13.4.2.6 Port x MAC Receive 128 to 255 Byte Count Register (MAC_RX_128_TO_255_CNT_x)

Register #:	Port0: 0413h Port1: 0813h Port2: 0C13h	Size:	32 bits

This register provides a counter of received packets between the size of 128 to 255 bytes. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX 128 to 255 Bytes** Count of packets (including bad packets) that have between 128 and 255 bytes. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 848 hours.	RC	00000000h

Note: A bad packet is defined as a packet that has an FCS or Symbol error. For this counter, a packet that is not an integral number of bytes is rounded down to the nearest byte.

13.4.2.7 Port x MAC Receive 256 to 511 Byte Count Register (MAC_RX_256_TO_511_CNT_x)

Register #:	Port0: 0414h Port1: 0814h Port2: 0C14h	Size:	32 bits

This register provides a counter of received packets between the size of 256 to 511 bytes. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX 256 to 511 Bytes** Count of packets (including bad packets) that have between 256 and 511 bytes. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 1581 hours.	RC	00000000h

Note: A bad packet is defined as a packet that has an FCS or Symbol error. For this counter, a packet that is not an integral number of bytes is rounded down to the nearest byte.

13.4.2.8 Port x MAC Receive 512 to 1023 Byte Count Register (MAC_RX_512_TO_1023_CNT_x)

Register #:	Port0: 0415h Port1: 0815h Port2: 0C15h	Size:	32 bits

This register provides a counter of received packets between the size of 512 to 1023 bytes. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX 512 to 1023 Bytes** Count of packets (including bad packets) that have between 512 and 1023 bytes. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 3047 hours.	RC	00000000h

Note: A bad packet is defined as a packet that has an FCS or Symbol error. For this counter, a packet that is not an integral number of bytes is rounded down to the nearest byte.

13.4.2.9 Port x MAC Receive 1024 to Max Byte Count Register (MAC_RX_1024_TO_MAX_CNT_x)

Register #:	Port0: 0416h Port1: 0816h Port2: 0C16h	Size:	32 bits

This register provides a counter of received packets between the size of 1024 to the maximum allowable number bytes. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX 1024 to Max Bytes** Count of packets (including bad packets) that have between 1024 and the maximum allowable number of bytes. The max number of bytes is 1518 for untagged packets and 1522 for tagged packets. If the Jumbo2K bit is set in the Port x MAC Receive Configuration Register (MAC_RX_CFG_x), the max number of bytes is 2048. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 5979 hours.	RC	00000000h

Note: A bad packet is defined as a packet that has an FCS or Symbol error. For this counter, a packet with the maximum number of bytes that is not an integral number of bytes (e.g. a 1518 1/2 byte packet) is counted.

13.4.2.10 Port x MAC Receive Oversize Count Register (MAC_RX_OVRSZE_CNT_x)

Register #:	Port0: 0417h Port1: 0817h Port2: 0C17h	Size:	32 bits

This register provides a counter of received packets with a size greater than the maximum byte size. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX Oversize** Count of packets that have more than the maximum allowable number of bytes and a valid FCS. The max number of bytes is 1518 for untagged packets and 1522 for tagged packets. If the Jumbo2K bit is set in the Port x MAC Receive Configuration Register (MAC_RX_CFG_x), the max number of bytes is 2048. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 8813 hours.	RC	00000000h

Note: For this counter, a packet with the maximum number of bytes that is not an integral number of bytes (e.g. a 1518 1/2 byte packet) is not considered oversize.

13.4.2.11 Port x MAC Receive OK Count Register (MAC_RX_PKTOK_CNT_x)

Register #:	Port0: 0418h Port1: 0818h Port2: 0C18h	Size:	32 bits

This register provides a counter of received packets that are or proper length and are free of errors. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX OK** Count of packets that are of proper length and are free of errors. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

Note: A bad packet is one that has a FCS or Symbol error.

13.4.2.12 Port x MAC Receive CRC Error Count Register (MAC_RX_CRCERR_CNT_x)

Register #:	Port0: 0419h Port1: 0819h Port2: 0C19h	Size:	32 bits

This register provides a counter of received packets that with CRC errors. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX CRC** Count of packets that have between 64 and the maximum allowable number of bytes and have a bad FCS, but do not have an extra nibble. The max number of bytes is 1518 for untagged packets and 1522 for tagged packets. If the Jumbo2K bit is set in the Port x MAC Receive Configuration Register (MAC_RX_CFG_x), the max number of bytes is 2048. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 137 hours.	RC	00000000h

13.4.2.13 Port x MAC Receive Multicast Count Register (MAC_RX_MULCST_CNT_x)

Register #:	Port0: 041Ah Port1: 081Ah Port2: 0C1Ah	Size:	32 bits

This register provides a counter of valid received packets with a multicast destination address. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX Multicast** Count of good packets (proper length and free of errors), including MAC control frames, that have a multicast destination address (not including broadcasts). **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

Note: A bad packet is one that has a FCS or Symbol error.

13.4.2.14 Port x MAC Receive Broadcast Count Register (MAC_RX_BRDCST_CNT_x)

Register #:	Port0: 041Bh Port1: 081Bh Port2: 0C1Bh	Size:	32 bits

This register provides a counter of valid received packets with a broadcast destination address. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX Broadcast** Count of valid packets (proper length and free of errors) that have a broadcast destination address. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

Note: A bad packet is one that has a FCS or Symbol error.

13.4.2.15 Port x MAC Receive Pause Frame Count Register (MAC_RX_PAUSE_CNT_x)

Register #:	Port0: 041Ch Port1: 081Ch Port2: 0C1Ch	Size:	32 bits

This register provides a counter of valid received pause frame packets. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX Pause Frame** Count of valid packets (proper length and free of errors) that have a type field of 8808h and an op-code of 0001(Pause). **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

Note: A bad packet is one that has a FCS or Symbol error.

13.4.2.16 Port x MAC Receive Fragment Error Count Register (MAC_RX_FRAG_CNT_x)

Register #:	Port0: 041Dh Port1: 081Dh Port2: 0C1Dh	Size:	32 bits

This register provides a counter of received packets of less than 64 bytes and a FCS error. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX Fragment** Count of packets that have less than 64 bytes and a FCS error. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 115 hours.	RC	00000000h

13.4.2.17 Port x MAC Receive Jabber Error Count Register (MAC_RX_JABB_CNT_x)

Register #:	Port0: 041Eh Port1: 081Eh Port2: 0C1Eh	Size:	32 bits

This register provides a counter of received packets with greater than the maximum allowable number of bytes and a FCS error. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX Jabber** Count of packets that have more than the maximum allowable number of bytes and a FCS error. The max number of bytes is 1518 for untagged packets and 1522 for tagged packets. If the Jumbo2K bit is set in the Port x MAC Receive Configuration Register (MAC_RX_CFG_x), the max number of bytes is 2048. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 8813 hours.	RC	00000000h

Note: For this counter, a packet with the maximum number of bytes that is not an integral number of bytes (e.g. a 1518 1/2 byte packet) and contains a FCS error is not considered jabber and is not counted here.

13.4.2.18 Port x MAC Receive Alignment Error Count Register (MAC_RX_ALIGN_CNT_x)

Register #:	Port0: 041Fh Port1: 081Fh Port2: 0C1Fh	Size:	32 bits

This register provides a counter of received packets with 64 bytes to the maximum allowable, and a FCS error. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX Alignment** Count of packets that have between 64 bytes and the maximum allowable number of bytes and are not byte aligned and have a bad FCS. The max number of bytes is 1518 for untagged packets and 1522 for tagged packets. If the Jumbo2K bit is set in the Port x MAC Receive Configuration Register (MAC_RX_CFG_x), the max number of bytes is 2048. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

Note: For this counter, a packet with the maximum number of bytes that is not an integral number of bytes (e.g. a 1518 1/2 byte packet) and a FCS error is considered an alignment error and is counted.

13.4.2.19 Port x MAC Receive Packet Length Count Register (MAC_RX_PKTLEN_CNT_x)

Register #:	Port0: 0420h Port1: 0820h Port2: 0C20h	Size:	32 bits

This register provides a counter of total bytes received. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX Bytes** Count of total bytes received (including bad packets). **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 5.8 hours.	RC	00000000h

Note: If necessary, for oversized packets, the packet is either truncated at 1518 bytes (untagged, Jumbo2K=0), 1522 bytes (tagged, Jumbo2K=0), or 2048 bytes (Jumbo2K=1). If this occurs, the byte count recorded is 1518, 1522, or 2048, respectively. The Jumbo2K bit is located in the Port x MAC Receive Configuration Register (MAC_RX_CFG_x).

Note: A bad packet is one that has an FCS or Symbol error. For this counter, a packet that is not an integral number of bytes (e.g. a 1518 1/2 byte packet) is rounded down to the nearest byte.

13.4.2.20 Port x MAC Receive Good Packet Length Count Register (MAC_RX_GOODPKTLEN_CNT_x)

Register #:	Port0: 0421h Port1: 0821h Port2: 0C21h	Size:	32 bits

This register provides a counter of total bytes received in good packets. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX Good Bytes** Count of total bytes received in good packets (proper length and free of errors). **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 5.8 hours.	RC	00000000h

Note: A bad packet is one that has an FCS or Symbol error.

13.4.2.21 Port x MAC Receive Symbol Error Count Register (MAC_RX_SYMBOL_CNT_x)

Register #:	Port0: 0422h Port1: 0822h Port2: 0C22h	Size:	32 bits

This register provides a counter of received packets with a symbol error. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX Symbol** Count of packets that had a receive symbol error. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 115 hours.	RC	00000000h

13.4.2.22 Port x MAC Receive Control Frame Count Register (MAC_RX_CTLFRM_CNT_x)

Register #:	Port0: 0423h Port1: 0823h Port2: 0C23h	Size:	32 bits

This register provides a counter of good packets with a type field of 8808h. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX Control Frame** Count of good packets (proper length and free of errors) that have a type field of 8808h. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

Note: A bad packet is one that has an FCS or Symbol error.

13.4.2.23 Port x MAC Transmit Configuration Register (MAC_TX_CFG_x)

Register #:	Port0: 0440h Port1: 0840h Port2: 0C40h	Size:	32 bits

This read/write register configures the transmit packet parameters of the port.

BITS	DESCRIPTION	TYPE	DEFAULT
31:8	**RESERVED**	RO	-
7	**MAC Counter Test** When set, TX and RX counters that normally clear to 0 when read, will be set to 7FFF_FFFCh when read with the exception of the Port x MAC Receive Packet Length Count Register (MAC_RX_PKTLEN_CNT_x), Port x MAC Transmit Packet Length Count Register (MAC_TX_PKTLEN_CNT_x), and Port x MAC Receive Good Packet Length Count Register (MAC_RX_GOODPKTLEN_CNT_x) counters which will be set to 7FFF_FF80h.	R/W	0b
6:2	**IFG Config** These bits control the transmit inter-frame gap. IFG bit times = (IFG Config *4) + 12 **Note:** IFG Config values less than 15 are unsupported.	R/W	10101b
1	**TX Pad Enable** When set, packets shorter than 64 bytes are padded with zeros if needed and a FCS is appended. Packets that are 60 bytes or less will become 64 bytes. Packets that are 61, 62, and 63 bytes will become 65, 66, and 67 bytes respectively.	R/W	1b
0	**TX Enable** When set, the transmit port is enabled. When cleared, the transmit port is disabled.	R/W	1b

13.4.2.24 Port x MAC Transmit Flow Control Settings Register (MAC_TX_FC_SETTINGS_x)

Register #:	Port0: 0441h Port1: 0841h Port2: 0C41h	Size:	32 bits

This read/write register configures the flow control settings of the port.

BITS	DESCRIPTION	TYPE	DEFAULT
31:18	**RESERVED**	RO	-
17:16	**Backoff Reset RX/TX** Half duplex-only. Determines when the truncated binary exponential backoff attempts counter is reset. **00 = Reset on successful transmission (IEEE standard)** **01 = Reset on successful reception** **1X = Reset on either successful transmission or reception**	R/W	00b
15:0	**Pause Time Value** The value that is inserted into the transmitted pause packet when the switch wants to “XOFF” its link partner.	R/W	FFFFh

13.4.2.25 Port x MAC Transmit Deferred Count Register (MAC_TX_DEFER_CNT_x)

Register #:	Port0: 0451h Port1: 0851h Port2: 0C51h	Size:	32 bits

This register provides a counter deferred packets. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX Deferred** Count of packets that were available for transmission but were deferred on the first transmit attempt due to network traffic (either on receive or prior transmission). This counter is not incremented on collisions. This counter is incremented only in half-duplex operation. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

13.4.2.26 Port x MAC Transmit Pause Count Register (MAC_TX_PAUSE_CNT_x)

Register #:	Port0: 0452h Port1: 0852h Port2: 0C52h	Size:	32 bits

This register provides a counter of transmitted pause packets. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX Pause** Count of pause packets transmitted. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

13.4.2.27 Port x MAC Transmit OK Count Register (MAC_TX_PKTOK_CNT_x)

Register #:	Port0: 0453h Port1: 0853h Port2: 0C53h	Size:	32 bits

This register provides a counter of successful transmissions. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX OK** Count of successful transmissions. Undersize packets are not included in this count. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

13.4.2.28 Port x MAC Transmit 64 Byte Count Register (MAC_TX_64_CNT_x)

Register #:	Port0: 0454h Port1: 0854h Port2: 0C54h	Size:	32 bits

This register provides a counter of 64 byte packets transmitted by the port. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX 64 Bytes** Count of packets that have exactly 64 bytes. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

13.4.2.29 Port x MAC Transmit 65 to 127 Byte Count Register (MAC_TX_65_TO_127_CNT_x)

Register #:	Port0: 0455h Port1: 0855h Port2: 0C55h	Size:	32 bits

This register provides a counter of transmitted packets between the size of 65 to 127 bytes. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX 65 to 127 Bytes** Count of packets that have between 65 and 127 bytes. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 487 hours.	RC	00000000h

13.4.2.30 Port x MAC Transmit 128 to 255 Byte Count Register (MAC_TX_128_TO_255_CNT_x)

Register #:	Port0: 0456h Port1: 0856h Port2: 0C56h	Size:	32 bits

This register provides a counter of transmitted packets between the size of 128 to 255 bytes. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX 128 to 255 Bytes** Count of packets that have between 128 and 255 bytes. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 848 hours.	RC	00000000h

13.4.2.31 Port x MAC Transmit 256 to 511 Byte Count Register (MAC_TX_256_TO_511_CNT_x)

Register #:	Port0: 0457h Port1: 0857h Port2: 0C57h	Size:	32 bits

This register provides a counter of transmitted packets between the size of 256 to 511 bytes. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX 256 to 511 Bytes** Count of packets that have between 256 and 511 bytes. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 1581 hours.	RC	00000000h

13.4.2.32 Port x MAC Transmit 512 to 1023 Byte Count Register (MAC_TX_512_TO_1023_CNT_x)

Register #:	Port0: 0458h Port1: 0858h Port2: 0C58h	Size:	32 bits

This register provides a counter of transmitted packets between the size of 512 to 1023 bytes. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX 512 to 1023 Bytes** Count of packets that have between 512 and 1023 bytes. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 3047 hours.	RC	00000000h

13.4.2.33 Port x MAC Transmit 1024 to Max Byte Count Register (MAC_TX_1024_TO_MAX_CNT_x)

Register #:	Port0: 0459h Port1: 0859h Port2: 0C59h	Size:	32 bits

This register provides a counter of transmitted packets between the size of 1024 to the maximum allowable number bytes. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX 1024 to Max Bytes** Count of packets that have more than 1024 bytes. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 5979 hours.	RC	00000000h

13.4.2.34 Port x MAC Transmit Undersize Count Register (MAC_TX_UNDSZE_CNT_x)

Register #:	Port0: 045Ah Port1: 085Ah Port2: 0C5Ah	Size:	32 bits

This register provides a counter of undersized packets transmitted by the port. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX Undersize** Count of packets that have less than 64 bytes. **Note:** This condition could occur when TX padding is disabled and a tag is removed. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 458 hours.	RC	00000000h

13.4.2.35 Port x MAC Transmit Packet Length Count Register (MAC_TX_PKTLEN_CNT_x)

Register #:	Port0: 045Ch Port1: 085Ch Port2: 0C5Ch	Size:	32 bits

This register provides a counter of total bytes transmitted. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX Bytes** Count of total bytes transmitted (does not include bytes from collisions, but does include bytes from Pause packets). **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 5.8 hours.	RC	00000000h

13.4.2.36 Port x MAC Transmit Broadcast Count Register (MAC_TX_BRDCST_CNT_x)

Register #:	Port0: 045Dh Port1: 085Dh Port2: 0C5Dh	Size:	32 bits

This register provides a counter of transmitted broadcast packets. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX Broadcast** Count of broadcast packets transmitted. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

13.4.2.37 Port x MAC Transmit Multicast Count Register (MAC_TX_MULCST_CNT_x)

Register #:	Port0: 045Eh Port1: 085Eh Port2: 0C5Eh	Size:	32 bits

This register provides a counter of transmitted multicast packets. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX Multicast** Count of multicast packets transmitted including MAC Control Pause frames. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

13.4.2.38 Port x MAC Transmit Late Collision Count Register (MAC_TX_LATECOL_CNT_x)

Register #:	Port0: 045Fh Port1: 085Fh Port2: 0C5Fh	Size:	32 bits

This register provides a counter of transmitted packets which experienced a late collision. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX Late Collision** Count of transmitted packets that experienced a late collision. This counter is incremented only in half-duplex operation. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

13.4.2.39 Port x MAC Transmit Excessive Collision Count Register (MAC_TX_EXCCOL_CNT_x)

Register #:	Port0: 0460h Port1: 0860h Port2: 0C60h	Size:	32 bits

This register provides a counter of transmitted packets which experienced 16 collisions. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX Excessive Collision** Count of transmitted packets that experienced 16 collisions. This counter is incremented only in half-duplex operation. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 1466 hours.	RC	00000000h

13.4.2.40 Port x MAC Transmit Single Collision Count Register (MAC_TX_SNGLECOL_CNT_x)

Register #:	Port0: 0461h Port1: 0861h Port2: 0C61h	Size:	32 bits

This register provides a counter of transmitted packets which experienced exactly 1 collision. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX Excessive Collision** Count of transmitted packets that experienced exactly 1 collision. This counter is incremented only in half-duplex operation. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 573 hours.	RC	00000000h

13.4.2.41 Port x MAC Transmit Multiple Collision Count Register (MAC_TX_MULTICOL_CNT_x)

Register #:	Port0: 0462h Port1: 0862h Port2: 0C62h	Size:	32 bits

This register provides a counter of transmitted packets which experienced between 2 and 15 collisions. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX Excessive Collision** Count of transmitted packets that experienced between 2 and 15 collisions. This counter is incremented only in half-duplex operation. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 664 hours.	RC	00000000h

13.4.2.42 Port x MAC Transmit Total Collision Count Register (MAC_TX_TOTALCOL_CNT_x)

Register #:	Port0: 0463h Port1: 0863h Port2: 0C63h	Size:	32 bits

This register provides a counter of total collisions including late collisions. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX Total Collision** Total count of collisions including late collisions. This counter is incremented only in half-duplex operation. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 92 hours.	RC	00000000h

13.4.2.43 Port x MAC Interrupt Mask Register (MAC_IMR_x)

Register #:	Port0: 0480h Port1: 0880h Port2: 0C80h	Size:	32 bits

This register contains the Port x interrupt mask. Port x related interrupts in the Port x MAC Interrupt Pending Register (MAC_IPR_x) may be masked via this register. An interrupt is masked by setting the corresponding bit of this register. Clearing a bit will unmask the interrupt. Refer to Chapter 5, "System Interrupts," on page 62 for more information.

Note: There are no possible Port x interrupt conditions available. This register exists for future use, and should be configured as indicated for future compatibility.

BITS	DESCRIPTION	TYPE	DEFAULT
31:8	**RESERVED**	RO	-
7:0	**RESERVED** **Note:** These bits must be written as 11h	R/W	11h

13.4.2.44 Port x MAC Interrupt Pending Register (MAC_IPR_x)

Register #:	Port0: 0481h Port1: 0881h Port2: 0C81h	Size:	32 bits

This read-only register contains the pending Port x interrupts. A set bit indicates an interrupt has been triggered. All interrupts in this register may be masked via the Port x MAC Interrupt Pending Register (MAC_IPR_x) register. Refer to Chapter 5, "System Interrupts," on page 62 for more information.

Note: There are no possible Port x interrupt conditions available. This register exists for future use.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RESERVED**	RO	-

13.4.3 Switch Engine CSRs

This section details the Switch Engine related CSRs. These registers allow configuration and monitoring of the various Switch Engine components including the ALR, VLAN, Port VID, and DIFFSERV tables. A list of the general switch CSRs and their corresponding register numbers is included in Table 13.14.

13.4.3.1 Switch Engine ALR Command Register (SWE_ALR_CMD)

Register #: 1800h Size: 32 bits

This register is used to manually read and write MAC addresses from/into the ALR table.

For a read access, the Switch Engine ALR Read Data 0 Register (SWE_ALR_RD_DAT_0) and Switch Engine ALR Read Data 1 Register (SWE_ALR_RD_DAT_1) should be read following the setting of the Get First Entry bit or Get Next Entry bit of this register.

For write access, the Switch Engine ALR Write Data 0 Register (SWE_ALR_WR_DAT_0) and Switch Engine ALR Write Data 1 Register (SWE_ALR_WR_DAT_1) registers should first be written with the MAC address, followed by the setting of the Make Entry bit of this register. The Make Pending bit in the Switch Engine ALR Command Status Register (SWE_ALR_CMD_STS) register indicates when the command is finished.

Refer to Chapter 6, "Switch Fabric," on page 67 for more information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:3	**RESERVED**	RO	-
2	**Make Entry** When set, the contents of SWE_ALR_WR_DAT_0 and SWE_ALR_WR_DAT_1 are written into the ALR table. The ALR logic determines the location where the entry is written. This command can also be used to change or delete a previously written or automatically learned entry. This bit has no affect when written low. This bit must be cleared once the ALR Make command is completed, which can be determined by the Make Pending bit in the Switch Engine ALR Command Status Register (SWE_ALR_CMD_STS) register.	R/W	0b
1	**Get First Entry** When set, the ALR read pointer is reset to the beginning of the ALR table and the ALR table is searched for the first valid entry, which is loaded into the SWE_ALR_RD_DAT_0 and SWE_ALR_RD_DAT_1 registers. The bit has no affect when written low. This bit must be cleared after it is set.	R/W	0b
0	**Get Next Entry** When set, the next valid entry in the ALR MAC address table is loaded into the SWE_ALR_RD_DAT_0 and SWE_ALR_RD_DAT_1 registers. This bit has no affect when written low. This bit must be cleared after it is set.	R/W	0b

13.4.3.2 Switch Engine ALR Write Data 0 Register (SWE_ALR_WR_DAT_0)

Register #: 1801h Size: 32 bits

This register is used in conjunction with the Switch Engine ALR Write Data 1 Register (SWE_ALR_WR_DAT_1) and contains the first 32 bits of ALR data to be manually written via the Make Entry command in the Switch Engine ALR Command Register (SWE_ALR_CMD).

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**MAC Address** This field contains the first 32 bits of the ALR entry that will be written into the ALR table. These bits correspond to the first 32 bits of the MAC address. Bit 0 holds the LSB of the first byte (the multicast bit).	R/W	00000000h

13.4.3.3 Switch Engine ALR Write Data 1 Register (SWE_ALR_WR_DAT_1)

Register #: 1802h Size: 32 bits

This register is used in conjunction with the Switch Engine ALR Write Data 0 Register (SWE_ALR_WR_DAT_0) and contains the last 32 bits of ALR data to be manually written via the Make Entry command in the Switch Engine ALR Command Register (SWE_ALR_CMD).

BITS	DESCRIPTION	TYPE	DEFAULT
31:27	**RESERVED**	RO	-
26	**Valid** When set, this bit makes the entry valid. It can be cleared to invalidate a previous entry that contained the specified MAC address.	R/W	0b
25	**Age/Override** This bit is used by the aging and forwarding processes. If the Static bit of this register is cleared, this bit should be set so that the entry will age in the normal amount of time. If the Static bit is set, this bit is used as a port state override bit. When set, packets received with a destination address that matches the MAC address in the SWE_ALR_WR_DAT_1 and SWE_ALR_WR_DAT_0 registers will be forwarded regardless of the port state (except the Disabled state) of the ingress or egress port(s). This is typically used to allow the reception of BPDU packets in the non-forwarding state.	R/W	0b
24	**Static** When this bit is set, this entry will not be removed by the aging process and/or be changed by the learning process. When this bit is cleared, this entry will be automatically removed after 5 to 10 minutes of inactivity. Inactivity is defined as no packets being received with a source address that matches this MAC address. **Note:** This bit is normally set when adding manual entries.	R/W	0b
23	**Filter** When set, packets with a destination address that matches this MAC address will be filtered.	R/W	0b
22	**Priority Enable** When set, this bit enables usage of the Priority field for this MAC address entry. When clear, the Priority field is not used.	R/W	0b
21:19	**Priority** These bits specify the priority that is used for packets with a destination address that matches this MAC address. This priority is only used if both the Priority Enable bit of this register and the DA Highest Priority bit of the Switch Engine Global Ingress Configuration Register (SWE_GLOBAL_INGRSS_CFG) are set.	R/W	000b

<table>
<tr><th>BITS</th><th>DESCRIPTION</th><th>TYPE</th><th>DEFAULT</th></tr>
<tr><td>18:16</td><td>Port
These bits indicate the port(s) associated with this MAC address. When bit 18 is cleared, a single port is selected. When bit 18 is set, multiple ports are selected.
<table>
<tr><th>VALUE</th><th>ASSOCIATED PORT(S)</th></tr>
<tr><td>000</td><td>Port 0</td></tr>
<tr><td>001</td><td>Port 1</td></tr>
<tr><td>010</td><td>Port 2</td></tr>
<tr><td>011</td><td>RESERVED</td></tr>
<tr><td>100</td><td>Port 0 and Port 1</td></tr>
<tr><td>101</td><td>Port 0 and Port 2</td></tr>
<tr><td>110</td><td>Port 1 and Port 2</td></tr>
<tr><td>111</td><td>Port 0, Port 1, and Port 2</td></tr>
</table></td><td>R/W</td><td>000b</td></tr>
<tr><td>15:0</td><td>MAC Address
These field contains the last 16 bits of the ALR entry that will be written into the ALR table. They correspond to the last 16 bits of the MAC address. Bit 15 holds the MSB of the last byte (the last bit on the wire). The first 32 bits of the MAC address are located in the Switch Engine ALR Write Data 0 Register (SWE_ALR_WR_DAT_0).</td><td>R/W</td><td>0000h</td></tr>
</table>

13.4.3.4 Switch Engine ALR Read Data 0 Register (SWE_ALR_RD_DAT_0)

Register #: 1805h Size: 32 bits

This register is used in conjunction with the Switch Engine ALR Read Data 1 Register (SWE_ALR_RD_DAT_1) to read the ALR table. It contains the first 32 bits of the ALR entry and is loaded via the Get First Entry or Get Next Entry commands in the Switch Engine ALR Command Register (SWE_ALR_CMD). This register is only valid when either of the Valid or End of Table bits in the Switch Engine ALR Read Data 1 Register (SWE_ALR_RD_DAT_1) are set.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**MAC Address** This field contains the first 32 bits of the ALR entry. These bits correspond to the first 32 bits of the MAC address. Bit 0 holds the LSB of the first byte (the multicast bit).	RO	00000000h

13.4.3.5 Switch Engine ALR Read Data 1 Register (SWE_ALR_RD_DAT_1)

Register #: 1806h Size: 32 bits

This register is used in conjunction with the Switch Engine ALR Read Data 0 Register (SWE_ALR_RD_DAT_0) to read the ALR table. It contains the last 32 bits of the ALR entry and is loaded via the Get First Entry or Get Next Entry commands in the Switch Engine ALR Command Register (SWE_ALR_CMD). This register is only valid when either of the Valid or End of Table bits are set.

BITS	DESCRIPTION	TYPE	DEFAULT
31:27	**RESERVED**	RO	-
26	**Valid** This bit is cleared when the Get First Entry or Get Next Entry bits of the Switch Engine ALR Command Register (SWE_ALR_CMD) are written. This bit is set when a valid entry is found in the ALR table. This bit stays cleared when the top of the ALR table is reached without finding an entry.	RO	0b
25	**End of Table** This bit indicates that the end of the ALR table has been reached and further Get Next Entry commands are not required. **Note:** The Valid bit may or may not be set when the end of the table is reached.	RO	0b
24	**Static** Indicates that this entry will not be removed by the aging process. When this bit is cleared, this entry will be automatically removed after 5 to 10 minutes of inactivity. Inactivity is defined as no packets being received with a source address that matches this MAC address.	RO	0b
23	**Filter** When set, indicates that packets with a destination address that matches this MAC address will be filtered.	RO	0b
22	**Priority Enable** Indicates whether or not the usage of the Priority field is enabled for this MAC address entry.	RO	0b
21:19	**Priority** These bits specify the priority that is used for packets with a destination address that matches this MAC address. This priority is only used if both the Priority Enable bit of this register and the DA Highest Priority bit in the Switch Engine Global Ingress Configuration Register (SWE_GLOBAL_INGRSS_CFG) are set.	RO	000b

<table>
<tr><th>BITS</th><th>DESCRIPTION</th><th>TYPE</th><th>DEFAULT</th></tr>
<tr><td>18:16</td><td>Port
These bits indicate the port(s) associated with this MAC address. When bit 18 is cleared, a single port is selected. When bit 18 is set, multiple ports are selected.
<table>
<tr><th>VALUE</th><th>ASSOCIATED PORT(S)</th></tr>
<tr><td>000</td><td>Port 0</td></tr>
<tr><td>001</td><td>Port 1</td></tr>
<tr><td>010</td><td>Port 2</td></tr>
<tr><td>011</td><td>RESERVED</td></tr>
<tr><td>100</td><td>Port 0 and Port 1</td></tr>
<tr><td>101</td><td>Port 0 and Port 2</td></tr>
<tr><td>110</td><td>Port 1 and Port 2</td></tr>
<tr><td>111</td><td>Port 0, Port 1, and Port 2</td></tr>
</table></td><td>RO</td><td>000b</td></tr>
<tr><td>15:0</td><td>MAC Address
These field contains the last 16 bits of the ALR entry. They correspond to the last 16 bits of the MAC address. Bit 15 holds the MSB of the last byte (the last bit on the wire). The first 32 bits of the MAC address are located in the Switch Engine ALR Read Data 0 Register (SWE_ALR_RD_DAT_0).</td><td>RO</td><td>0000h</td></tr>
</table>

13.4.3.6 Switch Engine ALR Command Status Register (SWE_ALR_CMD_STS)

Register #:	1808h	Size:	32 bits

This register indicates the current ALR command status.

BITS	DESCRIPTION	TYPE	DEFAULT
31:2	**RESERVED**	RO	-
1	**ALR Init Done** When set, indicates that the ALR table has finished being initialized by the reset process. The initialization is performed upon any reset that resets the Switch Fabric. The initialization takes approximately 20uS. During this time, any received packet will be dropped. Software should monitor this bit before writing any of the ALR tables or registers.	RO SS	Note 13.77
0	**Make Pending** When set, indicates that the Make Entry command is taking place. This bit is cleared once the Make Entry command has finished.	RO SC	0b

Note 13.77 The default value of this bit is 0 immediately following any Switch Fabric reset and then self-sets to 1 once the ALR table is initialized.

13.4.3.7 Switch Engine ALR Configuration Register (SWE_ALR_CFG)

Register #: 1809h Size: 32 bits

This register controls the ALR aging timer duration.

BITS	DESCRIPTION	TYPE	DEFAULT
31:1	**RESERVED**	RO	-
0	**ALR Age Test** When set, this bit decreases the aging timer from 5 minutes to 50mS.	R/W	0b

13.4.3.8 Switch Engine VLAN Command Register (SWE_VLAN_CMD)

Register #: 180Bh Size: 32 bits

This register is used to read and write the VLAN or Port VID tables. A write to this address performs the specified access.

For a read access, the Operation Pending bit in the Switch Engine VLAN Command Status Register (SWE_VLAN_CMD_STS) indicates when the command is finished. The Switch Engine VLAN Read Data Register (SWE_VLAN_RD_DATA) can then be read.

For a write access, the Switch Engine VLAN Write Data Register (SWE_VLAN_WR_DATA) register should be written first. The Operation Pending bit in the Switch Engine VLAN Command Status Register (SWE_VLAN_CMD_STS) indicates when the command is finished.

BITS	DESCRIPTION	TYPE	DEFAULT
31:6	**RESERVED**	RO	-
5	**VLAN RnW** This bit specifies a read(1) or a write(0) command.	R/W	0b
4	**PVIDnVLAN** When set, this bit selects the Port VID table. When cleared, this bit selects the VLAN table.	R/W	0b
3:0	**VLAN/Port** This field specifies the VLAN(0-15) or port(0-2) to be read or written. **Note:** Values outside of the valid range may cause unexpected results.	R/W	0h

13.4.3.9 Switch Engine VLAN Write Data Register (SWE_VLAN_WR_DATA)

Register #:	180Ch	Size:	32 bits

This register is used write the VLAN or Port VID tables.

BITS	DESCRIPTION	TYPE	DEFAULT
31:18	**RESERVED**	RO	-

<table>
<tr><th>BITS</th><th>DESCRIPTION</th><th>TYPE</th><th>DEFAULT</th></tr>
<tr><td>17:0</td><td>
Port Default VID and Priority
When the port VID table is selected (PVIDnVLAN=1 of the Switch Engine VLAN Command Register (SWE_VLAN_CMD)), bits 11:0 of this field specify the default VID for the port and bits 14:12 specify the default priority. All other bits of this field are reserved. These bits are used when a packet is received without a VLAN tag or with a NULL VLAN ID. The default VID is also used when the 802.1Q VLAN Disable bit is set. The default priority is also used when no other priority choice is selected. By default, the VID for all three ports is 1 and the priority for all three ports is 0.
Note: Values of 0 and FFFh should not be used since they are special VLAN IDs per the IEEE 802.3Q specification.

VLAN Data
When the VLAN table is selected (PVIDnVLAN=0 of the Switch Engine VLAN Command Register (SWE_VLAN_CMD)), the bits form the VLAN table entry as follows:
<table>
<tr><th>BITS</th><th>DESCRIPTION</th><th>DEFAULT</th></tr>
<tr><td>17</td><td>Member Port 2
Indicates the configuration of Port 2 for this VLAN entry.

1 = Member - Packets with a VID that matches this entry are allowed on ingress. The port is a member of the broadcast domain on egress.

0 = Not a Member - Packets with a VID that matches this entry are filtered on ingress unless the Admit Non Member bit in the Switch Engine Admit Non Member Register (SWE_ADMT_N_MEMBER) is set for this port. The port is not a member of the broadcast domain on egress.</td><td>0b</td></tr>
<tr><td>16</td><td>Un-Tag Port 2
When this bit is set, packets with a VID that matches this entry will have their tag removed when re-transmitted on Port 2 when it is designated as a Hybrid port via the Buffer Manager Egress Port Type Register (BM_EGRSS_PORT_TYPE).</td><td>0b</td></tr>
<tr><td>15</td><td>Member Port 1
See description for Member Port 2.</td><td>0b</td></tr>
<tr><td>14</td><td>Un-Tag Port 1
See description for Un-Tag Port 2.</td><td>0b</td></tr>
<tr><td>13</td><td>Member Port 0
See description for Member Port 2.</td><td>0b</td></tr>
<tr><td>12</td><td>Un-Tag Port 0
See description for Un-Tag Port 2.</td><td>0b</td></tr>
<tr><td>11:0</td><td>VID
These bits specify the VLAN ID associated with this VLAN entry.

To disable a VLAN entry, a value of 0 should be used.
Note: A value of 0 is considered a NULL VLAN and should not normally be used other than to disable a VLAN entry.
Note: A value of 3FFh is considered reserved by IEEE 802.1Q and should not be used.</td><td>000h</td></tr>
</table>
</td><td>R/W</td><td>0b</td></tr>
</table>

13.4.3.10 Switch Engine VLAN Read Data Register (SWE_VLAN_RD_DATA)

Register #:	180Eh	Size:	32 bits

This register is used to read the VLAN or Port VID tables.

BITS	DESCRIPTION	TYPE	DEFAULT
31:18	**RESERVED**	RO	-

BITS	DESCRIPTION	TYPE	DEFAULT
17:0	**Port Default VID and Priority** When the port VID table is selected (PVIDnVLAN=1 of the Switch Engine VLAN Command Register (SWE_VLAN_CMD)), bits 11:0 of this field specify the default VID for the port and bits 14:12 specify the default priority. All other bits of this field are reserved. These bits are used when a packet is received without a VLAN tag or with a NULL VLAN ID. The default VID is also used when the 802.1Q VLAN Disable bit is set. The default priority is also used when no other priority choice is selected. By default, the VID for all three ports is 1 and the priority for all three ports is 0. **Note:** Values of 0 and FFFh should not be used since they are special VLAN IDs per the IEEE 802.3Q specification. **VLAN Data** When the VLAN table is selected (PVIDnVLAN=0 of the Switch Engine VLAN Command Register (SWE_VLAN_CMD)), the bits form the VLAN table entry as follows:	RO	00000h

BITS	DESCRIPTION	DEFAULT
17	**Member Port 2** Indicates the configuration of Port 2 for this VLAN entry. **1 = Member** - Packets with a VID that matches this entry are allowed on ingress. The port is a member of the broadcast domain on egress. **0 = Not a Member** - Packets with a VID that matches this entry are filtered on ingress unless the Admit Non Member bit in the Switch Engine Admit Non Member Register (SWE_ADMT_N_MEMBER) is set for this port. The port is not a member of the broadcast domain on egress.	0b
16	**Un-Tag Port 2** When this bit is set, packets with a VID that matches this entry will have their tag removed when re-transmitted on Port 2 when it is designated as a Hybrid port via the Buffer Manager Egress Port Type Register (BM_EGRSS_PORT_TYPE)	0b
15	**Member Port 1** See description for Member Port 2.	0b
14	**Un-Tag Port 1** See description for Un-Tag Port 2.	0b
13	**Member Port 0** See description for Member Port 2.	0b
12	**Un-Tag Port 0** See description for Un-Tag Port 2.	0b
11:0	**VID** These bits specify the VLAN ID associated with this VLAN entry. To disable a VLAN entry, a value of 0 should be used. **Note:** A value of 0 is considered a NULL VLAN and should not normally be used other than to disable a VLAN entry. **Note:** A value of 3FFh is considered reserved by IEEE 802.1Q and should not be used.	000h

13.4.3.11 Switch Engine VLAN Command Status Register (SWE_VLAN_CMD_STS)

Register #: 1810h Size: 32 bits

This register indicates the current VLAN command status.

BITS	DESCRIPTION	TYPE	DEFAULT
31:1	**RESERVED**	RO	-
0	**Operation Pending** When set, this bit indicates that the read or write command is taking place. This bit is cleared once the command has finished.	RO SC	0b

13.4.3.12 Switch Engine DIFFSERV Table Command Register (SWE_DIFFSERV_TBL_CFG)

Register #: 1811h Size: 32 bits

This register is used to read and write the DIFFSERV table. A write to this address performs the specified access. This table is used to map the received IP ToS/CS to a priority.

For a read access, the Operation Pending bit in the Switch Engine DIFFSERV Table Command Status Register (SWE_DIFFSERV_TBL_CMD_STS) indicates when the command is finished. The Switch Engine DIFFSERV Table Read Data Register (SWE_DIFFSERV_TBL_RD_DATA) can then be read.

For a write access, the Switch Engine DIFFSERV Table Write Data Register (SWE_DIFFSERV_TBL_WR_DATA) register should be written first. The Operation Pending bit in the Switch Engine DIFFSERV Table Command Status Register (SWE_DIFFSERV_TBL_CMD_STS) indicates when the command is finished.

BITS	DESCRIPTION	TYPE	DEFAULT
31:8	**RESERVED**	RO	-
7	**DIFFSERV Table RnW** This bit specifies a read(1) or a write(0) command.	R/W	0b
6	**RESERVED**	RO	-
5:0	**DIFFSERV Table Index** This field specifies the ToS/CS entry that is accessed.	R/W	0h

13.4.3.13 Switch Engine DIFFSERV Table Write Data Register (SWE_DIFFSERV_TBL_WR_DATA)

Register #: 1812h Size: 32 bits

This register is used to write the DIFFSERV table. The DIFFSERV table is not initialized upon reset on power-up. If DIFFSERV is enabled, the full table should be initialized by the host.

BITS	DESCRIPTION	TYPE	DEFAULT
31:3	**RESERVED**	RO	-
2:0	**DIFFSERV Priority** These bits specify the assigned receive priority for IP packets with a ToS/CS field that matches this index.	R/W	000b

13.4.3.14 Switch Engine DIFFSERV Table Read Data Register (SWE_DIFFSERV_TBL_RD_DATA)

Register #: 1813h Size: 32 bits

This register is used to read the DIFFSERV table.

BITS	DESCRIPTION	TYPE	DEFAULT
31:3	**RESERVED**	RO	-
2:0	**DIFFSERV Priority** These bits specify the assigned receive priority for IP packets with a ToS/CS field that matches this index.	RO	000b

13.4.3.15 Switch Engine DIFFSERV Table Command Status Register (SWE_DIFFSERV_TBL_CMD_STS)

Register #: 1814h Size: 32 bits

This register indicates the current DIFFSERV command status.

BITS	DESCRIPTION	TYPE	DEFAULT
31:1	**RESERVED**	RO	-
0	**Operation Pending** When set, this bit indicates that the read or write command is taking place. This bit is cleared once the command has finished.	RO SC	0b

13.4.3.16 Switch Engine Global Ingress Configuration Register (SWE_GLOBAL_INGRSS_CFG)

Register #: 1840h Size: 32 bits

This register is used to configure the global ingress rules.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15	**802.1Q VLAN Disable** When set, the VID from the VLAN tag is ignored and the per port default VID (PVID) is used for purposes of VLAN rules. This does not affect the packet tag on egress.	R/W	0b
14	**Use Tag** When set, the priority from the VLAN tag is enabled as a transmit priority queue choice.	R/W	0b
13	**Allow Monitor Echo** When set, monitoring packets are allowed to be echoed back to the source port. When cleared, monitoring packets, like other packets, are never sent back to the source port. This bit is useful when the monitor port wishes to receive it's own IGMP packets.	R/W	0b
12:10	**IGMP Monitor Port** This field is the port bit map where IPv4 IGMP packets are sent.	R/W	0b
9	**Use IP** When set, the IPv4 TOS or IPv6 SC field is enabled as a transmit priority queue choice.	R/W	0b
8	**RESERVED**	R/W	-
7	**Enable IGMP Monitoring** When set, IPv4 IGMP packets are monitored and sent to the IGMP monitor port.	R/W	0b
6	**SWE Counter Test** When this bit is set the Switch Engine counters that normally clear to 0 when read will be set to 7FFF_FFFCh when read.	R/W	0b
5	**DA Highest Priority** When this bit is set and the priority enable bit in the ALR table for the destination MAC address is set, the transmit priority queue that is selected is taken from the ALR Priority bits (see the Switch Engine ALR Read Data 1 Register (SWE_ALR_RD_DAT_1)).	R/W	0b
4	**Filter Multicast** When this bit is set, packets with a multicast destination address are filtered if the address is not found in the ALR table. Broadcasts are not included in this filter.	R/W	0b
3	**Drop Unknown** When this bit is set, packets with a unicast destination address are filtered if the address is not found in the ALR table.	R/W	0b

BITS	DESCRIPTION	TYPE	DEFAULT
2	**Use Precedence** When the priority is taken from an IPV4 packet (enabled via the Use IP bit), this bit selects between precedence bits in the TOS octet or the DIFFSERV table. When set, IPv4 packets will use the precedence bits in the TOS octet to select the transmit priority queue. When cleared, IPv4 packets will use the DIFFSERV table to select the transmit priority queue.	R/W	1b
1	**VL Higher Priority** When this bit is set and VLAN priority is enabled (via the Use Tag bit), the priority from the VLAN tag has higher priority than the IP TOS/SC field.	R/W	1b
0	**VLAN Enable** When set, VLAN ingress rules are enabled.	R/W	0b

13.4.3.17 Switch Engine Port Ingress Configuration Register (SWE_PORT_INGRSS_CFG)

Register #:	1841h	Size:	32 bits

This register is used to configure the per port ingress rules.

BITS	DESCRIPTION	TYPE	DEFAULT
31:6	**RESERVED**	RO	-
5:3	**Enable Learning on Ingress** When set, source addresses are learned when a packet is received on the corresponding port and the corresponding Port State in the Switch Engine Port State Register (SWE_PORT_STATE) is set to forwarding or learning. There is one enable bit per ingress port. Bits 5,4,3 correspond to switch ports 2,1,0 respectively.	R/W	111b
2:0	**Enable Membership Checking** When set, VLAN membership is checked when a packet is received on the corresponding port. The packet will be filtered if the ingress port is not a member of the VLAN (unless the Admit Non Member bit is set for the port in the Switch Engine Admit Non Member Register (SWE_ADMT_N_MEMBER)) For destination addresses that are found in the ALR table, the packet will be filtered if the egress port is not a member of the VLAN (for destination addresses that are not found in the ALR table only the ingress port is checked for membership). The VLAN Enable bit in the Switch Engine Global Ingress Configuration Register (SWE_GLOBAL_INGRSS_CFG) needs to be set for these bits to have an affect. There is one enable bit per ingress port. Bits 2,1,0 correspond to switch ports 2,1,0 respectively.	R/W	000b

13.4.3.18 Switch Engine Admit Only VLAN Register (SWE_ADMT_ONLY_VLAN)

Register #: 1842h Size: 32 bits

This register is used to configure the per port ingress rule for allowing only VLAN tagged packets.

BITS	DESCRIPTION	TYPE	DEFAULT
31:3	**RESERVED**	RO	-
2:0	**Admit Only VLAN** When set, untagged and priority tagged packets are filtered. The VLAN Enable bit in the Switch Engine Global Ingress Configuration Register (SWE_GLOBAL_INGRSS_CFG) needs to be set for these bits to have an affect. There is one enable bit per ingress port. Bits 2,1,0 correspond to switch ports 2,1,0 respectively.	R/W	000b

13.4.3.19 Switch Engine Port State Register (SWE_PORT_STATE)

Register #:	1843h	Size:	32 bits

This register is used to configure the per port spanning tree state.

BITS	DESCRIPTION	TYPE	DEFAULT
31:6	**RESERVED**	RO	-
5:4	**Port State Port 2** These bits specify the spanning tree port states for Port 2. **00 = Forwarding** **01 = Listening/Blocking** **10 = Learning** **11 = Disabled**	R/W	00b
3:2	**Port State Port 1** These bits specify the spanning tree port states for Port 1. **00 = Forwarding** **01 = Listening/Blocking** **10 = Learning** **11 = Disabled**	R/W	00b
1:0	**Port State Port 0** These bits specify the spanning tree port states for Port 0. **00 = Forwarding** **01 = Listening/Blocking** **10 = Learning** **11 = Disabled**	R/W	00b

13.4.3.20 Switch Engine Priority to Queue Register (SWE_PRI_TO_QUE)

Register #: 1845h Size: 32 bits

This register specifies the Traffic Class table that maps the packet priority into the egress queues.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:14	**Priority 7 traffic Class** These bits specify the egress queue that is used for packets with a priority of 7.	R/W	11b
13:12	**Priority 6 traffic Class** These bits specify the egress queue that is used for packets with a priority of 6.	R/W	11b
11:10	**Priority 5 traffic Class** These bits specify the egress queue that is used for packets with a priority of 5.	R/W	10b
9:8	**Priority 4 traffic Class** These bits specify the egress queue that is used for packets with a priority of 4.	R/W	10b
7:6	**Priority 3 traffic Class** These bits specify the egress queue that is used for packets with a priority of 3.	R/W	01b
5:4	**Priority 2 traffic Class** These bits specify the egress queue that is used for packets with a priority of 2.	R/W	00b
3:2	**Priority 1 traffic Class** These bits specify the egress queue that is used for packets with a priority of 1.	R/W	00b
1:0	**Priority 0 traffic Class** These bits specify the egress queue that is used for packets with a priority of 0.	R/W	01b

13.4.3.21 Switch Engine Port Mirroring Register (SWE_PORT_MIRROR)

Register #: 1846h Size: 32 bits

This register is used to configure port mirroring.

BITS	DESCRIPTION	TYPE	DEFAULT
31:9	**RESERVED**	RO	-
8	**Enable RX Mirroring Filtered** When set, packets that would normally have been filtered are included in the receive mirroring function and are sent only to the sniffer port. When cleared, filtered packets are not mirrored. **Note:** The Ingress Filtered Count Registers will still count these packets as filtered and the Switch Engine Interrupt Pending Register (SWE_IPR) will still register a drop interrupt.	R/W	0b
7:5	**Sniffer Port** These bits specify the sniffer port that transmits packets that are monitored. Bits 7,6,5 correspond to switch ports 2,1,0 respectively. **Note:** Only one port should be set as the sniffer.	R/W	00b
4:2	**Mirrored Port** These bits specify if a port is to be mirrored. Bits 4,3,2 correspond to switch ports 2,1,0 respectively. **Note:** Multiple ports can be set as mirrored.	R/W	00b
1	**Enable RX Mirroring** This bit enables packets received on the mirrored ports to be also sent to the sniffer port.	R/W	0b
0	**Enable TX Mirroring** This bit enables packets transmitted on the mirrored ports to be also sent to the sniffer port.	R/W	0b

13.4.3.22 Switch Engine Ingress Port Type Register (SWE_INGRSS_PORT_TYP)

Register #: 1847h Size: 32 bits

This register is used to enable the special tagging mode used to determine the destination port based on the VLAN tag contents.

BITS	DESCRIPTION	TYPE	DEFAULT
31:6	**RESERVED**	RO	-
5:4	**Ingress Port Type Port 2** A setting of 11b enables the usage of the VLAN tag to specify the packet destination. All other values disable this feature.	R/W	00b
3:2	**Ingress Port Type Port 1** A setting of 11b enables the usage of the VLAN tag to specify the packet destination. All other values disable this feature.	R/W	00b
1:0	**Ingress Port Type Port 0** A setting of 11b enables the usage of the VLAN tag to specify the packet destination. All other values disable this feature.	R/W	00b

13.4.3.23 Switch Engine Broadcast Throttling Register (SWE_BCST_THROT)

Register #: 1848h Size: 32 bits

This register configures the broadcast input rate throttling.

BITS	DESCRIPTION	TYPE	DEFAULT
31:27	**RESERVED**	RO	-
26	**Broadcast Throttle Enable Port 2** This bit enables broadcast input rate throttling on Port 2.	R/W	0b
25:18	**Broadcast Throttle Level Port 2** These bits specify the number of bytes x 64 allowed to be received per every 1.72mS interval.	R/W	02h
17	**Broadcast Throttle Enable Port 1** This bit enables broadcast input rate throttling on Port 1.	R/W	0b
16:9	**Broadcast Throttle Level Port 1** These bits specify the number of bytes x 64 allowed to be received per every 1.72mS interval.	R/W	02h
8	**Broadcast Throttle Enable Port 0** This bit enables broadcast input rate throttling on Port 0.	R/W	0b
7:0	**Broadcast Throttle Level Port 0** These bits specify the number of bytes x 64 allowed to be received per every 1.72mS interval.	R/W	02h

13.4.3.24 Switch Engine Admit Non Member Register (SWE_ADMT_N_MEMBER)

Register #: 1849h Size: 32 bits

This register is used to allow access to a VLAN even if the ingress port is not a member.

BITS	DESCRIPTION	TYPE	DEFAULT
31:3	**RESERVED**	RO	-
2:0	**Admit Non Member** When set, a received packet is accepted even if the ingress port is not a member of the destination VLAN. The VLAN still must be active in the switch. There is one bit per ingress port. Bits 2,1,0 correspond to switch ports 2,1,0 respectively.	R/W	000b

13.4.3.25 Switch Engine Ingress Rate Configuration Register (SWE_INGRSS_RATE_CFG)

Register #: 184Ah Size: 32 bits

This register, along with the settings accessible via the Switch Engine Ingress Rate Command Register (SWE_INGRSS_RATE_CMD), is used to configure the ingress rate metering/coloring.

BITS	DESCRIPTION	TYPE	DEFAULT
31:3	**RESERVED**	RO	-
2:1	**Rate Mode** These bits configure the rate metering/coloring mode. **00 = Source Port & Priority** **01 = Source Port Only** **10 = Priority Only** **11 = RESERVED**	R/W	00b
0	**Ingress Rate Enable** When set, ingress rates are metered and packets are colored and dropped if necessary.	R/W	0b

13.4.3.26 Switch Engine Ingress Rate Command Register (SWE_INGRSS_RATE_CMD)

Register #: 184Bh Size: 32 bits

This register is used to indirectly read and write the ingress rate metering/color table registers. A write to this address performs the specified access.

For a read access, the Operation Pending bit in the Switch Engine Ingress Rate Command Status Register (SWE_INGRSS_RATE_CMD_STS) indicates when the command is finished. The Switch Engine Ingress Rate Read Data Register (SWE_INGRSS_RATE_RD_DATA) can then be read.

For a write access, the Switch Engine Ingress Rate Write Data Register (SWE_INGRSS_RATE_WR_DATA) should be written first. The Operation Pending bit in the Switch Engine Ingress Rate Command Status Register (SWE_INGRSS_RATE_CMD_STS) indicates when the command is finished.

For details on 16-bit wide Ingress Rate Table registers indirectly accessible by this register, see Section 13.4.3.26.1 below.

BITS	DESCRIPTION	TYPE	DEFAULT
31:8	**RESERVED**	RO	-
7	**Ingress Rate RnW** These bits specify a read(1) or write(0) command.	R/W	0b
6:5	**Type** These bits select between the ingress rate metering/color table registers as follows: **00 = RESERVED** **01 = Committed Information Rate Registers (uses CIS Address field)** **10 = Committed Burst Register** **11 = Excess Burst Register**	R/W	00b
4:0	**CIR Address** These bits select one of the 24 Committed Information Rate registers. When Rate Mode is set to Source Port & Priority in the Switch Engine Ingress Rate Configuration Register (SWE_INGRSS_RATE_CFG), the first set of 8 registers (CIR addresses 0-7) are for to Port 0, the second set of 8 registers (CIR addresses 8-15) are for Port 1, and the third set of registers (CIR addresses 16-23) are for Port 2. Priority 0 is the lower register of each set (e.g. 0, 8, and 16). When Rate Mode is set to Source Port Only, the first register (CIR address 0) is for Port 0, the second register (CIR address 1) is for Port 1, and the third register (CIR address 2) is for Port 2. When Rate Mode is set to Priority Only, the first register (CIR address 0) is for priority 0, the second register (CIR address 1) is for priority 1, and so forth up to priority 23. **Note:** Values outside of the valid range may cause unexpected results.	R/W	0h

13.4.3.26.1 INGRESS RATE TABLE REGISTERS

The ingress rate metering/color table consists of 24 Committed Information Rate (CIR) registers (one per port/priority), a Committed Burst Size register, and an Excess Burst Size register. All metering/color table registers are 16-bits in size and are accessed indirectly via the Switch Engine Ingress Rate Command Register (SWE_INGRSS_RATE_CMD). Descriptions of these registers are detailed in Table 13.15 below.

Table 13.15 Metering/Color Table Register Descriptions

DESCRIPTION	TYPE	DEFAULT
Excess Burst Size This register specifies the maximum excess burst size in bytes. Bursts larger than this value that exceed the excess data rate are dropped. **Note:** Either this value or the Committed Burst Size should be set larger than or equal to the largest possible packet expected. **Note:** All of the Excess Burst token buckets are initialized to this default value. If a lower value is programmed into this register, the token buckets will need to be normally depleted below this value before this value has any affect on limiting the token bucket maximum values. This register is 16-bits wide.	R/W	0600h
Committed Burst Size This register specifies the maximum committed burst size in bytes. Bursts larger than this value that exceed the committed data rate are subjected to random dropping. **Note:** Either this value or the Excess Burst Size should be set larger than or equal to the largest possible packet expected. **Note:** All of the Committed Burst token buckets are initialized to this default value. If a lower value is programmed into this register, the token buckets will need to be normally depleted below this value before this value has any affect on limiting the token bucket maximum values. This register is 16-bits wide.	R/W	0600h
Committed Information Rate (CIR) These registers specify the committed data rate for the port/priority pair. The rate is specified in time per byte. The time is this value plus 1 times 20nS. There are 24 of these registers each 16-bits wide.	R/W	0014h

13.4.3.27 Switch Engine Ingress Rate Command Status Register (SWE_INGRSS_RATE_CMD_STS)

Register #: 184Ch Size: 32 bits

This register indicates the current ingress rate command status.

BITS	DESCRIPTION	TYPE	DEFAULT
31:1	**RESERVED**	RO	-
0	**Operation Pending** When set, indicates that the read or write command is taking place. This bit is cleared once the command has finished.	RO SC	0b

13.4.3.28 Switch Engine Ingress Rate Write Data Register (SWE_INGRSS_RATE_WR_DATA)

Register #: 184Dh Size: 32 bits

This register is used to write the ingress rate table registers.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:0	**Data** This is the data to be written to the ingress rate table registers as specified in the Switch Engine Ingress Rate Command Register (SWE_INGRSS_RATE_CMD). Refer to Section 13.4.3.26.1, "Ingress Rate Table Registers," on page 318 for details on these registers.	R/W	0000h

13.4.3.29 Switch Engine Ingress Rate Read Data Register (SWE_INGRSS_RATE_RD_DATA)

Register #: 184Eh Size: 32 bits

This register is used to read the ingress rate table registers.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:0	**Data** This is the read data from the ingress rate table registers as specified in the Switch Engine Ingress Rate Command Register (SWE_INGRSS_RATE_CMD). Refer to Section 13.4.3.26.1, "Ingress Rate Table Registers," on page 318 for details on these registers.	RO	0000h

13.4.3.30 Switch Engine Port 0 Ingress Filtered Count Register (SWE_FILTERED_CNT_0)

Register #: 1850h Size: 32 bits

This register counts the number of packets filtered at ingress on Port 0. This count includes packets filtered due to broadcast throttling but does not include packets dropped due to ingress rate limiting (which are counted separately).

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Filtered** This field is a count of packets filtered at ingress and is cleared when read. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

13.4.3.31 Switch Engine Port 1 Ingress Filtered Count Register (SWE_FILTERED_CNT_1)

Register #: 1851h Size: 32 bits

This register counts the number of packets filtered at ingress on Port 1. This count includes packets filtered due to broadcast throttling but does not include packets dropped due to ingress rate limiting (which are counted separately).

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Filtered** This field is a count of packets filtered at ingress and is cleared when read. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

13.4.3.32 Switch Engine Port 2 Ingress Filtered Count Register (SWE_FILTERED_CNT_2)

Register #: 1852h Size: 32 bits

This register counts the number of packets filtered at ingress on Port 2. This count includes packets filtered due to broadcast throttling but does not include packets dropped due to ingress rate limiting (which are counted separately).

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Filtered** This field is a count of packets filtered at ingress and is cleared when read. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

13.4.3.33 Switch Engine Port 0 Ingress VLAN Priority Regeneration Table Register (SWE_INGRSS_REGEN_TBL_0)

Register #: 1855h Size: 32 bits

This register provides the ability to map the received VLAN priority to a regenerated priority. The regenerated priority is used in determining the output priority queue. By default, the regenerated priority is identical to the received priority.

BITS	DESCRIPTION	TYPE	DEFAULT
31:24	**RESERVED**	RO	-
23:21	**Regen7** These bits specify the regenerated priority for received priority 7.	R/W	7h
20:18	**Regen6** These bits specify the regenerated priority for received priority 6.	R/W	6h
17:15	**Regen5** These bits specify the regenerated priority for received priority 5.	R/W	5h
14:12	**Regen4** These bits specify the regenerated priority for received priority 4.	R/W	4h
11:9	**Regen3** These bits specify the regenerated priority for received priority 3.	R/W	3h
8:6	**Regen2** These bits specify the regenerated priority for received priority 2.	R/W	2h
5:3	**Regen1** These bits specify the regenerated priority for received priority 1.	R/W	1h
2:0	**Regen0** These bits specify the regenerated priority for received priority 0.	R/W	0h

13.4.3.34 Switch Engine Port 1 Ingress VLAN Priority Regeneration Table Register (SWE_INGRSS_REGEN_TBL_1)

Register #: 1856h Size: 32 bits

This register provides the ability to map the received VLAN priority to a regenerated priority. The regenerated priority is used in determining the output priority queue. By default, the regenerated priority is identical to the received priority.

BITS	DESCRIPTION	TYPE	DEFAULT
31:24	**RESERVED**	RO	-
23:21	**Regen7** These bits specify the regenerated priority for received priority 7.	R/W	7h
20:18	**Regen6** These bits specify the regenerated priority for received priority 6.	R/W	6h
17:15	**Regen5** These bits specify the regenerated priority for received priority 5.	R/W	5h
14:12	**Regen4** These bits specify the regenerated priority for received priority 4.	R/W	4h
11:9	**Regen3** These bits specify the regenerated priority for received priority 3.	R/W	3h
8:6	**Regen2** These bits specify the regenerated priority for received priority 2.	R/W	2h
5:3	**Regen1** These bits specify the regenerated priority for received priority 1.	R/W	1h
2:0	**Regen0** These bits specify the regenerated priority for received priority 0.	R/W	0h

13.4.3.35 Switch Engine Port 2 Ingress VLAN Priority Regeneration Table Register (SWE_INGRSS_REGEN_TBL_2)

Register #: 1857h Size: 32 bits

This register provides the ability to map the received VLAN priority to a regenerated priority. The regenerated priority is used in determining the output priority queue. By default, the regenerated priority is identical to the received priority.

BITS	DESCRIPTION	TYPE	DEFAULT
31:24	**RESERVED**	RO	-
23:21	**Regen7** These bits specify the regenerated priority for received priority 7.	R/W	7h
20:18	**Regen6** These bits specify the regenerated priority for received priority 6.	R/W	6h
17:15	**Regen5** These bits specify the regenerated priority for received priority 5.	R/W	5h
14:12	**Regen4** These bits specify the regenerated priority for received priority 4.	R/W	4h
11:9	**Regen3** These bits specify the regenerated priority for received priority 3.	R/W	3h
8:6	**Regen2** These bits specify the regenerated priority for received priority 2.	R/W	2h
5:3	**Regen1** These bits specify the regenerated priority for received priority 1.	R/W	1h
2:0	**Regen0** These bits specify the regenerated priority for received priority 0.	R/W	0h

13.4.3.36 Switch Engine Port 0 Learn Discard Count Register (SWE_LRN_DISCRD_CNT_0)

Register #: 1858h Size: 32 bits

This register counts the number of MAC addresses on Port 0 that were not learned or were overwritten by a different address due to address table space limitations.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Learn Discard** This field is a count of MAC addresses not learned or overwritten and is cleared when read. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

13.4.3.37 Switch Engine Port 1 Learn Discard Count Register (SWE_LRN_DISCRD_CNT_1)

Register #:	1859h	Size:	32 bits

This register counts the number of MAC addresses on Port 1 that were not learned or were overwritten by a different address due to address table space limitations.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Learn Discard** This field is a count of MAC addresses not learned or overwritten and is cleared when read. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

13.4.3.38 Switch Engine Port 2 Learn Discard Count Register (SWE_LRN_DISCRD_CNT_2)

Register #:	185Ah	Size:	32 bits

This register counts the number of MAC addresses on Port 2 that were not learned or were overwritten by a different address due to address table space limitations.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Learn Discard** This field is a count of MAC addresses not learned or overwritten and is cleared when read. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

13.4.3.39 Switch Engine Interrupt Mask Register (SWE_IMR)

Register #:	1880h	Size:	32 bits

This register contains the Switch Engine interrupt mask, which masks the interrupts in the Switch Engine Interrupt Pending Register (SWE_IPR). All Switch Engine interrupts are masked by setting the Interrupt Mask bit. Clearing this bit will unmask the interrupts. Refer to Chapter 5, "System Interrupts," on page 62 for more information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:1	**RESERVED**	RO	-
0	**Interrupt Mask** When set, this bit masks interrupts from the Switch Engine. The status bits in the Switch Engine Interrupt Pending Register (SWE_IPR) are not affected.	R/W	1b

13.4.3.40 Switch Engine Interrupt Pending Register (SWE_IPR)

Register #:	1881h	Size:	32 bits

This register contains the Switch Engine interrupt status. The status is double buffered. All interrupts in this register may be masked via the Switch Engine Interrupt Mask Register (SWE_IMR) register. Refer to Chapter 5, "System Interrupts," on page 62 for more information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:15	**RESERVED**	RO	-
14:11	**Drop Reason B** When the Set B Valid bit is set, these bits indicate the reason a packet was dropped per the table below:	RC	0h

BIT VALUES	DESCRIPTION
0000	Admit Only VLAN was set and the packet was untagged or priority tagged.
0001	The destination address was not in the ALR table (unknown or broadcast), Enable Membership Checking on ingress was set, Admit Non Member was cleared and the source port was not a member of the incoming VLAN.
0010	The destination address was found in the ALR table but the source port was not in the forwarding state.
0011	The destination address was found in the ALR table but the destination port was not in the forwarding state.
0100	The destination address was found in the ALR table but Enable Membership Checking on ingress was set and the destination port was not a member of the incoming VLAN.
0101	The destination address was found in the ALR table but the Enable Membership Checking on ingress was set, Admit Non Member was cleared and the source port was not a member of the incoming VLAN.
0110	Drop Unknown was set and the destination address was a unicast but not in the ALR table.
0111	Filter Multicast was set and the destination address was a multicast and not in the ALR table.
1000	The packet was a broadcast but exceeded the Broadcast Throttling limit.
1001	The destination address was not in the ALR table (unknown or broadcast) and the source port was not in the forwarding state.
1010	The destination address was found in the ALR table but the source and destination ports were the same.
1011	The destination address was found in the ALR table and the Filter bit was set for that address.
1100	RESERVED.
1101	RESERVED
1110	A packet was received with a VLAN ID of FFFh.
1111	RESERVED

BITS	DESCRIPTION	TYPE	DEFAULT
10:9	**Source Port B** When the Set B Valid bit is set, these bits indicate the source port on which the packet was dropped. **00 = Port 0** **01 = Port 1** **10 = Port 2** **11 = RESERVED**	RC	00b
8	**Set B Valid** When set, bits 14:9 are valid.	RC	0b
7:4	**Drop Reason A** When the Set A Valid bit is set, these bits indicate the reason a packet was dropped. See the Drop Reason B description above for definitions of each value of this field.	RC	0h
3:2	**Source port A** When the Set A Valid bit is set, these bits indicate the source port on which the packet was dropped. **00 = Port 0** **01 = Port 1** **10 = Port 2** **11 = RESERVED**	RC	00b
1	**Set A Valid** When set, bits 7:2 are valid.	RC	0b
0	**Interrupt Pending** When set, a packet dropped event(s) is indicated.	RC	0b

13.4.4 Buffer Manager CSRs

This section details the Buffer Manager (BM) registers. These registers allow configuration and monitoring of the switch buffer levels and usage. A list of the general switch CSRs and their corresponding register numbers is included in Table 13.14.

13.4.4.1 Buffer Manager Configuration Register (BM_CFG)

Register #:	1C00h	Size:	32 bits

This register enables egress rate pacing and ingress rate discarding.

BITS	DESCRIPTION	TYPE	DEFAULT
31:7	**RESERVED**	RO	-
6	**BM Counter Test** When this bit is set, Buffer Manager (BM) counters that normally clear to 0 when read, will be set to 7FFF_FFFC when read.	R/W	0b
5	**Fixed Priority Queue Servicing** When set, output queues are serviced with a fixed priority ordering. When cleared, output queues are serviced with a weighted round robin ordering.	R/W	0b
4:2	**Egress Rate Enable** When set, egress rate pacing is enabled. Bits 4,3,2 correspond to switch ports 2,1,0 respectively.	R/W	0b
1	**Drop on Yellow** When this bit is set, packets that exceed the Ingress Committed Burst Size (colored Yellow) are subjected to random discard. **Note:** See Section 13.4.3.26, "Switch Engine Ingress Rate Command Register (SWE_INGRSS_RATE_CMD)," on page 317 for information on configuring the Ingress Committed Burst Size.	R/W	0b
0	**Drop on Red** When this bit is set, packets that exceed the Ingress Excess Burst Size (colored Red) are discarded. **Note:** See Section 13.4.3.26, "Switch Engine Ingress Rate Command Register (SWE_INGRSS_RATE_CMD)," on page 317 for information on configuring the Ingress Excess Burst Size.	R/W	0b

13.4.4.2 Buffer Manager Drop Level Register (BM_DROP_LVL)

Register #: 1C01h Size: 32 bits

This register configures the overall buffer usage limits.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:8	**Drop Level Low** These bits specify the buffer limit that can be used per ingress port during times when 2 or 3 ports are active. Each buffer is 128 bytes. **Note:** A port is "active" when 36 buffers are in use for that port.	R/W	49h
7:0	**Drop Level High** These bits specify the buffer limit that can be used per ingress port during times when 1 port is active. Each buffer is 128 bytes. **Note:** A port is "active" when 36 buffers are in use for that port.	R/W	64h

13.4.4.3 Buffer Manager Flow Control Pause Level Register (BM_FC_PAUSE_LVL)

Register #: 1C02h Size: 32 bits

This register configures the buffer usage level when a Pause frame or backpressure is sent.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:8	**Pause Level Low** These bits specify the buffer usage level during times when 2 or 3 ports are active. Each buffer is 128 bytes. **Note:** A port is “active” when 36 buffers are in use for that port.	R/W	21h
7:0	**Pause Level High** These bits specify the buffer usage level during times when 1 port is active. Each buffer is 128 bytes. **Note:** A port is “active” when 36 buffers are in use for that port.	R/W	3Ch

13.4.4.4 Buffer Manager Flow Control Resume Level Register (BM_FC_RESUME_LVL)

Register #: 1C03h Size: 32 bits

This register configures the buffer usage level when a Pause frame with a pause value of 1 is sent.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:8	**Resume Level Low** These bits specify the buffer usage level during times when 2 or 3 ports are active. Each buffer is 128 bytes. **Note:** A port is “active” when 36 buffers are in use for that port.	R/W	03h
7:0	**Resume Level High** These bits specify the buffer usage level during times when 0 or 1 ports are active. Each buffer is 128 bytes. **Note:** A port is “active” when 36 buffers are in use for that port.	R/W	07h

13.4.4.5 Buffer Manager Broadcast Buffer Level Register (BM_BCST_LVL)

Register #: 1C04h Size: 32 bits

This register configures the buffer usage limits for broadcasts, multicasts, and unknown unicasts.

BITS	DESCRIPTION	TYPE	DEFAULT
31:8	**RESERVED**	RO	-
7:0	**Broadcast Drop Level** These bits specify the maximum number of buffers that can be used by broadcasts, multicasts, and unknown unicasts. Each buffer is 128 bytes.	R/W	31h

13.4.4.6 Buffer Manager Port 0 Drop Count Register (BM_DRP_CNT_SRC_0)

Register #: 1C05h Size: 32 bits

This register counts the number of packets dropped by the Buffer Manager that were received on Port 0. This count includes packets dropped due to buffer space limits and ingress rate limit discarding (Red and random Yellow dropping).

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Dropped Count** These bits count the number of dropped packets received on Port 0 and is cleared when read. **Note:** The counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

13.4.4.7 Buffer Manager Port 1 Drop Count Register (BM_DRP_CNT_SRC_1)

Register #: 1C06h Size: 32 bits

This register counts the number of packets dropped by the Buffer Manager that were received on Port 1. This count includes packets dropped due to buffer space limits and ingress rate limit discarding (Red and random Yellow dropping).

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Dropped Count** These bits count the number of dropped packets received on Port 1 and is cleared when read. **Note:** The counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

13.4.4.8 Buffer Manager Port 2 Drop Count Register (BM_DRP_CNT_SRC_2)

Register #: 1C07h Size: 32 bits

This register counts the number of packets dropped by the Buffer Manager that were received on Port 2. This count includes packets dropped due to buffer space limits and ingress rate limit discarding (Red and random Yellow dropping).

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Dropped Count** These bits count the number of dropped packets received on Port 2 and is cleared when read. **Note:** The counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

13.4.4.9 Buffer Manager Reset Status Register (BM_RST_STS)

Register #: 1C08h Size: 32 bits

This register indicates when the Buffer Manager has been initialized by the reset process.

BITS	DESCRIPTION	TYPE	DEFAULT
31:1	**RESERVED**	RO	-
0	**BM Ready** When set, indicates the Buffer Manager tables have finished being initialized by the reset process. The initialization is performed upon any reset that resets the Switch Fabric.	RO SS	Note 13.78

Note 13.78 The default value of this bit is 0 immediately following any Switch Fabric reset and then self-sets to 1 once the ALR table is initialized.

13.4.4.10 Buffer Manager Random Discard Table Command Register (BM_RNDM_DSCRD_TBL_CMD)

Register #: 1C09h Size: 32 bits

This register is used to read and write the Random Discard Weight table. A write to this address performs the specified access. This table is used to set the packet drop probability verses the buffer usage.

For a read access, the Buffer Manager Random Discard Table Read Data Register (BM_RNDM_DSCRD_TBL_RDATA) can be read following a write to this register.

For a write access, the Buffer Manager Random Discard Table Write Data Register (BM_RNDM_DSCRD_TBL_WDATA) should be written before writing this register.

<table>
<tr><th>BITS</th><th>DESCRIPTION</th><th>TYPE</th><th>DEFAULT</th></tr>
<tr><td>31:5</td><td>RESERVED</td><td>RO</td><td>-</td></tr>
<tr><td>4</td><td>Random Discard Weight Table RnW
Specifies a read (1) or a write (0) command.</td><td>R/W</td><td>0b</td></tr>
<tr><td>3:0</td><td>Random Discard Weight Table Index
Specifies the buffer usage range that is accessed.

There are a total of 16 probability entries. Each entry corresponds to a range of the number of buffers used by the ingress port. The ranges are structured to give more resolution towards the lower buffer usage end.
<table>
<tr><th>BIT VALUES</th><th>BUFFER USAGE LEVEL</th></tr>
<tr><td>0000</td><td>0 to 7</td></tr>
<tr><td>0001</td><td>8 to 15</td></tr>
<tr><td>0010</td><td>16 to 23</td></tr>
<tr><td>0011</td><td>24 to 31</td></tr>
<tr><td>0100</td><td>32 to 39</td></tr>
<tr><td>0101</td><td>40 to 47</td></tr>
<tr><td>0110</td><td>48 to 55</td></tr>
<tr><td>0111</td><td>56 to 63</td></tr>
<tr><td>1000</td><td>64 to 79</td></tr>
<tr><td>1001</td><td>80 to 95</td></tr>
<tr><td>1010</td><td>96 to 111</td></tr>
<tr><td>1011</td><td>112 to 127</td></tr>
<tr><td>1100</td><td>128 to 159</td></tr>
<tr><td>1101</td><td>160 to 191</td></tr>
<tr><td>1110</td><td>192 to 223</td></tr>
<tr><td>1111</td><td>224 to 255</td></tr>
</table></td><td>R/W</td><td>0h</td></tr>
</table>

13.4.4.11 Buffer Manager Random Discard Table Write Data Register (BM_RNDM_DSCRD_TBL_WDATA)

Register #: 1C0Ah Size: 32 bits

This register is used to write the Random Discard Weight table.

Note: The Random Discard Weight table is not initialized upon reset or power-up. If a random discard is enabled, the full table should be initialized by the host.

BITS	DESCRIPTION	TYPE	DEFAULT
31:10	**RESERVED**	RO	-
9:0	**Drop Probability** These bits specify the discard probability of a packet that has been colored Yellow by the ingress metering. The probability is given in 1/1024's. For example, a setting of 1 is one in 1024, or approximately 0.1%. A setting of all ones (1023) is 1023 in 1024, or approximately 99.9%. There are a total of 16 probability entries. Each entry corresponds to a range of the number of buffers used by the ingress port, as specified in Section 13.4.4.10, "Buffer Manager Random Discard Table Command Register (BM_RNDM_DSCRD_TBL_CMD)".	R/W	000h

13.4.4.12 Buffer Manager Random Discard Table Read Data Register (BM_RNDM_DSCRD_TBL_RDATA)

Register #: 1C0Bh Size: 32 bits

This register is used to read the Random Discard Weight table.

BITS	DESCRIPTION	TYPE	DEFAULT
31:10	**RESERVED**	RO	-
9:0	**Drop Probability** These bits specify the discard probability of a packet that has been colored Yellow by the ingress metering. The probability is given in 1/1024's. For example, a setting of 1 is one in 1024, or approximately 0.1%. A setting of all ones (1023) is 1023 in 1024, or approximately 99.9%. There are a total of 16 probability entries. Each entry corresponds to a range of the number of buffers used by the ingress port, as specified in Section 13.4.4.10, "Buffer Manager Random Discard Table Command Register (BM_RNDM_DSCRD_TBL_CMD)".	RO	000h

13.4.4.13 Buffer Manager Egress Port Type Register (BM_EGRSS_PORT_TYPE)

Register #: 1C0Ch Size: 32 bits

This register is used to configure the egress VLAN tagging rules. See Section 6.5.6, "Adding, Removing, and Changing VLAN Tags," on page 92 for additional details.

BITS	DESCRIPTION	TYPE	DEFAULT
31:23	**RESERVED**	RO	-
22	**VID/Priority Select Port 2** This bit determines the VID and priority in inserted or changed tags. **0: The default VID of the ingress port / priority calculated on ingress.** **1: The default VID / priority of the egress port.** This is only used when the Egress Port Type is set as Hybrid.	R/W	0b
21	**Insert Tag Port 2** When set, untagged packets will have a tag added.The VID and priority is determined by the VID/Priority Select Port 2 bit. The un-tag bit in the VLAN table for the default VLAN ID also needs to be cleared in order for the tag to be inserted. This is only used when the Egress Port Type is set as Hybrid.	R/W	0b
20	**Change VLAN ID Port 2** When set, regular tagged packets will have their VLAN ID overwritten with the Default VLAN ID of either the ingress or egress port, as determined by the VID/Priority Select Port 2 bit. The Change Tag bit also needs to be set. The un-tag bit in the VLAN table for the incoming VLAN ID also needs to be cleared, otherwise the tag will be removed instead. Priority tagged packets will have their VLAN ID overwritten with the Default VLAN ID of either the ingress or egress port independent of this bit. This is only used when the Egress Port Type is set as Hybrid.	R/W	0b
19	**Change Priority Port 2** When set, regular tagged and priority tagged packets will have their Priority overwritten with the priority determined by the VID/Priority Select Port 2 bit. For regular tagged packets, the Change Tag bit also needs to be set. The un-tag bit in the VLAN table for the incoming VLAN ID also needs to be cleared, otherwise the tag would be removed instead. This is only used when the Egress Port Type is set as Hybrid.	R/W	0b
18	**Change Tag Port 2** When set, allows the Change Tag and Change Priority bits to affect regular tagged packets. This bit has no affect on priority tagged packets. This is only used when the Egress Port Type is set as Hybrid.	R/W	0b

<table>
<tr><th>BITS</th><th>DESCRIPTION</th><th>TYPE</th><th>DEFAULT</th></tr>
<tr><td>17:16</td><td>Egress Port Type Port 2
These bits set the egress port type which determines the tagging/un-tagging rules.
<table>
<tr><th>BIT VALUES</th><th>EGRESS PORT TYPE</th></tr>
<tr><td>00</td><td>Dumb
Packets from regular ports pass untouched. Special tagged packets from the External MII port have their tagged stripped.</td></tr>
<tr><td>01</td><td>Access
Tagged packets (including special tagged packets from the External MII port) have their tagged stripped.</td></tr>
<tr><td>10</td><td>Hybrid
Supports a mix of tagging, un-tagging and changing tags. See Section 6.5.6, "Adding, Removing, and Changing VLAN Tags," on page 92 for additional details.</td></tr>
<tr><td>11</td><td>CPU
A special tag is added to indicate the source of the packet. See Section 6.5.6, "Adding, Removing, and Changing VLAN Tags," on page 92 for additional details.</td></tr>
</table></td><td>R/W</td><td>0b</td></tr>
<tr><td>15</td><td>RESERVED</td><td>RO</td><td>-</td></tr>
<tr><td>14</td><td>VID/Priority Select Port 1
Identical to VID/Priority Select Port 2 definition above.</td><td>R/W</td><td>0b</td></tr>
<tr><td>13</td><td>Insert Tag Port 1
Identical to Insert Tag Port 2 definition above.</td><td>R/W</td><td>0b</td></tr>
<tr><td>12</td><td>Change VLAN ID Port 1
Identical to Change VLAN ID Port 2 definition above.</td><td>R/W</td><td>0b</td></tr>
<tr><td>11</td><td>Change Priority Port 1
Identical to Change Priority Port 2 definition above.</td><td>R/W</td><td>0b</td></tr>
<tr><td>10</td><td>Change Tag Port 1
Identical to Change Tag Port 2 definition above.</td><td>R/W</td><td>0b</td></tr>
<tr><td>9:8</td><td>Egress Port Type Port 1
Identical to Egress Port Type Port 2 definition above.</td><td>R/W</td><td>0b</td></tr>
<tr><td>7</td><td>RESERVED</td><td>RO</td><td>-</td></tr>
<tr><td>6</td><td>VID/Priority Select Port 0
Identical to VID/Priority Select Port 2 definition above.</td><td>R/W</td><td>0b</td></tr>
<tr><td>5</td><td>Insert Tag Port 0
Identical to Insert Tag Port 2 definition above.</td><td>R/W</td><td>0b</td></tr>
<tr><td>4</td><td>Change VLAN ID Port 0
Identical to Change VLAN ID Port 2 definition above.</td><td>R/W</td><td>0b</td></tr>
<tr><td>3</td><td>Change Priority Port 0
Identical to Change Priority Port 2 definition above.</td><td>R/W</td><td>0b</td></tr>
<tr><td>2</td><td>Change Tag Port 0
Identical to Change Tag Port 2 definition above.</td><td>R/W</td><td>0b</td></tr>
<tr><td>1:0</td><td>Egress Port Type Port 0
Identical to Egress Port Type Port 2 definition above.</td><td>R/W</td><td>0b</td></tr>
</table>

13.4.4.14 Buffer Manager Port 0 Egress Rate Priority Queue 0/1 Register (BM_EGRSS_RATE_00_01)

Register #: 1C0Dh Size: 32 bits

This register, along with the Buffer Manager Configuration Register (BM_CFG), is used to configure the egress rate pacing.

BITS	DESCRIPTION	TYPE	DEFAULT
31:26	**RESERVED**	RO	-
25:13	**Egress Rate Port 0 Priority Queue 1** These bits specify the egress data rate for the Port 0 priority queue 1. The rate is specified in time per byte. The time is this value plus 1 times 20nS.	R/W	0000h
12:0	**Egress Rate Port 0 Priority Queue 0** These bits specify the egress data rate for the Port 0 priority queue 0. The rate is specified in time per byte. The time is this value plus 1 times 20nS.	R/W	0000h

13.4.4.15 Buffer Manager Port 0 Egress Rate Priority Queue 2/3 Register (BM_EGRSS_RATE_02_03)

Register #: 1C0Eh Size: 32 bits

This register, along with the Buffer Manager Configuration Register (BM_CFG), is used to configure the egress rate pacing.

BITS	DESCRIPTION	TYPE	DEFAULT
31:26	**RESERVED**	RO	-
25:13	**Egress Rate Port 0 Priority Queue 3** These bits specify the egress data rate for the Port 0 priority queue 3. The rate is specified in time per byte. The time is this value plus 1 times 20nS.	R/W	0000h
12:0	**Egress Rate Port 0 Priority Queue 2** These bits specify the egress data rate for the Port 0 priority queue 2. The rate is specified in time per byte. The time is this value plus 1 times 20nS.	R/W	0000h

13.4.4.16 Buffer Manager Port 1 Egress Rate Priority Queue 0/1 Register (BM_EGRSS_RATE_10_11)

Register #: 1C0Fh Size: 32 bits

This register, along with the Buffer Manager Configuration Register (BM_CFG), is used to configure the egress rate pacing.

BITS	DESCRIPTION	TYPE	DEFAULT
31:26	**RESERVED**	RO	-
25:13	**Egress Rate Port 1 Priority Queue 1** These bits specify the egress data rate for the Port 1 priority queue 1. The rate is specified in time per byte. The time is this value plus 1 times 20nS.	R/W	0000h
12:0	**Egress Rate Port 1 Priority Queue 0** These bits specify the egress data rate for the Port 1 priority queue 0. The rate is specified in time per byte. The time is this value plus 1 times 20nS.	R/W	0000h

13.4.4.17 Buffer Manager Port 1 Egress Rate Priority Queue 2/3 Register (BM_EGRSS_RATE_12_13)

Register #: 1C10h Size: 32 bits

This register, along with the Buffer Manager Configuration Register (BM_CFG), is used to configure the egress rate pacing.

BITS	DESCRIPTION	TYPE	DEFAULT
31:26	**RESERVED**	RO	-
25:13	**Egress Rate Port 1 Priority Queue 3** These bits specify the egress data rate for the Port 1 priority queue 3. The rate is specified in time per byte. The time is this value plus 1 times 20nS.	R/W	0000h
12:0	**Egress Rate Port 1 Priority Queue 2** These bits specify the egress data rate for the Port 1 priority queue 2. The rate is specified in time per byte. The time is this value plus 1 times 20nS.	R/W	0000h

13.4.4.18 Buffer Manager Port 2 Egress Rate Priority Queue 0/1 Register (BM_EGRSS_RATE_20_21)

Register #: 1C11h Size: 32 bits

This register, along with the Buffer Manager Configuration Register (BM_CFG), is used to configure the egress rate pacing.

BITS	DESCRIPTION	TYPE	DEFAULT
31:26	**RESERVED**	RO	-
25:13	**Egress Rate Port 2 Priority Queue 1** These bits specify the egress data rate for the Port 2 priority queue 1. The rate is specified in time per byte. The time is this value plus 1 times 20nS.	R/W	0000h
12:0	**Egress Rate Port 2 Priority Queue 0** These bits specify the egress data rate for the Port 2 priority queue 0. The rate is specified in time per byte. The time is this value plus 1 times 20nS.	R/W	0000h

13.4.4.19 Buffer Manager Port 2 Egress Rate Priority Queue 2/3 Register (BM_EGRSS_RATE_22_23)

Register #: 1C12h Size: 32 bits

This register, along with the Buffer Manager Configuration Register (BM_CFG), is used to configure the egress rate pacing.

BITS	DESCRIPTION	TYPE	DEFAULT
31:26	**RESERVED**	RO	-
25:13	**Egress Rate Port 2 Priority Queue 3** These bits specify the egress data rate for the Port 2 priority queue 3. The rate is specified in time per byte. The time is this value plus 1 times 20nS.	R/W	0000h
12:0	**Egress Rate Port 2 Priority Queue 2** These bits specify the egress data rate for the Port 2 priority queue 2. The rate is specified in time per byte. The time is this value plus 1 times 20nS.	R/W	0000h

13.4.4.20 Buffer Manager Port 0 Default VLAN ID and Priority Register (BM_VLAN_0)

Register #: 1C13h Size: 32 bits

This register is used to specify the default VLAN ID and priority of Port 0.

BITS	DESCRIPTION	TYPE	DEFAULT
31:15	**RESERVED**	RO	-
14:12	**Default Priority** These bits specify the default priority that is used when a tag is inserted or changed on egress.	R/W	000b
11:0	**Default VLAN ID** These bits specify the default that is used when a tag is inserted or changed on egress.	R/W	001h

13.4.4.21 Buffer Manager Port 1 Default VLAN ID and Priority Register (BM_VLAN_1)

Register #: 1C14h Size: 32 bits

This register is used to specify the default VLAN ID and priority of Port 1.

BITS	DESCRIPTION	TYPE	DEFAULT
31:15	**RESERVED**	RO	-
14:12	**Default Priority** These bits specify the default priority that is used when a tag is inserted or changed on egress.	R/W	000b
11:0	**Default VLAN ID** These bits specify the default that is used when a tag is inserted or changed on egress.	R/W	001h

13.4.4.22 Buffer Manager Port 2 Default VLAN ID and Priority Register (BM_VLAN_2)

Register #: 1C15h Size: 32 bits

This register is used to specify the default VLAN ID and priority of Port 2.

BITS	DESCRIPTION	TYPE	DEFAULT
31:15	**RESERVED**	RO	-
14:12	**Default Priority** These bits specify the default priority that is used when a tag is inserted or changed on egress.	R/W	000b
11:0	**Default VLAN ID** These bits specify the default that is used when a tag is inserted or changed on egress.	R/W	001h

13.4.4.23 Buffer Manager Port 0 Ingress Rate Drop Count Register (BM_RATE_DRP_CNT_SRC_0)

Register #:	1C16h	Size:	32 bits

This register counts the number of packets received on Port 0 that were dropped by the Buffer Manager due to ingress rate limit discarding (Red and random Yellow dropping).

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Dropped Count** These bits count the number of dropped packets received on Port 0 and is cleared when read. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

13.4.4.24 Buffer Manager Port 1 Ingress Rate Drop Count Register (BM_RATE_DRP_CNT_SRC_1)

Register #: 1C17h Size: 32 bits

This register counts the number of packets received on Port 1 that were dropped by the Buffer Manager due to ingress rate limit discarding (Red and random Yellow dropping).

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Dropped Count** These bits count the number of dropped packets received on Port 1 and is cleared when read. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

13.4.4.25 Buffer Manager Port 2 Ingress Rate Drop Count Register (BM_RATE_DRP_CNT_SRC_2)

Register #: 1C18h Size: 32 bits

This register counts the number of packets received on Port 2 that were dropped by the Buffer Manager due to ingress rate limit discarding (Red and random Yellow dropping).

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Dropped Count** These bits count the number of dropped packets received on Port 2 and is cleared when read. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

13.4.4.26 Buffer Manager Interrupt Mask Register (BM_IMR)

Register #: 1C20h Size: 32 bits

This register contains the Buffer Manager interrupt mask, which masks the interrupts in the Buffer Manager Interrupt Pending Register (BM_IPR). All Buffer Manager interrupts are masked by setting the Interrupt Mask bit. Clearing this bit will unmask the interrupts. Refer to Chapter 5, "System Interrupts," on page 62 for more information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:1	**RESERVED**	RO	-
0	**Interrupt Mask** When set, this bit masks interrupts from the Buffer Manager. The status bits in the Buffer Manager Interrupt Pending Register (BM_IPR) are not affected.	R/W	1b

13.4.4.27 Buffer Manager Interrupt Pending Register (BM_IPR)

Register #:	1C21h	Size:	32 bits

This register contains the Buffer Manager interrupt status. The status is double buffered. All interrupts in this register may be masked via the Buffer Manager Interrupt Mask Register (BM_IMR) register. Refer to Chapter 5, "System Interrupts," on page 62 for more information.

<table>
<tr><th>BITS</th><th>DESCRIPTION</th><th>TYPE</th><th>DEFAULT</th></tr>
<tr><td>31:14</td><td>RESERVED</td><td>RO</td><td>-</td></tr>
<tr><td>13:10</td><td>Drop Reason B
When the Status B Pending bit is set, these bits indicate the reason a packet was dropped per the table below:
<table>
<tr><th>BIT VALUES</th><th>DESCRIPTION</th></tr>
<tr><td>0000</td><td>The destination address was not in the ALR table (unknown or broadcast), and the Broadcast Buffer Level was exceeded.</td></tr>
<tr><td>0001</td><td>Drop on Red was set and the packet was colored Red.</td></tr>
<tr><td>0010</td><td>There were no buffers available.</td></tr>
<tr><td>0011</td><td>There were no memory descriptors available.</td></tr>
<tr><td>0100</td><td>The destination address was not in the ALR table (unknown or broadcast) and there were no valid destination ports.</td></tr>
<tr><td>0101</td><td>The packet had a receive error and was >64 bytes.</td></tr>
<tr><td>0110</td><td>The Buffer Drop Level was exceeded.</td></tr>
<tr><td>0111</td><td>RESERVED</td></tr>
<tr><td>1000</td><td>RESERVED</td></tr>
<tr><td>1001</td><td>Drop on Yellow was set, the packet was colored Yellow and was randomly selected to be dropped.</td></tr>
<tr><td>1010</td><td>RESERVED</td></tr>
<tr><td>1011</td><td>RESERVED</td></tr>
<tr><td>1100</td><td>RESERVED</td></tr>
<tr><td>1101</td><td>RESERVED</td></tr>
<tr><td>1110</td><td>RESERVED</td></tr>
<tr><td>1111</td><td>RESERVED</td></tr>
</table></td><td>RC</td><td>0h</td></tr>
<tr><td>9:8</td><td>Source Port B
When the Status B Pending bit is set, these bits indicate the source port on which the packet was dropped.

00 = Port 0
01 = Port 1
10 = Port 2
11 = RESERVED</td><td>RC</td><td>00b</td></tr>
<tr><td>7</td><td>Status B Pending
When set, bits 13:8 are valid.</td><td>RC</td><td>0b</td></tr>
</table>

BITS	DESCRIPTION	TYPE	DEFAULT
6:3	**Drop Reason A** When the Set A Valid bit is set, these bits indicate the reason a packet was dropped. See the Drop Reason B description above for definitions of each value of this field.	RC	0h
2:1	**Source port A** When the Set A Valid bit is set, these bits indicate the source port on which the packet was dropped. **00 = Port 0** **01 = Port 1** **10 = Port 2** **11 = RESERVED**	RC	00b
0	**Set A Valid** When set, bits 6:1 are valid.	RC	0b

Chapter 14 Operational Characteristics

14.1 Absolute Maximum Ratings*

Supply Voltage (VDD33A1, VDD33A2, VDD33BIAS, VDD33IO) (Note 14.1) . . . . 0V to +3.6V

Positive voltage on signal pins, with respect to ground (Note 14.2) . . . . +6V

Negative voltage on signal pins, with respect to ground (Note 14.3) . . . . -0.5V

Positive voltage on XI, with respect to ground. . . . . +4.6V

Positive voltage on XO, with respect to ground . . . . +2.5V

Ambient Operating Temperature in Still Air (T_A). . . . . Note 14.4

Storage Temperature. . . . .-55^{o}C to +150^{o}C

Lead Temperature Range . . . . Refer to JEDEC Spec. J-STD-020

HBM ESD Performance per JESD 22-A114-E. . . . .+/- 8kV

Contact Discharge ESD Performance per IEC61000-4-2 (Note 14.5). . . . .+/- 8kV

Air-Gap Discharge ESD Performance per IEC61000-4-2 (Note 14.5). . . . .+/- 15kV

Latch-up Performance per EIA/JESD 78 . . . .+/- 200mA

Note 14.1 When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

Note 14.2 This rating does not apply to the following pins: XI, XO, EXRES.

Note 14.3 This rating does not apply to the following pins: EXRES.

Note 14.4 0^{o}C to +70^{o}C for commercial version, -40^{o}C to +85^{o}C for industrial version.

Note 14.5 Performed by independant 3rd party test facility.

*Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Section 14.2, "Operating Conditions**", Section 14.4, "DC Specifications", or any other applicable section of this specification is not implied. Note, device signals are *NOT* 5 volt tolerant.

14.2 Operating Conditions**

Supply Voltage (VDD33A1, VDD33A2, VDD33BIAS, VDD33IO). . . . . +3.3V +/- 300mV

Ambient Operating Temperature in Still Air (T_A). . . . . Note 14.4

**Proper operation of the device is guaranteed only within the ranges specified in this section.

14.3 Power Consumption

This section details the device's typical supply current for 10BASE-T, 100BASE-TX and power management modes of operation.

Table 14.1 Supply and Current (10BASE-T Full-Duplex)

PARAMETER	TYPICAL	UNIT
Supply current @ 3.3V (VDD33A1, VDD33A2, VDD33BIAS, VDD33IO)	111	mA
Ambient Operating Temperature in Still Air (T_A)	24	^oC

Note: The typical supply current value was measured with 100% network loading. Each port's transformer uses an additional 104ma @ 3.3V

Table 14.2 Supply and Current (100BASE-TX Full-Duplex)

PARAMETER	TYPICAL	UNIT
Supply current @ 3.3V (VDD33A1, VDD33A2, VDD33BIAS, VDD33IO)	190	mA
Ambient Operating Temperature in Still Air (T_A)	24	^oC

Note: The typical supply current value was measured with 100% network loading. Each port's transformer uses an additional 42ma @ 3.3V

Table 14.3 Supply and Current (Power Management)

PARAMETER	TYPICAL	UNIT
Both internal PHYs in Energy Detect Power Down @ 3.3V	74	mA
Both Internal PHYs in General Power Down @ 3.3V	44	mA
Ambient Operating Temperature in Still Air (T_A)	24	^oC

Note: Power dissipation is determined by operating frequency, temperature, and supply voltage, as well as external source/sink current requirements. All power dissipation values were measured with both internal PHYs operating.

14.4 DC Specifications

Table 14.4 I/O Buffer Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
IS Type Input Buffer						
Low Input Level	V_{ILI}	-0.3			V	
High Input Level	V_{IHI}			3.6	V	
Negative-Going Threshold	V_{ILT}	1.01	1.18	1.35	V	Schmitt trigger
Positive-Going Threshold	V_{IHT}	1.39	1.6	1.8	V	Schmitt trigger
SchmittTrigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	345	420	485	mV	
Input Leakage	I_{IN}	-10		10	uA	Note 14.6
Input Capacitance	C_{IN}			3	pF	
O8 Type Buffers						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	VDD33IO - 0.4			V	I_{OH} = -8mA
OD8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	VDD33IO - 0.4			V	I_{OH} = -12mA
OD12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
OS12						
High Output Level	V_{OH}	VDD33IO - 0.4			V	I_{OH} = -12mA
O16 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 16mA
High Output Level	V_{OH}	VDD33IO - 0.6			V	I_{OH} = -16mA
ICLK Type Buffer (XI Input)						Note 14.7
Low Input Level	V_{ILI}	-0.3		0.5	V	
High Input Level	V_{IHI}	1.4		3.6	V	

Note 14.6 This specification applies to all IS type inputs and tri-stated bi-directional pins. Internal pull-down and pull-up resistors add +/- 50uA per-pin (typical).

Note 14.7 XI can optionally be driven from a 25MHz single-ended clock oscillator.

Table 14.5 100BASE-TX Transceiver Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Peak Differential Output Voltage High	V_{PPH}	950	-	1050	mVpk	Note 14.8
Peak Differential Output Voltage Low	V_{PPL}	-950	-	-1050	mVpk	Note 14.8
Signal Amplitude Symmetry	V_{SS}	98	-	102	%	Note 14.8
Signal Rise and Fall Time	T_{RF}	3.0	-	5.0	nS	Note 14.8
Rise and Fall Symmetry	T_{RFS}	-	-	0.5	nS	Note 14.8
Duty Cycle Distortion	D_{CD}	35	50	65	%	Note 14.9
Overshoot and Undershoot	V_{OS}	-	-	5	%	
Jitter				1.4	nS	Note 14.10

Note 14.8 Measured at line side of transformer, line replaced by 100Ω (+/- 1%) resistor.

Note 14.9 Offset from 16nS pulse width at 50% of pulse peak.

Note 14.10 Measured differentially.

Table 14.6 10BASE-T Transceiver Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Transmitter Peak Differential Output Voltage	V_{OUT}	2.2	2.5	2.8	V	Note 14.11
Receiver Differential Squelch Threshold	V_{DS}	300	420	585	mV	

Note 14.11 Min/max voltages guaranteed as measured with 100Ω resistive load.

14.5 AC Specifications

This section details the various AC timing specifications of the device.

Note: The I^2C timing adheres to the NXP *I^2C-Bus Specification*. Refer to the NXP *I^2C-Bus Specification* for detailed I^2C timing information.

Note: The MII/SMI timing adheres to the IEEE 802.3 specification.

Note: The RMII timing adheres to the RMII Consortium RMII Specification R1.2.

14.5.1 Equivalent Test Load

Output timing specifications assume the 25pF equivalent test load, unless otherwise noted, as illustrated in Figure 14.1 below.

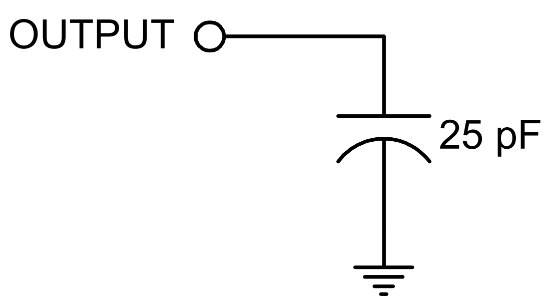


Figure 14.1 Output Equivalent Test Load

14.5.2 Reset and Configuration Strap Timing

This diagram illustrates the nRST pin timing requirements and its relation to the configuration strap pins and output drive. Assertion of nRST is not a requirement. However, if used, it must be asserted for the minimum period specified. Please refer to Section 4.2, "Resets," on page 48 for additional information.

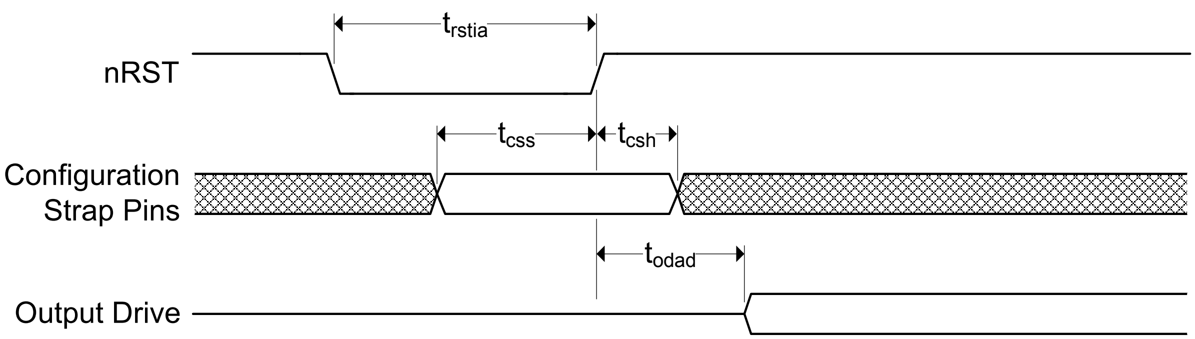


Figure 14.2 nRST Reset Pin Timing

Table 14.7 nRST Reset Pin Timing Values

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{rstia}	nRST input assertion time	200			µS
t_{css}	Configuration strap pins setup to nRST deassertion	200			nS
t_{csh}	Configuration strap pins hold after nRST deassertion	10			nS
t_{odad}	Output drive after deassertion	30			nS

Note: Device configuration straps are latched as a result of nRST assertion. Refer to Section 4.2.4, "Configuration Straps," on page 52 for details.

14.5.3 Power-On Configuration Strap Valid Timing

This diagram illustrates the configuration strap valid timing requirements in relation to power-on. In order for valid configuration strap values to be read at power-on, the following timing requirements must be met.

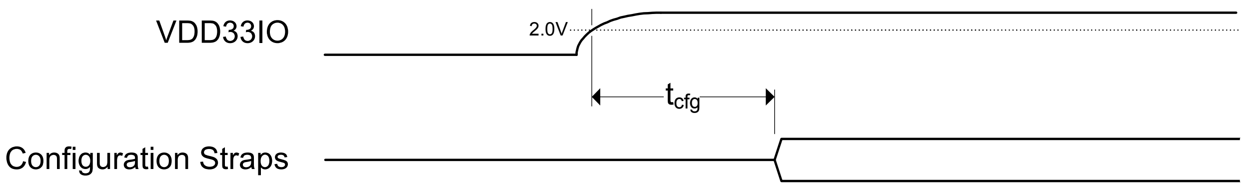


Figure 14.3 Power-On Configuration Strap Latching Timing

Table 14.8 Power-On Configuration Strap Latching Timing Values

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{cfg}	Configuration strap valid time			15	mS

Note: Configuration straps must only be pulled high or low. Configuration straps must not be driven as inputs.

Note: Device configuration straps are also latched as a result of nRST assertion. Refer to Section 14.5.2, "Reset and Configuration Strap Timing," on page 368 and Section 4.2.4, "Configuration Straps," on page 52 for additional details.

14.5.4 MII Interface Timing (MAC Mode)

This section specifies the MII interface input and output timing when in MAC mode. Please refer to Chapter 9, "MII Data Interfaces," on page 129 for additional details.

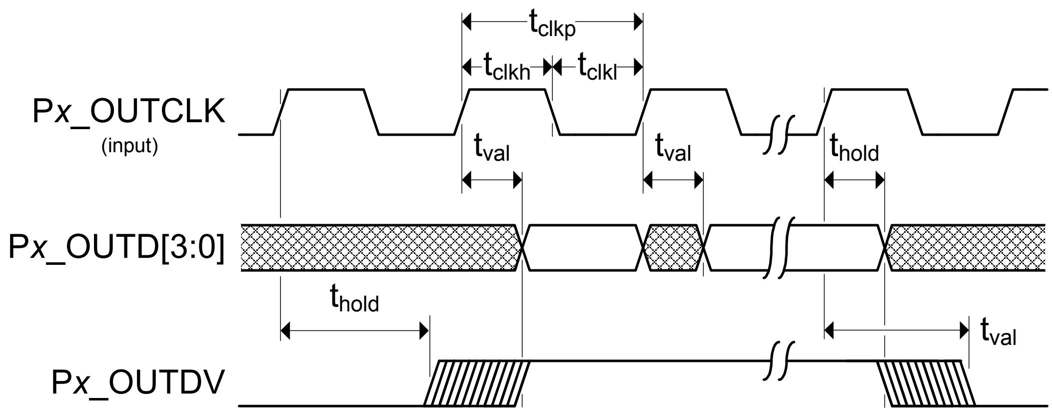


Figure 14.4 MII Output Timing (MAC Mode)

Table 14.9 MII Output Timing Values (MAC Mode)

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
t_{clkp}	Px_OUTCLK period	40		ns	
t_{clkh}	Px_OUTCLK high time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{clkl}	Px_OUTCLK low time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{val}	Px_OUTD[3:0], Px_OUTDV output valid from rising edge of Px_OUTCLK		22.0	ns	Note 14.12
t_{hold}	Px_OUTD[3:0], Px_OUTDV output hold from rising edge of Px_OUTCLK	0		ns	Note 14.12

Note 14.12 Timing was designed for system load between 10pf and 25 pf.

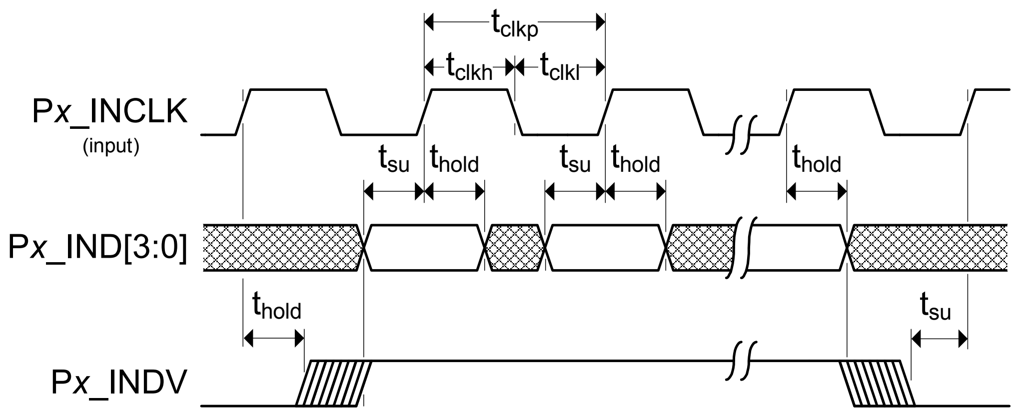


Figure 14.5 MII Input Timing (MAC Mode)

Table 14.10 MII Input Timing Values (MAC Mode)

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
t_{clkp}	Px_INCLK period	40		ns	
t_{clkh}	Px_INCLK high time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{clkl}	Px_INCLK low time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{su}	Px_IND[3:0], Px_INDV setup time to rising edge of Px_INCLK	8.0		ns	Note 14.13
t_{hold}	Px_IND[3:0], Px_INDV hold time after rising edge of Px_INCLK	9.0		ns	Note 14.13

Note 14.13 Timing was designed for system load between 10pf and 25 pf.

14.5.5 MII Interface Timing (PHY Mode)

This section specifies the MII interface input and output timing when in PHY mode. Please refer to Chapter 9, "MII Data Interfaces," on page 129 for additional details.

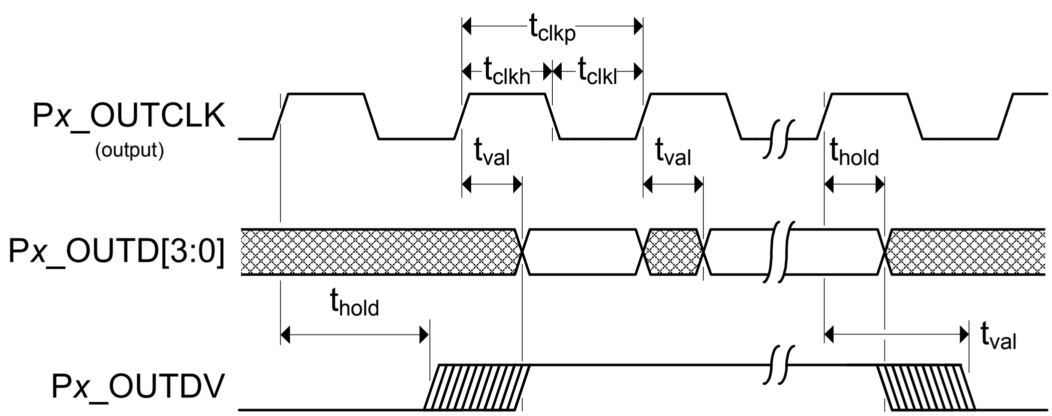


Figure 14.6 MII Output Timing (PHY Mode)

Table 14.11 MII Output Timing Values (PHY Mode)

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
t_{clkp}	Px_OUTCLK period	40		ns	
t_{clkh}	Px_OUTCLK high time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{clkl}	Px_OUTCLK low time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{val}	Px_OUTD[3:0], Px_OUTDV output valid from rising edge of Px_OUTCLK		28.0	ns	Note 14.14
t_{hold}	Px_OUTD[3:0], Px_OUTDV output hold from rising edge of Px_OUTCLK	10.0		ns	Note 14.14

Note 14.14 Timing was designed for system load between 10 pf and 25 pf.

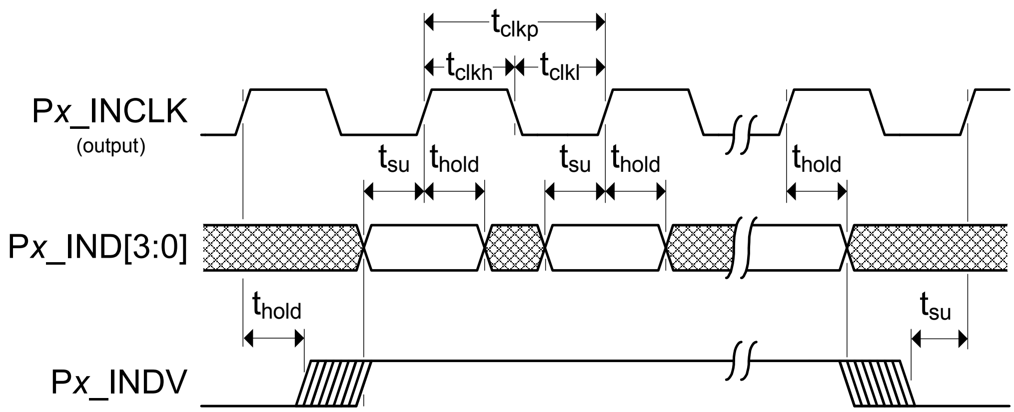


Figure 14.7 MII Input Timing (PHY Mode)

Table 14.12 MII Input Timing Values (PHY Mode)

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
t_{clkp}	Px_INCLK period	40		ns	
t_{clkh}	Px_INCLK high time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{clkl}	Px_INCLK low time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{su}	Px_IND[3:0], Px_INDV setup time to rising edge of Px_INCLK	9.0		ns	Note 14.15
t_{hold}	Px_IND[3:0], Px_INDV hold time after rising edge of Px_INCLK	0		ns	Note 14.15

Note 14.15 Timing was designed for system load between 10 pf and 25 pf.

14.5.6 Turbo MII Interface Timing (MAC Mode)

This section specifies the Turbo MII interface input and output timing when in MAC mode. Please refer to Chapter 9, "MII Data Interfaces," on page 129 for additional details.

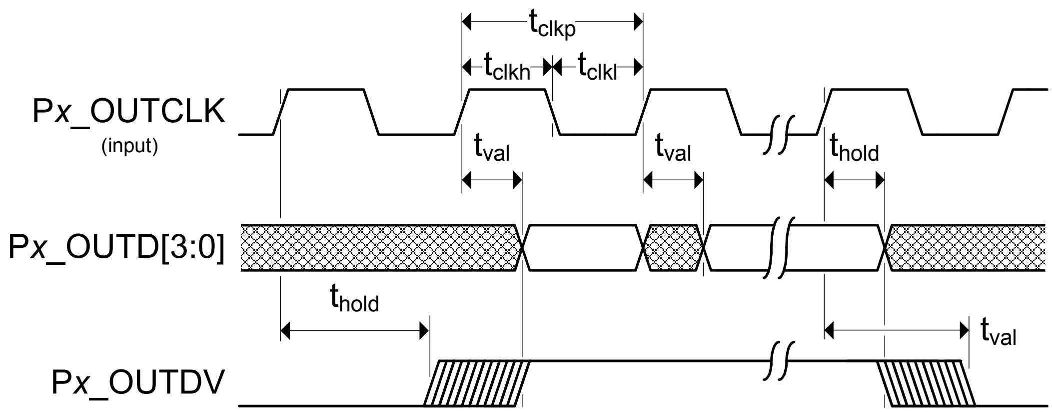


Figure 14.8 Turbo MII Output Timing (MAC Mode)

Table 14.13 Turbo MII Output Timing Values (MAC Mode)

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
t_{clkp}	Px_OUTCLK period	20		ns	
t_{clkh}	Px_OUTCLK high time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{clkl}	Px_OUTCLK low time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{val}	Px_OUTD[3:0], Px_OUTDV output valid from rising edge of Px_OUTCLK		11.0	ns	Note 14.16
t_{hold}	Px_OUTD[3:0], Px_OUTDV output hold from rising edge of Px_OUTCLK	2.0		ns	Note 14.16

Note 14.16 Timing was designed for system load between 10pf and 15 pf.

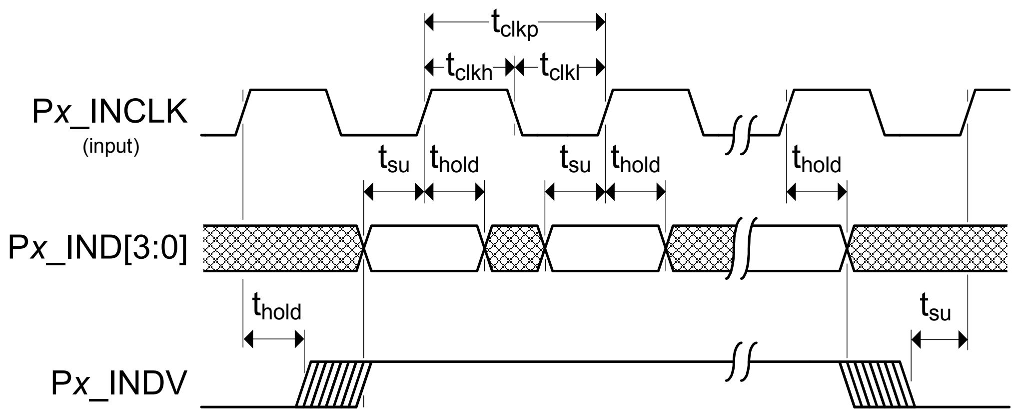


Figure 14.9 Turbo MII Input Timing (MAC Mode)

Table 14.14 Turbo MII Input Timing Values (MAC Mode)

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
t_{clkp}	Px_INCLK period	20		ns	
t_{clkh}	Px_INCLK high time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{clkl}	Px_INCLK low time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{su}	Px_IND[3:0], Px_INDV setup time to rising edge of Px_INCLK	4.0		ns	Note 14.17
t_{hold}	Px_IND[3:0], Px_INDV hold time after rising edge of Px_INCLK	0		ns	Note 14.17

Note 14.17 Timing was designed for system load between 10pf and 15 pf.

14.5.7 Turbo MII Interface Timing (PHY Mode)

This section specifies the Turbo MII interface input and output timing when in PHY mode. Please refer to Chapter 9, "MII Data Interfaces," on page 129 for additional details.

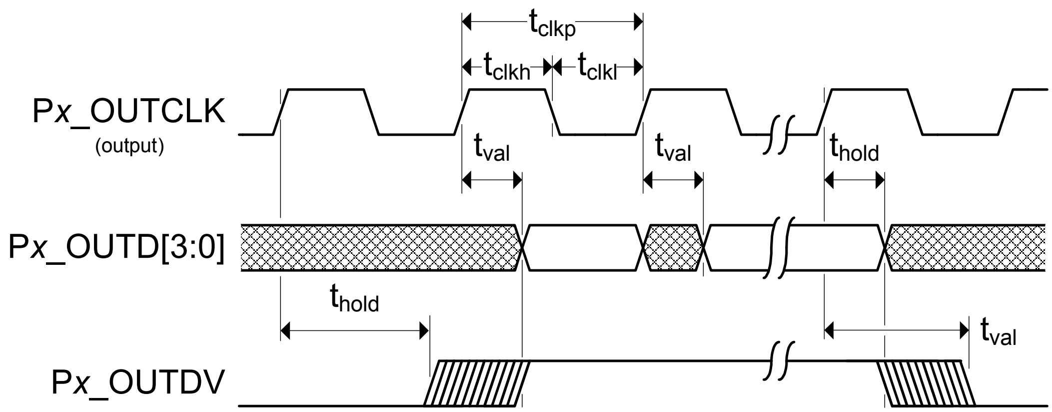


Figure 14.10 Turbo MII Output Timing (PHY Mode)

Table 14.15 Turbo MII Output Timing Values (PHY Mode)

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
t_{clkp}	Px_OUTCLK period	20		ns	
t_{clkh}	Px_OUTCLK high time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{clkl}	Px_OUTCLK low time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{val}	Px_OUTD[3:0], Px_OUTDV output valid from rising edge of Px_OUTCLK		14.0	ns	Note 14.18
t_{hold}	Px_OUTD[3:0], Px_OUTDV output hold from rising edge of Px_OUTCLK	2.0		ns	Note 14.18

Note 14.18 Timing was designed for system load between 10 pf and 15 pf.

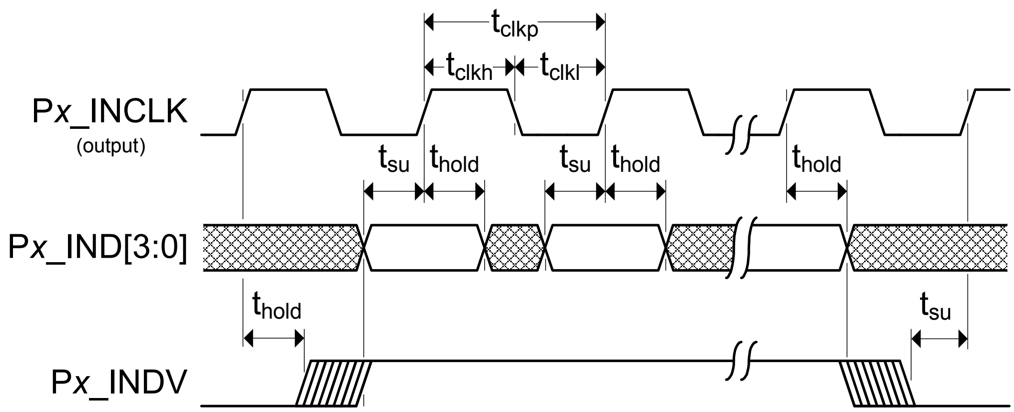


Figure 14.11 Turbo MII Input Timing (PHY Mode)

Table 14.16 Turbo MII Input Timing Values (PHY Mode)

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
t_{clkp}	Px_INCLK period	20		ns	
t_{clkh}	Px_INCLK high time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{clkl}	Px_INCLK low time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{su}	Px_IND[3:0], Px_INDV setup time to rising edge of Px_INCLK	7.0		ns	Note 14.19
t_{hold}	Px_IND[3:0], Px_INDV hold time after rising edge of Px_INCLK	0		ns	Note 14.19

Note 14.19 Timing was designed for system load between 10 pf and 15 pf.

14.5.8 RMII Interface Timing

This section specifies the RMII interface timing for Px_OUTCLK input and output modes. Please refer to Chapter 9, "MII Data Interfaces," on page 129 for additional details.

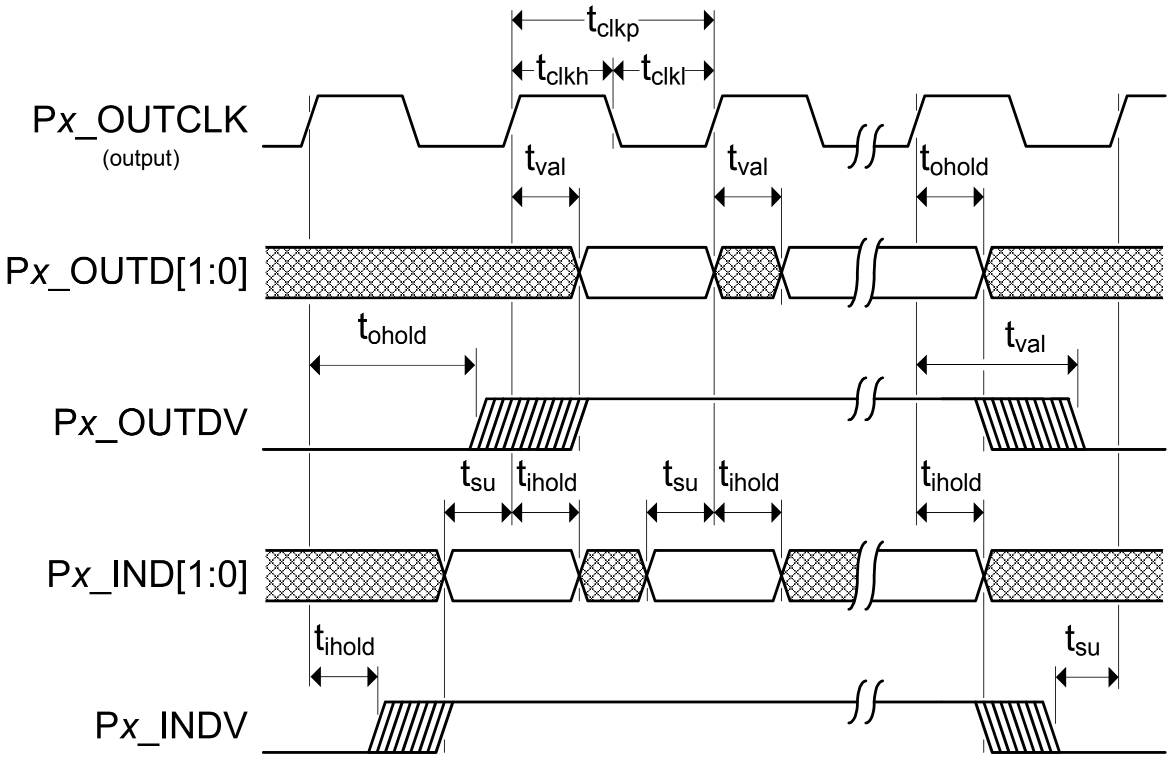


Figure 14.12 RMII Px_OUTCLK Output Mode Timing

Table 14.17 RMII Px_OUTCLK Output Mode Timing Values

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
t_{clkp}	Px_OUTCLK period	20		ns	
t_{clkh}	Px_OUTCLK high time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{clkl}	Px_OUTCLK low time	t_{clkp}*0.4	t_{clkp}*0.6	ns	
t_{val}	Px_OUTD[1:0], Px_OUTDV output valid from rising edge of Px_OUTCLK		14.0	ns	Note 14.20
t_{ohold}	Px_OUTD[1:0], Px_OUTDV output hold from rising edge of Px_OUTCLK	2.0		ns	Note 14.20
t_{su}	Px_IND[1:0], Px_INDV setup time to rising edge of Px_INCLK	4.0		ns	Note 14.20
t_{ihold}	Px_IND[1:0], Px_INDV input hold time after rising edge of Px_INCLK	1.5		ns	Note 14.20

Note 14.20 Timing was designed for system load between 10 pf and 25 pf.

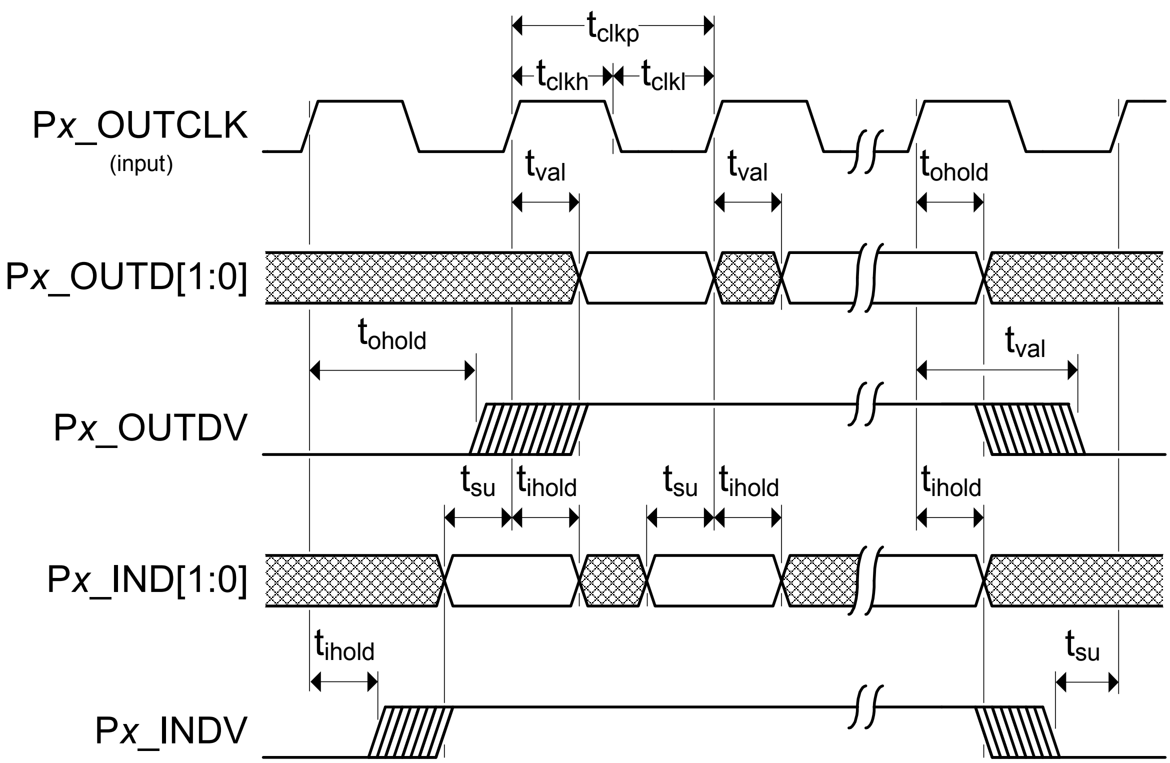


Figure 14.13 RMII Px_OUTCLK Input Mode Timing

Table 14.18 RMII Px_OUTCLK Input Mode Timing Values

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
t_{clkp}	Px_OUTCLK period	20		ns	
t_{clkh}	Px_OUTCLK high time	t_{clkp}*0.35	t_{clkp}*0.65	ns	
t_{clkl}	Px_OUTCLK low time	t_{clkp}*0.35	t_{clkp}*0.65	ns	
t_{oval}	Px_OUTD[1:0], Px_OUTDV output valid from rising edge of Px_OUTCLK		14.0	ns	Note 14.21
t_{ohold}	Px_OUTD[1:0], Px_OUTDV output hold from rising edge of Px_OUTCLK	3.0		ns	Note 14.21
t_{su}	Px_IND[1:0], Px_INDV setup time to rising edge of Px_INCLK	4.0		ns	Note 14.21
t_{ihold}	Px_IND[1:0], Px_INDV input hold time after rising edge of Px_INCLK	1.5		ns	Note 14.21

Note 14.21 Timing was designed for system load between 10 pf and 25 pf.

14.5.9 SMI Timing

This section specifies the SMI timing of the device in both master and slave modes. Please refer to Chapter 9, "MII Data Interfaces," on page 129 for additional details.

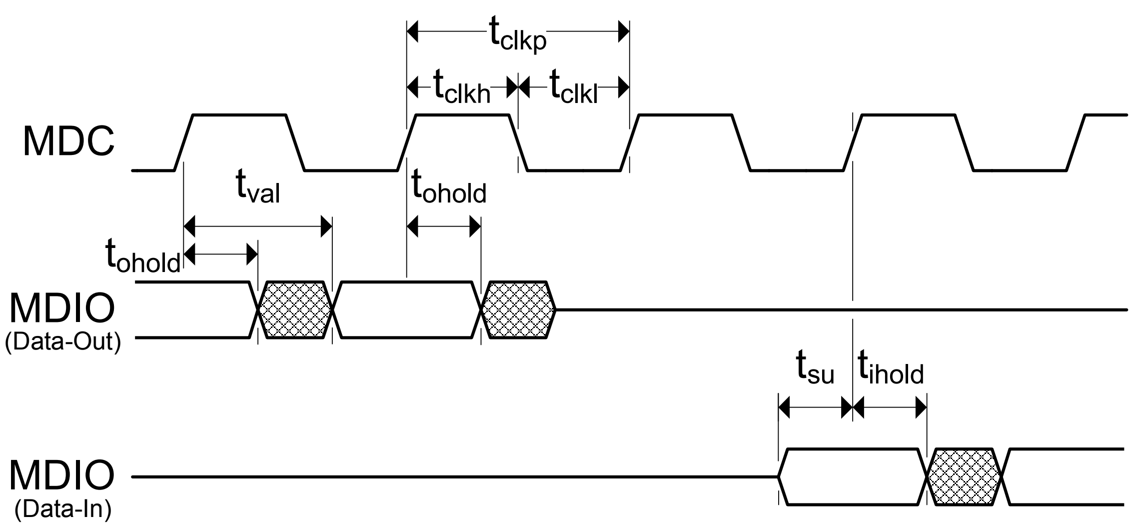


Figure 14.14 SMI Timing

Table 14.19 SMI Timing Values

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
t_{clkp}	MDC period	400		ns	
t_{clkh}	MDC high time (slave mode - clock is input)	160 (80%)		ns	
	MDC high time (master mode - clock is output)	180 (90%)		ns	
t_{clkl}	MDC low time (slave mode - clock is input)	160 (80%)		ns	
	MDC low time (master mode - clock is output)	180 (90%)		ns	
t_{val}	MDIO (slave mode - read from PHY) output valid from rising edge of MDC		300	ns	
	MDIO (master mode - write to PHY) output valid from rising edge of MDC		250	ns	
t_{ohold}	MDIO (slave mode - read from PHY) output hold from rising edge of MDC	10		ns	
	MDIO (master mode - write to PHY) output hold from rising edge of MDC	50		ns	
t_{su}	MDIO (slave mode - write to PHY) setup time to rising edge of MDC	10		ns	
	MDIO (master mode - read from PHY) setup time to rising edge of MDC	70		ns	

Table 14.19 SMI Timing Values

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
t_{ihold}	MDIO (slave mode - write to PHY) input hold time after rising edge of MDC	5		ns	
	MDIO (master mode - read from PHY) input hold time after rising edge of MDC	0		ns	

14.6 Clock Circuit

The device can accept either a 25MHz crystal (preferred) or a 25MHz single-ended clock oscillator (+/-50ppm) input. If the single-ended clock oscillator method is implemented, XO should be left unconnected and XI should be driven with a nominal 0-3.3V clock signal. The input clock duty cycle is 40% minimum, 50% typical and 60% maximum.

It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (XI/XO). See Table 14.20 for crystal specifications.

Table 14.20 Crystal Specifications

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS	NOTES
Crystal Cut	AT, typ					
Crystal Oscillation Mode	Fundamental Mode					
Crystal Calibration Mode	Parallel Resonant Mode					
Frequency	F_{fund}	-	25.000	-	MHz	
Frequency Tolerance @ 25^{o}C	F_{tol}	-	-	+/-50	PPM	Note 14.22
Frequency Stability Over Temp	F_{temp}	-	-	+/-50	PPM	Note 14.22
Frequency Deviation Over Time	F_{age}	-	+/-3 to 5	-	PPM	Note 14.23
Total Allowable PPM Budget		-	-	+/-50	PPM	Note 14.24
Shunt Capacitance	C_O	-	7 typ	-	pF	
Load Capacitance	C_L	-	20 typ	-	pF	
Drive Level	P_W	300	-	-	uW	
Equivalent Series Resistance	R_1	-	-	30	Ohm	
Operating Temperature Range		Note 14.25	-	Note 14.26	^{o}C	
XI Pin Capacitance		-	3 typ	-	pF	Note 14.27
XO Pin Capacitance		-	3 typ	-	pF	Note 14.27

Note 14.22 The maximum allowable values for Frequency Tolerance and Frequency Stability are application dependant. Since any particular application must meet the IEEE +/-50 PPM Total PPM Budget, the combination of these two values must be approximately +/-45 PPM (allowing for aging).

Note 14.23 Frequency Deviation Over Time is also referred to as Aging.

Note 14.24 The total deviation for the Transmitter Clock Frequency is specified by IEEE 802.3 as +/- 50 PPM.

Note 14.25 0^{o}C for commercial version, -40^{o}C for industrial version.

Note 14.26 +70^{o}C for commercial version, +85^{o}C for industrial version.

Note 14.27 This number includes the pad, the bond wire and the lead frame. PCB capacitance is not included in this value. The XO/XI pin and PCB capacitance values are required to accurately calculate the value of the two external load capacitors. These two external load capacitors determine the accuracy of the 25.000 MHz frequency.

Chapter 15 Package Outline

15.1 72-QFN Package Outline

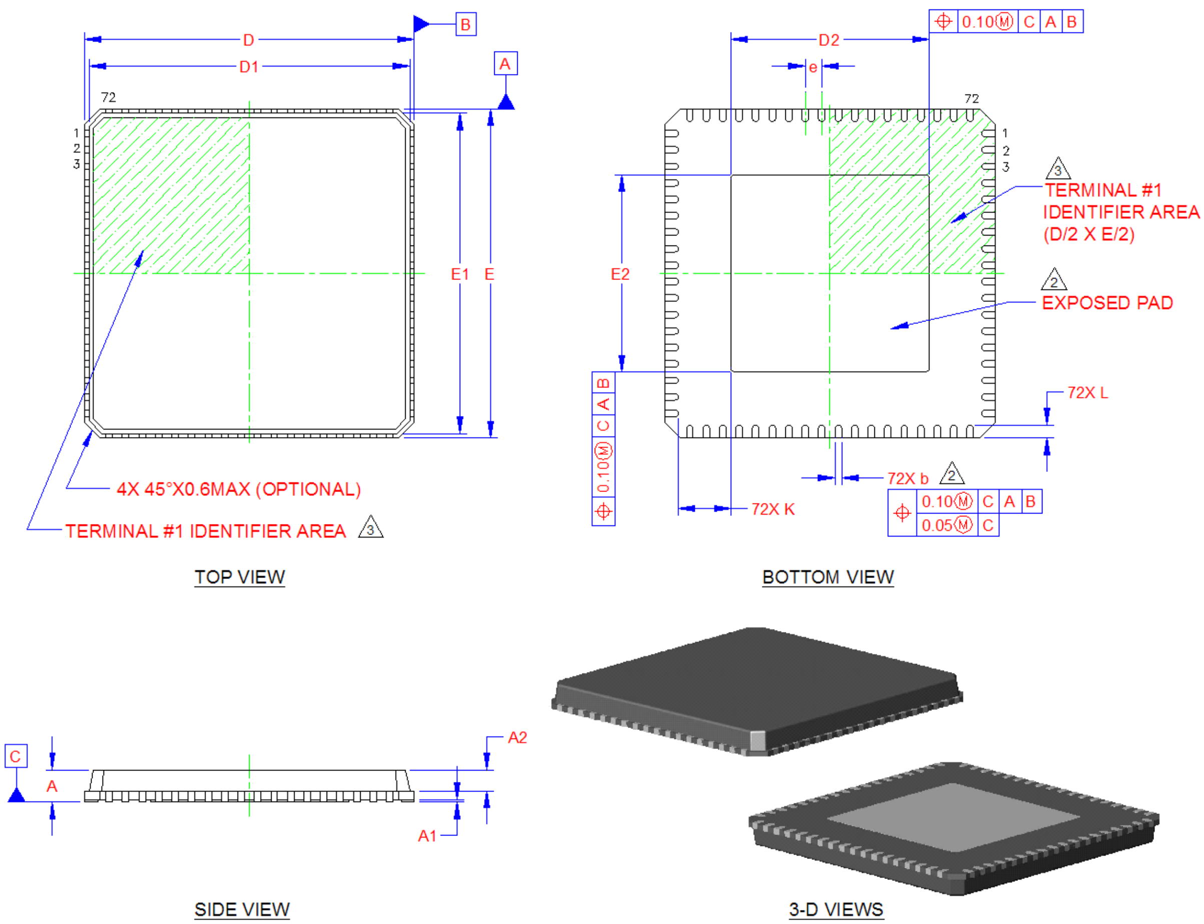


Figure 15.1 72-QFN Package Definition

Table 15.1 72-QFN Dimensions

	MIN	NOMINAL	MAX	REMARKS
A	0.80	0.85	1.00	Overall Package Height
A1	0	0.02	0.05	Standoff
A2	-	0.65	0.80	Mold Cap Thickness
D/E	9.90	10.00	10.10	X/Y Body Size
D1/E1	9.65	9.75	9.85	X/Y Mold Cap Size
D2/E2	5.90	6.00	6.10	X/Y Exposed Pad Size
L	0.30	0.40	0.50	Terminal Length
b	0.18	0.25	0.30	Terminal Width
e	0.50 BSC			Terminal Pitch

Notes:

1. All dimensions are in millimeters unless otherwise noted.
2. Dimension “b” applies to plated terminals and is measured between 0.15 and 0.30mm from the terminal tip.
3. The pin 1 identifier may vary, but is always located within the zone indicated

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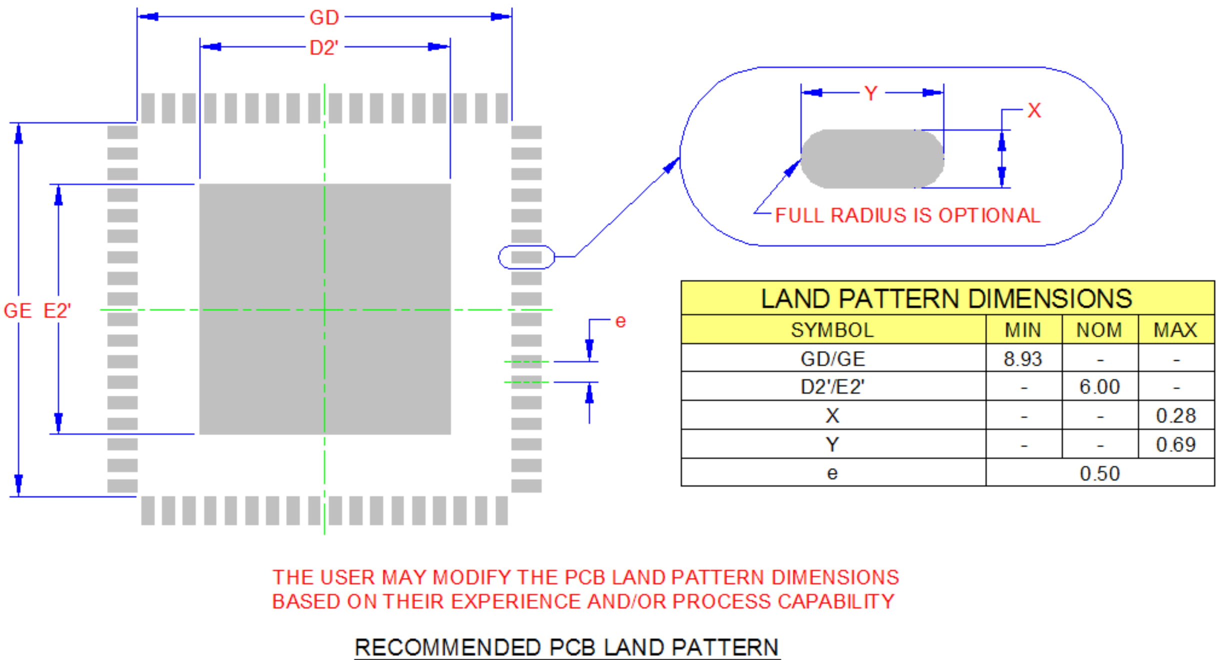

LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	8.93	-	-
D2'/E2'	-	6.00	-
X	-	-	0.28
Y	-	-	0.69
e		0.50	

Figure 15.2 72-QFN Recommended PCB Land Pattern

Chapter 16 Datasheet Revision History

Table 16.1 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.5 (07-08-11)	Table 14.19, “SMI Timing Values,” on page 380	Changed t_{val} to 300 from 200 for slave mode.
	Table 4.3, “Hard-Strap Configuration Strap Definitions,” on page 59	Added notes to the P0_rmii_clock_dir_strap and P1_rmii_clock_dir_strap: “The value of this strap is the inverse of the Px_MODE1 pin.” (where x is the appropriate port)
Rev. 1.4 (07-07-10)	Table 3.7, “Serial Management/EEPROM Pins,” on page 44	Added note to EE_SDA/SDA and EE_SCL/SCL pin descriptions stating “This pin must be pulled-up by an external resistor at all times.”
	Section 13.4.2.23, "Port x MAC Transmit Configuration Register (MAC_TX_CFG_x)," on page 265	Added note to IFG Config bit: “IFG Config values less than 15 are unsupported.”
	Section 13.4.3.10, "Switch Engine VLAN Read Data Register (SWE_VLAN_RD_DATA)," on page 299	Updated field descriptions for Port Default VID and Prioroty, bits 16 and 11:0 to match those of the SWE_VLAN_WR_DATA register.
	Table 7.2, “4B/5B Code Table,” on page 99	Corrected typo in 10001 code group receiver interpretation. “J” changed to “/J/”.
	Section 1.1, "General Terms," on page 13	Added 10BASE-T and 100BASE-TX definitions to general terms list, replacing “100BT”.
	Table 6.1, “Switch Fabric Flow Control Enable Logic,” on page 71	Corrected typo in last column title. “RX FLOW CONTROL ENABLE” changed to “TX FLOW CONTROL ENABLE”
	Section 13.2.6.4, "Virtual PHY Identification LSB Register (VPHY_ID_LSB)," on page 187, Section 13.3.2.4, "Port x PHY Identification LSB Register (PHY_ID_LSB_x)," on page 213	Clarified default values using binary.
	Figure 14.2 nRST Reset Pin Timing on page 368	Updated diagram with correct shading.
Rev. 1.3 (08-27-09)	Section 14.5, "AC Specifications," on page 367	Added MII, RMII, and SMI timing diagrams and specifications.
	Section 14.1, "Absolute Maximum Ratings*," on page 363 and Cover	Added ESD rating information
	Section 14.3, "Power Consumption," on page 364	Added power consumption information

Table 16.1 Customer Revision History (continued)

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
	All	Updated part number information throughout document: “LAN9303DM/LAN9303DMi” changed to “LAN9303M/LAN9303iM”
Rev. 1.2 (12-19-08)		Initial Release