MIC2876

4.8A I_{SW}, Synchronous Boost Regulator with Bi-Directional Load Disconnect

Features

- Up to 95% Efficiency
- Input Voltage Range from 2.5V to 5.5V
- Fully Integrated, High-Efficiency, 2 MHz Synchronous Boost Regulator
- Bi-Directional True Load Disconnect
- Integrated Anti-Ringing Switch
- <1 µA Shutdown Current
- Bypass Mode for $V_{IN} \geq V_{OUT}$
- Overcurrent Protection and Thermal Shutdown
- Fixed and Adjustable Output Versions
- 8-Lead 2 mm × 2 mm UDFN Package

Applications

- Tablets and Smartphones
- USB OTG and HDMI Hosts
- Portable Power Reserve Supplies
- High-Current Parallel Lithium Cell Applications
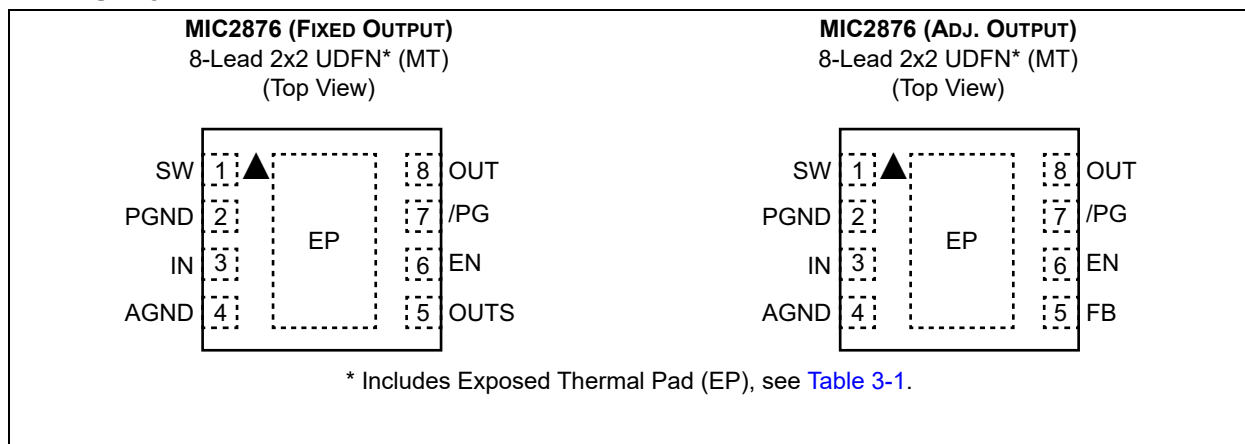- Portable Equipment

General Description

The MIC2876 is a compact and highly efficient 2 MHz synchronous boost regulator with a 4.8A switch. It features a bi-directional load disconnect function that prevents any leakage current between the input and output when the device is disabled. The MIC2876 operates in bypass mode automatically when the input voltage is greater than the target output voltage. At light loads, the boost converter goes to the PFM mode to improve the efficiency.

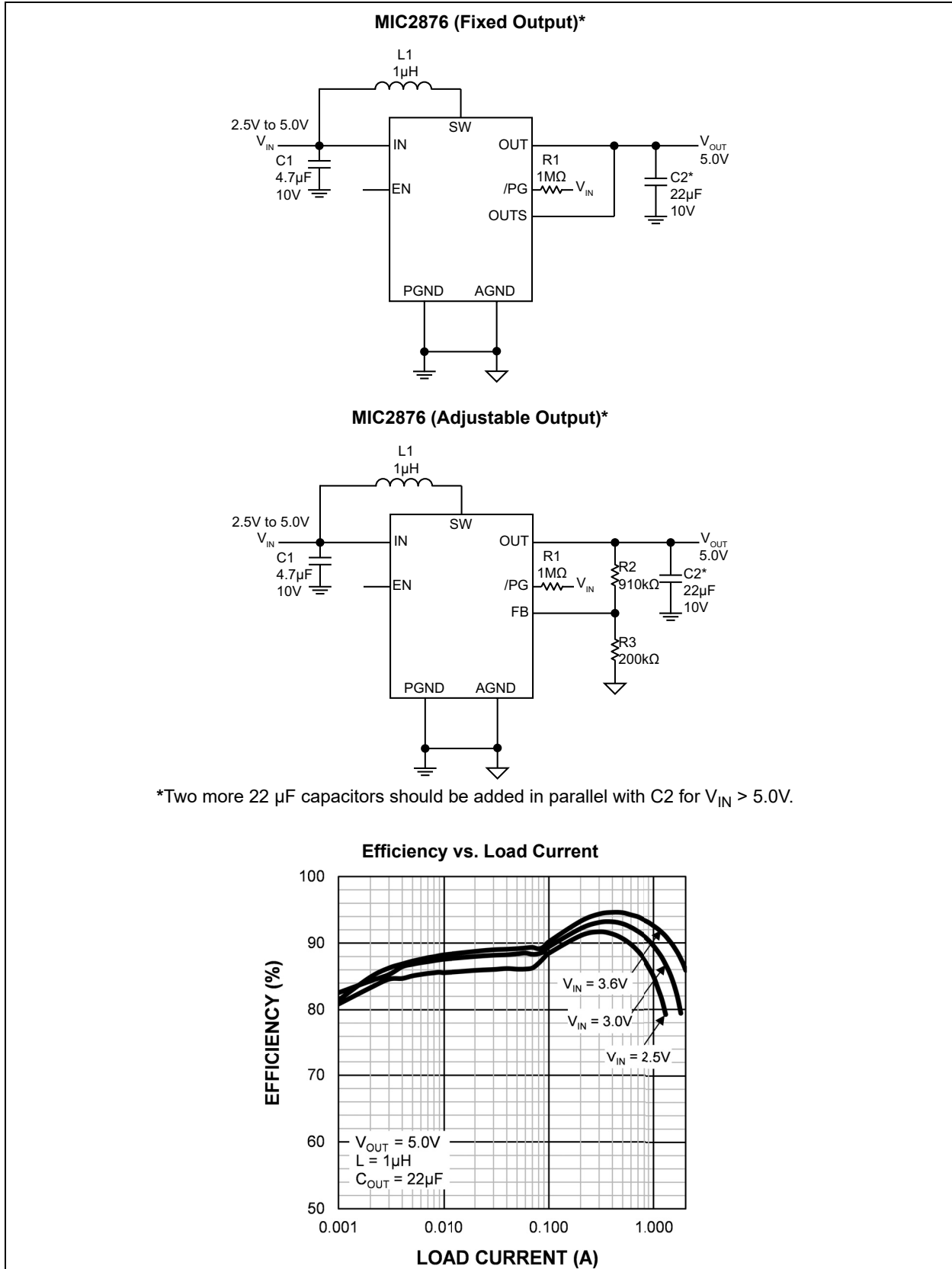The MIC2876 also features an integrated anti-ringing switch to minimize EMI.

The MIC2876 is available in a 8-lead 2 mm × 2 mm UDFN package, with a junction temperature range of –40°C to +125°C.
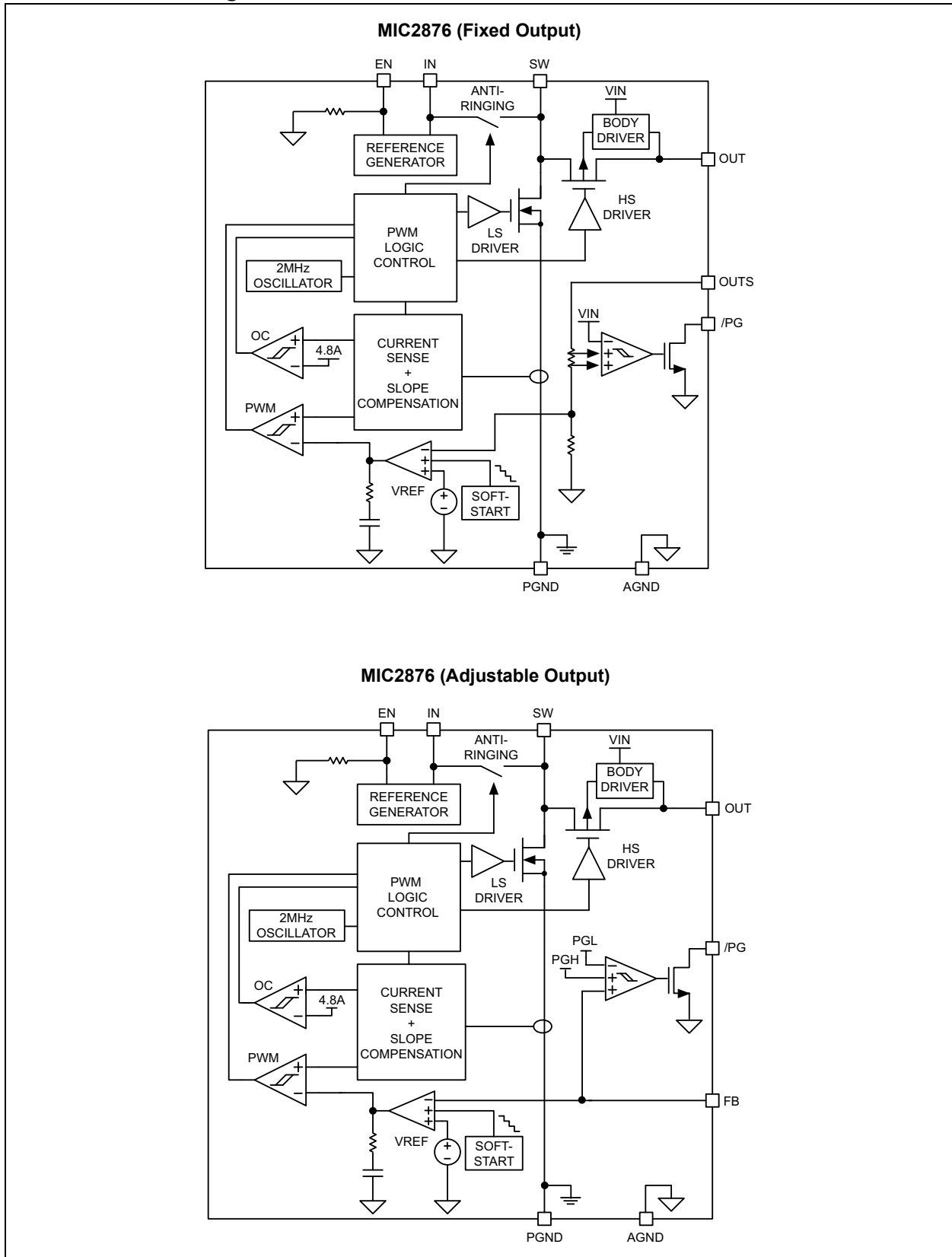
Package Types

MIC2876 (FIXED OUTPUT)
8-Lead 2x2 UDFN* (MT)
(Top View)

SW	1	8 OUT
PGND	2	7 /PG
IN	3	6 EN
AGND	4	5 OUTS

MIC2876 (ADJ. OUTPUT)
8-Lead 2x2 UDFN* (MT)
(Top View)

SW	1	8 OUT
PGND	2	7 /PG
IN	3	6 EN
AGND	4	5 FB

* Includes Exposed Thermal Pad (EP), see Table 3-1.

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Typical Application Schematics

MIC2876 (Fixed Output)*

MIC2876 (Adjustable Output)*

*Two more 22 μF capacitors should be added in parallel with C2 for V_{IN} > 5.0V.

Efficiency vs. Load Current

Functional Block Diagrams

MIC2876 (Fixed Output)

MIC2876 (Adjustable Output)

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1.0   ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

IN, EN, OUT, FB, /PG to PGND .... –0.3V to +6V
AGND to PGND.. –0.3V to +0.3V
ESD Rating (HBM) (Note 1) .... 1.5 kV
ESD Rating (MM) (Note 1) 200V
Power Dissipation (Note 2)..Internally Limited

Operating Ratings ‡

Supply Voltage (V_{IN})... +2.5V to +5.5V
Output Voltage (V_{OUT})..Up to +5.5V
Enable Voltage (V_{EN}) .... 0V to V_{IN}

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

2: The maximum allowable power dissipation of any T_A (ambient temperature) is $P_{D(max)} = (T_{J(max)} - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{IN} = 3.6V, V_{OUT} = 5V, C_{IN} = 4.7 µF, C_{OUT} = 22 µF, L = 1 µH, T_A = 25°C, unless noted. **Bold** values are valid for –40°C ≤ T_J ≤ +125°C. **(Note 1)**.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Supply						
Supply Voltage Range	V_{IN}	**2.5**	—	**5.5**	V	—
UVLO Rising Threshold	V_{UVLOR}	—	2.32	**2.49**	V	—
UVLO Hysteresis	V_{UVLOH}	—	200	—	mV	—
Quiescent Current	I_{VIN}	—	109	—	µA	Non-switching
V_{IN} Shutdown Current	I_{VINSD}	—	1	**3**	µA	V_{EN} = 0V, V_{IN} = 5.5V, V_{OUT} = 0V
V_{OUT} Shutdown Current	I_{VOUTSD}	—	2	**5**	µA	V_{EN} = 0V, V_{IN} = 0.3V, V_{OUT} = 5.5V
Output Voltage	V_{OUT}	V_{IN}	—	5.5	V	—
Feedback Voltage	V_{FB}	**0.8865**	0.9	**0.9135**	V	Adjustable version, I_{OUT} = 0A
Voltage Accuracy	—	**−1.5**	—	**+1.5**	%	Fixed version, I_{OUT} = 0A
Line Regulation	—	—	0.3	—	%/V	2.5V < V_{IN} < 4.5V, I_{OUT} = 500 mA
Load Regulation	—	—	0.2	—	%/A	I_{OUT} = 200 mA to 1200 mA
Maximum Duty Cycle	D_{MAX}	—	92	—	%	—
Minimum Duty Cycle	D_{MIN}	—	6.5	—	%	—
Low-Side Switch Current Limit (Note 2)	I_{LS}	**3.8**	4.8	**5.8**	A	V_{IN} = 2.5V
Switch On-Resistance	PMOS	—	79	—	mΩ	V_{IN} = 3.0V, I_{SW} = 200 mA, V_{OUT} = 5.0V
	NMOS	—	82	—		V_{IN} = 3.0V, I_{SW} = 200 mA, V_{OUT} = 5.0V
Switch Leakage Current	I_{SW}	—	0.2	**5**	µA	V_{EN} = 0V, V_{IN} = 5.5V
Oscillator Frequency	F_{OSC}	**1.6**	2	**2.4**	MHz	—
Overtemperature Shutdown Threshold	T_{SD}	—	155	—	°C	—
Overtemperature Shutdown Hysteresis	—	—	15	—	°C	—
Soft-Start						
Soft-Start Time	T_{SS}	—	1.1	—	ms	V_{OUT} = 5.0V
EN, /PG Control Pins						
EN Threshold Voltage	V_{EN}	**1.5**	—	—	V	Boost converter and chip logic ON
		—	—	**0.4**		Boost converter and chip logic OFF
EN Pin Current	—	—	1.5	**3**	µA	V_{IN} = V_{EN} = 3.6V

Note 1: Specification for packaged product only.

2: Guaranteed by design and characterization.

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{IN} = 3.6V, V_{OUT} = 5V, C_{IN} = 4.7 µF, C_{OUT} = 22 µF, L = 1 µH, T_A = 25°C, unless noted. **Bold** values are valid for –40°C ≤ T_J ≤ +125°C. **(Note 1)**.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Good Threshold (Rising)	$V_{/PG\text{-}THR}$	—	0.9 x V_{OUT}	—	V	—
Power Good Threshold (Falling)	$V_{/PG\text{-}THF}$	—	0.83 x V_{OUT}	—	V	—

Note 1: Specification for packaged product only.

2: Guaranteed by design and characterization.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Operating Temperature	T_J	–40	—	+125	°C	Note 1
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 10s
Package Thermal Resistances						
Thermal Resistance, 8-Lead 2x2 UDFN	θ_{JA}	—	90	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.
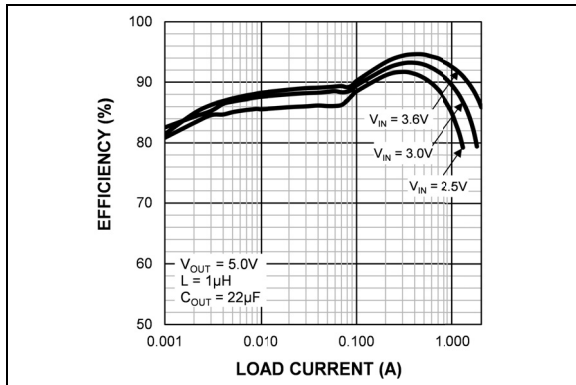
FIGURE 2-1: *Efficiency vs. Load Current.*

FIGURE 2-2: *Output Voltage vs. Load Current.*

FIGURE 2-3: *Output Voltage vs. Input Voltage.*

FIGURE 2-4: *Oscillator Frequency vs. Temperature.*

FIGURE 2-5: *Output Shutdown Current vs. Temperature.*
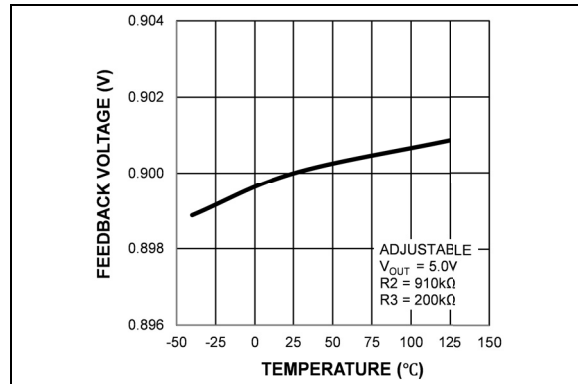
FIGURE 2-6: *Feedback Voltage vs. Temperature.*
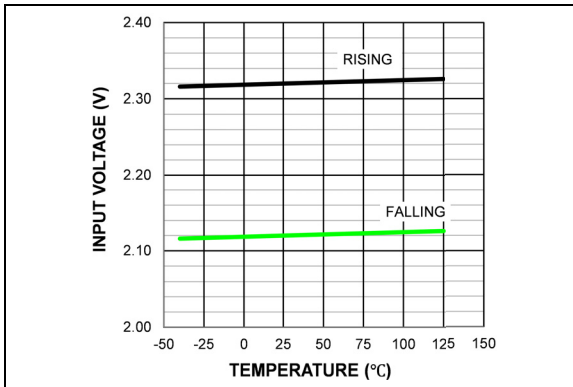
FIGURE 2-7: *UVLO Threshold vs. Temperature.*
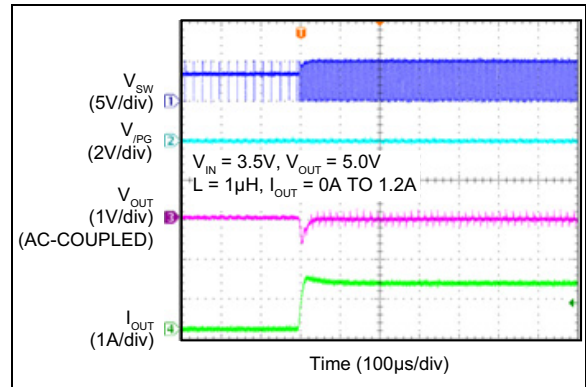
FIGURE 2-10: *Load Transient (0A to 1.2A).*
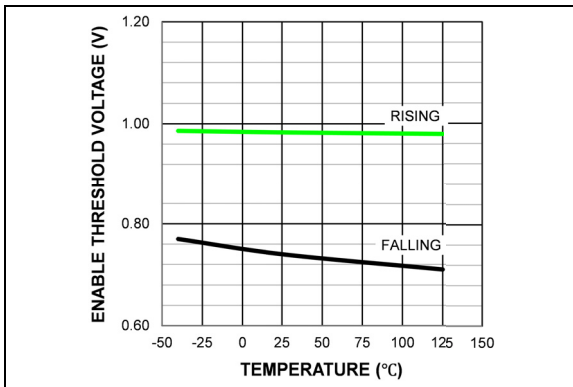
FIGURE 2-8: *Enable Threshold vs. Temperature.*
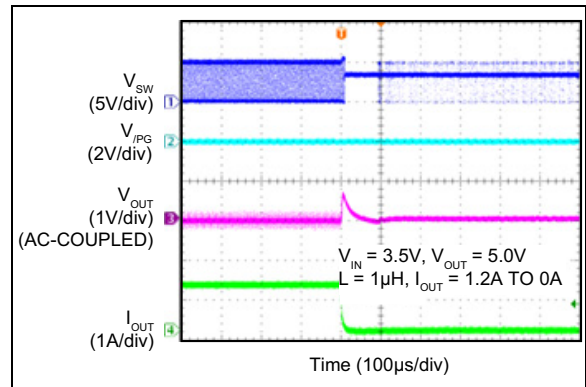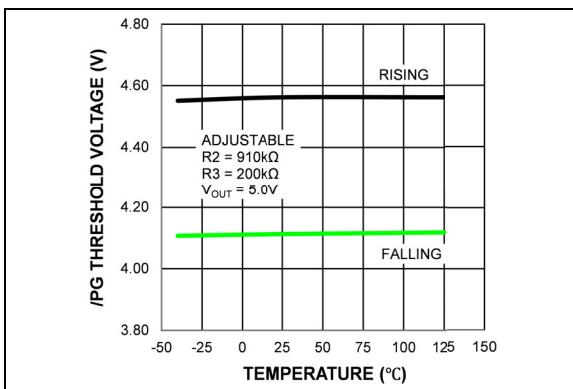

FIGURE 2-11: *Load Transient (1.2A to 0A).*

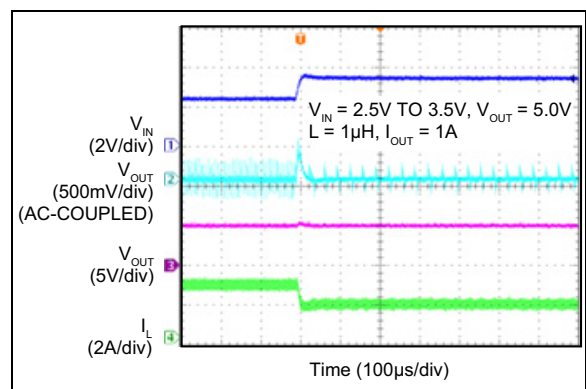**FIGURE 2-9:** *Power Good Threshold vs. Temperature.*

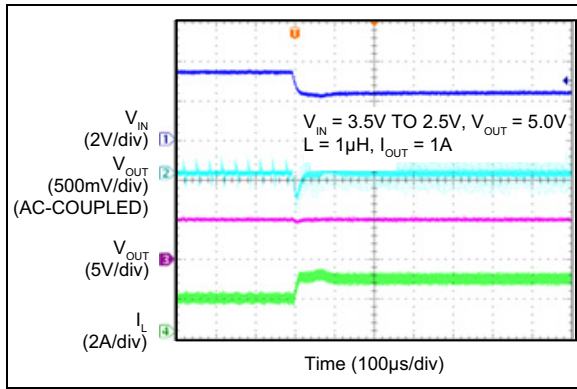**FIGURE 2-12:** *Line Transient (2.5V to 3.5V).*

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FIGURE 2-13: *Line Transient (3.5V to 2.5V).*

FIGURE 2-14: *Line Transient (2.5V to 5.5V).*

FIGURE 2-15: *Line Transient (5.5V to 2.5V).*

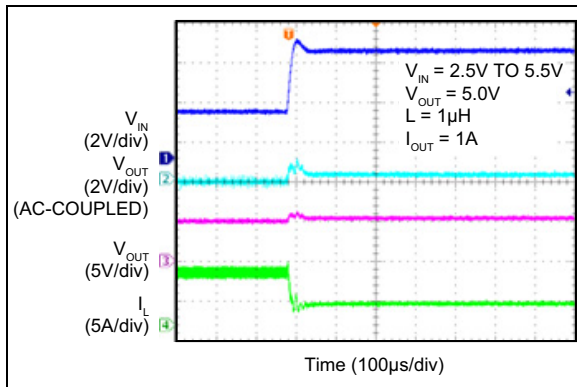**FIGURE 2-16:** *Output Ripple (Pulse Skipping Mode).*

FIGURE 2-17: *Output Ripple (PWM Mode).*
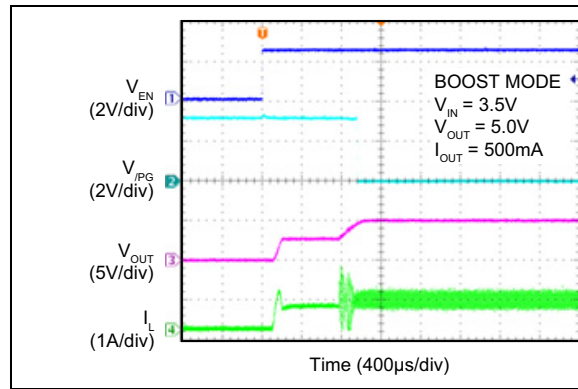

FIGURE 2-18: *Soft-Start (Boost Mode).*
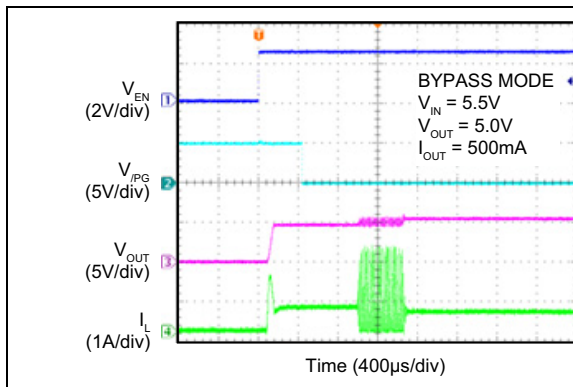
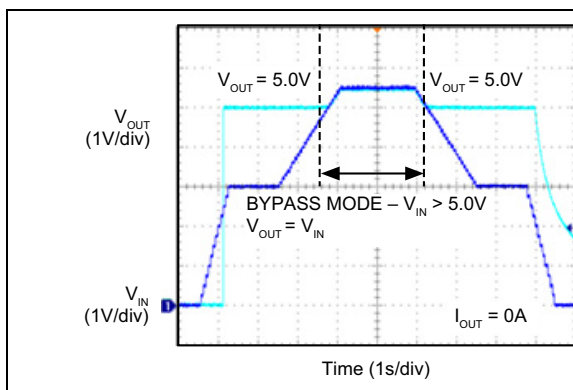**FIGURE 2-19:** *Soft-Start (Bypass Mode).*
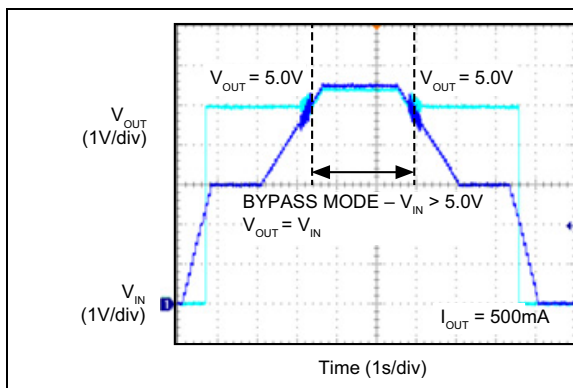

FIGURE 2-20: *Bypass Mode.*

FIGURE 2-21: *Bypass Mode.*

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3.0   PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1:   PIN FUNCTION TABLE

Pin Number Fixed Output	Pin Number Adj. Output	Pin Name	Description
1	1	SW	Boost Converter Switch Node: Connect the inductor between IN and SW pins.
2	2	PGND	Power Ground: The power ground for the synchronous boost DC/DC converter power stage.
3	3	IN	Supply Input: Connect at least 1 µF ceramic capacitor between IN and AGND pins.
4	4	AGND	Analog Ground: The analog ground for the regulator control loop.
5	—	OUTS	Output Voltage Sense Pin: For output voltage regulation in fixed voltage version. Connect to the boost converter output.
—	5	FB	Feedback Pin: For output voltage regulation in adjustable version. Connect to the feedback resistor divider.
6	6	EN	Boost Converter Enable: When this pin is driven low, the IC enters shutdown mode. The EN pin has an internal 2.5 MΩ pull-down resistor. The output is disabled when this pin is left floating.
7	7	/PG	Open Drain Power Good Output (Active Low): The /PG pin is high impedance when the output voltage is below the power good threshold and becomes low once the output is above the power good threshold. The /PG pin has a typical $R_{DS(ON)}$ = 90Ω and requires a pull up resistor of 1 MΩ. Connect /PG pin to AGND when the /PG signal is not used.
8	8	OUT	Boost Converter Output.
EP	EP	ePad	Exposed Heat Sink Pad. Connect to AGND for best thermal performance.

4.0 FUNCTIONAL DESCRIPTION

4.1 Input (IN)

The input supply provides power to the internal MOSFET's gate drivers and control circuitry for the boost regulator. The operating input voltage range is from 2.5V to 5.5V. A 1 µF low-ESR ceramic input capacitor should be connected from IN to AGND as close to MIC2876 as possible to ensure a clean supply voltage for the device. A minimum voltage rating of 10V is recommended for the input capacitor.

4.2 Switch Node (SW)

The MIC2876 has internal low-side and synchronous MOSFET switches. The switch node (SW) between the internal MOSFET switches connects directly to one end of the inductor and provides the current path during switching cycles. The other end of the inductor is connected to the input supply voltage. Due to the high-speed switching on this pin, the switch node should be routed away from sensitive nodes wherever possible.

4.3 Ground Path (AGND)

The ground path (AGND) is for the internal biasing and control circuitry. AGND should be connected to the PCB pad for the package exposed pad. The current loop of the analog ground should be separated from that of the power ground (PGND). AGND should be connected to PGND at a single point.

4.4 Power Ground (PGND)

The power ground (PGND) is the ground path for the high current in the boost switches. The current loop for the power ground should be as short as possible and separate from the AGND loop as applicable.

4.5 Boost Converter Output (OUT)

A low-ESR ceramic capacitor of 22 µF (for operation with $V_{IN} \leq 5.0V$), or 66 µF (for operation with $V_{IN} > 5.0V$) should be connected from V_{OUT} and PGND as close as possible to the MIC2876. A minimum voltage rating of 10V is recommended for the output capacitor.

4.6 Enable (EN)

Enable pin of the MIC2876. A logic high on this pin enables the MIC2876. When this pin is driven low, the MIC2876 enters the shutdown mode. When the EN pin is left floating, it is pulled-down internally by a built-in 2.5 MΩ resistor.

4.7 Feedback/Output Voltage Sense (FB/OUTS)

Feedback or output voltage sense pin for the boost converter. For the fixed voltage version, this pin should be connected to the OUT pin. For the adjustable version, connect a resistor divider to set the output voltage (see "Output Voltage Programming" for more information).

4.8 Power Good Output (/PG)

The open-drain active-low power-good output (/PG) is low when the output voltage is above the power-good threshold. A pull-up resistor of 1 MΩ is recommended.

4.9 Exposed Heat Sink Pad (EP)

The exposed heat sink pad, or ePad (EP), should be connected to AGND for best thermal performance.

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5.0 APPLICATION INFORMATION

5.1 General Description

The MIC2876 is a 2 MHz, current-mode, PWM, synchronous boost converter with an operating input voltage range of 2.5V to 5.5V. At light load, the converter enters pulse-skipping mode to maintain high efficiency over a wide range of load current. The maximum peak current in the boost switch is limited to 4.8A (typical).

5.2 Bi-Directional Output Disconnect

The power stage of the MIC2876 consists of a NMOS transistor as the main switch and a PMOS transistor as the synchronous rectifier. A control circuit turns off the back gate diode of the PMOS to isolate the output from the input supply when the chip is disabled (V_{EN} = 0V). An "always on" maximum supply selector switches the cathode of the backgate diode to either the IN or the OUT (whichever of the two has the higher voltage). As a result, the output of the MIC2876 is bi-directionally isolated from the input as long as the device is disabled. The maximum supply selector and hence the output disconnect function requires only 0.3V at the IN pin to operate.

5.3 Integrated Anti-Ringing Switch

The MIC2876 includes an anti-ringing switch that eliminates the ringing on the SW node of a conventional boost converter operating in the discontinuous conduction mode (DCM). At the end of a switching cycle during DCM operation, both the NMOS and PMOS are turned off. The anti-ringing switch in the MIC2876 clamps the SW pin voltage to IN to dissipate the remaining energy stored in the inductor and the parasitic elements of the power switches.

5.4 Automatic Bypass Mode

The MIC2876 automatically operates in bypass mode when the input voltage is higher than the target output voltage. In bypass mode, the NMOS is turned off while the PMOS is fully turned on to provide a very low impedance path from IN to OUT.

5.5 Soft-Start

The MIC2876 integrates an internal soft-start circuit to limit the inrush current during start-up. When the device is enabled, the PMOS is turned-on slowly to charge the output capacitor to a voltage close to the input voltage. Then, the device begins boost switching cycles to gradually charge up the output voltage to the target V_{OUT}.

5.6 Output Voltage Programming

The MIC2876 has an adjustable version that allows the output voltage to be set by an external resistor divider R2 and R3. The typical feedback voltage is 900 mV, the recommended maximum and minimum output voltage is 5.5V and 3.2V, respectively. The current through the resistor divider should be significantly larger than the current into the FB pin (typically 0.01 µA). It is recommended that 0.1% tolerance feedback resistors must be used and the total resistance of R2 + R3 should be around 1 MΩ. The appropriate R2 and R3 values for the desired output voltage are calculated as in Equation 5-1:

EQUATION 5-1:

$$R2 = R3 \times \left(\frac{V_{OUT}}{0.9\,V} - 1 \right)$$

Example 1:

With a V_{OUT} of 3.3V and an R3 value of 281.2 kΩ (standard value is 280 kΩ), R2 calculates out to 750 kΩ.

Example 2:

With a V_{OUT} of 5V and an R3 value of 200 kΩ, R2 calculates out to 911.1 kΩ (standard value is 910 kΩ).

5.7 Current Limit Protection

The MIC2876 has a current limit feature to protect the part against heavy load conditions. When the current limit comparator determines that the NMOS switch has a peak current higher than 4.8A, the NMOS is turned off and the PMOS is turned on until the next switching cycle. The current limit protection is reset cycle by cycle.

6.0   COMPONENT SELECTION

6.1   Inductor

Inductor selection is a trade-off between efficiency, stability, cost, size, and rated current. Because the boost converter is compensated internally, the recommended inductance is limited from 1 µH to 2.2 µH to ensure system stability and presents a good balance between these considerations.

A large inductance value reduces the peak-to-peak inductor ripple current hence the output ripple voltage. This also reduces both the DC loss and the transition loss at the same inductor's DC resistance (DCR). However, the DCR of an inductor usually increases with the inductance in the same package size. This is due to the longer windings required for an increase in inductance. Since the majority of the input current passes through the inductor, the higher the DCR the lower the efficiency is, and more significantly at higher load currents. On the other hand, inductor with smaller DCR but the same inductance usually has a larger size. The saturation current rating of the selected inductor must be higher than the maximum peak inductor current to be encountered and should be at least 20% to 30% higher than the average inductor current at maximum output current.

6.2   Input Capacitor to the Device Supply

A ceramic capacitor of 1 µF or larger with low ESR is recommended to reduce the input voltage ripple to ensure a clean supply voltage for the device. The input capacitor should be placed as close as possible to the MIC2876 IN and AGND pins with short traces to ensure good noise performance. X5R or X7R type ceramic capacitors are recommended for better tolerance over temperature. The Y5V and Z5U type temperature rating ceramic capacitors are not recommended due to their large reduction in capacitance over temperature and increased resistance at high frequencies. The use of these reduces their ability to filter out high-frequency noise. The rated voltage of the input capacitor should be at least 20% higher than the maximum operating input voltage over the operating temperature range.

6.3   Input Capacitor to the Power Path

A ceramic capacitor of a 4.7 µF of larger with low ESR is recommended to reduce the input voltage fluctuation at the voltage supply of the high-current power path. An input capacitor should be placed close to the V_{IN} supply to the power inductor and PGND for good device performance at heavy load condition. X5R- or X7R-type ceramic capacitors are recommended for better tolerance over temperature.

The Y5V and Z5U type temperature rating ceramic capacitors are not recommended due to their large reduction in capacitance over temperature and increased resistance at high frequencies. These reduce their ability to filter out high-frequency noise. The rated voltage of the input capacitor should be at least 20% higher than the maximum operating input voltage over the operating temperature range.

6.4   Output Capacitor

Output capacitor selection is also a trade-off between performance, size, and cost. Increasing the output capacitor will lead to an improved transient response; however, the size and cost also increase. For operation with V_{IN} ≤ 5.0V, a minimum of 22 µF output capacitor with ESR less than 10 mΩ is required. For operation with V_{IN} > 5.0V, a minimum of 66 µF output capacitor with ESR less than 10 mΩ is required. X5R or X7R type ceramic capacitors are recommended for better tolerance over temperature. Additional capacitors can be added to improve the transient response, and to reduce the ripple of the output when the MIC2876 operates in and out of bypass mode.

The Y5V and Z5U type ceramic capacitors are not recommended due to their wide variation in capacitance over temperature and increased resistance at high frequencies. The rated voltage of the output capacitor should be at least 20% higher than the maximum operating output voltage over the operating temperature range. The 0805 size ceramic capacitor is recommended for smaller ESL at output capacitor which contributes to a smaller voltage spike value at the output voltage of the high-frequency switching boost converter.

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7.0 POWER DISSIPATION

As with all power devices, the ultimate current rating of the output is limited by the thermal properties of the device package and the PCB on which the device is mounted. There is a simple, Ohm's law-type relationship between thermal resistance, power dissipation, and temperature which are analogous to an electrical circuit (see Figure 7-1):
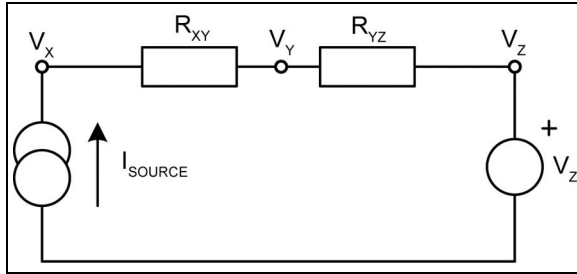

FIGURE 7-1: *Series Electrical Resistance Circuit.*

From this simple circuit we can calculate V_X if we know I_{SOURCE}, V_Z, and the resistor values, R_{XY} and R_{YZ} using Equation 7-1:

EQUATION 7-1:

$$V_X = I_{SOURCE} \times (R_{XY} + R_{YZ}) + V_Z$$

Thermal circuits can be considered using this same rule and can be drawn similarly by replacing current sources with power dissipation (in watts), resistance with thermal resistance (in °C/W) and voltage sources with temperature (in °C).
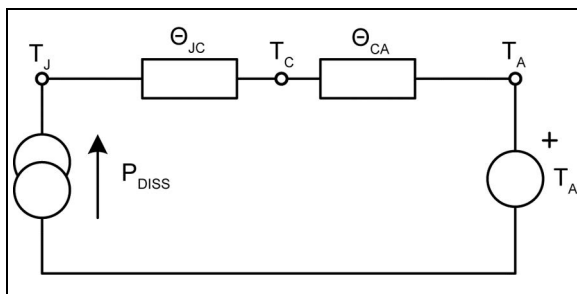

FIGURE 7-2: *Series Thermal Resistance Circuit.*

Now replacing the variables in the equation for V_X, we can find the junction temperature (T_J) from the power dissipation, ambient temperature and the known thermal resistance of the PCB (θ_{CA}) and the package (θ_{JC}).

EQUATION 7-2:

$$T_J = P_{DISS} \times (\theta_{JC} + \theta_{CA}) + T_A$$

As can be seen in the diagram, total thermal resistance $\theta_{JA} = \theta_{JC} + \theta_{CA}$. This can also be written as in Equation 7-3:

EQUATION 7-3:

$$T_J = P_{DISS} \times (\theta_{JA}) + T_A$$

Given that all of the power losses (minus the inductor losses) are effectively in the converter and dissipated within the MIC2876 package, P_{DISS} can be calculated thusly:

EQUATION 7-4:

$$P_{DISS} = \left[P_{OUT} \times \left(\frac{1}{\eta} - 1 \right) \right] - I_{OUT}^2 \times DCR$$

For Linear Mode.

EQUATION 7-5:

$$P_{DISS} = \left[P_{OUT} \times \left(\frac{1}{\eta} - 1 \right) \right] - \left(\frac{I_{OUT}}{1-D} \right)^2 \times DCR$$

For Boost Mode.

EQUATION 7-6:

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

Duty Cycle (Boost).

In the equations above, η is the efficiency taken from the efficiency curves and DCR represents the inductor DCR. θ_{JC} and θ_{JA} are found in the temperature specifications section of the data sheet.

Where the real board area differs from 1" square, θ_{CA} (the PCB thermal resistance), values for various PCB copper areas can be taken from Figure 7-3.

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PC Board Heat Sink Thermal Resistance vs. Area

(Graph: PCB Heat Sink Thermal Resistance (°C/W) on the y-axis from 0 to 70, PCB Heat Sink Area (mm²) on the x-axis from 0 to 6000. Solid trace decreasing from ~70 to ~22. Dashed trace decreasing from ~48 to ~15.)
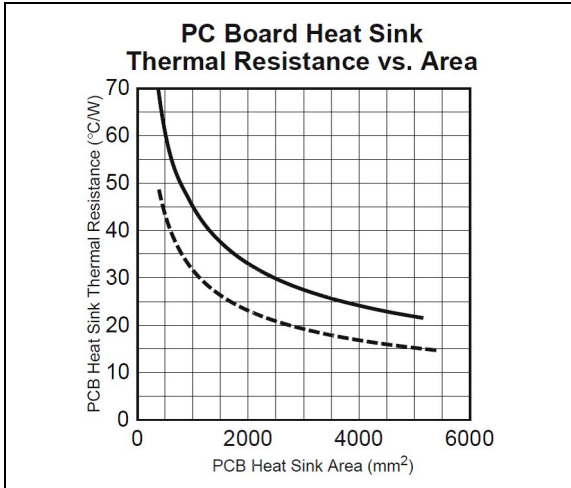
FIGURE 7-3: *Determining PCB Area for a Given PCB Thermal Resistance.*

Figure 7-3 shows the total area of a round or square pad, centered on the device. The solid trace represents the area of a square, single-sided, horizontal, solder masked, copper PC board trace heat sink, measured in square millimeters. No airflow is assumed. The dashed line shows the PC board's trace heat sink covered in black oil-based paint and with 1.3 m/sec (250 feet per minute) airflow. This approaches a "best case" pad heat sink. Conservative design dictates using the solid trace data, which indicates that a maximum pad size of 5000 mm^2 is needed. This is a pad 71 mm × 71 mm (2.8 inches per side).

MIC2876

8.0   PCB LAYOUT GUIDELINES

PCB layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths. The following guidelines should be followed to ensure proper operation of the device. Please refer to the MIC2876 evaluation board document for the recommended placement and layout of components.

8.1   Integrated Circuit (IC)

- Place the IC close to the point-of-load.
- Use fat traces to route the input and output power lines.
- Analog grounds and power ground should be kept separate and connected at a single location at the PCB pad for exposed pad of the IC.
- Place as many thermal vias as possible on the PCB pad for the exposed pad and connect it to the ground plane to ensure a good PCB thermal resistance.

8.2   IN Decoupling Capacitor

- The IN decoupling capacitor must be placed close to the IN pin of the IC and preferably connected directly to the pin and not through any via. The capacitor must be located right at the IC.
- The IN decoupling capacitor should be connected as close as possible to AGND.
- The IN terminal is noise sensitive and the placement of capacitor is very critical.

8.3 V_{IN} Power Path Bulk Capacitor

- The V_{IN} power path bulk capacitor should be placed and connected close to the V_{IN} supply to the power inductor and the PGND of the IC.
- Use either X5R or X7R temperature rating ceramic capacitors. Do not use Y5V or Z5U type ceramic capacitors.

8.4   Inductor

- Keep both the inductor connections to the switch node (SW) and input power line short and wide enough to handle the switching current. Keep the areas of the switching current loops small to minimize the EMI problem.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (SW) away from the noise sensitive pins.
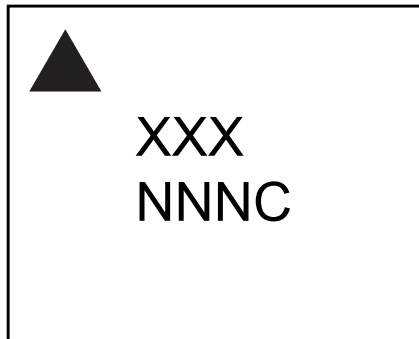- To minimize noise, place a ground plane underneath the inductor.

8.5   Output Capacitor

- Use wide and short traces to connect the output capacitor as close as possible to the OUT and PGND pins without going through via holes to minimize the switching current loop during the main switch off cycle and the switching noise.
- Use either X5R or X7R temperature rating ceramic capacitors. Do not use Y5V or Z5U type ceramic capacitors.
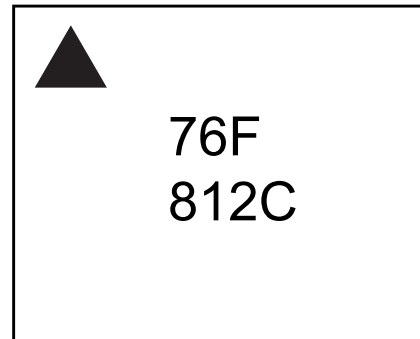
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

8-Lead UDFN*

▲

XXX
NNNC

Example

▲

76F
812C

Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

●, ▲, ▼ Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.
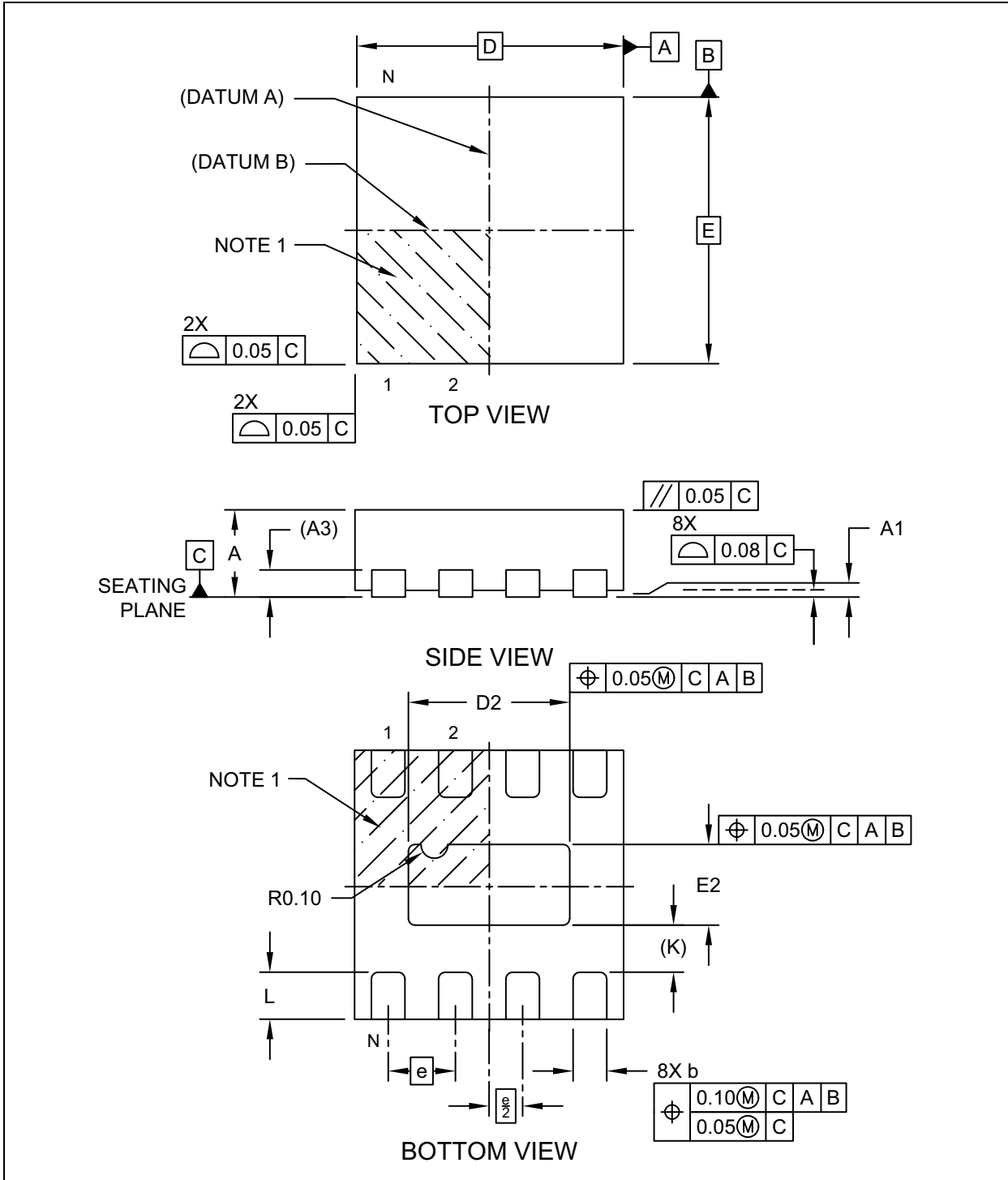
Underbar (_) symbol may not be to scale.

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN; 2 Characters = NN; 1 Character = N

Note: The "C" on the package marking drawings above represents copper bonding wire.

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8-Lead UDFN 2 mm x 2 mm Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

TOP VIEW

SIDE VIEW

BOTTOM VIEW

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8-Lead UDFN 2 mm x 2 mm Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
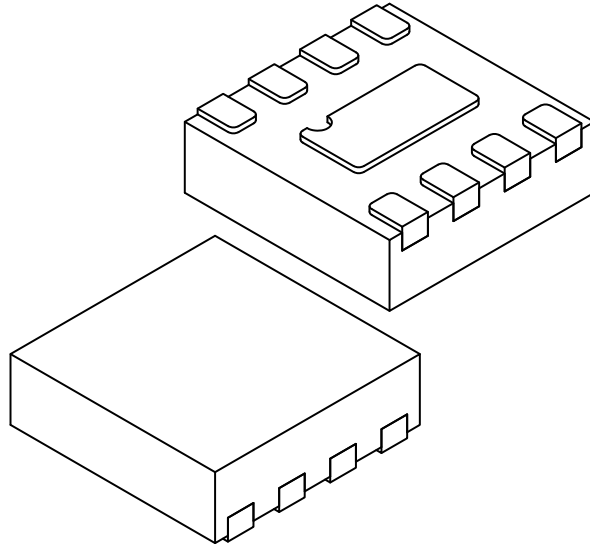
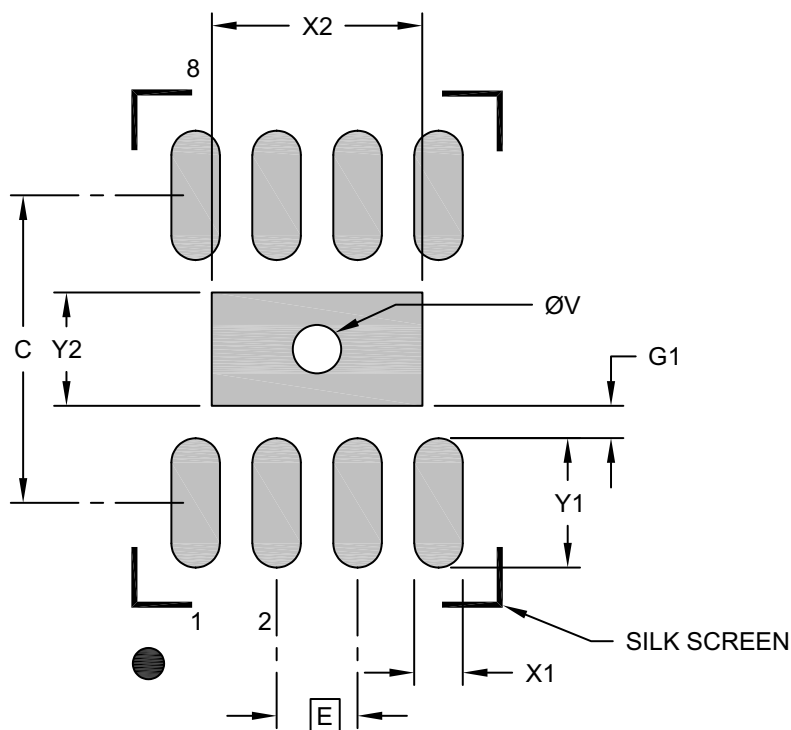|	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.152 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.10	1.20	1.30
Overall Width	E		2.00 BSC	
Exposed Pad Width	E2	0.50	0.60	0.70
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.35	0.40
Terminal-to-Exposed-Pad	K		0.35 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

MIC2876

8-Lead UDFN 2 mm x 2 mm Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			1.30
Optional Center Pad Length	Y2			0.70
Contact Pad Spacing	C		1.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.80
Contact Pad to Center Pad (X8)	G1	0.20		
Thermal Via Diameter	V		0.30	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

    BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

APPENDIX A: REVISION HISTORY

Revision A (July 2016)

- Converted Micrel document MIC2876 to Microchip data sheet DS20005572B.
- Minor text changes throughout.
- Updated TDFN package information to Microchip-standard UDFN.

Revision B (July 2022)

- Corrected package marking drawings and added note below legend in Section 9.1, Package Marking Information.
- Removed incorrect TDFN package outline and replaced with correct UDFN package outline.
- Minor text corrections where needed.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO. – XX X XX – XX

Device | Output Voltage | Temperature | Package | Media Type

Device: MIC2876: 4.8A I$_{SW}$, Synchronous Boost Regulator with Bi-Directional Load Disconnect

Output Voltage:
4.75 = 4.75V
5.0 = 5.00V
5.25 = 5.25V
5.5 = 5.50V
A = Adjustable

Temperature: Y = –40°C to +125°C

Package: MT = 8-Pin 2 mm x 2 mm UDFN (Note)

Media Type:
T5 = 500/Reel
TR = 5,000/Reel

Note: Ultra-Thin DFN is an RoHS-compliant package. Lead finish is Pb-free and Matte Tin. Mold compound is Halogen free.
▲ = UDFN Pin 1 identifier

Examples:

a) MIC2876-4.75YMT-T5: MIC2876, 4.75V Output Voltage, –40°C to +125°C Temp. Range, 8-Pin UDFN, 500/Reel

b) MIC2876-4.75YMT-TR: MIC2876, 4.75V Output Voltage, –40°C to +125°C Temp. Range, 8-Pin UDFN, 5,000/Reel

c) MIC2876-5.0YMT-T5: MIC2876, 5.00V Output Voltage, –40°C to +125°C Temp. Range, 8-Pin UDFN, 500/Reel

d) MIC2876-5.0YMT-TR: MIC2876, 5.00V Output Voltage, –40°C to +125°C Temp. Range, 8-Pin UDFN, 5,000/Reel

e) MIC2876-5.25YMT-T5: MIC2876, 5.25V Output Voltage, –40°C to +125°C Temp. Range, 8-Pin UDFN, 500/Reel

f) MIC2876-5.25YMT-TR: MIC2876, 5.25V Output Voltage, –40°C to +125°C Temp. Range, 8-Pin UDFN, 5,000/Reel

g) MIC2876-5.5YMT-T5: MIC2876, 5.50V Output Voltage, –40°C to +125°C Temp. Range, 8-Pin UDFN, 500/Reel

h) MIC2876-5.5YMT-TR: MIC2876, 5.50V Output Voltage, –40°C to +125°C Temp. Range, 8-Pin UDFN, 5,000/Reel

i) MIC2876-AYMT-T5: MIC2876, Adjustable Output Voltage, –40°C to +125°C Temp. Range, 8-Pin UDFN, 500/Reel

j) MIC2876-AYMT-TR: MIC2876, Adjustable Output Voltage, –40°C to +125°C Temp. Range, 8-Pin UDFN, 5,000/Reel

NOTES:

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