Platform Cable USB II

DS593 (v1.2) June 9, 2008 **Advance Product Specification**

Features

- High-performance FPGA and PROM programming and configuration
  - Includes innovative FPGA-based acceleration firmware encapsulated in a small form factor pod attached to the cable
  - Leverages high-speed Slave Serial mode programming interface
  - Recommended for prototyping use only
- Easy to use
  - Fully integrated and optimized for use with Xilinx® iMPACT software
  - Intuitive multiple cable management from a single application
  - Supported on the following operating systems:
    - Microsoft Windows XP Professional
    - Microsoft Windows Vista
    - Red Hat Enterprise Linux
    - SUSE Linux Enterprise
  - Automatically senses and adapts to target I/O voltage
  - Interfaces to devices operating at 5V (TTL), 3.3V (LVCMOS), 2.5V, 1.8V and 1.5V
  - Intuitive flyleads-to-cable interface labeling
- Reliable
  - Backwards compatibility with Platform Cable USB, including Pb-Free (RoHS-compliant)
  - USB Integrators Forum (USB-IF) certified
  - CE and FCC compliant
  - Leverages industry standards, including JTAG Boundary-Scan IEEE 1149.1, SPI and USB 2.0
- Programs and configures all Xilinx devices
  - XC18V00 ISP PROMs
  - Platform Flash XCF00S/XCF00P/XL PROMs
  - All Virtex®, Spartan® and XC4000 FPGA families
  - XC9500 / XC9500XL / XC9500XV and CoolRunner™ XPLA3 / CoolRunner-II CPLDs

  Note: Xilinx iMPACT software is required for programming and configuration
- Third-party PROM device programming support
  - Directly programs selected Serial Peripheral Interface (SPI) flash memory devices
  - Indirectly programs selected SPI or parallel flash memory devices via FPGA JTAG port
- Highly optimized for use with Xilinx design tools
  - ISE® Foundation™ Software
  - Embedded Development Kit
  - ChipScope™ Pro Analyzer
  - System Generator for DSP

Platform Cable USB II Description

Much more than just a simple USB cable, Platform Cable USB II (Figure 1) provides integrated firmware (hardware and software) to deliver high-performance, reliable and easy-to-perform configuration of Xilinx devices.

Platform Cable USB II attaches to user hardware for the purpose of configuring Xilinx FPGAs, programming Xilinx PROMs and CPLDs, and directly programming third-party SPI flash devices. In addition, the cable provides a means of indirectly programming Platform Flash XL, third-party SPI flash memory devices, and third-party parallel NOR flash memory devices via the FPGA JTAG port. Furthermore, Platform Cable USB II is a cost effective tool for debugging embedded software and firmware when used with applications such as Xilinx's Embedded Development Kit and ChipScope Pro Analyzer.

Platform Cable USB II is an upgrade to and replaces Platform Cable USB. Similar to its popular predecessor, Platform Cable USB II is intended for prototyping environments only. Platform Cable USB II is backwards compatible with Platform Cable USB and is supported by all Xilinx design tools that support Platform Cable USB.

Platform Cable USB II attaches to the USB port on a desktop or laptop PC using an off-the-shelf Hi-Speed USB A–B cable. The cable derives all operating power from the hub port controller — no external power supply is required.

Note: Sustained data transfer rates in a Hi-Speed USB environment vary according to the number of USB devices sharing the hub bandwidth. Native signaling rate (480 MHz) is not directly correlated to application throughput.

Device configuration and programming operations using Platform Cable USB II are supported by Xilinx iMPACT download software using Boundary-Scan (IEEE 1149.1 / IEEE 1532), Slave Serial mode, or serial peripheral interface (SPI).

Note: iMPACT is bundled with Foundation ISE software and WebPACK™ ISE software.

In addition, Platform Cable USB II is optimized for use with Xilinx Embedded Development Kit, ChipScope Pro Analyzer and System Generator for DSP. When used with these software tools, the cable provides a connection to embedded target systems for hardware configuration, software download, and real-time debug and verification. Target clock speeds are selectable from 750 kHz to 24 MHz.

Platform Cable USB II attaches to target systems using a 14-conductor ribbon cable designed for high-bandwidth data transfers. An optional adapter for attaching a flying lead set is included for backward compatibility with target systems not using a ribbon cable connector.

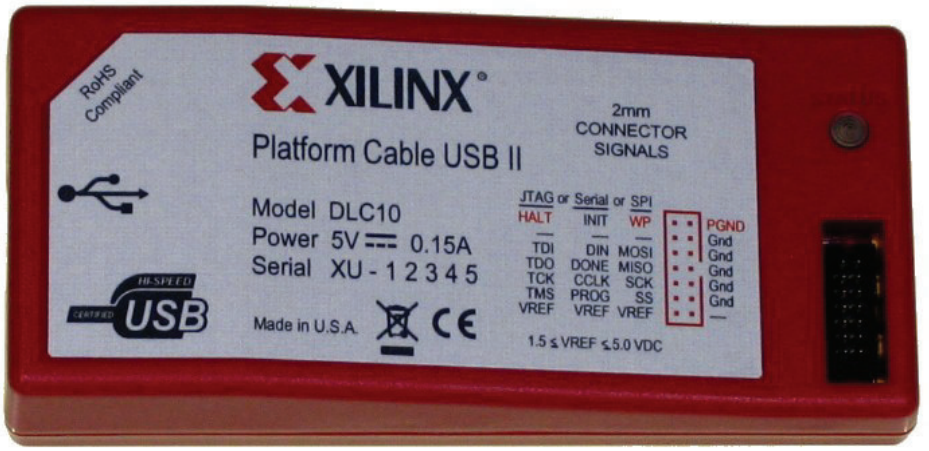

Figure 1: **Xilinx Platform Cable USB II**

Physical Description

The Platform Cable USB II electronics are housed in a recyclable, fire-retardant plastic case (Figure 2). An internal EMI shield attenuates internally generated emissions and protects against susceptibility to radiated emissions.

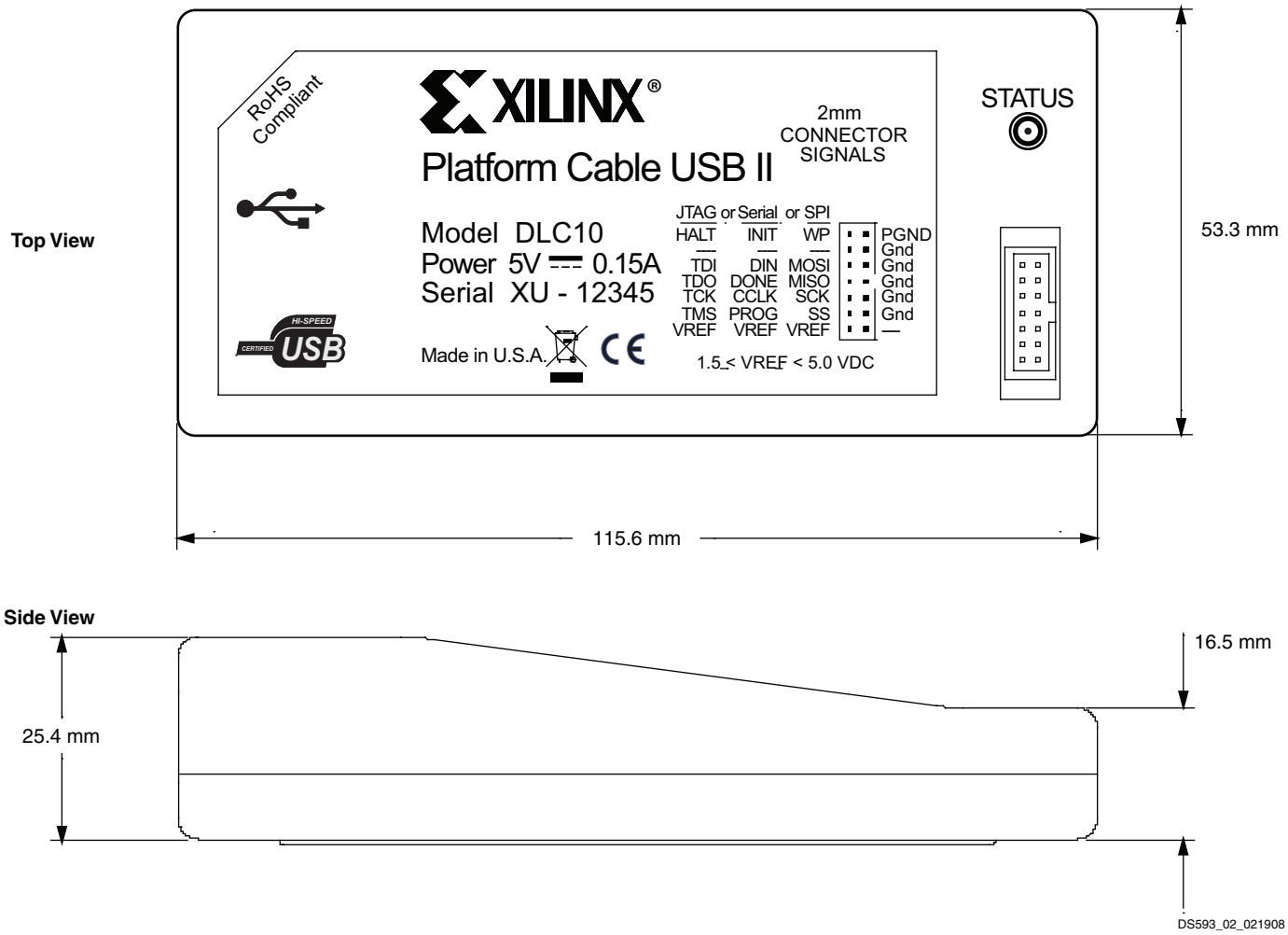

Figure 2: **Plastic Case Physical Description**

Operation

This section describes how to connect and use Platform Cable USB II.

Minimum Host System Requirements

The host computer must contain a USB Host Controller with one or more USB ports. The controller can reside on the PC motherboard, or can be added using an expansion or PCMCIA card.

Platform Cable USB II is designed to take full advantage of the bandwidth of USB 2.0 ports, but it is also backward-compatible with USB 1.1 ports. Refer to "USB Hub Types and Cable Performance," page 26 for additional information on connection environments and bandwidth.

Table 1 lists Platform Cable USB II compatibility with the Xilinx design tools.

Table 1: **Platform Cable USB II Software Compatibility**

Software	Version
ISE Foundation / ISE WebPACK	6.3i SP3 and later
ChipScope Pro Analyzer	6.3i SP3 and later
Embedded Development Kit	7.1i and later
System Generator for DSP	8.1i and later

Notes:

1. An installer must be run to enable Platform Cable USB II for use with Xilinx design tools prior to 10.1. Refer to "Device Driver Installation," page 4 for additional details.

The minimum system requirements for these applications are located on the Xilinx website at:

http://www.xilinx.com/products/design_resources/design_tool/index.htm

Note: To receive the current enhancements and bug fixes, Xilinx recommends using the newest version of a tool and applying the latest service pack.

Operating Power

Platform Cable USB II is a bus-powered device (drawing less than 150 mA from the host USB port under all operating conditions), automatically adapting to the capabilities of the host USB port to achieve the highest possible performance.

Platform Cable USB II enumerates on any USB port type: USB ports on root hubs, external bus-powered hubs, external self-powered hubs and legacy USB 1.1 hubs (see "USB Hub Types and Cable Performance," page 26). However, performance is not optimal when attached to USB 1.1 hubs (refer to "Hot Plug and Play," page 5 for an explanation of USB enumeration).

Device Driver Installation

For a complete guide to installation of the Platform Cable USB II refer to UG344, *USB Cable Installation Guide*.

A proprietary device driver is required to use Platform Cable USB II. This driver is automatically installed when a supported Xilinx design tool is installed.

Note: Automatic driver installation is available beginning with version 10.1 of Xilinx design tools. For earlier versions, a driver installer must be run prior to using the cable. Refer to the *USB Cable Installation Guide* for instructions on downloading and running the installer.

Firmware Updates

The Platform Cable USB II firmware resides in an USB microcontroller and a FPGA/PROM. The microcontroller is RAM-based and firmware is downloaded each time the cable is connected and detected by the host operating system. Additional firmware can also be downloaded to the microcontroller once a design tool establishes a connection with the cable. The USB protocol guarantees that the firmware is successfully downloaded.

Upgraded firmware for the USB microcontroller is periodically distributed in Xilinx design tool releases or, on rare occasions, in a Xilinx Answer Record. In most cases, an upgrade requires replacing one or more of the design tool's application files and depending on operating system, one or more cable driver files.

Platform Cable USB II contains a Xilinx Spartan-3A FPGA with an in-system programmable Xilinx XCF02S PROM. Each time a design tool establishes a connection with the cable, the firmware version stored in the PROM is examined. The PROM is automatically reprogrammed over the cable if the firmware version is out of date. If an update is required, the design tool displays the following warning message:

```
Warning: USB Cable firmware must be updated.
This operation may take up to 40 seconds.
Please do not stop the process or disconnect
the cable prior to completion. The cable
STATUS LED will be RED for the duration of the
update process.
```

Similarly, upgraded firmware for the FPGA/PROM is periodically distributed in Xilinx design tool releases or, on rare occasions, in a Xilinx Answer Record. In most cases, an upgrade requires replacing a single design tool application file. The PROM is reprogrammed with the new firmware the next time the tool connects to the cable. PROM reprogramming takes approximately 40 seconds over a USB 2.0 port and 60 seconds over a USB 1.1 port. Reprogramming times vary depending on the Xilinx design tool version, the type of USB port and the performance of the host system.

During a PROM update, the cable's status LED illuminates red (Figure 8, page 9), and a progress bar indicates

communication activity. PROM updates should never be interrupted. When an update is complete, the status LED returns to either amber or green, and the cable is ready for normal operation.

Hot Plug and Play

Platform Cable USB II can be attached and removed from the host computer without the need to power-down or reboot. There is a momentary delay after connecting the cable to an available port before the status LED illuminates — this process is called enumeration.

Connecting to the Cable in iMPACT

This section describes some of the ways to connect to Platform Cable USB II using the Xilinx iMPACT graphical user interface (GUI). For cable communication using other Xilinx design tools or methods, please refer to the appropriate software user guide.

Select a Flow

From the iMPACT GUI, select a flow on the "Modes" tab (Figure 3). Double-click on the desired flow.

Note: For a description of the different flows, please refer to **iMPACT → Help**.

Establishing a Connection

Once a flow is selected, there are a number of ways to establish a connection with the cable. Two common options are described here:

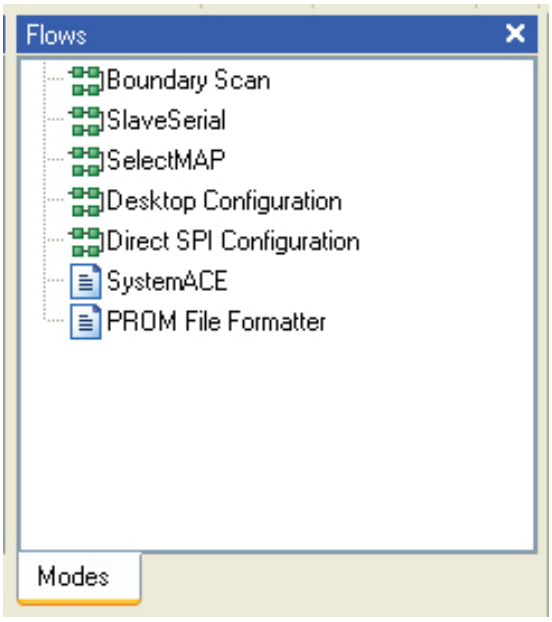

Figure 3: **iMPACT (9.2i) Modes Tab**

Option 1: Cable Auto Connect

To auto connect the cable, select **Output → Cable Auto Connect** (Figure 4).

Note: During the auto-connect sequence, iMPACT selects Parallel Cable IV (PC4) as the active cable if both PC4 and Platform Cable USB II are connected to the same host system. If two or more USB cables are connected to the same host, the active cable is the first USB cable physically connected to the host system. See "Multiple USB Cable Management," page 6, for information on controlling more than one USB cable from a single application.

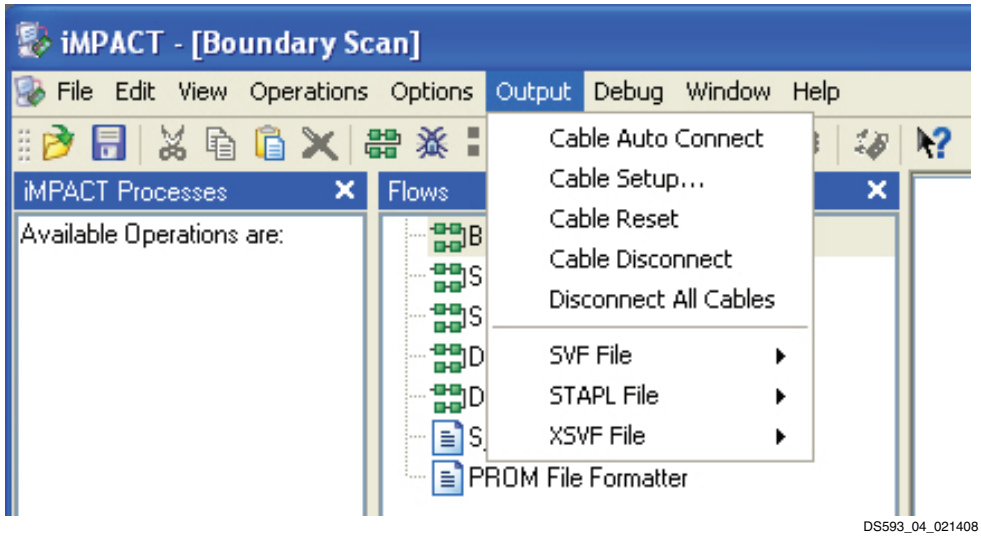

Figure 4: **iMPACT (9.2i) Output Pull-Down Menu**

Option 2: Manual Cable Connect

To manually connect the cable, select **Output** → **Cable Setup**. Select the **Xilinx USB Cable** radio button in the Cable Communication Setup dialog box (Figure 5).

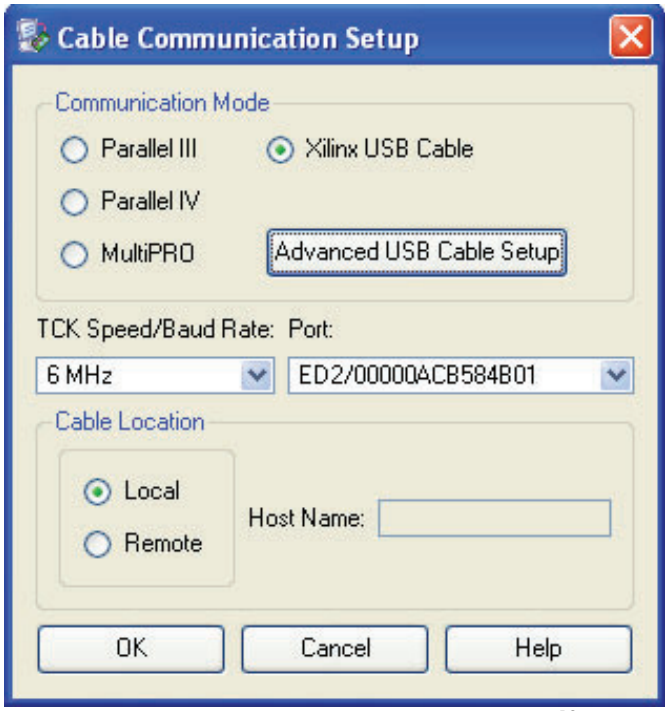

Figure 5: **iMPACT (10.1) Cable Communication Setup**

It is necessary to perform a cable disconnect when switching from Boundary Scan or Direct SPI Configuration mode to Slave-Serial mode, or vice versa. iMPACT can be disconnected from the cable using **Output** → **Cable Disconnect** (Figure 4, page 5). After the mode switch is complete, reestablish the cable connection using the **Output** → **Cable Setup** dialog. It is not necessary, however, to perform a cable disconnect when switching between Boundary-Scan and Direct SPI Configuration modes.

If an iMPACT session is active when an **Output** → **Cable Disconnect** or **Output** → **Disconnect All Cables** operation is performed, or if the cable is physically disconnected from the host system, the Cable Status Bar (Figure 7, page 8) at the bottom, right-hand edge of the GUI immediately indicates "No Cable Connection."

Xilinx design tools employ system semaphores to manage access to Xilinx cables, allowing multiple applications to simultaneously access (connect to) a single cable (but only one application can perform cable operations at a given time). For example, assume two instances of iMPACT (instance A and instance B) are connected to a single cable. If A begins a programming operation, and B then attempts a programming operation, B is temporarily blocked from accessing the cable. B receives a message indicating that the cable is *locked,* and the operation must be attempted again later.

Multiple USB Cable Management

Platform Cable USB II contains a 64-bit electronic serial number used by applications to uniquely identify and access a specific USB cable when multiple USB cables (up to 127) are connected to the same host. iMPACT provides a dialog box (Figure 6, page 6) allowing users to select a specific cable from a list of attached cables. When one of the cables in the list is highlighted, the status LED on the appropriate cable blinks, allowing users to make a logical-to-physical association. When the desired cable is *connected* and the dialog box closed, the status LED no longer blinks.

The Cable Setup Information dialog box (Figure 6) appears when the **Advanced USB Cable Setup** button is pressed in the Cable Communication Setup dialog box (Figure 5).

Note: The multiple USB cable management feature is only available in iMPACT version 10.1 and later. Refer to the iMPACT section of Xilinx ISE software manuals for additional details on this feature.

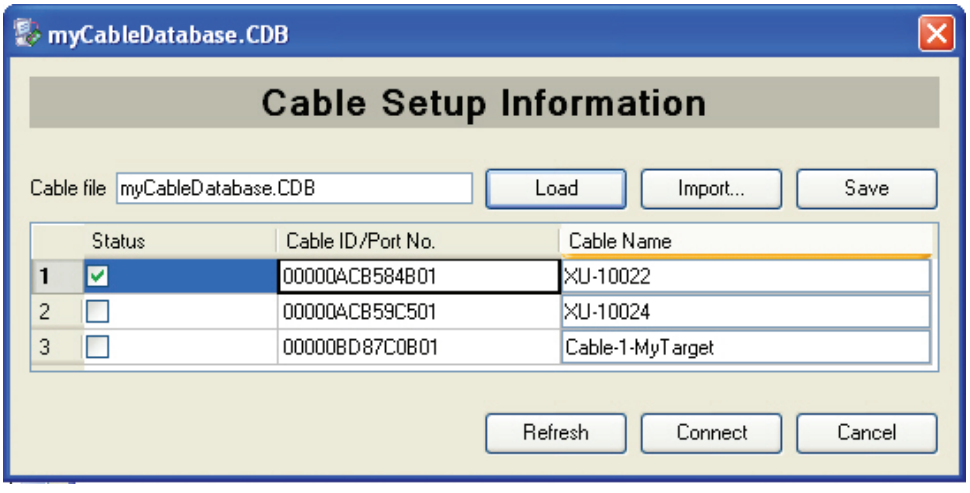

Figure 6: **iMPACT (10.1) Cable Setup Information**

Configuration Clock Speed

The Platform Cable USB II configuration clock (TCK_CCLK_SCK) frequency is selectable. Table 2 shows the complete set of available TCK_CCLK_SCK speed selections.

Table 2: **Configuration Speed Selections**

TCK_CCLK_SCK Frequency	Units
24	MHz
12	MHz
6 (Default)	MHz
3	MHz
1.5	MHz
750	kHz

iMPACT 7.1i (and later) provides a feature wherein the BSDL file of each device in a target JTAG chain is scanned to determine the maximum Boundary-Scan clock (JTAG TCK) frequency. iMPACT 7.1i (and later) automatically restricts the available TCK_CCLK_SCK selections to frequencies less than or equal to the slowest device in the chain. By default, iMPACT 7.1i (or later) selects either 6 MHz or the highest common frequency when any device in the JTAG chain is not capable of 6 MHz operation. Table 3 shows the maximum supported JTAG TCK frequency for a variety of Xilinx devices. See the device data sheet or BSDL file for maximum JTAG TCK specifications.

Note: Certain Xilinx design tools and iMPACT versions earlier than 7.1i do not restrict the TCK_CCLK_SCK selections in JTAG mode. Accordingly, users should take care to select a TCK_CCLK_SCK frequency matching the JTAG TCK specifications for the slowest device in the target chain.

In Slave Serial or Direct SPI Configuration mode, the TCK_CCLK_SCK speed can be set to any one of the available selections. By default, the TCK_CCLK_SCK speed is set to 6 MHz. Users should take care to select a TCK_CCLK_SCK frequency matching the Slave Serial clock (CCLK or SPI clock) specification of the target device.

Table 3: **Maximum JTAG Clock Frequencies**

Device Family	Maximum JTAG Clock Frequency (MHz)
XC9500/XL/XV	10
XPLA3	10
CoolRunner-II	33
XC18V00	10
XCF00S/XCF00P	15
Virtex	33
Virtex-II	33
Virtex-II Pro	33
Virtex-4	33
Virtex-5	33
Spartan	5
Spartan-II	33
Spartan-3	33
Spartan-3A	33
Spartan-3AN (50, 200 and 400 densities)	33
Spartan-3AN (700 and 1400 densities)	20
Spartan-3E	30

iMPACT Cable Status Bar

A status bar on the bottom edge of the iMPACT GUI (Figure 7) provides information about cable operating conditions. For example, if the host port is USB 2.0, Platform Cable USB II connects at Hi-Speed and the status bar shows usb-hs. If the host port is USB 1.1, Platform Cable USB II connects at full-speed, and the status bar shows usb-fs. Finally, the status bar displays the active cable and TCK_CCLK_SCK frequency.

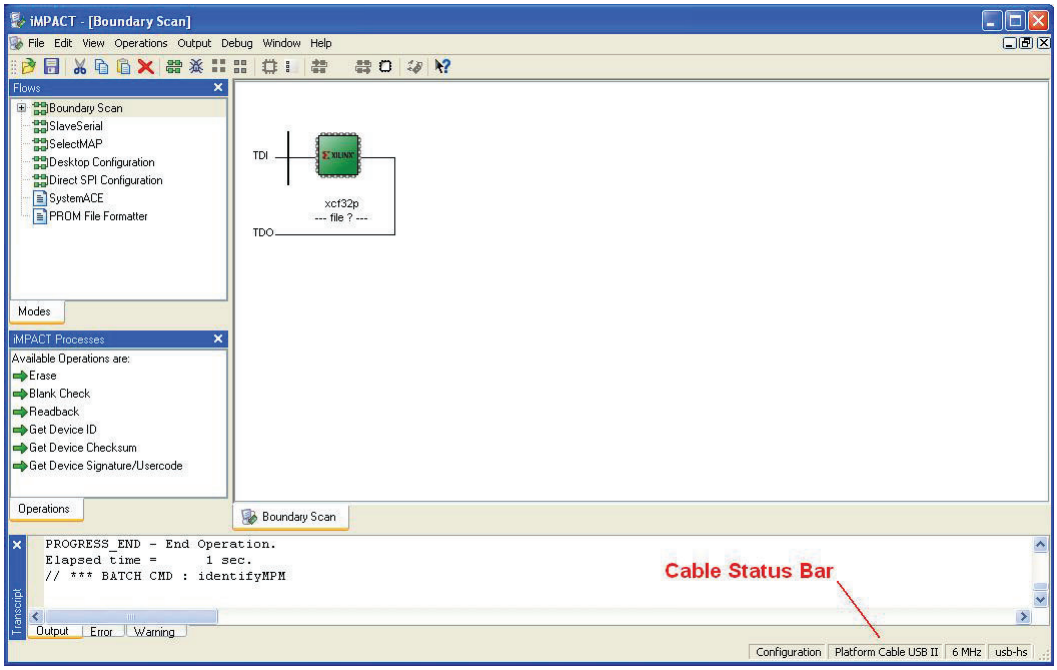

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Figure 7: **iMPACT (10.1) Cable Status Bar**

Status Indicator

Platform Cable USB II uses a tri-color status LED to indicate the presence of target voltage and to indicate that a cable firmware update is in progress (Figure 8).

When the cable is connected (using a ribbon cable, or flying leads) to a mating connector on the target system, the status LED is illuminated as a function of the voltage present on pin 2 (V_{REF}). Users must design their system hardware with pin 2 attached to a voltage plane suppling the JTAG, SPI, or Slave Serial pins on the target device(s). Some devices have separate power pins for this purpose (V_{AUX}), while others have a common supply for both V_{CCIO} and the JTAG pins (TCK, TMS, TDI, and TDO). Refer to the target device data sheet for details on JTAG, Slave Serial or SPI pins.

The status LED is amber when any one or more of the following conditions exist:

- The cable is not connected to a target system
- The target system is not powered
- The voltage on the V_{REF} pin is ≤ +1.3V.

The status LED is green when all of the following conditions exist:

- The cable is connected to a target system
- The target system is powered
- The voltage on the V_{REF} pin is ≥ +1.5V.

Note: There is 200 mV of hysteresis in the V_{REF} detection circuit. If V_{REF} drops below 1.3V, the status LED turns amber and does not turn green until V_{REF} is raised above 1.5V.

The status LED is red whenever a cable firmware update is in progress.

The status LED is off whenever Platform Cable USB II enters a suspend state (see "System Suspend," page 9), is disconnected from a USB port, or is connected to an un-powered USB port.

Table 4 summarizes the various status LED states.

Table 4: **Interpreting the Status LED**

LED Color	LED State	Condition
OFF	Continuous	Host power OFF
AMBER	Continuous	Target V_{REF} ≤ 1.3V
AMBER	Blinking	Target V_{REF} ≤ 1.3V AND multiple cable identification active
GREEN	Continuous	Target VREF ≥ 1.5V
GREEN	Blinking	Target VREF ≥ 1.5V AND multiple cable identification active
RED	Continuous	FPGA firmware update in progress

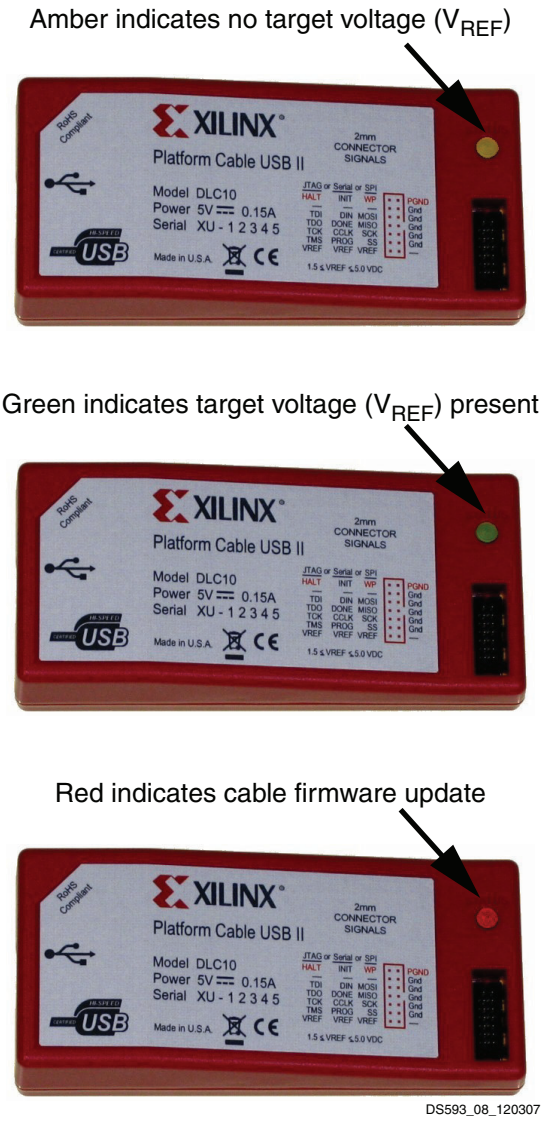


Figure 8: **Cable Status LED**

System Suspend

The cable's status LED is extinguished when the host system enters a suspend (power-saving) state. A system can suspend for a number of reasons. For example:

- The user puts the host system into standby or hibernate.
- The suspend function key on a laptop computer is pressed.
- The display panel of a laptop is closed.
- The host system is configured to suspend (standby or hibernate) after a specified amount of inactivity.

The current drawn by the cable while suspended depends on the type of suspend state: standby or hibernate. While the host system is in standby, the cable draws approximately 350 µA from the USB port. When the host is hibernating, all power is removed from the USB ports so the cable draws no current while in this state.

The target interface output drivers are not powered while the host is suspended. These signals float to any DC bias level provided by the target hardware during suspend.

If an iMPACT (10.1 or later) operation is in progress when suspend is attempted, iMPACT displays a message (Figure 9) indicating that suspend is blocked until the operation is complete or manually aborted.

Note: This feature is not supported in earlier versions of iMPACT, while iMPACT is operating in batch mode, or by other Xilinx design tools. In these cases, it is recommended that suspend be disabled in the host system when performing long, continuous operations.

The cable is automatically disconnected when the host system is suspended. A reconnect is necessary when the host re-awakens from the suspend state (see "Connecting to the Cable in iMPACT," page 5).

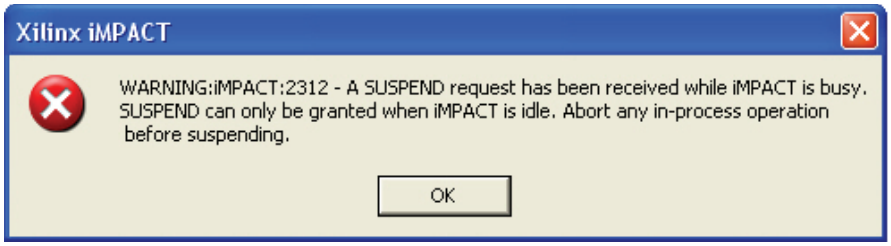


Figure 9: **Suspend Warning When iMPACT (10.1 or later) is Busy**

Platform Cable USB II Connections

This section discusses physical connections from Platform Cable USB II to the host PC and the target system.

High Performance Ribbon Cable

A 6-inch ribbon cable is supplied and recommended for connection to target systems (Figure 10). The cable incorporates multiple signal-ground pairs and facilitates error-free connections. The Xilinx product number for the 6-inch ribbon cable is HW-RIBBON14.

To take advantage of the ribbon cable, a mating connector must be incorporated into the target system. This connector is normally installed only during prototype checkout. When the production hardware is functional and the ISP devices can be configured from alternate sources, the connector can be eliminated to reduce cost. Maintaining the footprint for this connector is recommended if space permits.

The connector is a 2-mm shrouded keyed header. See Table 5, page 14 for vendor part numbers and pin assignments.

Notes:

1. Ribbon Cable: 14-pin conductor, 1.0 mm center, round-conductor flat cable, 28 AWG (7 x 36) stranded conductors, gray PVC with pin 1 edge marked.
2. 2-mm ribbon female polarized connector, IDC connection to ribbon. Contacts are beryllium copper plated 30 micro-inches gold plating over 50-micro-inches nickel. The connectors mate to 0.5-mm square posts on 2-mm centers.

Figure 10: **High Performance Ribbon Cable**

Flying Wire Adapter

An adapter with wires (Figure 11) is provided for attachment to legacy target systems that do not incorporate a shrouded 2-mm connector. The adapter makes it possible to use flying wires for connections to distributed terminals on a target system.

The adapter is a small circuit board with two connectors (Figure 12). The connector on the bottom side of the adapter mates with the 14-pin Platform Cable USB II male 2-mm connector. A 7-pin right-angle header on the top side of the adapter mates with the standard Xilinx flying wire set.

Note: This method of connection is not recommended because it can result in poor signal integrity. Additionally, damage can result if the leads are unintentionally connected to high voltages.

The Xilinx product number for the flying wire set is HW-USB-FLYLEADS-G.

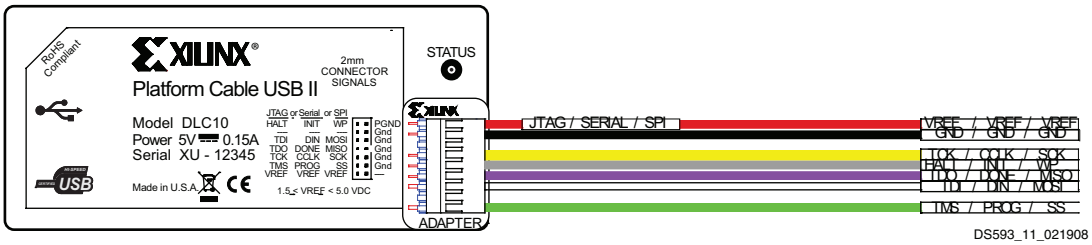


Figure 11: **Flying Wire Adaptor (Top) with Wires**

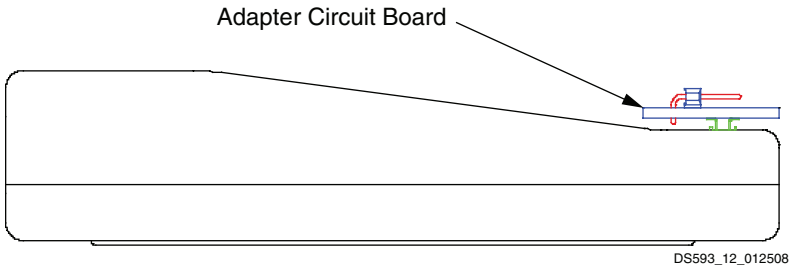


Figure 12: **Flying Wire Adapter (Side) without Wires**

Physical Connection to the Host

Each Platform Cable USB II includes a detachable, Hi-Speed-USB-certified, 1.8-meter A–B cable (Figure 13). Under no circumstances should user-supplied cables exceed 5 meters. Sub-channel cables (intended for low-speed 1.5 Mb/s signaling) should not be used with Platform Cable USB II.

A standard series B receptacle (Figure 13) is incorporated into the case for mating with the detachable Hi-Speed A–B cable. A separate chassis ground is attached to the A–B cable drain wire and returns ESD current to the host system ground.

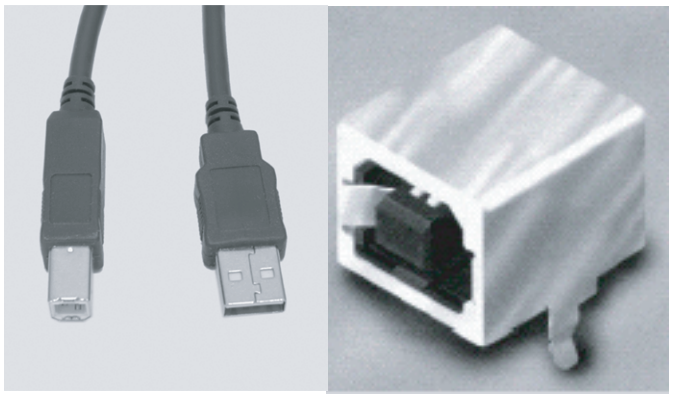


Figure 13: **Standard A-B Host Interface Cable and Series B Receptacle**

Target Interface Connectors

Mating connectors for attachment of the high-performance ribbon cable to a target system are available in both through-hole and surface mount configurations (Figure 14). Shrouded and keyed versions should always be used to guarantee proper orientation when inserting the cable. The connector requires only 105 mm^2 of board space.

The target system voltage applied to pin 2 of this connector is used as a power source for the output buffers that drive the output pins (see "Target Interface Reference Voltage and Signals," page 19).

Table 5, page 14 provides some third-party sources for mating connectors that are compatible with the Platform Cable USB II ribbon cable.

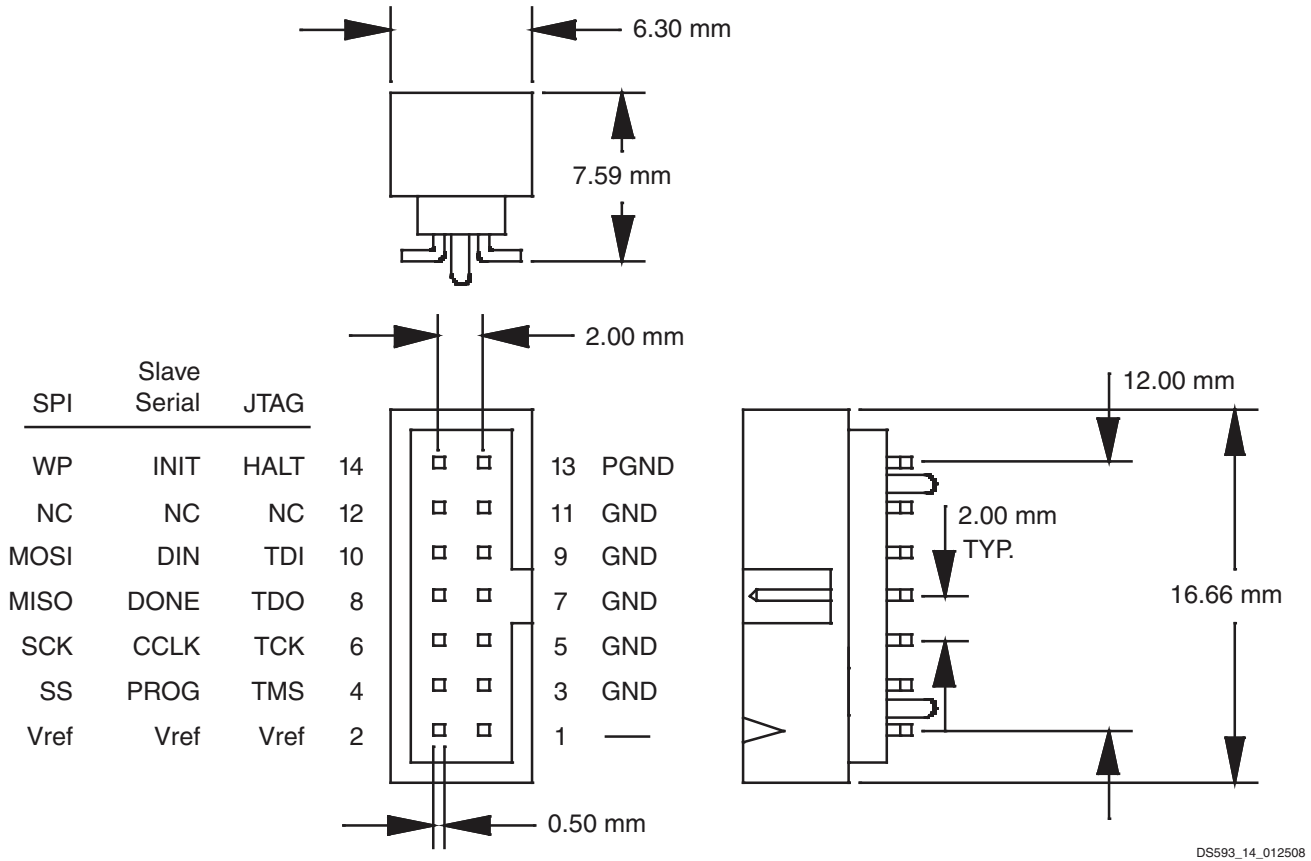


Figure 14: **Target Interface Connector Dimensions and Signal Assignments**

Table 5: **Mating Connectors for 2 mm pitch, 14-Conductor Ribbon Cable**

Manufacturer(1)	SMT, Vertical	Through-Hole, Vertical	Through-Hole, Right Angle	Web Site
Molex	87832-1420	87831-1420	87833-1420	www.molex.com
FCI	98424-G52-14	98414-G06-14	98464-G61-14	www.fciconnect.com
Comm Con Connectors	2475-14G2	2422-14G2	2401R-G2-14	www.commcon.com

Notes:

1. Some manufacturer pin assignments do not conform to Xilinx pin assignments. Please refer to the manufacturer's data sheet for more information.
2. Additional ribbon cables can be purchased separately from the Xilinx Online Store.

Target System Connections

This section provides examples of the various configuration topologies supported by Platform Cable USB II. Each example incorporates the 2-mm connector (see "Target Interface Connectors," page 13) as the cable interface. Diagrams in this section provide a functional relationship between the cable interface and the target devices.

Note: Signal integrity is not considered in these examples. Refer to "Signal Integrity," page 25 for details on buffering and termination.

JTAG and Slave Serial

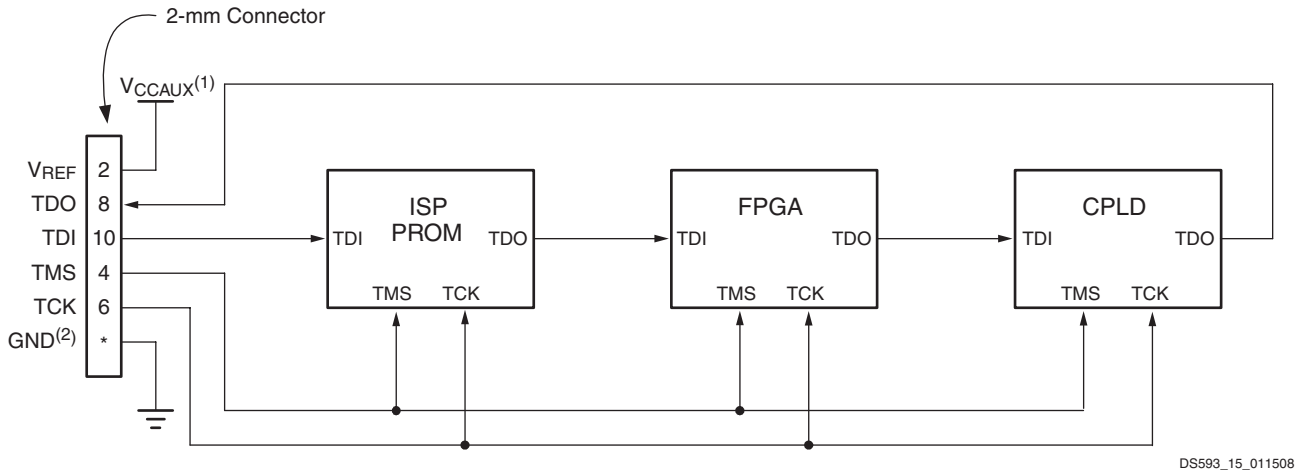
Multiple devices can be cascaded when using either a JTAG or slave-serial topology in target systems. Figure 15 and Figure 17, page 17 show typical routing for JTAG and Slave Serial topologies, respectively.

Platform Cable USB II provides a multi-use signal on its target interface connector called pseudo ground (PGND). The PGND pin is connected to an open-drain driver (see "Pseudo Ground Signal," page 21); hence, it is either Low or high-Z. The behavior of PGND is determined by the host application connected to the cable. In iMPACT, PGND is active-Low during JTAG, Slave Serial and SPI operations (for example, programming, configuration, read back, etc.) and high-Z when the cable is idle.

Figure 16, page 16 shows a typical use of PGND as a control signal to manage a target system's JTAG chain. PGND drives the select (S) term on a set of multiplexers that switch between the primary configuration source and the cable. When PGND is active-Low, the cable drives the JTAG chain. When PGND is high-Z, the primary configuration source drives the JTAG chain. This capability allows Platform Cable USB II to remain attached to the target system while remaining isolated from the primary configuration source. A similar scheme can be used with Slave Serial topologies.

PGND control is available only in iMPACT versions 10.1 and later. PGND remains high-Z in earlier versions of iMPACT and in Xilinx design tools where the PGND signal is not supported.

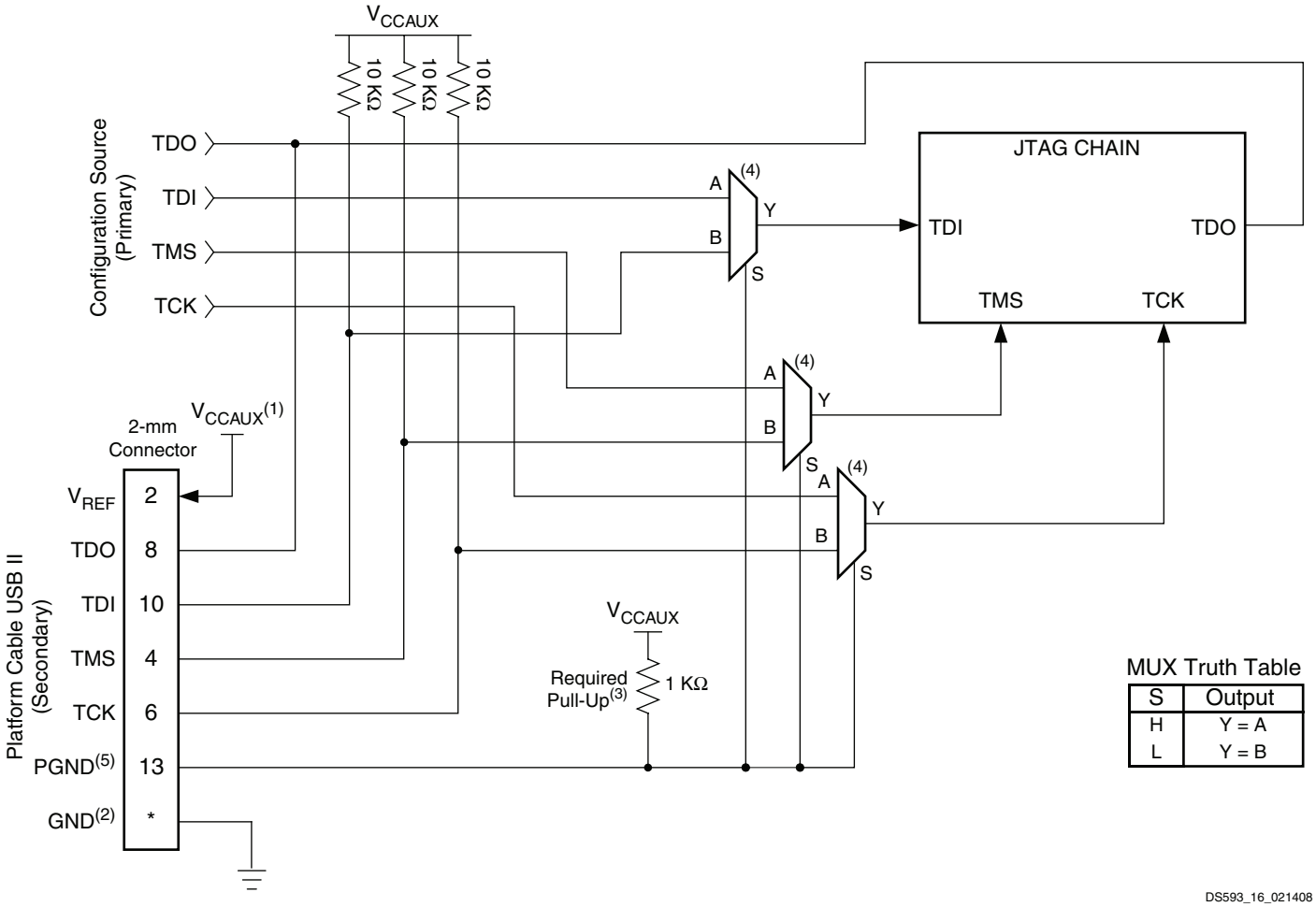
The DONE pin on FPGAs can be programmed to be an open-drain or active driver. For cascaded Slave Serial topologies, an external pull-up resistor should be used, and all devices should be programmed for open-drain operation.



Notes:

1. Example implies that V_{CCO}, V_{CCJ}, and V_{CCAUX} for various devices are set to the same voltage. Refer to the device data sheet for the appropriate JTAG voltage-supply levels.
2. Attach the following 2-mm connector pins to digital ground: 3, 5, 7, 9, and 11.

Figure 15: **Example of JTAG Chain Topology**



Notes:

1. Example implies that V_{CCO}, V_{CCJ}, and/or V_{CCAUX} for various devices in the JTAG chain are set to the same voltage.
2. Attach the following 2-mm connector pins to digital ground: 3, 5, 7, 9, and 11.
3. The cable uses an open-drain driver to control the pseudo ground (PGND) signal — an external pull-up resistor is required.
4. Assumes that the multiplexor supply voltages pins are connected to V_{CCAUX}.
5. Pin 13 is grounded on legacy Xilinx USB cables (models DLC9, DLC9G and DLC9LP), and Parallel Cable IV (model DLC7). These cables need to be manually detached from the 2-mm connector to allow the primary configuration source to have access to the JTAG chain.

Figure 16: **Example Using PGND in a JTAG Chain**

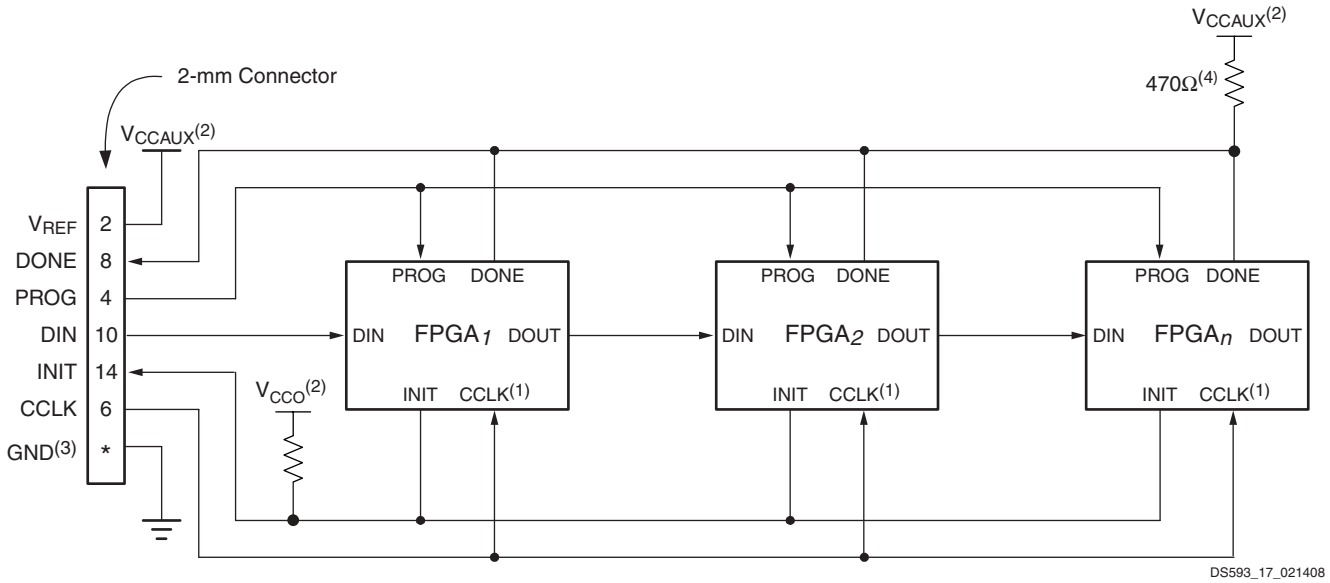
Direct SPI

Platform Cable USB II can connect directly to a single SPI flash device. Figure 18, page 18 shows an example SPI flash connection. XAPP951, *Configuring Xilinx FPGAs with SPI Serial Flash* provides additional details of the cable connections necessary to program a FPGA bitstream into a SPI flash device.

Note: See *Configuring Xilinx FPGAs with SPI Serial Flash* for a list of supported SPI devices.

By connecting PGND to PROG_B of the FPGA (Figure 17), the FPGA can be commanded to set its SPI signals to high-Z while the cable programs a SPI flash device. PGND is pulled Low when the cable is driving its SPI signals in SPI mode and set to high-Z when the cable is not driving its SPI signals. PGND eliminates the need for a hardware jumper to ground on the PROG_B signal and the need for additional control logic. PGND is controlled by an open-drain driver.

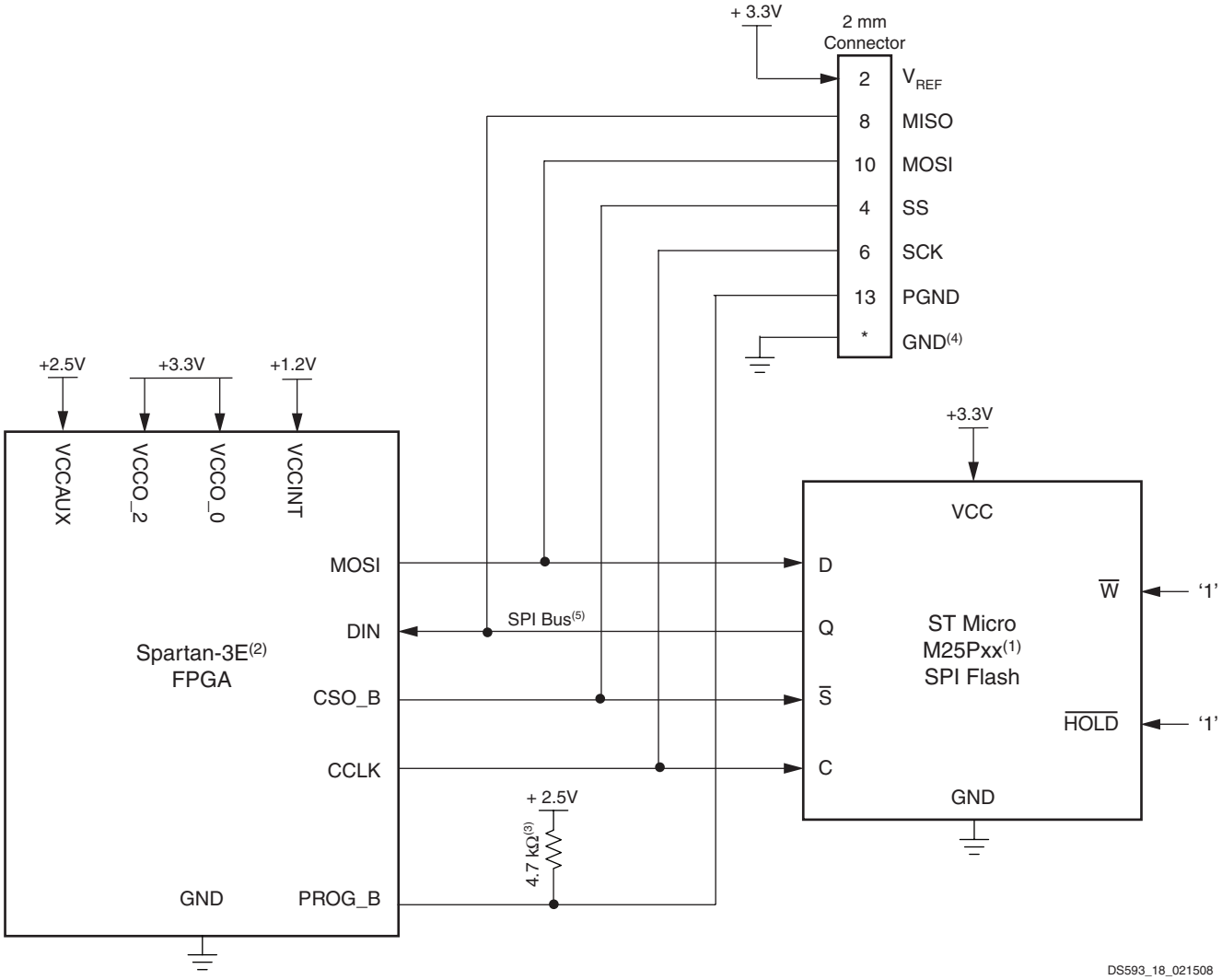
Note: PGND control for SPI programming is available in iMPACT versions 9.2i and later.



Notes:

1. Set Mode pins (M2-M0) on each FPGA to Slave-Serial mode when using the USB cable, so the CCLK is treated as an input.
2. Example uses generalized nomenclature for the voltages-supply levels. Refer to the device data sheet for the appropriate serial configuration voltage-supply levels.
3. Attach the following 2-mm connector pins to digital ground: 3, 5, 7, 9, and 11.
4. A pull-up is required when two or more devices are cascaded and programmed for open-drain operation.

Figure 17: **Example of Cascaded Slave-Serial Topology**



Notes:

1. The pin names for a ST Microsystems M25Pxx serial flash device are shown in this example. SPI flash devices from other vendors can have different pin names and requirements. Refer to the SPI flash data sheet for the equivalent pins and device requirements.
2. The example shows the interconnect and device requirements for a Xilinx Spartan-3E FPGA. Other SPI-capable FPGAs can have different pin names and requirements. Please refer to the FPGA data sheet for equivalent pins and device requirements.
3. The cable uses an open-drain driver to control the pseudo ground (PGND) signal — an external pull-up resistor is required.
4. Attach the following 2-mm connector pins to digital ground: 3, 5, 7, 9 and 11.
5. Typically, an FPGA and other slave SPI devices (not shown) are connected to the SPI bus. The other devices on the SPI bus must be disabled when the cable is connected to the 2-mm connector to avoid signal contention. When a Xilinx FPGA is connected to the SPI bus, the cable holds the FPGA PROG_B pin Low to insure the FPGA SPI pins are 3-stated.

Figure 18: **Example of Direct SPI Topology**

Indirect SPI

When used with Xilinx design tools, Platform Cable USB II can be used to indirectly program some third-party SPI serial flash PROMs via the target FPGA's JTAG port. For a complete description on using Platform Cable USB II for indirect programming of third-party SPI serial flash PROMs and for a complete list of supported SPI serial flash memories, refer to XAPP974, *Indirect Programming of SPI Serial Flash PROMs with Spartan-3A FPGAs*.

Indirect BPI

When used with Xilinx design tools, Platform Cable USB II can be used to indirectly program Platform Flash XL, or some third-party NOR flash memories (BPI PROMs) via the target FPGA's JTAG port. For a description of the indirect Platform Flash programming solution, see UG438, *Platform Flash XL User Guide*.

For a complete description on using Platform Cable USB II for indirect programming of third-BPI PROMs and for a complete list of supported BPI PROMs, refer to XAPP973, *Indirect Programming of BPI PROMs with Virtex-5 FPGAs*.

Target Interface Reference Voltage and Signals

Target Reference Voltage Sensing (VREF)

Platform Cable USB II incorporates an over-voltage clamp on the V_{REF} pin of the 2-mm ribbon cable connector. The clamped voltage (V_{REF_CLAMP}) supplies high-slew-rate buffers that drive each of the output signals (see "Output Driver Structure"). V_{REF} must be a regulated voltage.

Note: Do not insert a current-limiting resistor in the target system between the V_{REF} supply and pin 2 on the 2-mm connector.

When Platform Cable USB II is idle, a nominal amount of current is drawn from the target system V_{REF}. Figure 19 shows the V_{REF} current as a function of V_{REF} voltage.

No damage to Platform Cable USB II occurs if the A–B cable is unplugged from the host while the ribbon cable or flying leads are attached to a powered target system. Similarly, no damage to target systems occurs if Platform Cable USB II is powered and attached to the target system while the target system power is off.

Bidirectional Signal Pins

Platform Cable USB II provides five bidirectional signal pins: TDI_DIN_MOSI, TDO_DONE_MISO, TCK_CCLK_SCK, TMS_PROG_SS and HALT_INT_WP. Each pin incorporates the same I/O structure. The state of each pin (reading or writing) is determined by the current mode of the cable (JTAG, SPI or Slave Serial).

Output Driver Structure

Each output signal is routed through a NC7SZ126 ultra high-speed CMOS buffer (Figure 20, page 20). Series-damping resistors (30.1Ω) reduce reflections. Weak pull-up resistors (20 kΩ) terminating at V_{REF_CLAMP} maintain a defined logic level when the buffers are set to high-Z. Schottky diodes provide the output buffers with undershoot protection.

The FPGA sets the output buffers to high-Z when V_{REF} drops below 1.30 V. In addition, an over-voltage Zener on V_{REF} clamps V_{REF_CLAMP} to approximately 3.9V.

Figure 21, page 20 shows the relationship between the output drive voltage and V_{REF}.

Note: The output drivers are enabled only during cable operations; otherwise, they are set to high-Z between operations.

Xilinx design tools actively drive the outputs to logic 1 before setting the respective buffer to high-Z, avoiding the possibility of a slow rise-time transition caused by a charge path through the pull-up resistor into parasitic capacitance on the target system.

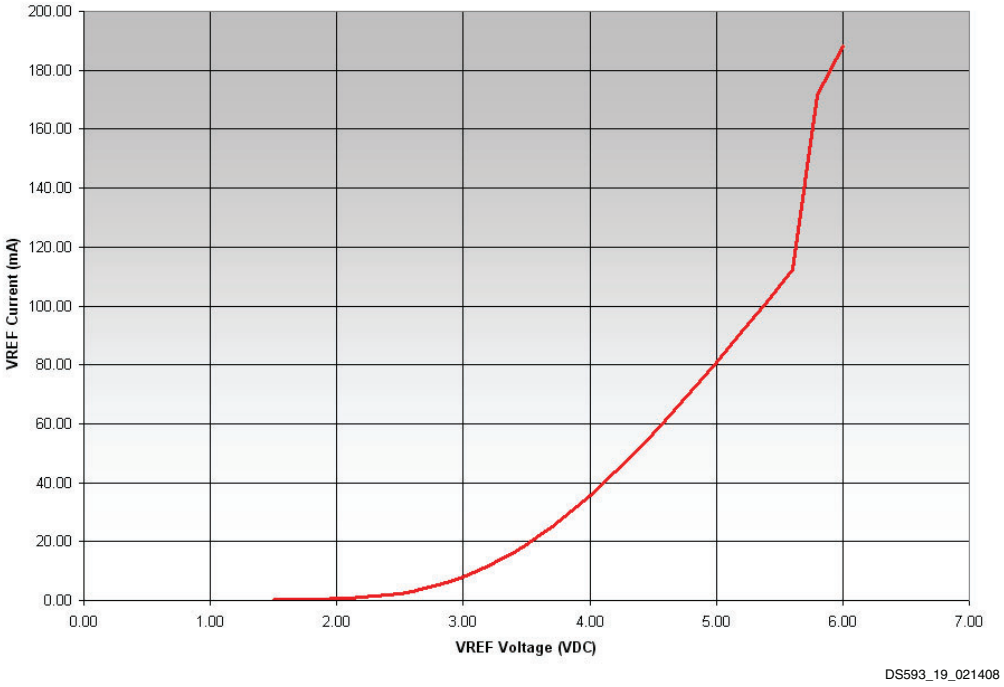


Figure 19: **V_{REF} Current vs. V_{REF} Voltage**

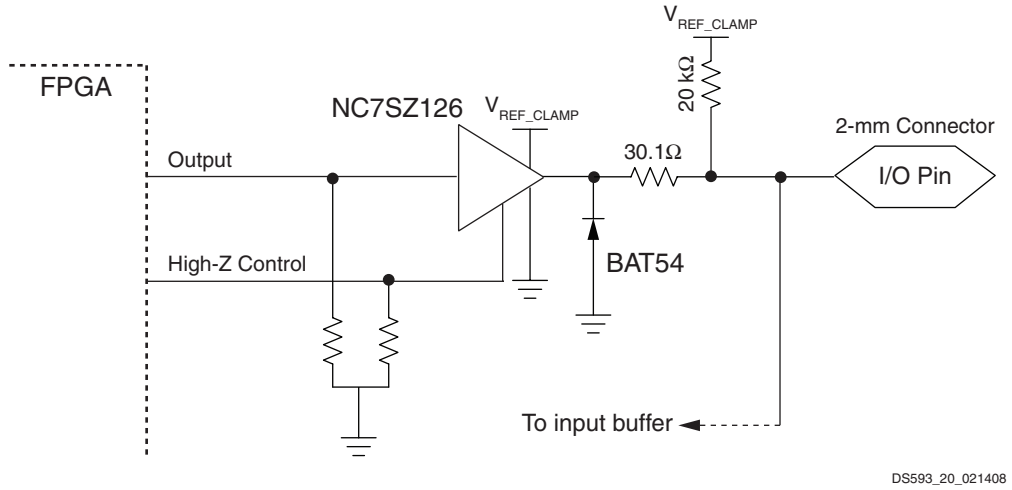


Figure 20: **Target Interface Driver Topology**

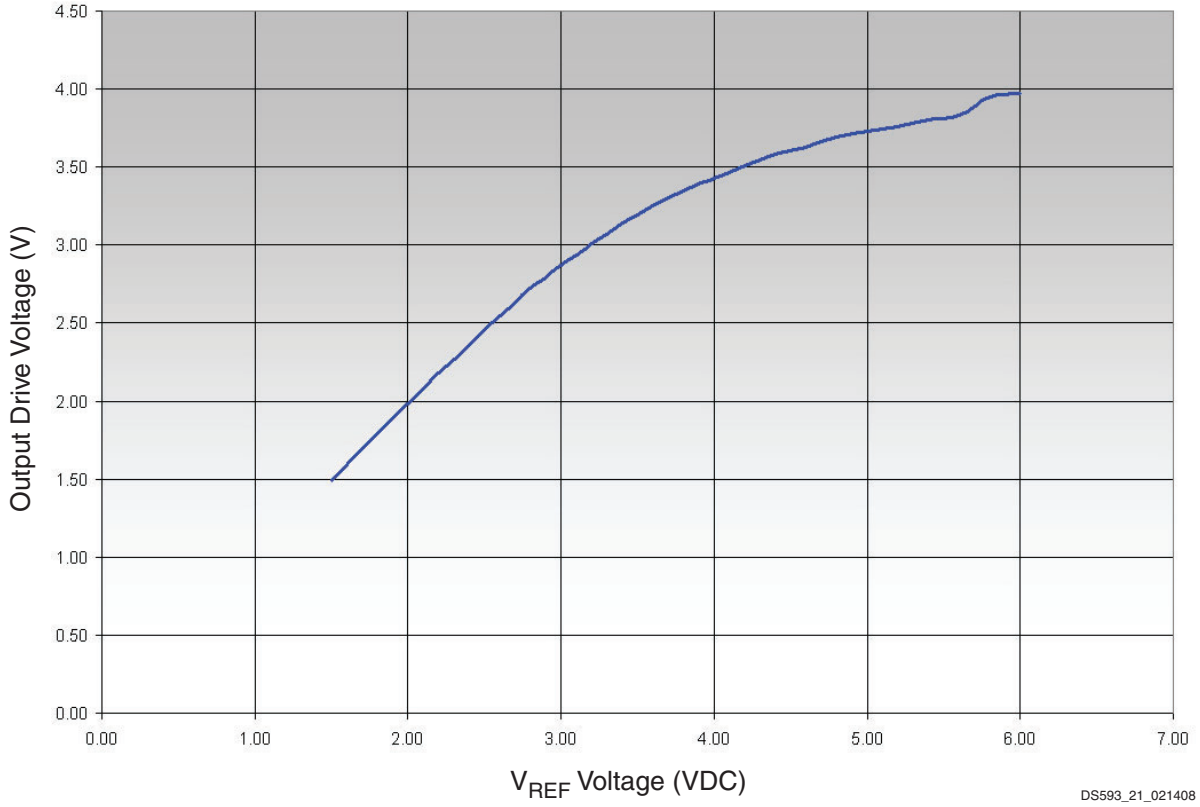


Figure 21: **Output Drive Voltage vs. V_{REF}**

Input Receive Structure

Each input signal is routed through a NC7WZ07 ultra high-speed CMOS, open-drain receive buffer. Series-termination resistors (499Ω) provide current limit protection for positive and negative excursions. Schottky diodes provide the input buffers with undershoot protection. The receive buffers are biased by an internal 1.8V power supply. See Table 9, page 29 for V_{IL} and V_{IH} specifications. The receive buffers can tolerate voltages higher than the bias voltage without damage, compensating for target system drivers in multi-device chains where the last device in the chain might be referenced to a voltage other than V_{REF} (for example, the TDO output at the end of a JTAG chain).

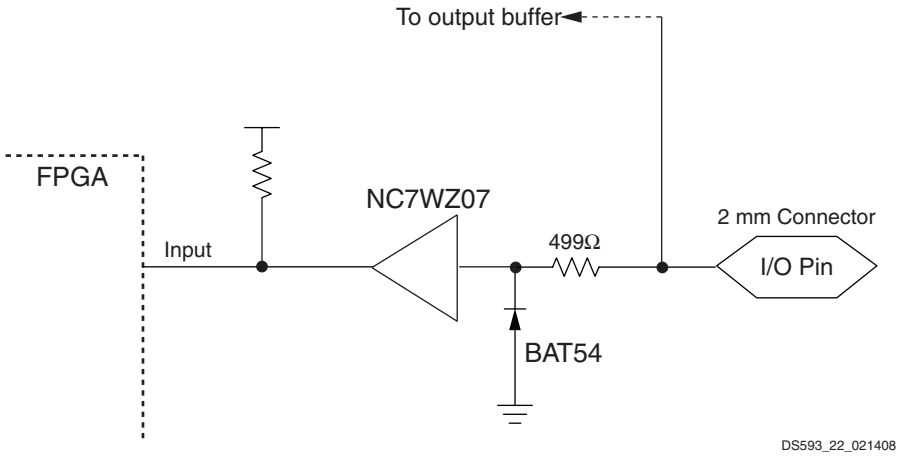


Figure 22: **Target Interface Receiver Topology**

Pseudo Ground Signal

The pseudo ground (PGND) pin on target interface connector is routed to a ultra-high-speed buffer with an open-drain output (Figure 23). A pull-up resistor is required on target systems that utilize this signal. The buffer can tolerate a pull-up voltage as high as 6.0V.

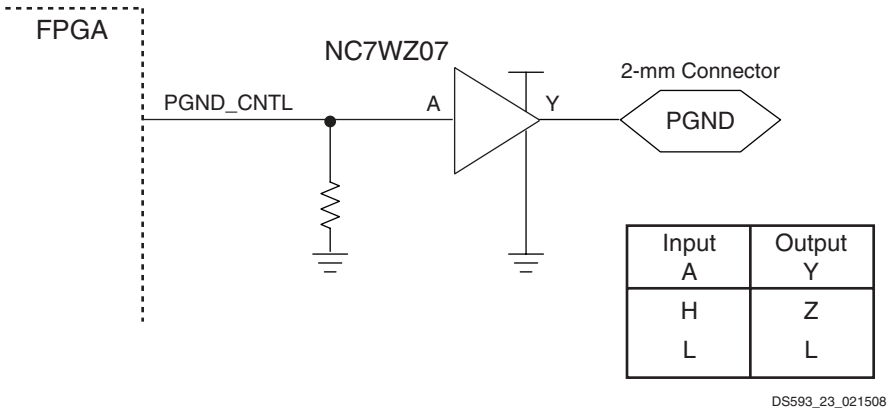


Figure 23: **PGND Signal**

HALT_INIT_WP Signal in iMPACT

Platform Cable USB II provides a second multi-use signal on its target interface connector called HALT_INIT_WP (this signal is referred to as HALT when the cable is in JTAG mode). The HALT_INIT_WP pin is connected to a three-state CMOS driver (see "Bidirectional Signal Pins," page 19).

The behavior of HALT_INIT_WP is determined by the host application connected to the cable. iMPACT provides the option of enabling the HALT pin during JTAG operations (Figure 24). This option is accessed by clicking on the Xilinx FPGA in the iMPACT GUI and selecting **Edit** → **Set Programming Properties...** to open the Device Programming Properties dialog box. Check "Assert Cable INIT during programming" to enable the HALT signal.

When enabled in iMPACT, HALT is active-Low while the cable is performing JTAG operations on any Xilinx FPGA and high-Z when the cable is idle. HALT is active-High while JTAG operations are being performed on other devices. The HALT signal remains high-Z when not enabled (iMPACT default) or when the cable is in Slave Serial or SPI modes.

Note: HALT signal control is available in iMPACT 9.2i and later. HALT remains high-Z in earlier versions of iMPACT and in Xilinx design tools where the HALT signal is not supported.

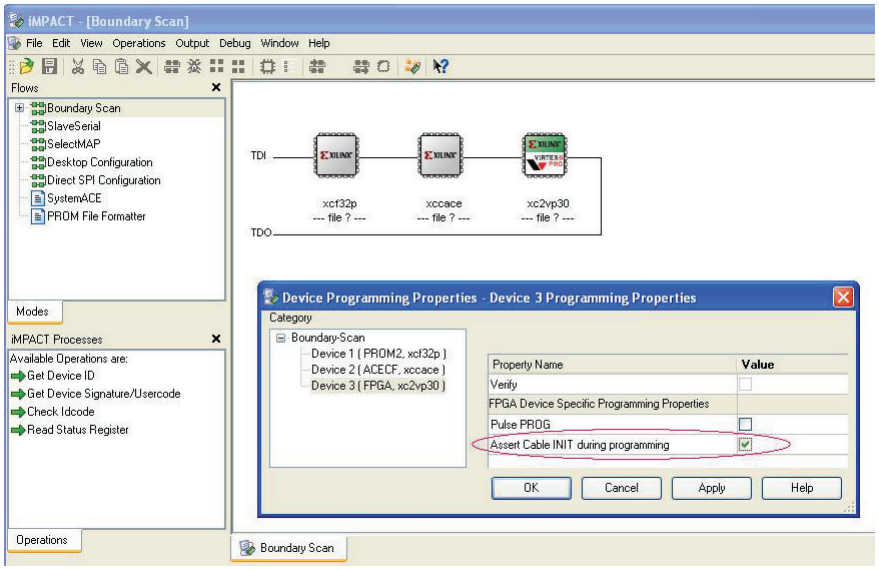


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Figure 24: **Enabling the HALT Signal in iMPACT (9.2i)**

Timing Specifications

For JTAG, SPI, and Slave Serial configuration modes, the TDI_DIN_MOSI and TMS_PROG_SS outputs change on falling edges of TCK_CCLK_SCK (Figure 25). Target devices sample TDI_DIN_MOSI and TMS_PROG_SS on rising edges of TCK_CCLK_SCK. The minimum setup time $T_{TSU(MIN)}$ for target device sampling of TDI_DIN_MOSI or TMS_PROG_SS is:

$$T_{TSU(MIN)} = T_{CLK/2} - T_{CPD(MAX)}$$
$$= 20.8\ ns - 16.0\ ns$$
$$= 4.8\ ns$$

where:

$T_{CLK/2}$ = TCK_CCLK_SCK low time at 24 MHz,

$T_{CPD(MAX)}$ = Maximum TDI_DIN_MOSI or TMS_PROG_SS propagation delay relative to TCK_CCLK_SCK inherent in the output stage of the cable.

Reducing the TCK_CCLK_SCK frequency increases the data setup time at the target.

Note: Timing specifications apply when V_{REF} = 3.3V. Operations at 24 MHz might not be possible when using a V_{REF} below 3.3V due to the increased propagation delay through the output buffer stage of the cable.

TDO/MISO Timing Considerations

Designers of target systems must take care to observe specific timing requirements for TDO (JTAG chains) or MISO (dedicated SPI in-system programming) when incorporating the 2-mm IDC connector. In particular, if an open-drain or open-collector buffer is inserted between TDO (MISO) and the cable, the value of the pull-up resistor at the output of such buffers must be relatively small (for example, less than 330Ω) to avoid delays associated with parasitic capacitance.

Figure 26, page 24 and Figure 27, page 24 show the timing relationship between TCK and TDO. The signal TDO_SMPL is an internal logic signal not available at the target interface, but is shown to highlight the location of the TDO sampling point. In Figure 26, the negative TCK transition at G1 causes the last device in the target system JTAG chain to drive TDO, which propagates to the cable at G2. The time from G1 to G2 is the sum of the propagation delays in the driver stage of the target device and the receiver stage of the cable (37 ns in this example).

In Figure 27, the cursors show the total setup time (42 ns) before TDO is sampled by the cable. Figure 28, page 25 is an analog representation of the logical condition shown in Figure 26 and Figure 27 captured at the target system.

Note: The propagation delay from TCK to TDO is 26 ns. Because Figure 26 shows a propagation delay of 37 ns, the difference of 11 ns is attributable exclusively to input delays in the cable. At 12 MHz, there is still sufficient setup time before the cable samples prior to the next negative TCK transition.

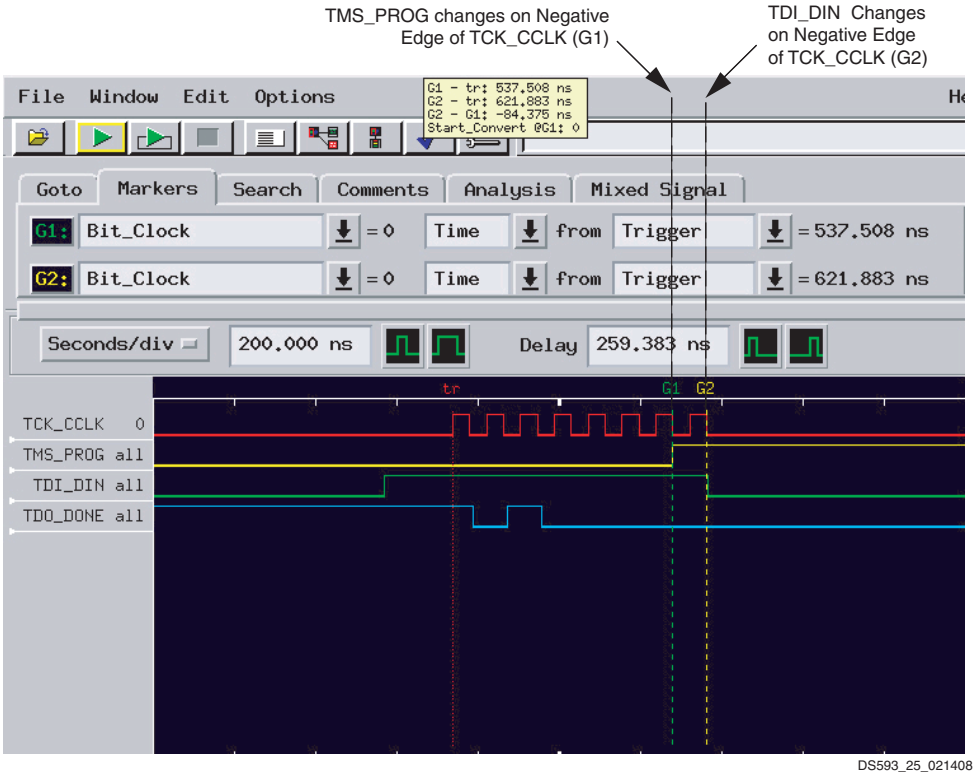

Figure 25: **TDI_DIN_MOSI and TMS_PROG_SS Timing with Respect to TCK_CCLK_SCK**

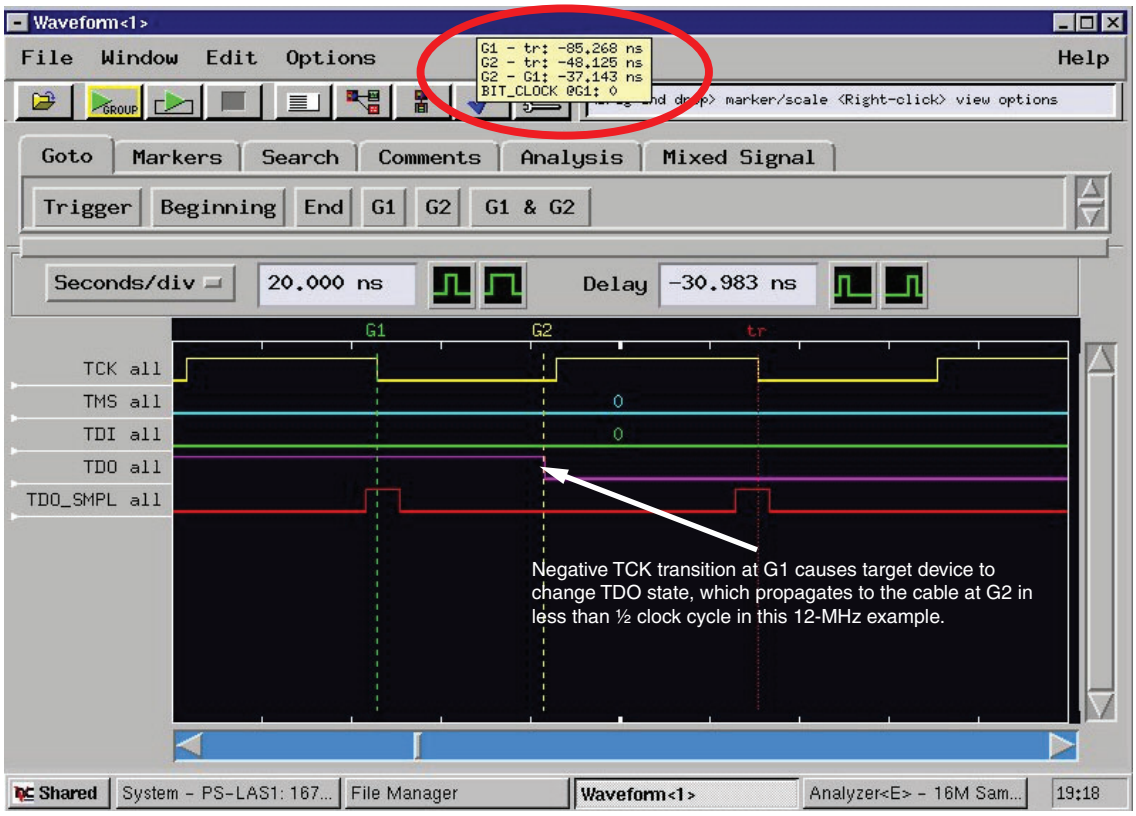

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Figure 26: **TDO Sampling Example at 12 MHz (TDO Propagation Delay)**

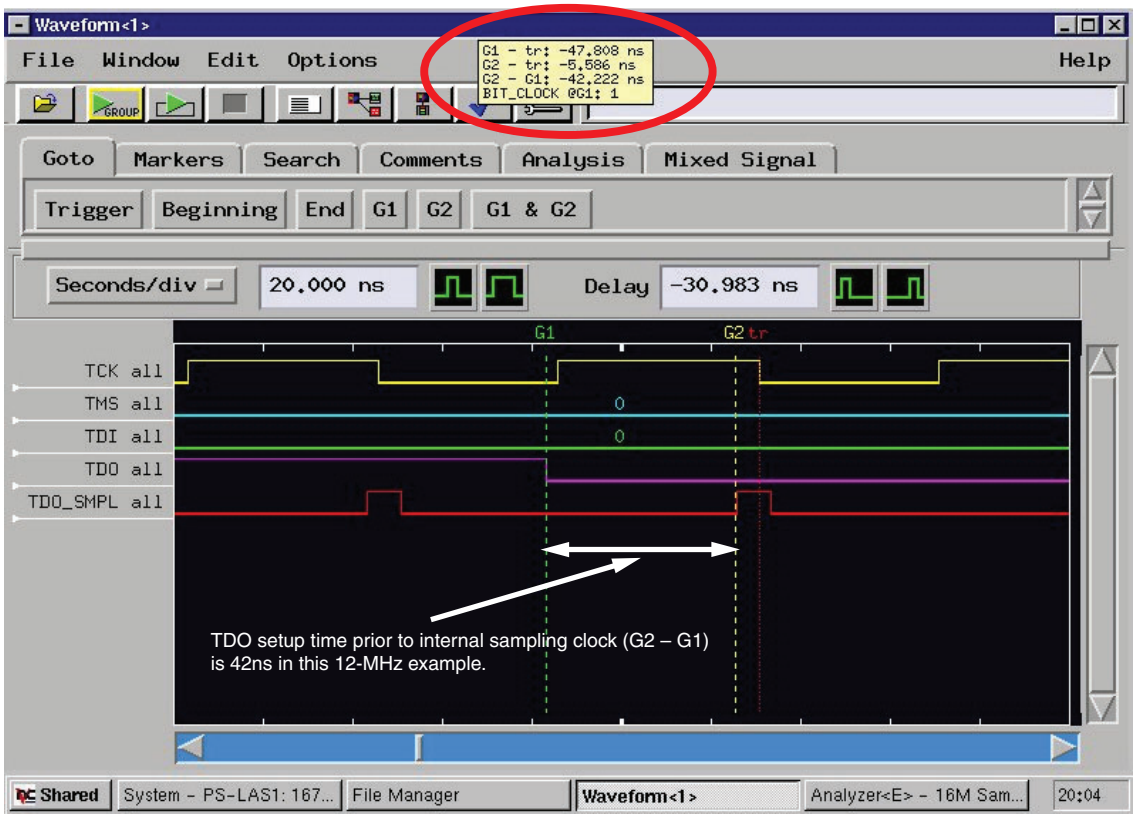

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Figure 27: **TDO Sampling Example at 12 MHz (TDO Setup Time Relative to Sampling Point)**

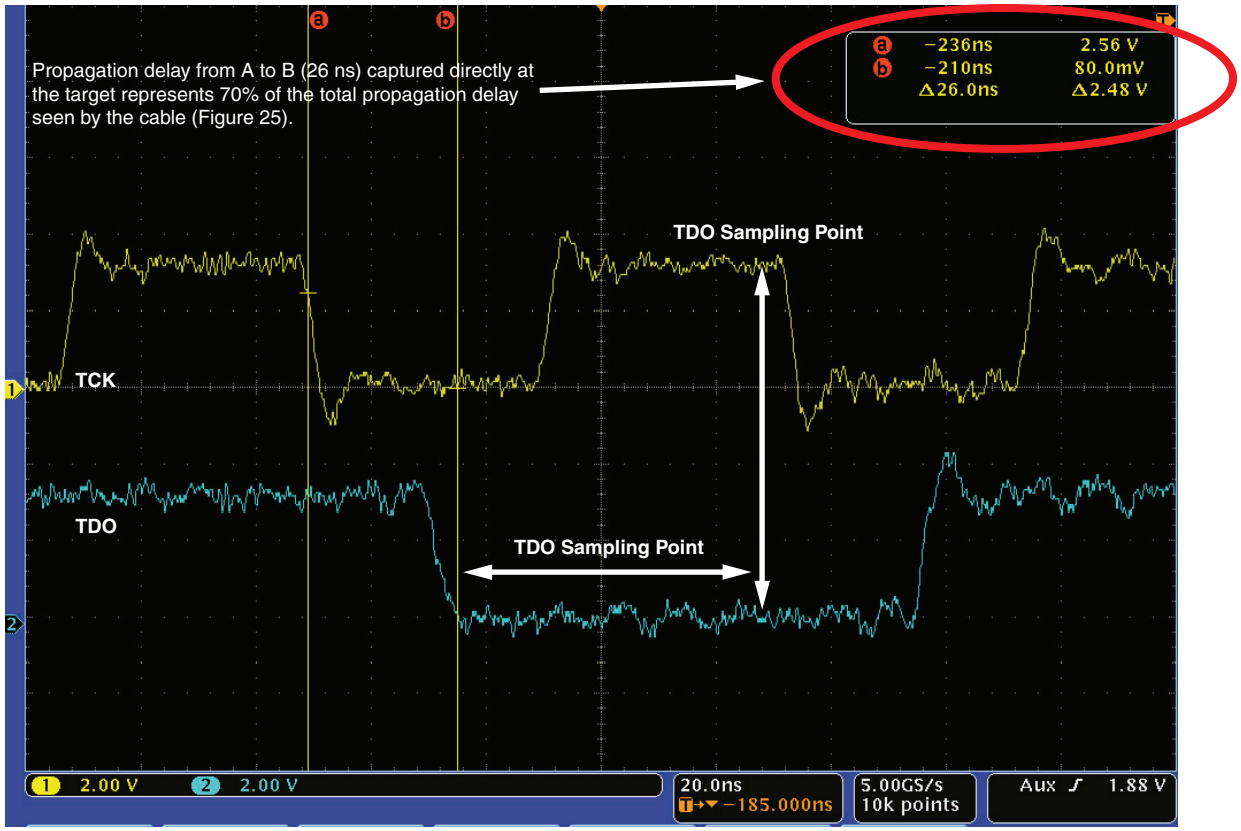


Figure 28: **TDO Sampling Example at 12 MHz (Analog Signals on Target System)**

Signal Integrity

Platform Cable USB II uses high-slew-rate buffers to drive its output pins. Each buffer has a 30.1Ω series termination resistor. Users should pay close attention to PCB layout to avoid transmission line effects. Visit the Xilinx Signal Integrity Central website, and see XAPP361, *Planning for High Speed XC9500XV Designs* for detailed signal integrity assistance.

If the target system has only one programmable device, the 2-mm connector should be located as close as possible to the target device. If there are multiple devices in a JTAG or slave-serial single chain on the target system, users should consider buffering TCK_CCLK_SCK. Differential driver/receiver pairs provide excellent signal quality when the rules identified in Figure 29 are followed. Buffering is essential if target devices are distributed over a large PCB area.

Each differential driver and/or receiver pair contributes approximately 5 ns of propagation delay. This delay is insignificant when using 12 MHz or slower clock speeds.

Each differential receiver can drive multiple target devices if there are no branches on the PCB trace and the total trace length is less than four inches. A series termination resistor should be placed adjacent to the single-ended output of the differential receiver.

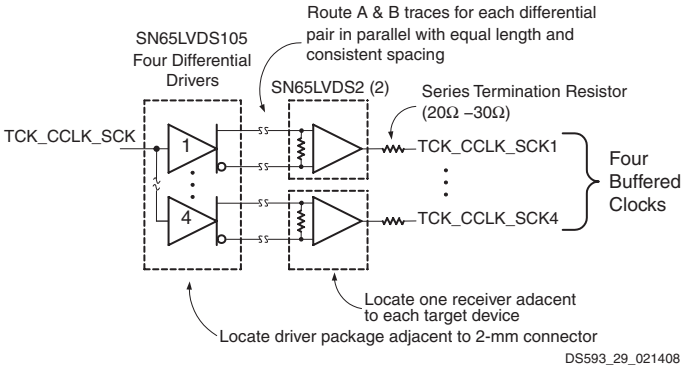


Figure 29: **Differential Clock Buffer Example**

Note: If the target chain has, for example, a JTAG or Slave Serial topology and a 24 MHz clock rate is desired, it is recommended that matching buffers be used for both TCK_CCLK_SCK and TMS_PROG_SS. Matching buffers maintains a consistent phase relationship between TCK_CCLK_SCK and TMS_PROG_SS. A buffer is not needed for TDI_DIN_MOSI, because it sees only one load.

USB Hub Types and Cable Performance

There are two important hub specifications affecting the performance of Platform Cable USB II: maximum port current and total bandwidth.

Maximum Port Current

Platform Cable USB II is a bus-powered device, drawing less than 150 mA from the host USB port under all operating conditions.

Note: Some older USB root hubs or external bus-powered hubs might restrict peripherals to 100 mA. Platform Cable USB II cannot enumerate on hubs with the 100 mA restriction.

Total Bandwidth

The maximum theoretical bandwidth is 480 Mb/s for a single USB 2.0 Hi-Speed device and 12 Mb/s for a single USB 1.1 full-speed device. However, because hub bandwidth must be shared among all connected devices, actual bandwidth is in practice lower than these theoretical values.

Platform Cable USB II performance is optimal when enumerated on a USB 2.0 Hi-Speed port. Hi-Speed USB operation is guaranteed only if the cable is attached directly to a USB 2.0 root hub (Figure 30E), or to an external, self-powered USB 2.0 hub connected directly to a USB 2.0 root hub (Figure 30D).

If Platform Cable USB II is attached to a USB 1.1 root hub (Figure 30A) or to USB 2.0 external hub connected to a USB 1.1 root hub (Figure 30B), the cable enumerates as a full-speed device and cable performance is degraded. Communication and protocol overhead limits any given USB device to approximately 30% of total bandwidth. For USB 1.1 hubs, the maximum achievable throughput is approximately 3.6 Mb/s.

Certain self-powered, USB 2.0 hubs can continue to function as USB 1.1 hubs when disconnected from their external power source (Figure 30C). When no external power source is present, these hubs draw their power from their upstream USB port. If Platform Cable USB II is connected to such a hub while operating at USB 1.1 speeds, the cable enumerates as a full-speed device. Furthermore, bus-powered hubs can only deliver a total of 500 mA to all connected devices. If individual ports on bus-powered hubs are limited to less than 150 mA, Platform Cable USB II does not enumerate and is unavailable for use by host software applications.

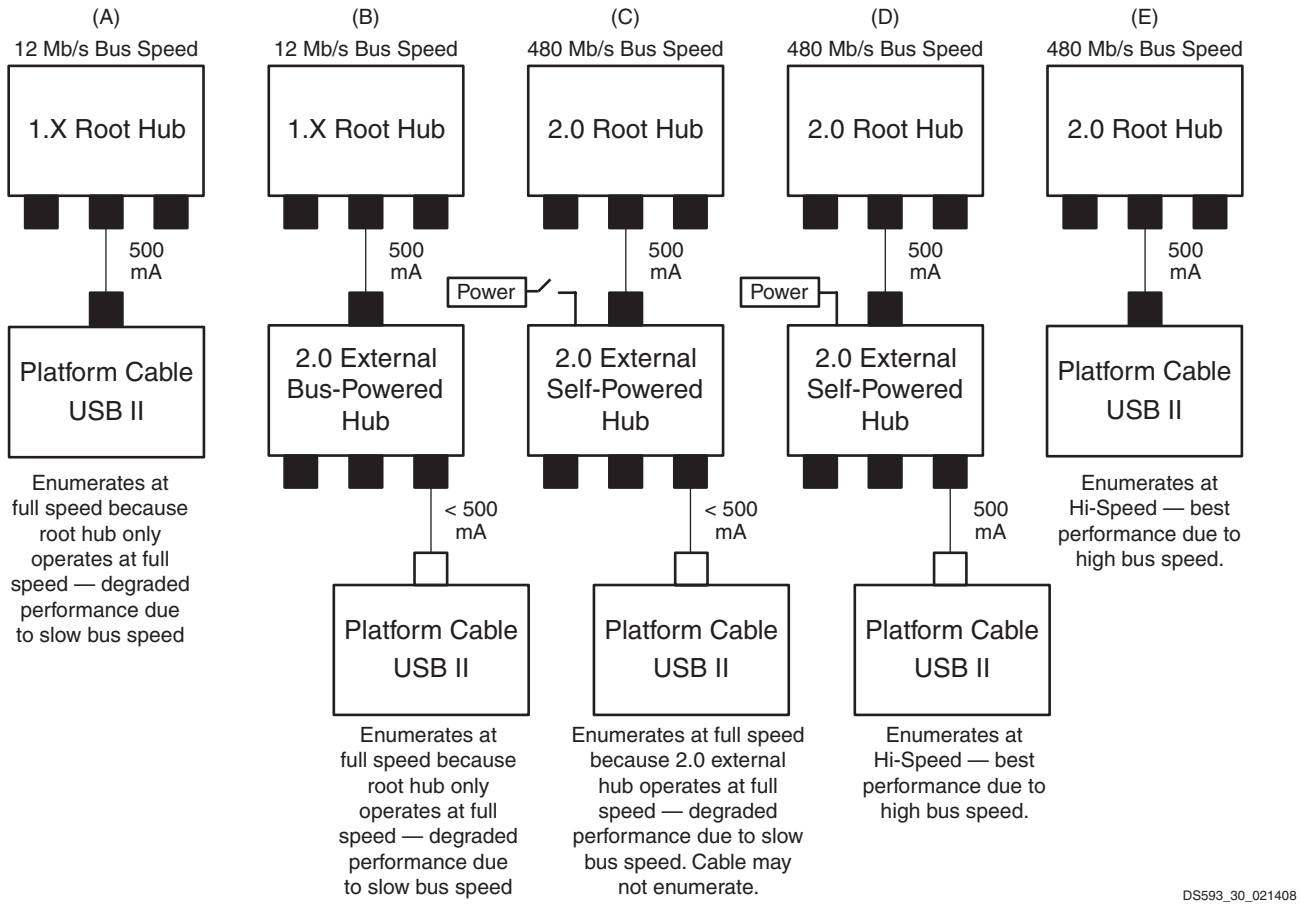


Figure 30: **Platform Cable USB II Performance with Various Hub Types**

Interface Pin Descriptions

Table 6: **JTAG/SPI/Slave Serial Port: 2-mm Connector Signals**

Pin Number	MODE			Direction(2)	Description
	JTAG Configuration	SPI Programming(1)	Slave-Serial Configuration		
2	V_{REF}	V_{REF}	V_{REF}	In	**Target Reference Voltage**(3). This pin should be connected to a voltage bus on the target system that serves the JTAG, SPI or Slave Serial interface. For example, when programming a CoolRunner-II device using JTAG, V_{REF} should be connected to the target V_{AUX} bus.
4	TMS	–	–	Out	**JTAG Test Mode Select**. This pin is the JTAG mode signal establishing appropriate TAP state transitions for target ISP devices sharing the same data stream.
6	TCK	–	–	Out	**JTAG Test Clock**. This pin is the clock signal for JTAG operations and should be connected to the TCK pin on all target ISP devices sharing the same data stream.
8	TDO	–	–	In	**JTAG Test Data Out**. This pin is the serial data stream received from the TDO pin on the last device in a JTAG chain.
10	TDI	–	–	Out	**JTAG Test Data In**. This pin outputs the serial data stream transmitted to the TDI pin on the first device in a JTAG chain.
13	PGND	–	–	Out	**JTAG Pseudo Ground.** Use of this pin is optional. PGND is pulled Low during JTAG operations; otherwise, it is high-Z. This pin is connected to an open-drain driver and requires a pull-up resistor on the target system.(4)
14	HALT	–	–	Out	**JTAG Halt.** Use of this pin is optional. Host applications can customize the behavior of this signal. See "HALT_INIT_WP Signal in iMPACT," page 22.
4	–	SS	–	Out	**SPI Select**. This pin is the active-Low SPI chip select signal and should be connected to the S(1) pin on the SPI flash device.
6	–	SCK	–	Out	**SPI Clock**. This pin is the clock signal for SPI operations and should be connected to the C(1) pin on the SPI flash PROM.
8	–	MISO	–	In	**SPI Master-Input, Slave-Output**. This pin is the target serial output data stream and should be connected to the Q(1) pin on the SPI flash device.
10	–	MOSI	–	Out	**SPI Master-Output Slave-Input**. This pin outputs the target serial input data stream for SPI operations and should be connected to the D(1) pin on the SPI flash device.
13	–	PGND	–	Out	**SPI Pseudo Ground**. PGND is pulled Low during SPI operations; otherwise, it is high-Z. When connected to PROG_B on an FPGA, the FPGA will high-Z its SPI signals while the cable is programming the SPI flash. This pin is connected to an open-drain driver and requires a pull-up resistor on the target system.(4)

Table 6: **JTAG/SPI/Slave Serial Port: 2-mm Connector Signals *(Cont'd)***

Pin Number	MODE			Direction(2)	Description
	JTAG Configuration	SPI Programming(1)	Slave-Serial Configuration		
14	–	WP	–	–	**SPI Write Protect**. This pin is reserved for future use. Do not connect for SPI programming.
4	–	–	PROG	Out	**Slave Serial Configuration Reset**. This pin is used to force a reconfiguration of the target FPGA(s) and should be connected to the PROG_B pin of the target FPGA for a single-device system, or to the PROG_B pin of all FPGAs in parallel in a daisy-chain configuration.
6	–	–	CCLK	Out	**Slave Serial Configuration Clock**. FPGAs load one configuration bit per CCLK cycle in Slave Serial mode. CCLK should be connected to the CCLK pin on the target FPGA for single-device configuration, or to the CCLK pin of all FPGAs in parallel in a daisy-chain configuration.
8	–	–	Done	In	**Slave Serial Configuration Done**. This pin indicates to Platform Cable USB II that target FPGAs have received the entire configuration bitstream and should be connected to the Done pin on all FPGAs in parallel for daisy-chained configurations. Additional CCLK cycles are issued following the positive transition of Done to insure that the configuration process is complete.
10	–	–	DIN	Out	**Slave Serial Configuration Data Input**. This pin outputs the serial input data stream for target FPGAs and should be connected to the DIN pin of the target FPGA in a single-device system, or to the DIN pin of the first FPGA in a daisy-chain configuration.
13	–	–	PGND	Out	**Slave Serial Pseudo Ground.** Use of this pin is optional. PGND is pulled Low during Slave Serial operations; otherwise, it is high-Z. This pin is connected to an open-drain driver and requires a pull-up resistor on the target system.(4)
14	–	–	INIT	In	**Slave Serial Configuration Initialization**. This pin indicates that configuration memory is being cleared and should be connected to the INIT_B pin of the target FPGA for a single-device system, or to the INIT_B pin on all FPGAs in parallel in a daisy-chain configuration.
3, 5, 7, 9, 11	–	–	–	–	**Digital Ground**. All ground pins should be connected to digital ground on the target system to minimize crosstalk.
1, 12	–	–	–	–	**Not Connected.**

Notes:

1. The listed SPI pin names match those of SPI flash devices from ST Microelectronics. Pin names of compatible SPI devices from other vendors can vary. Consult the vendor's SPI device data sheet for equivalent pin names.
2. The signal pins (HALT_INIT_WP, TDI_DIN_MOSI, TDO_DONE_MISO, TCK_CCLK_SCK, TMS_PROG_SS) are bidirectional. Their directions during cable operations are defined by the current configuration or programming mode (JTAG, SPI or Slave Serial).
3. The target reference voltage must be regulated and not have a current-limiting resistor in series with the V_{REF} pin.
4. For more details, see "Target System Connections," page 15 and "Pseudo Ground Signal," page 21.

Platform Cable USB II Operating Characteristics

Table 7: **Absolute Maximum Ratings(1)**

Symbol	Description	Conditions	Value	Units
V_{BUS}	USB Port Supply Voltage		5.25	V
V_{REF}	Target Reference Voltage		6.00	V
I_{REF}	Target Supply Current	V_{REF} = 5.25V	100	mA
T_A	Ambient Operating Temperature		70	°C
I_{OUT}	DC Output Current (TCK_CCLK_SCK, TMS_PROG_SS, TDI_DIN_MOSI, and INIT)		±24	mA

Notes:

1. Exposure to absolute rating conditions for extended periods of time can affect product reliability. The values listed in this table are stress ratings only. Functional operation of the product at these or any other conditions beyond those listed under Table 8: Recommended DC Operating Conditions is not implied or recommended.

Table 8: **Recommended DC Operating Conditions**

Symbol	Description	Conditions	Min	Max	Units
V_{BUS}	USB Port Supply Voltage		4.00	5.25	V
V_{REF}	Target Reference Voltage		1.5	5.00	V
T_A	Ambient Operating Temperature		0	70	°C
T_{STG}	Storage Temperature		–40	+85	°C

Table 9: **DC Electrical Characteristics**

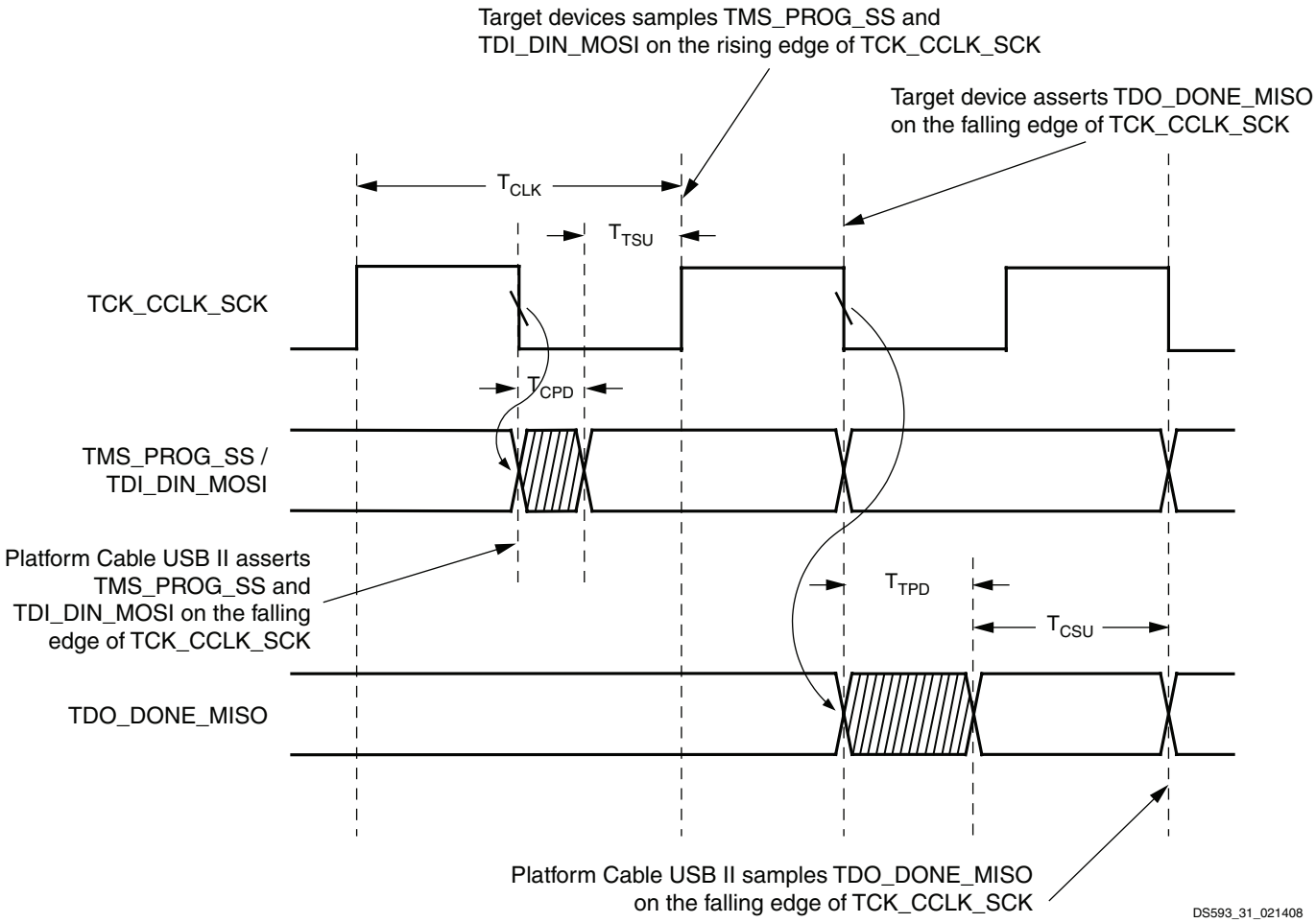
Symbol	Description	Conditions	Min	Max	Units
I_{REF}	Target Supply Current	V_{REF} = 3.3V		15	mA
		V_{REF} = 2.5V		3	
		V_{REF} = 1.8V		1	
		V_{REF} = 1.5V		1	
V_{OH}	High-Level Output Voltage	V_{REF} = 3.3V; I_{OH} = –8 mA	2.25		V
		V_{REF} = 2.5V; I_{OH} = –8 mA	2.15		
		V_{REF} = 1.8V; I_{OH} = –8 mA	1.55		
		V_{REF} = 1.5V; I_{OH} = –8 mA	1.30		
V_{OL}	Low-Level Output Voltage	V_{REF} = 3.3V; I_{OH} = 16 mA		0.40	V
		V_{REF} = 2.5V; I_{OH} = 8 mA		0.30	
		V_{REF} = 1.5V; I_{OH} = 4 mA		0.24	
V_{IH}	High-Level Input Voltage	V_{REF} = 1.5V to 3.3V	1.35		V
V_{IL}	Low-Level Input Voltage	V_{REF} = 1.5V to 3.3V		0.45	V
I_{CC1}	Dynamic Current(1)	V_{BUS} = 5.25V: TCK = 24 MHz	85	110	mA
I_{CC2}	Dynamic Current(2)	V_{BUS} = 5.25V; TCK = 6 MHz	85	100	mA
I_{CCSU}	Suspend Current	V_{BUS} = 5.25V	250	350	µA

Notes:

1. Operating at Hi-Speed on a USB 2.0 port.
2. Operating at full-speed on a USB 1.1 port.

Table 10: **Switching Characteristics**

Symbol	Description	Conditions		Min	Max	Units
T_{CLK}	Clock Period	TCK	750 kHz		1333	ns
			24 MHz	41.66		ns
T_{CPD}	Cable Propagation Delay Time (TDI or TMS relative to the negative edge of TCK)	V_{REF} = 1.5V to 3.3V			16	ns
T_{TSU}	Target Setup Time (TDI or TMS relative to the positive edge of TCK)	V_{REF} = 1.5V to 3.3V		4.8		ns
T_{CSU}	Cable Setup Time (TDO relative to the negative edge of TCK)	V_{REF} = 1.5V to 3.3V		15.8		ns
T_{TPD}	Target Propagation Delay Time (TDO relative to the negative edge of TCK)	V_{REF} = 1.5V to 3.3V			24.6	ns



Notes:

1. All times are in nanoseconds and are relative to the target system interface connector.
2. T_{TSU} Min is the minimum setup time guaranteed by Platform Cable USB II relative to the positive edge of TCK_CCLK_SCK.
3. T_{CSU} Min is the minimum setup required by Platform Cable USB II to properly sample TDO_DONE_MISO.
4. Propagation delays associated with buffers on the target system must be taken into account to satisfy the minimum setup times.

Figure 31: **Platform Cable USB II Timing Diagram**

USB-IF Compliance

Platform Cable USB II is certified by the USB Integrators Forum (USB-IF). Certification is achieved when a product passes a battery of tests required by the USB-IF Compliance Program. These tests (performed at an independent test facility) measure a product's conformity with Universal Serial Bus Specification Revision 2.0 and establish a reasonable level of acceptability. Products that pass this level of acceptability are added to the USB-IF Integrator's List and receive the rights of usage for the USB logo.

FCC Notice

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the data sheet, could cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case, the user is required to correct the interference at his own expense.

Industry Canada Information

This Class A digital apparatus complies with Canadian ICES-003.

Ordering Information

Platform Cable USB II ships with each of the items shown in Table 11 plus a 1.8-meter, Hi-Speed USB, A-B cable.

Table 11: **Ordering Information**

Item	Product Number
Platform Cable USB II	HW-USB-II-G
Ribbon Cable, 6-inch	HW-RIBBON14
Flying Wire Set	HW-USB-FLYLEADS-G

Marking Information

Table 12: **Marking Information**

Model Name	Serial Prefix	Description
DLC10	XU	Platform Cable USB II

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
03/03/08	1.0	Initial Xilinx release.
05/14/08	1.1	• Updated trademark references. • Added support for Platform Flash XL.
06/09/08	1.2	Corrected the functional descriptions of pins 6 and 8 in Table 6, page 27.

Notice of Disclaimer