MMBF4391L, MMBF4392L, MMBF4393L

JFET Switching Transistors

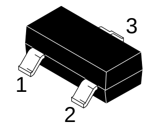
N−Channel

ON Semiconductor®

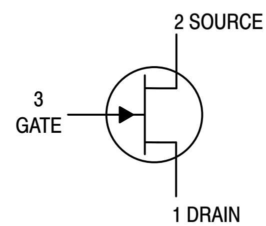
www.onsemi.com

Features

- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant*



SOT−23
CASE 318
STYLE 10



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain−Source Voltage	V_{DS}	30	Vdc
Drain−Gate Voltage	V_{DG}	30	Vdc
Gate−Source Voltage	V_{GS}	30	Vdc
Forward Gate Current	$I_{G(f)}$	50	mAdc

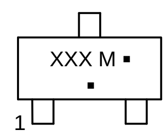
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR−5 Board (Note 1) T_A = 25°C Derate above 25°C	P_D	225 1.8	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	556	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. FR−5 = 1.0 × 0.75 × 0.062 in.

MARKING DIAGRAM



XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

MARKING & ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 2 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate−Source Breakdown Voltage (I_G = 1.0 μAdc, V_{DS} = 0)	$V_{(BR)GSS}$	30	−	Vdc
Gate Reverse Current (V_{GS} = 15 Vdc, V_{DS} = 0, T_A = 25°C) (V_{GS} = 15 Vdc, V_{DS} = 0, T_A = 100°C)	I_{GSS}	 − −	 1.0 0.20	 nAdc μAdc
Gate−Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 10 nAdc) MMBF4391LT1 MMBF4392LT1 MMBF4393LT1	$V_{GS(off)}$	 −4.0 −2.0 −0.5	 −10 −5.0 −3.0	Vdc
Off−State Drain Current (V_{DS} = 15 Vdc, V_{GS} = −12 Vdc) (V_{DS} = 15 Vdc, V_{GS} = −12 Vdc, T_A = 100°C)	$I_{D(off)}$	 − −	 1.0 1.0	 nAdc μAdc
ON CHARACTERISTICS				
Zero−Gate−Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0) MMBF4391LT1 MMBF4392LT1 MMBF4393LT1	I_{DSS}	 50 25 5.0	 150 75 30	mAdc
Drain−Source On−Voltage (I_D = 12 mAdc, V_{GS} = 0) MMBF4391LT1 (I_D = 6.0 mAdc, V_{GS} = 0) MMBF4392LT1 (I_D = 3.0 mAdc, V_{GS} = 0) MMBF4393LT1	$V_{DS(on)}$	 − − −	 0.4 0.4 0.4	Vdc
Static Drain−Source On−Resistance (I_D = 1.0 mAdc, V_{GS} = 0) MMBF4391LT1 MMBF4392LT1 MMBF4393LT1	$r_{DS(on)}$	 − − −	 30 60 100	Ω
SMALL− SIGNAL CHARACTERISTICS				
Input Capacitance (V_{DS} = 0 Vdc, V_{GS} = −15 Vdc, f = 1.0 MHz)	C_{iss}	−	14	pF
Reverse Transfer Capacitance (V_{DS} = 0 Vdc, V_{GS} = −12 Vdc, f = 1.0 MHz)	C_{rss}	−	3.5	pF

ORDERING INFORMATION

Device	Marking	Package	Shipping†
MMBF4391LT1G	6J	SOT−23 (Pb−Free)	3,000 / Tape & Reel
SMMBF4391LT1G*	6J	SOT−23 (Pb−Free)	3,000 / Tape & Reel
MMBF4392LT1G	6K	SOT−23 (Pb−Free)	3,000 / Tape & Reel
MMBF4393LT1G	M6G	SOT−23 (Pb−Free)	3,000 / Tape & Reel
SMMBF4393LT1G*	M6G	SOT−23 (Pb−Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable.

TYPICAL CHARACTERISTICS

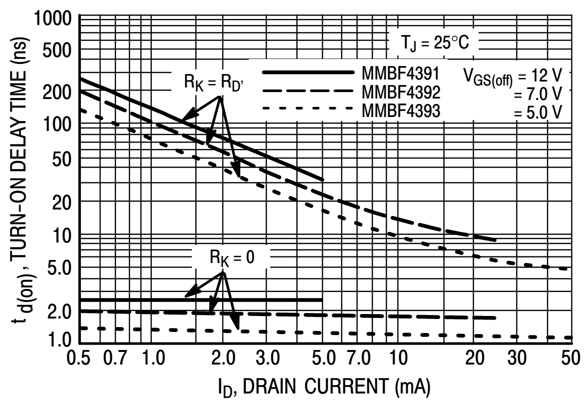


Figure 1. Turn−On Delay Time

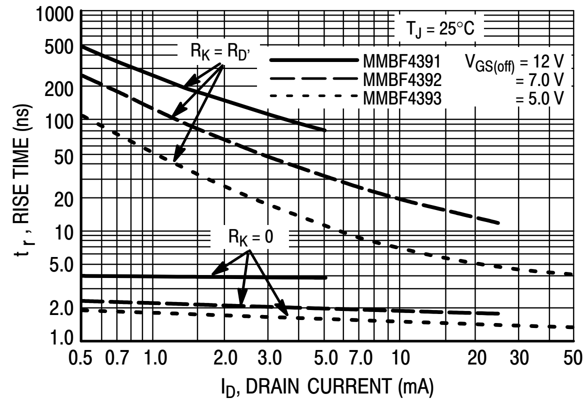


Figure 2. Rise Time

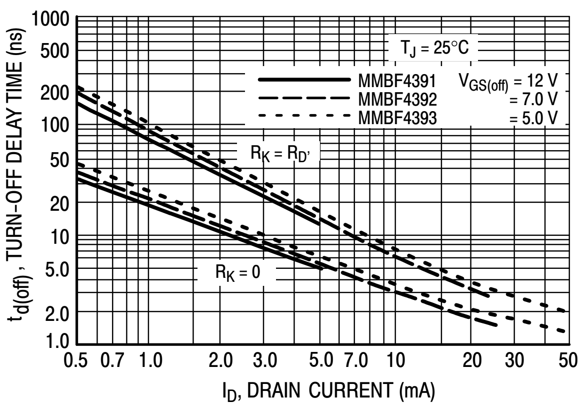


Figure 3. Turn−Off Delay Time

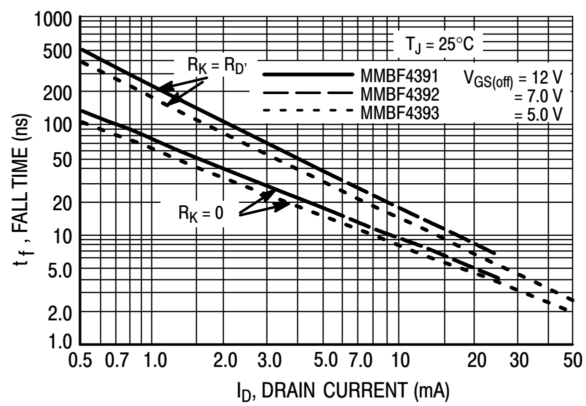


Figure 4. Fall Time

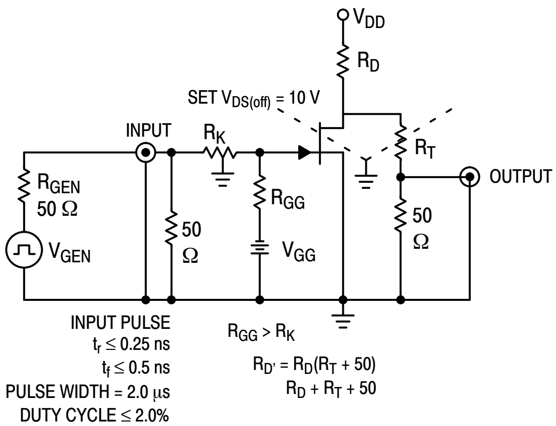


Figure 5. Switching Time Test Circuit

NOTE 1

The switching characteristics shown above were measured using a test circuit similar to Figure 5. At the beginning of the switching interval, the gate voltage is at Gate Supply Voltage ($-V_{GG}$). The Drain−Source Voltage (V_{DS}) is slightly lower than Drain Supply Voltage (V_{DD}) due to the voltage divider. Thus Reverse Transfer Capacitance (C_{rss}) of Gate−Drain Capacitance (C_{gd}) is charged to $V_{GG} + V_{DS}$.

During the turn−on interval, Gate−Source Capacitance (C_{gs}) discharges through the series combination of R_{Gen} and R_K. C_{gd} must discharge to $V_{DS(on)}$ through R_G and R_K in series with the parallel combination of effective load impedance (R'_D) and Drain−Source Resistance (r_{DS}). During the turn−off, this charge flow is reversed.

Predicting turn−on time is somewhat difficult as the channel resistance r_{DS} is a function of the gate−source voltage. While C_{gs} discharges, V_{GS} approaches zero and r_{DS} decreases. Since C_{gd} discharges through r_{DS}, turn−on time is non−linear. During turn−off, the situation is reversed with r_{DS} increasing as C_{gd} charges.

The above switching curves show two impedance conditions; 1) R_K is equal to $R_{D'}$ which simulates the switching behavior of cascaded stages where the driving source impedance is normally the load impedance of the previous stage, and 2) $R_K = 0$ (low impedance) the driving source impedance is that of the generator.

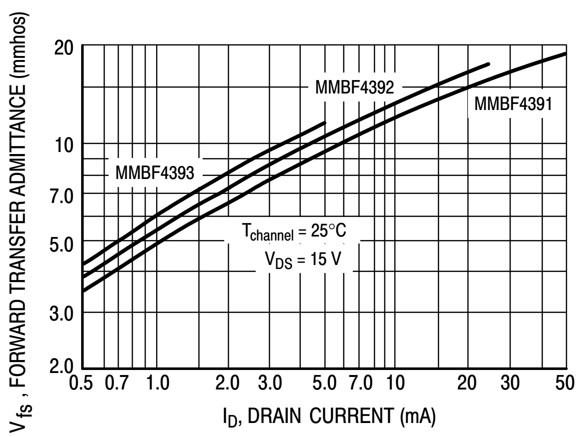


Figure 6. Typical Forward Transfer Admittance

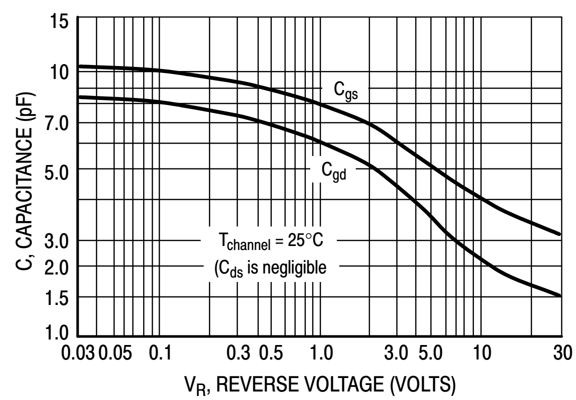


Figure 7. Typical Capacitance

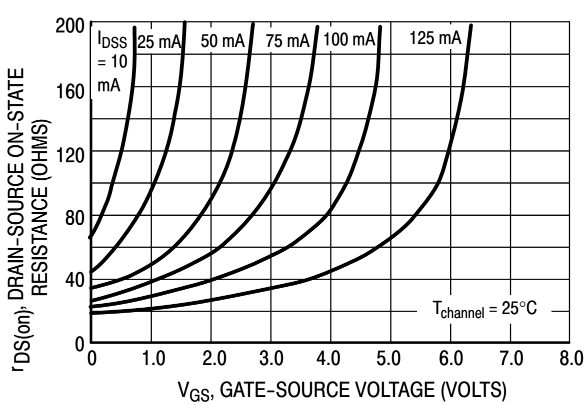


Figure 8. Effect of Gate−Source Voltage on Drain−Source Resistance

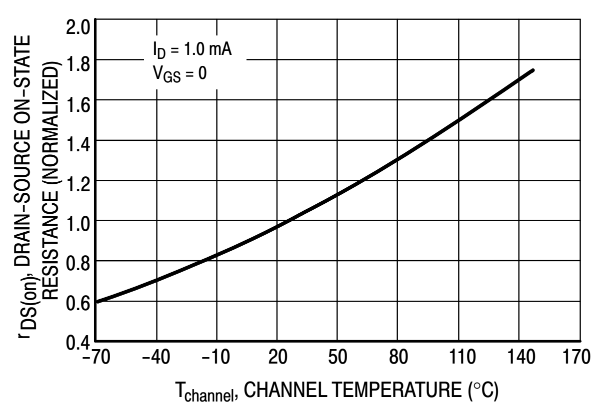


Figure 9. Effect of Temperature on Drain−Source On−State Resistance

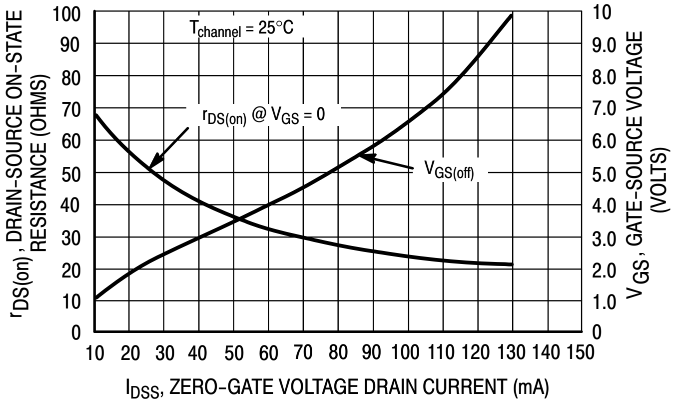


Figure 10. Effect of I_{DSS} on Drain−Source Resistance and Gate−Source Voltage

NOTE 2

The Zero−Gate−Voltage Drain Current (I_{DSS}) is the principle determinant of other J−FET characteristics. Figure 10 shows the relationship of Gate−Source Off Voltage ($V_{GS(off)}$) and Drain−Source On Resistance ($r_{DS(on)}$) to I_{DSS}. Most of the devices will be within ±10% of the values shown in Figure 10. This data will be useful in predicting the characteristic variations for a given part number.

For example:

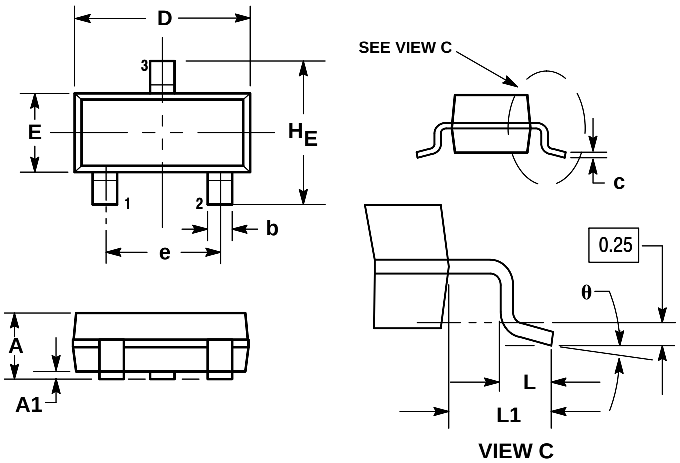
Unknown

$r_{DS(on)}$ and V_{GS} range for an MMBF4392

The electrical characteristics table indicates that an MMBF4392 has an I_{DSS} range of 25 to 75 mA. Figure 10 shows $r_{DS(on)}$ = 52 Ω for I_{DSS} = 25 mA and 30 Ω for I_{DSS} = 75 mA. The corresponding V_{GS} values are 2.2 V and 4.8 V.

PACKAGE DIMENSIONS

SOT−23 (TO−236)
CASE 318−08
ISSUE AP

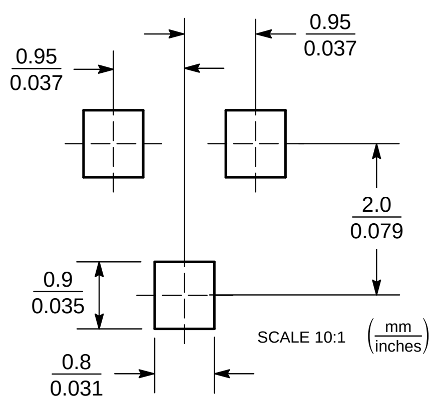


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104
θ	0°	−−−	10°	0°	−−−	10°

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

SOLDERING FOOTPRINT



PUBLICATION ORDERING INFORMATION

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