

N-channel 950 V, 0.65  $\Omega$  typ., 8 A Zener-protected SuperMESH™ 5 Power MOSFETs in D<sup>2</sup>PAK, TO-220FP, TO-220 and TO-247

Datasheet - production data

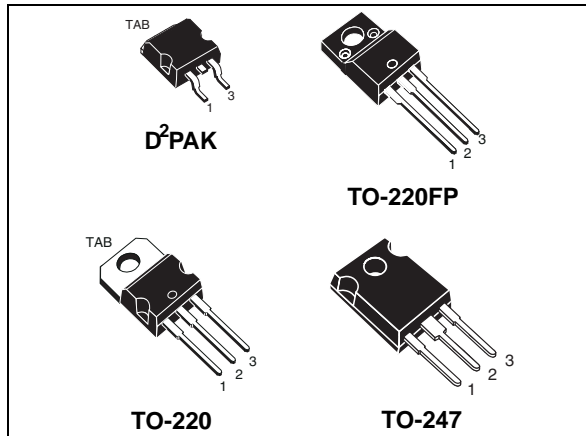
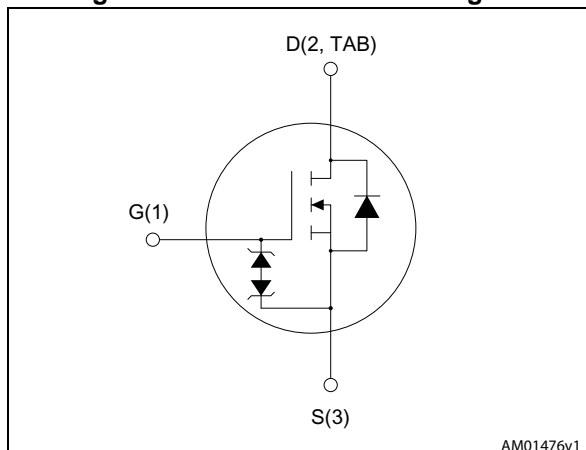


Figure 1. Internal schematic diagram



## Features

Order codes	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>	P <sub>TOT</sub>
STB10N95K5	950 V	0.8 $\Omega$	8 A	130 W
STF10N95K5				30 W
STP10N95K5				130 W
STW10N95K5				

- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

## Applications

- Switching applications

## Description

These N-channel Zener-protected Power MOSFETs are designed using ST's revolutionary avalanche-rugged very high voltage SuperMESH™ 5 technology, based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance, and ultra-low gate charge for applications which require superior power density and high efficiency.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB10N95K5	10N95K5	D <sup>2</sup> PAK	Tape and reel
STF10N95K5		TO-220FP	Tube
STP10N95K5		TO-220	
STW10N95K5		TO-247	

## Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
	2.1 Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuits</b> .....	<b>9</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>10</b>
<b>5</b>	<b>Packaging mechanical data</b> .....	<b>18</b>
<b>6</b>	<b>Revision history</b> .....	<b>20</b>

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220FP	D <sup>2</sup> PAK, TO-220, TO-247	
V <sub>GS</sub>	Gate- source voltage	±30		V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	8 <sup>(1)</sup>	8	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	5 <sup>(1)</sup>	5	A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	32		A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	30	130	W
I <sub>AR</sub>	Max current during repetitive or single pulse avalanche	2.5		A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>J</sub> = 25 °C, I <sub>D</sub> =I <sub>AS</sub> , V <sub>DD</sub> = 50 V)	122		mJ
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	4.5		V/ns
dv/dt <sup>(4)</sup>	MOSFET dv/dt ruggedness	50		V/ns
V <sub>ISO</sub>	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T <sub>C</sub> =25 °C)	2500		V
T <sub>J</sub> T <sub>stg</sub>	Operating junction temperature Storage temperature	- 55 to 150		°C

- Limited by maximum junction temperature.
- Pulse width limited by safe operating area.
- I<sub>SD</sub> ≤ 8 A, di/dt ≤ 100 A/μs, V<sub>DS(peak)</sub> ≤ V<sub>(BR)DSS</sub>.
- V<sub>SD</sub> ≤ 760 V

**Table 3. Thermal data**

Symbol	Parameter	Value			Unit
		TO-220FP	D <sup>2</sup> PAK	TO-220, TO-247	
R <sub>thj-case</sub>	Thermal resistance junction-case max	4.2	0.96		°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-amb max	62.5		62.5	°C/W
R <sub>thj-pcb</sub> <sup>(1)</sup>	Thermal resistance junction-pcb max		30		°C/W

- When mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board

## 2 Electrical characteristics

(T<sub>case</sub> = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0	950			V
I <sub>DSS</sub>	Zero gate voltage, V <sub>GS</sub> = 0 drain current	V <sub>DS</sub> = 950 V			1	μA
		V <sub>DS</sub> = 950 V, T <sub>C</sub> = 125 °C			50	μA
I <sub>GSS</sub>	Gate-body leakage current	V <sub>GS</sub> = ± 20 V; V <sub>DS</sub> = 0			±10	μA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100 μA	3	4	5	V
R <sub>DS(on)</sub>	Static drain-source on-resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4 A		0.65	0.8	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>ISS</sub>	Input capacitance	V <sub>DS</sub> = 100 V, f = 1 MHz, V <sub>GS</sub> = 0	-	630	-	pF
C <sub>OSS</sub>	Output capacitance		-	50	-	pF
C <sub>rSS</sub>	Reverse transfer capacitance		-	0.6	-	pF
C <sub>o(tr)</sub> <sup>(1)</sup>	Equivalent capacitance time related	V <sub>GS</sub> = 0, V <sub>DS</sub> = 0 to 760 V	-	77	-	pF
C <sub>o(er)</sub> <sup>(2)</sup>	Equivalent capacitance energy related		-	28	-	pF
R <sub>G</sub>	Intrinsic gate resistance	f = 1 MHz open drain	-	6.5	-	Ω
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 760 V, I <sub>D</sub> = 8 A V <sub>GS</sub> = 10 V (see <a href="#">Figure 20</a> )	-	22	-	nC
Q <sub>gs</sub>	Gate-source charge		-	5	-	nC
Q <sub>gd</sub>	Gate-drain charge		-	15	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C<sub>OSS</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>
2. energy related is defined as a constant equivalent capacitance giving the same stored energy as C<sub>OSS</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 475 \text{ V}$ , $I_D = 4 \text{ A}$ , $R_G = 4.7 \ \Omega$ , $V_{GS} = 10 \text{ V}$ (see Figure 19)	-	22	-	ns
$t_r$	Rise time		-	14	-	ns
$t_{d(off)}$	Turn-off-delay time		-	51	-	ns
$t_f$	Fall time		-	15	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$I_{SD}$	Source-drain current		-		8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		32	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 8 \text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 8 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see Figure 21)	-	404		ns
$Q_{rr}$	Reverse recovery charge		-	5.2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	25.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 8 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ , $T_J = 150 \text{ }^\circ\text{C}$ (see Figure 21)	-	596		ns
$Q_{rr}$	Reverse recovery charge		-	6.9		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	23		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$ , $I_D = 0$	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D<sup>2</sup>PAK and TO-220

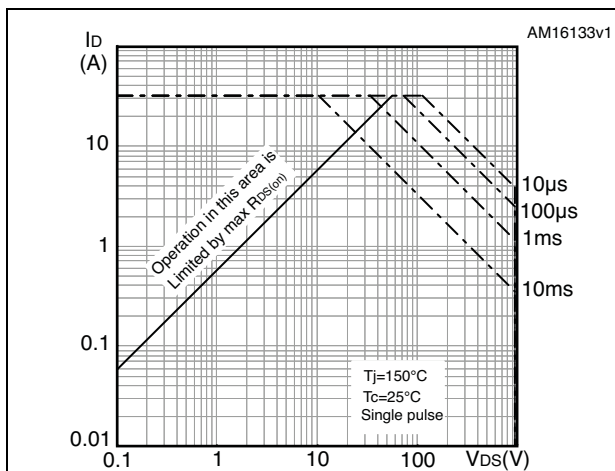


Figure 3. Thermal impedance for D<sup>2</sup>PAK and TO-220

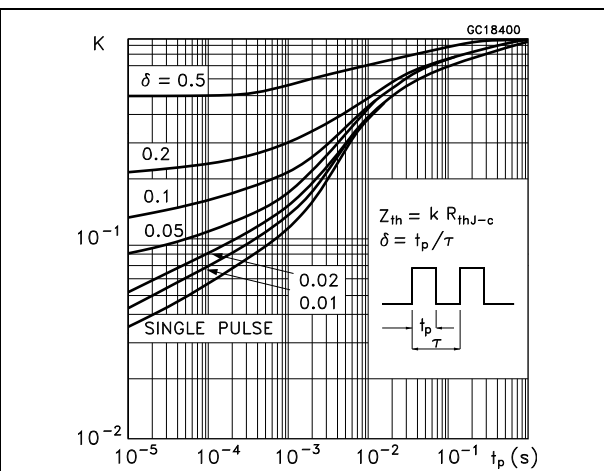


Figure 4. Safe operating area for TO-220FP

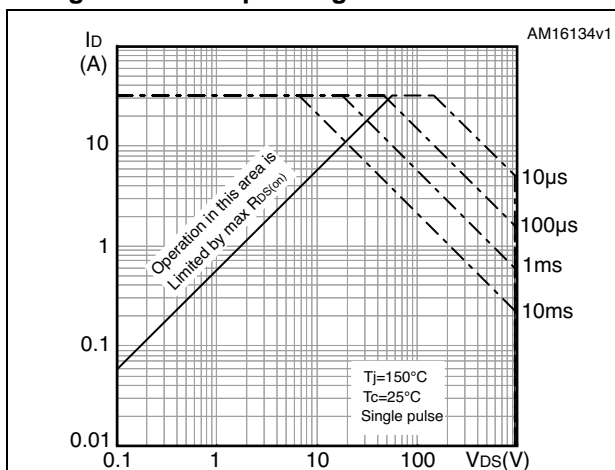


Figure 5. Thermal impedance for TO-220FP

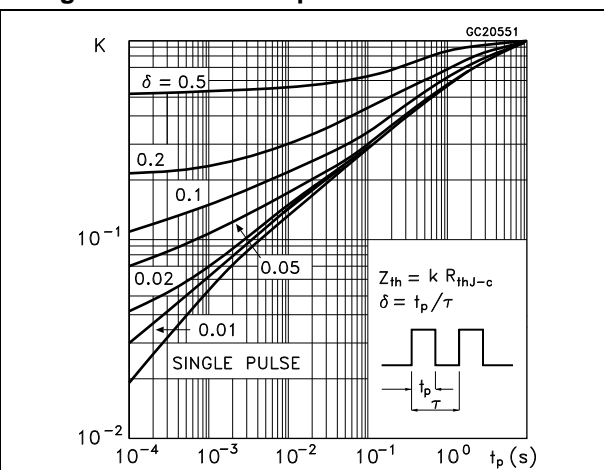


Figure 6. Safe operating area for TO-247

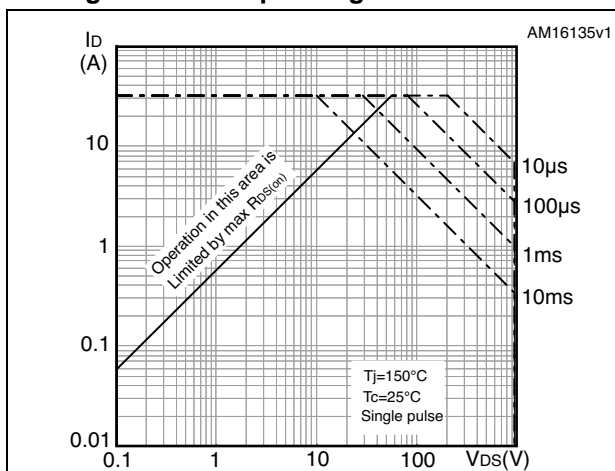


Figure 7. Thermal impedance for TO-247

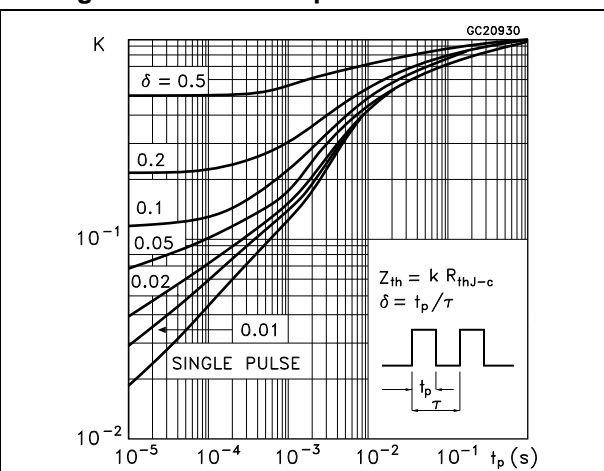


Figure 8. Output characteristics

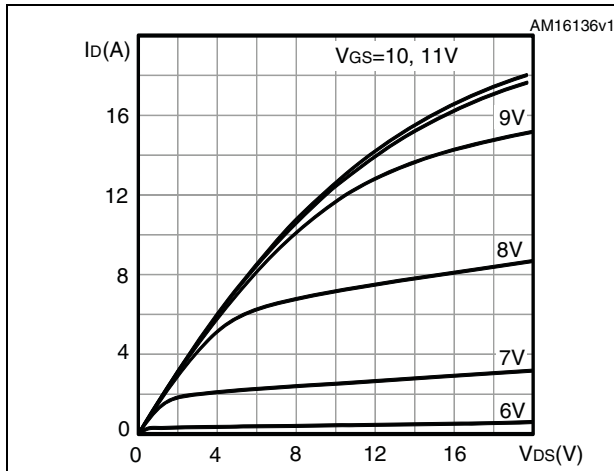


Figure 9. Transfer characteristics

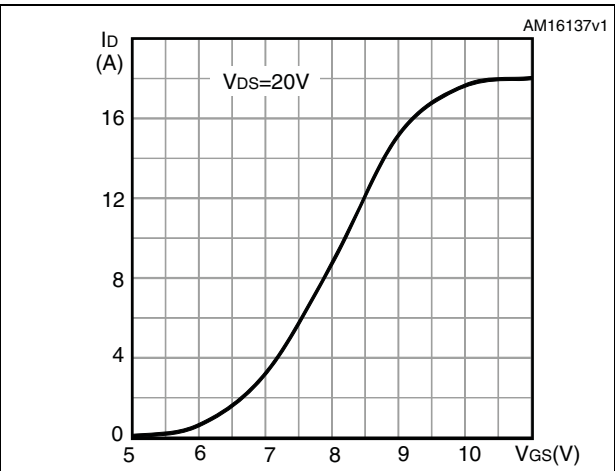


Figure 10. Gate charge vs gate-source voltage

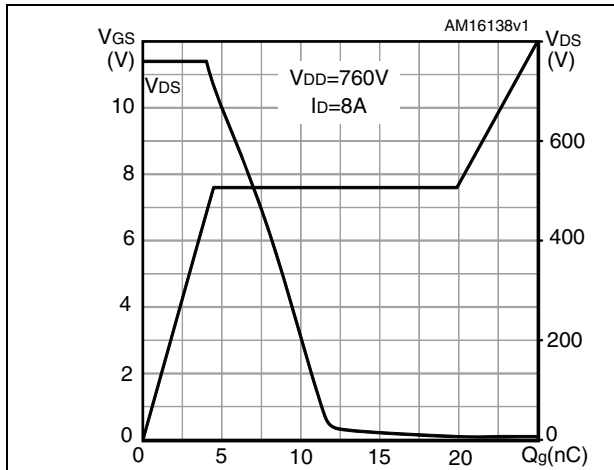


Figure 11. Static drain-source on-resistance

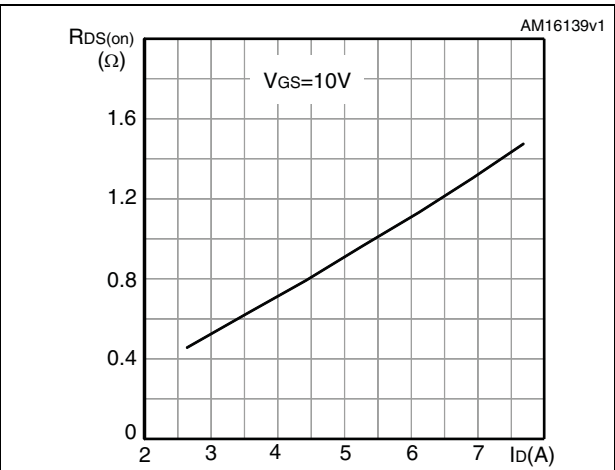


Figure 12. Capacitance variations

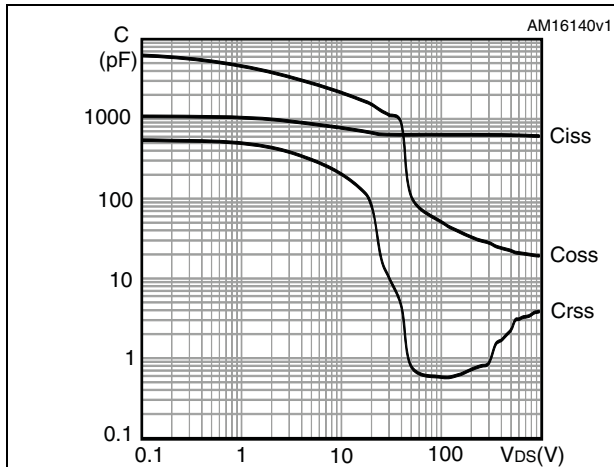


Figure 13. Output capacitance stored energy

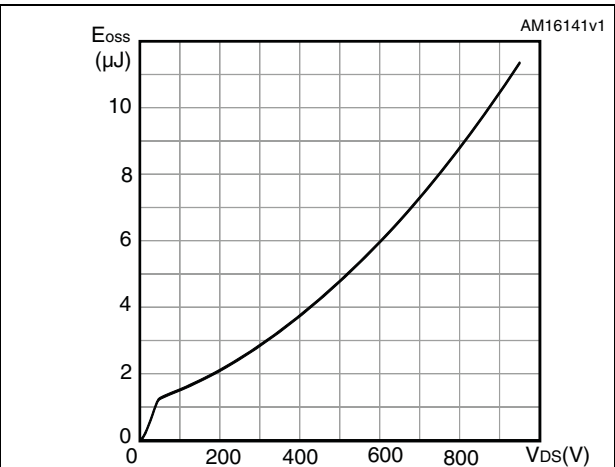


Figure 14. Normalized gate threshold voltage vs temperature

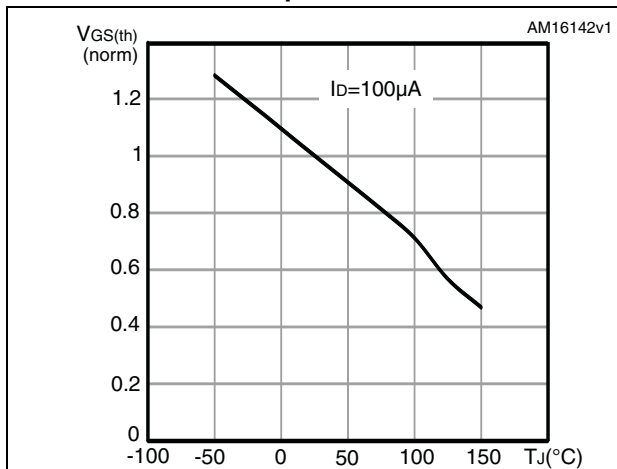


Figure 15. Normalized on-resistance vs temperature

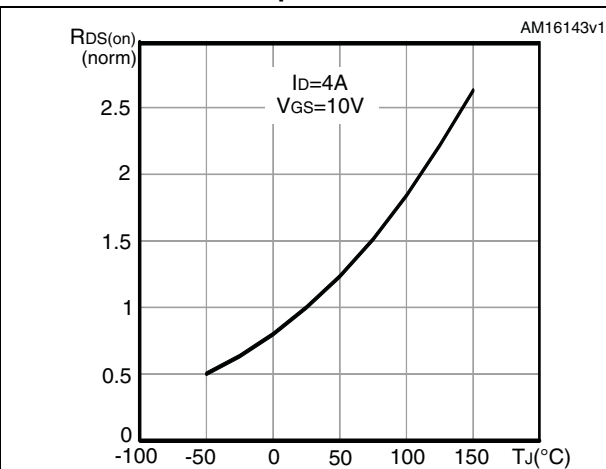


Figure 16. Normalized V<sub>DS</sub> vs temperature

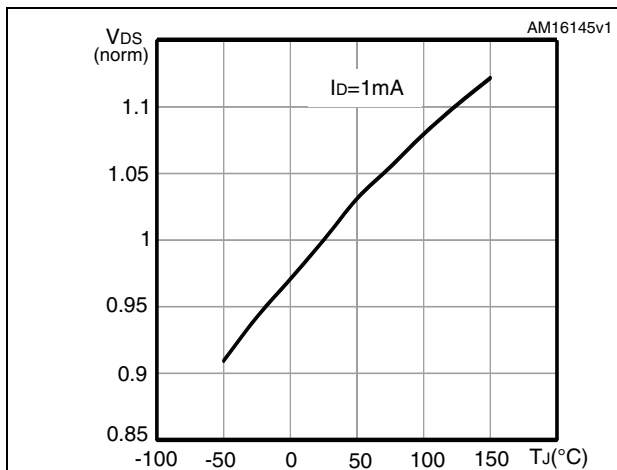


Figure 17. Source-drain diode forward characteristics

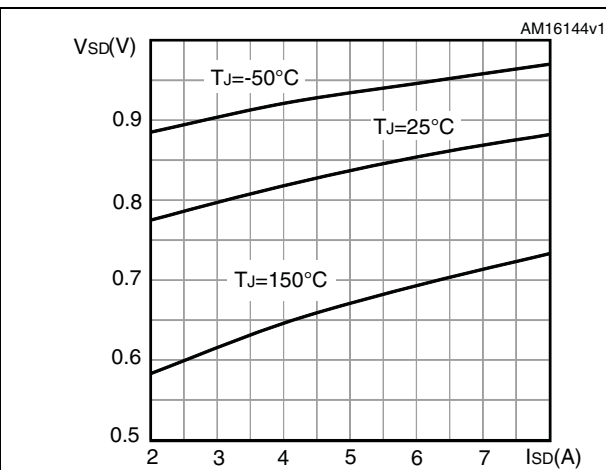
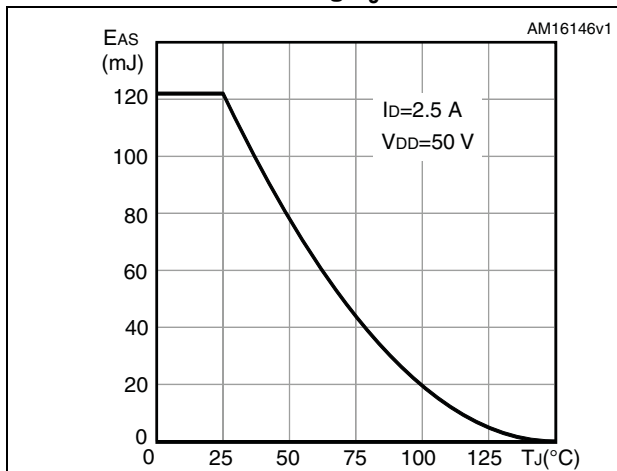


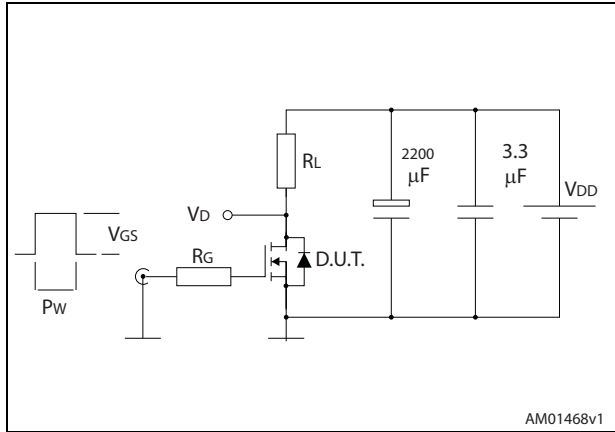
Figure 18. Maximum avalanche energy vs starting T<sub>J</sub>





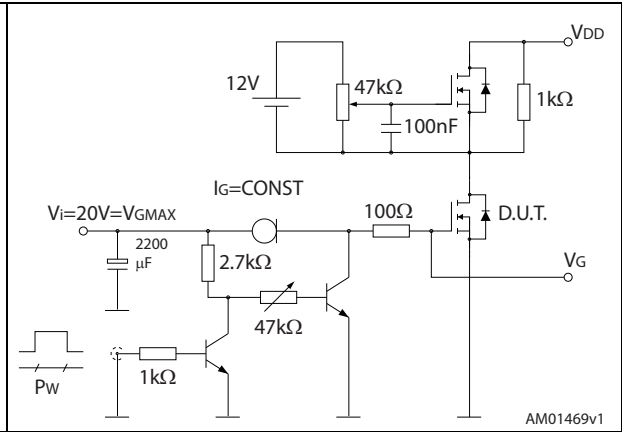
### 3 Test circuits

**Figure 19. Switching times test circuit for resistive load**



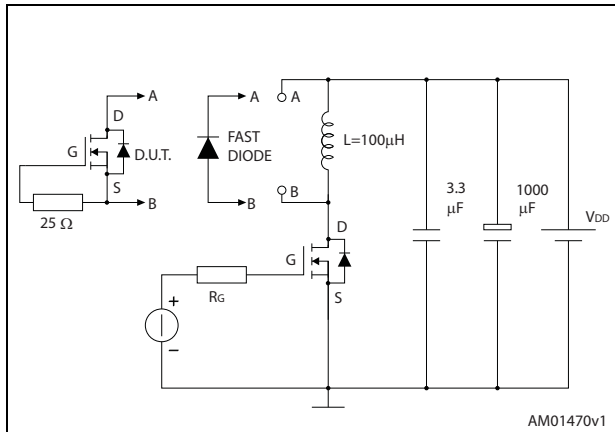
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**Figure 20. Gate charge test circuit**



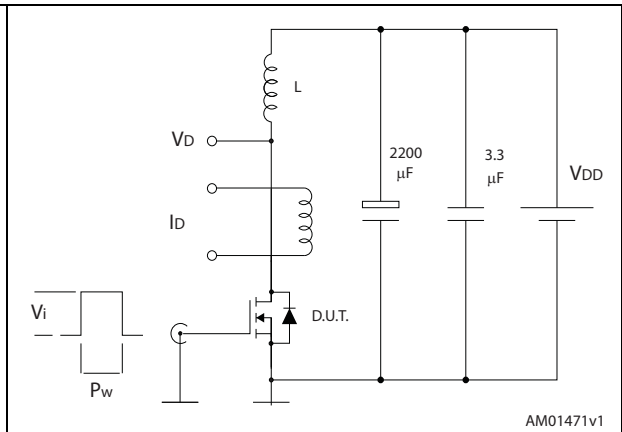
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**Figure 21. Test circuit for inductive load switching and diode recovery times**



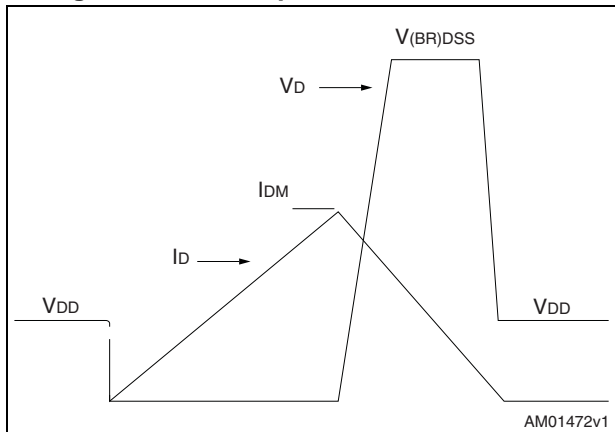
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**Figure 22. Unclamped inductive load test circuit**



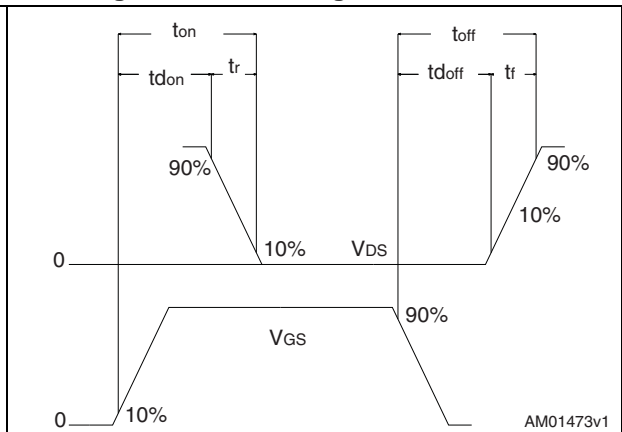
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**Figure 23. Unclamped inductive waveform**



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**Figure 24. Switching time waveform**

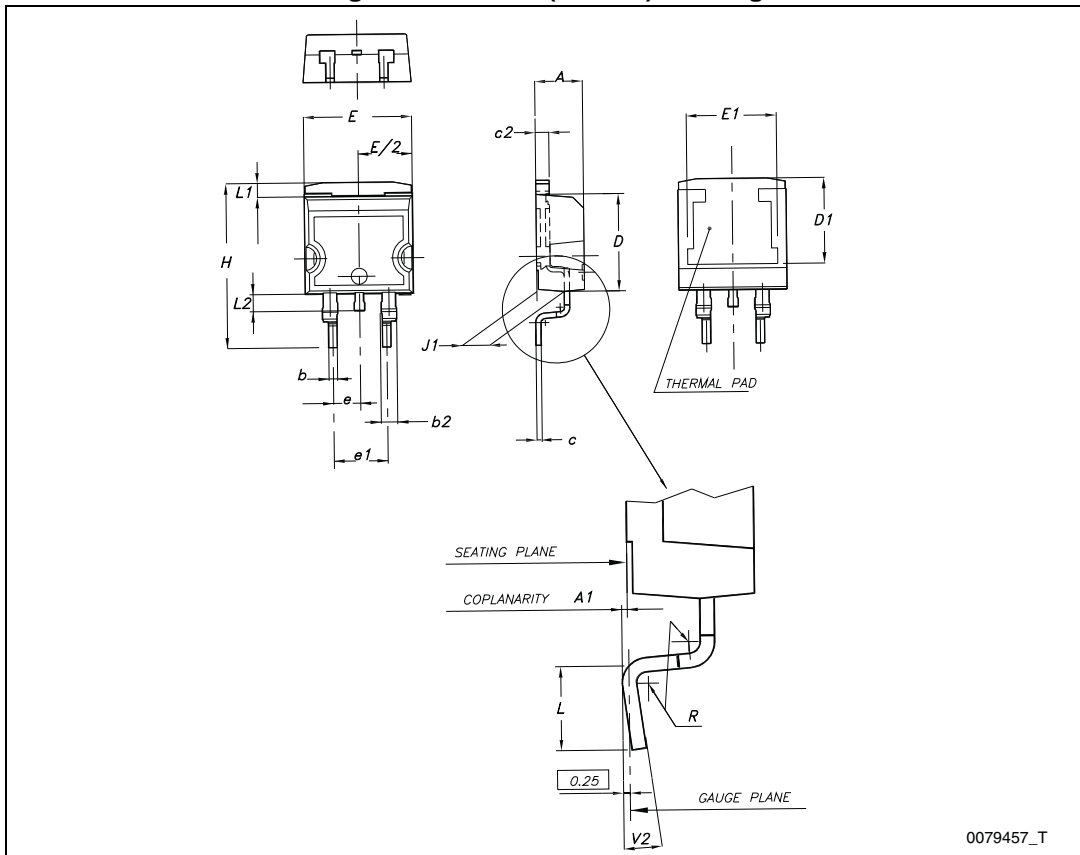


AM01473v1

## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 25. D<sup>2</sup>PAK (TO-263) drawing



0079457\_T

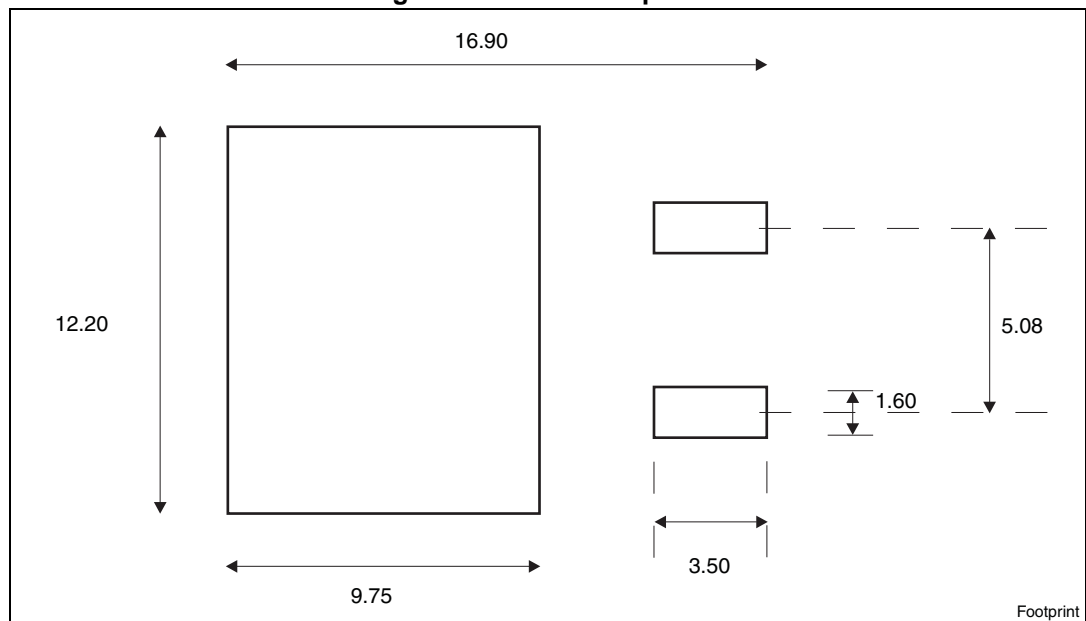
Table 9. D<sup>2</sup>PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85

Table 9. D<sup>2</sup>PAK (TO-263) mechanical data (continued)

Dim.	mm		
	Min.	Typ.	Max.
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 26. D<sup>2</sup>PAK footprint<sup>(a)</sup>



a. All dimension are in millimeters

Figure 27. TO-220FP drawing

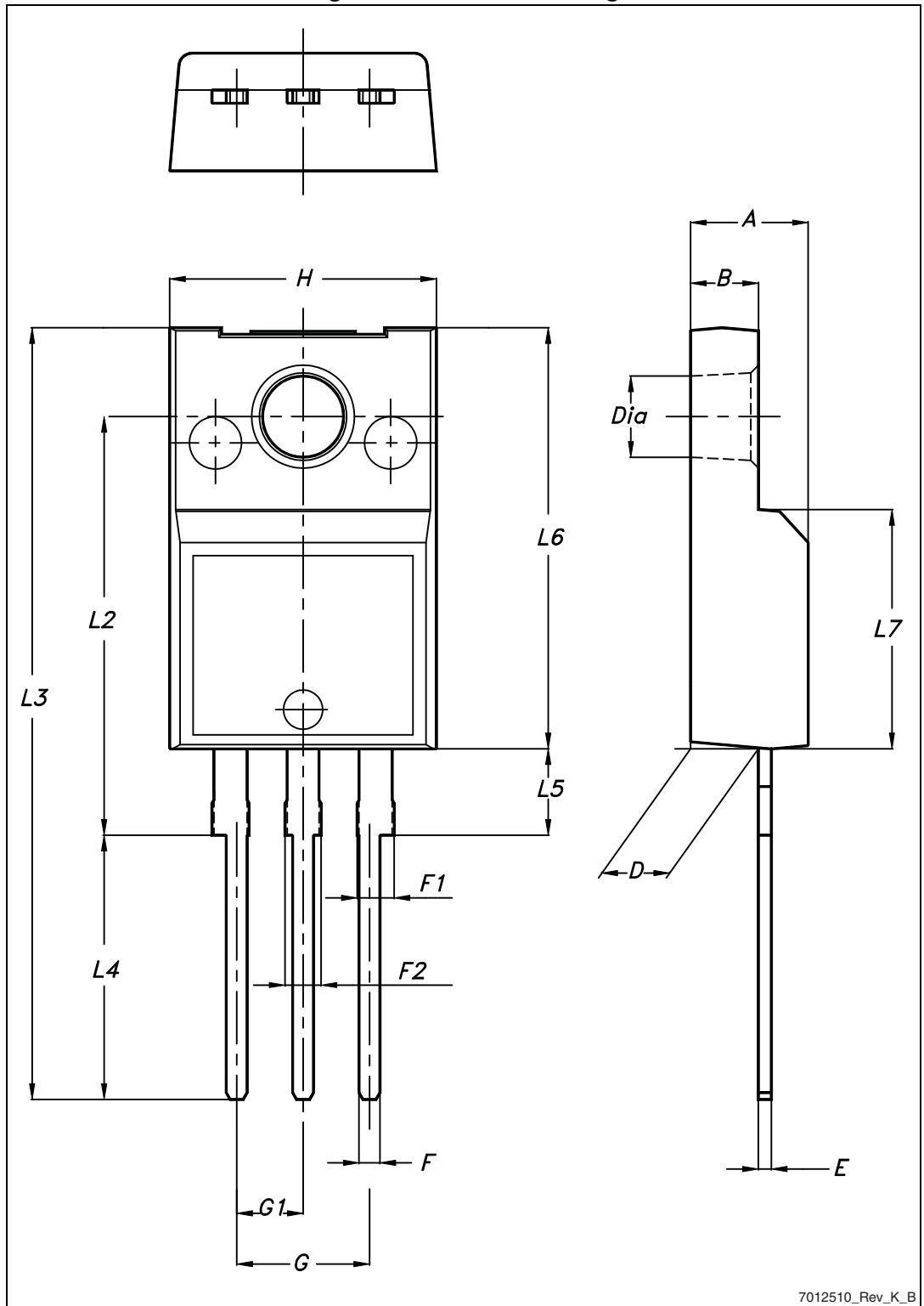


Table 10. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 28. TO-220 type A drawing

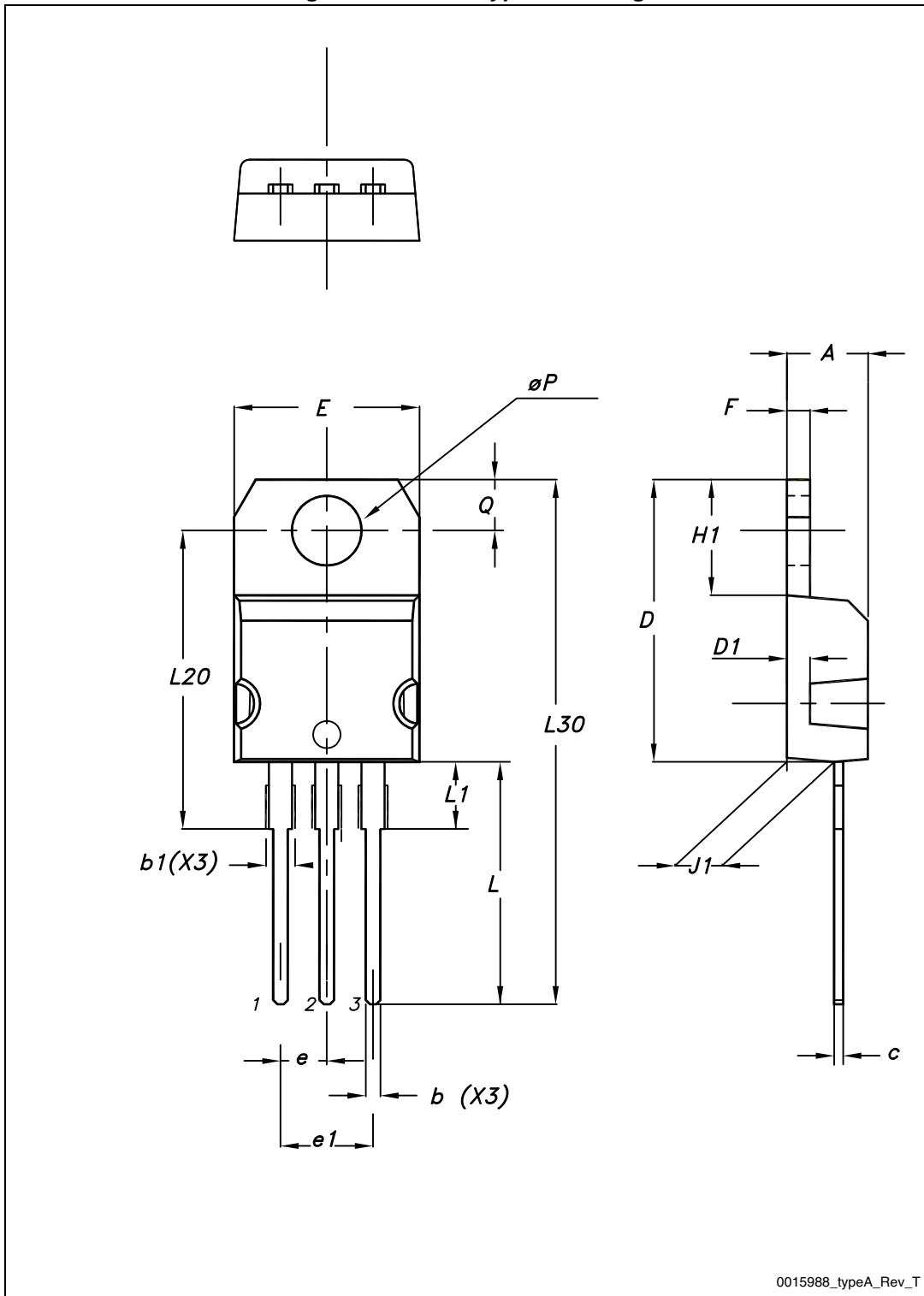
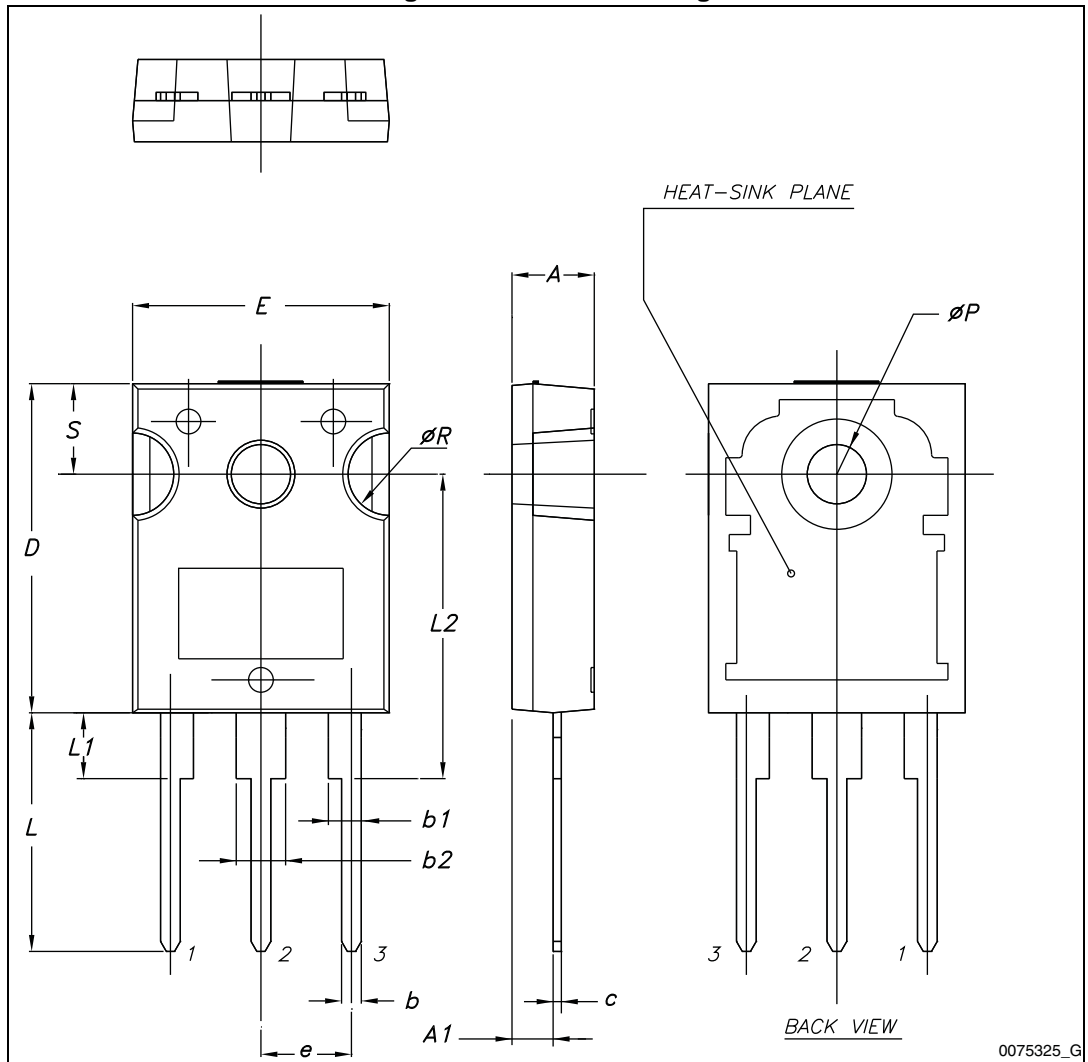


Table 11. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95



Figure 29. TO-247 drawing



0075325\_G

Table 12. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75

Table 12. TO-247 mechanical data (continued)

Dim.	mm.		
	Min.	Typ.	Max.
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

# 5 Packaging mechanical data

Figure 30. Tape

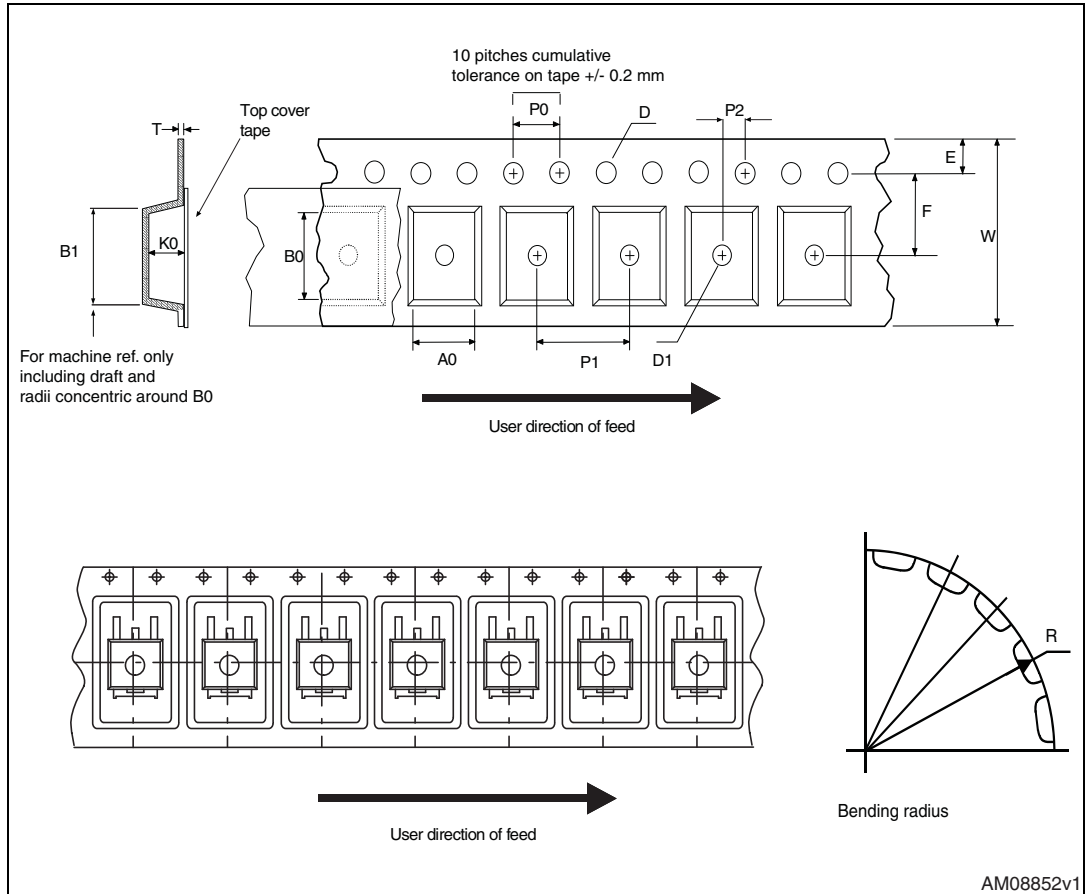


Figure 31. Reel

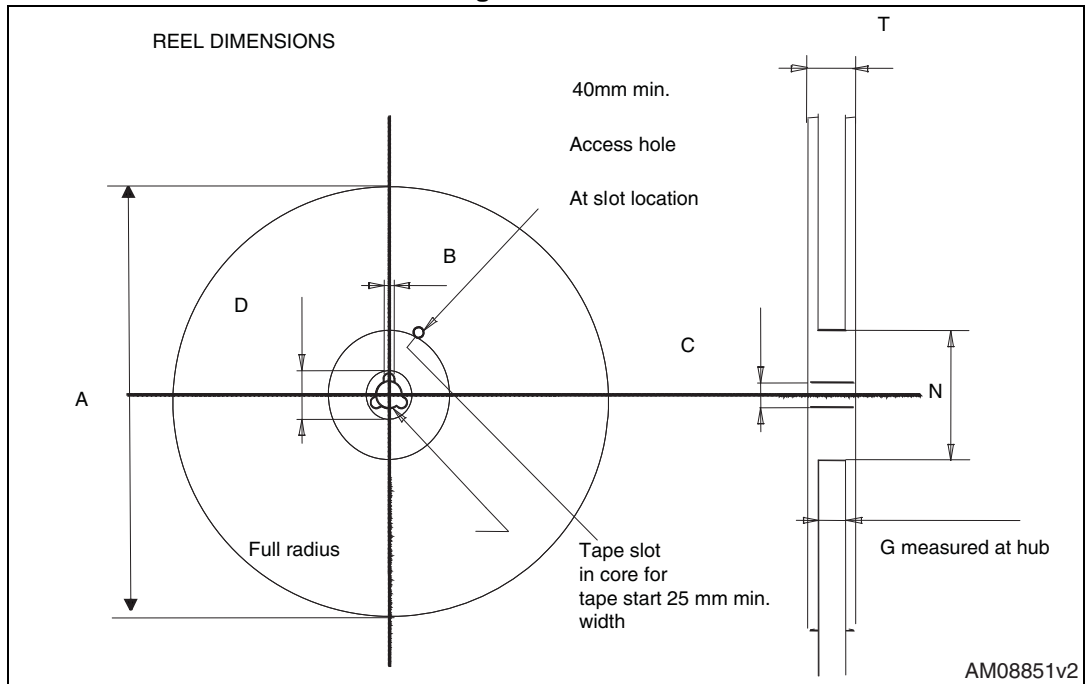


Table 13. D<sup>2</sup>PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

## 6 Revision history

Table 14. Document revision history

Date	Revision	Changes
24-Jun-2013	1	First release.
07-Oct-2013	2	<ul style="list-style-type: none"><li>– Added: D<sup>2</sup>PAK package</li><li>– Modified: <a href="#">note 4</a> in <a href="#">Table 2</a></li><li>– Added: Thermal resistance junction-pcb max parameter</li><li>– Modified: typical values in <a href="#">Table 5</a>, <a href="#">6</a> and <a href="#">7</a></li><li>– Added: <a href="#">Section 2.1: Electrical characteristics (curves)</a></li><li>– Updated: <a href="#">Section 4: Package mechanical data</a></li><li>– Minor text changes</li></ul>
29-Jan-2014	3	<ul style="list-style-type: none"><li>– Datasheet status promoted from preliminary data to production data</li><li>– Minor text changes</li></ul>

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