NUF2441FC

Integrated Passive Filter with ESD Protection

This device is designed for cell phone applications requiring **Headset and Speaker Phone**, **EMI Filtering** and **ESD Protection**. This device offers an integrated solution in a small package reducing PCB space and cost.

Features:

- Provides EMI Filtering and ESD Protection
- Single IC Offers Cost Savings by Replacing 2 Inductors, 4 Capacitors, and 4 TVs Diodes
- Compliance with IEC61000-4-2, (Level 4) 30 kV (Contact), 30 kV (air)
- Flip-Chip Package
- Moisture Sensitivity Level 1
- ESD Ratings: Machine Model = C
  Human Body Model = 3B
- Pb-Free Package is Available*

Benefits:

- Flip-Chip Package Minimizes PCB Space
- Integrated Circuit Increases System Reliability versus Discrete Component Implementation
- TVs Devices Provide ESD Protection That is Better than a Discrete Implementation because the Small IC minimizes Parasitic Inductances

Typical Applications:

- Cell Phones
- Communication Circuits

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
ESD Discharge IEC61000-4-2 Contact Discharge Air Discharge	V_{pp}	 30 30	kV
Operating Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Lead Solder Temperature (10 second duration)	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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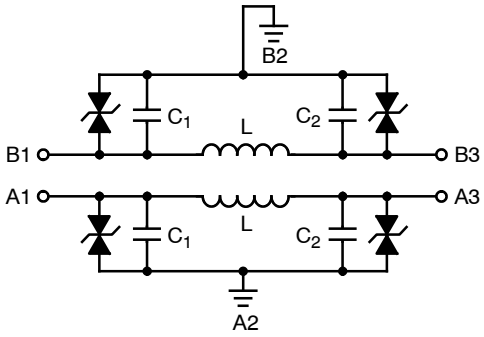
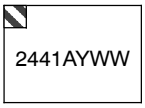
http://onsemi.com

CIRCUIT DESCRIPTION



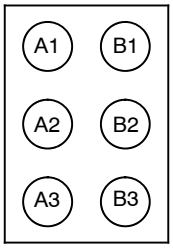
MARKING DIAGRAM

Flip-Chip
CASE 499J



2441	= Specific Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week

PIN CONFIGURATION



(Bump View)

ORDERING INFORMATION

Package	Device	Shipping†
NUF2441FCT1	Flip-Chip	3000/Tape & Reel
NUF2441FCT1G	Flip-Chip (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Device	Device Marking	V_{RWM} (Volts)	V_{BR} @ 1 mA (Volts)		Max I_R @ V_{RWM} = 12 V I/O Pin (μA)	Typical Capacitance $C_1 + C_2$ (pF) (Notes 1, 3, 4)	Typical Pass-Band Inductance L (nH)	Equivalent Series Resistance R_S (Ω) (Note 2)	
			Min	Max				Typ	Max
NUF2441FCT1G	2441	12	13.7	17.7	0.1	250	2.9	0.28	0.35

1. Measured at 25°C, V_R = 0, f = 1 MHz, Source A1, GND A2, Open A3.
2. Measured at room temperature.
3. Tolerance = ±20%.
4. Measured under zero light conditions.

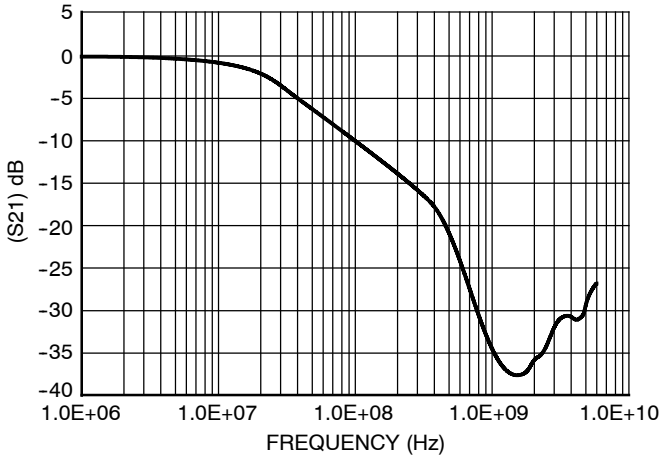


Figure 1. Insertion Loss Characteristic

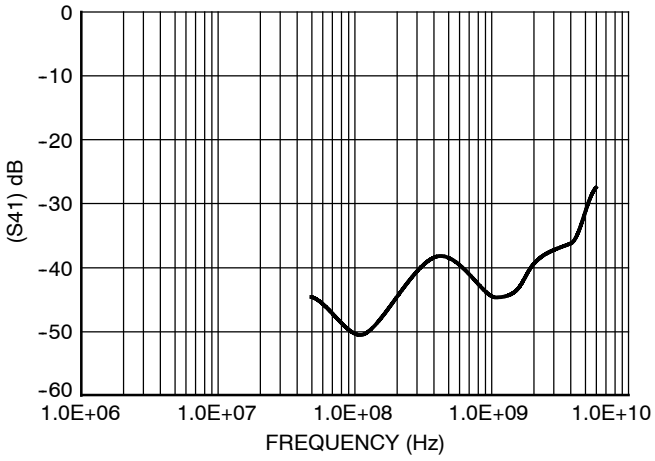


Figure 2. Analog Crosstalk

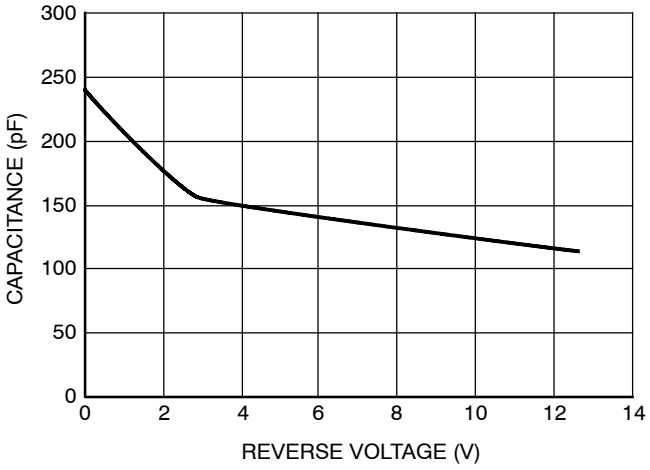


Figure 3. Typical Line Capacitance vs. Reverse Bias Voltage

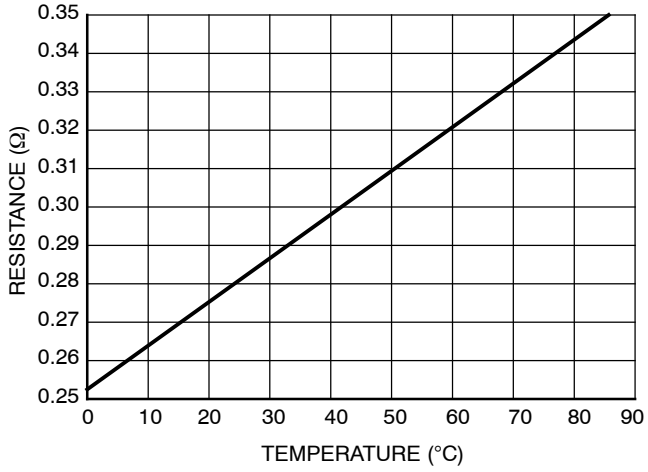


Figure 4. Typical Resistance vs. Temperature

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

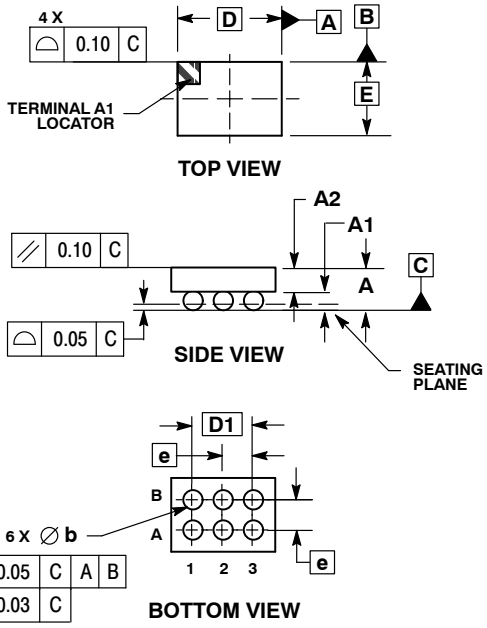
ON Semiconductor®

A1

SCALE 4:1

6 PIN FLIP−CHIP
1.72x1.22mm, 0.5 PITCH
CASE 499J−01
ISSUE O

DATE 05 FEB 2004



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.700
A1	0.210	0.270
A2	0.380	0.430
D	1.720 BSC	
E	1.220 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	1.000 BSC	

GENERIC MARKING DIAGRAM*

xx = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking.

DOCUMENT NUMBER:	**98AON13950D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**6 PIN FLIP−CHIP, 1.72x1.22mm, 0.5 PITCH**		**PAGE 1 OF 1**

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