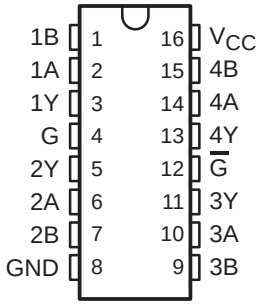
SLLS045B – JANUARY 1989 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ITU Recommendations V.10, V.11, X.26, and X.27**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **Designed to Operate Up to 20 Mbaud**
- **3-State Outputs**
- **Common-Mode Input Voltage Range – 7 V to 7 V**
- **Input Sensitivity . . . ±300 mV**
- **Input Hysteresis . . . 120 mV Typ**
- **High-Input Impedance . . . 12 kΩ Min**
- **Operates from Single 5-V Supply**
- **Low Supply-Current Requirement 35 mA Max**
- **Improved Speed and Power Consumption Compared to AM26LS32A**

D OR N PACKAGE
(TOP VIEW)



description

The SN75ALSI97 is a monolithic, quadruple line receiver with 3-state outputs designed using advanced, low-power, Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication. This, in turn, provides significantly lower power requirements and permits much higher data throughput than other designs. The device meets the specifications of ITU Recommendations V.10, V.11, X.26, and X.27. It features 3-state outputs that permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open.

The device is optimized for balanced, multipoint bus transmission at rates up to 20 megabits per second. The input features high-input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ±300 mV over a common-mode input voltage range of −7 V to 7 V. It also features active-high and active-low enable functions that are common to the four channels. The SN75ALS197 is designed for optimum performance when used with the SN75ALS192 quadruple differential line driver.

The SN75ALS197 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A – B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq 0.3$ V	H	X	H
	X	L	H
-0.3 V $< V_{ID} <$ 0.3 V	H	X	?
	X	L	?
$V_{ID} \leq -0.3$ V	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance (off)

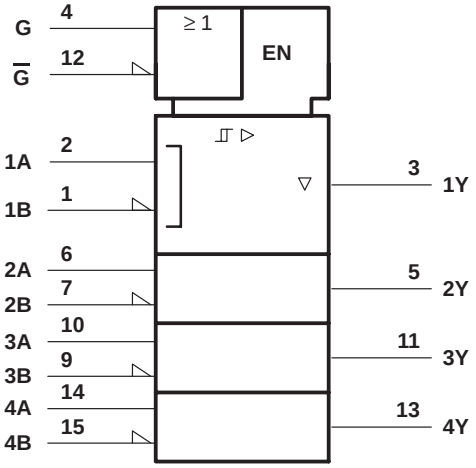
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1995, Texas Instruments Incorporated

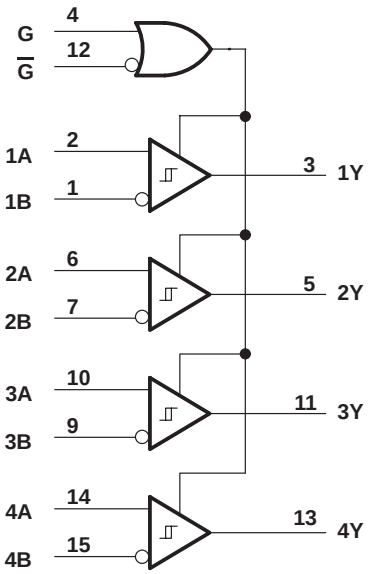
This datasheet has been downloaded from http://www.digchip.com at this page

logic symbol†

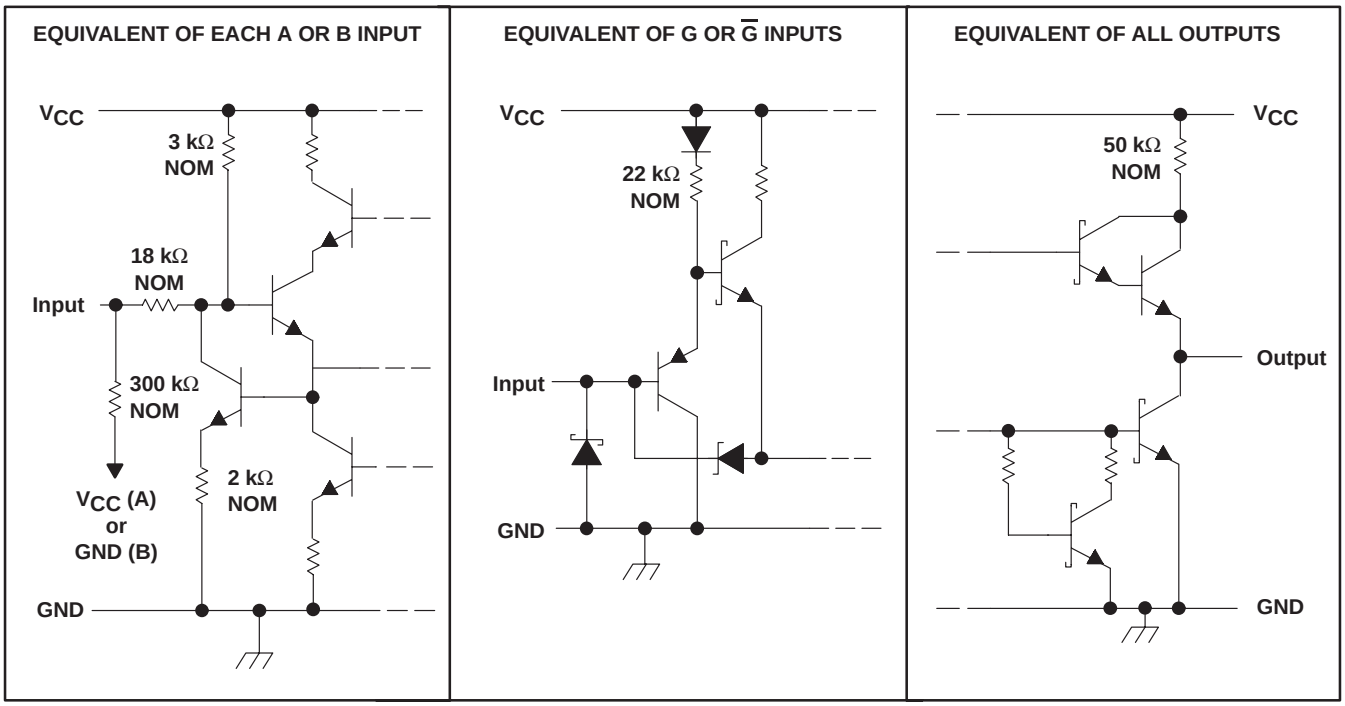


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I (A or B inputs) . . . . . ±15 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±15 V
Enable input voltage, V_I . . . . . 7 V
Low-level output current, I_{OL} . . . . . 50 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Differential input voltage, V_{ID}			±12	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			–400	µA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended range of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage					300	mV
V_{IT-}	Negative-going input threshold voltage			–300‡			mV
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)	See Figure 4			120		mV
V_{IK}	Enable-input clamp voltage	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 300 mV,	I_{OH} = – 400 µA	2.7	3.6		V
V_{OL}	Low-level output voltage	V_{ID} = – 300 mV	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_{CC} = 5.25 V	V_O = 2.4 V			20	µA
			V_{OH} = 0.4 V			–20	
I_I	Line input current	Other input at 0 V, See Note 3	V_I = 15 V		0.7	1.2	mA
			V_I = –15 V		–1.0	–1.7	
I_H	High-level enable-input current		V_{IH} = 2.7 V			20	µA
			V_{IH} = 5.25 V			100	
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				–100	µA
	Input resistance			12	18		kΩ
I_{OS}	Short-circuit output current§	V_{ID} = 3 V,	V_O = 0	–15	–78	–130	mA
I_{CC}	Supply current	Outputs disabled			22	35	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 3: Refer to ANSI Standard EIA/TIA-422-B and EIA/TIA-423-B for exact conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = – 2.5 V to 2.5 V, See Figure 2	C_L = 15 pF,		15	22	ns
t_{PHL}	Propagation delay time, high- to low-level output				15	22	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 3		13	25	ns
t_{PZL}	Output enable time to low level				11	25	
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 3		13	25	ns
t_{PLZ}	Output disable time from low level				15	22	

PARAMETER MEASUREMENT INFORMATION

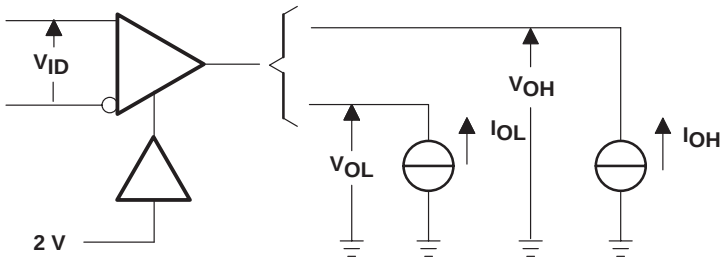
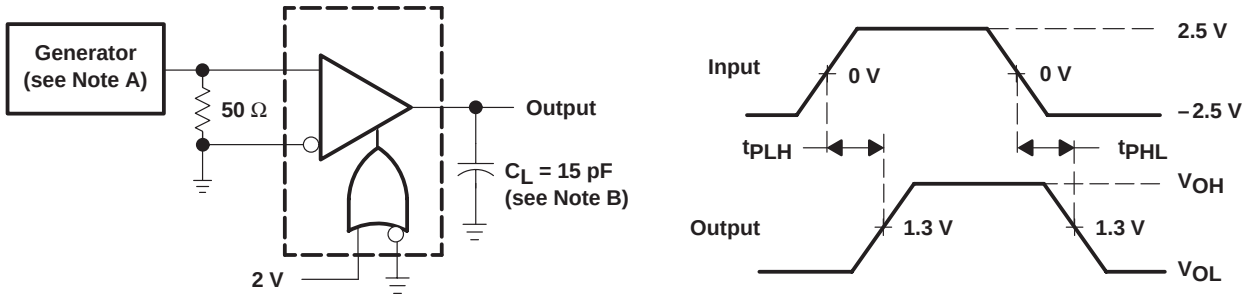


Figure 1. V_{OH} and V_{OL} Test Circuit

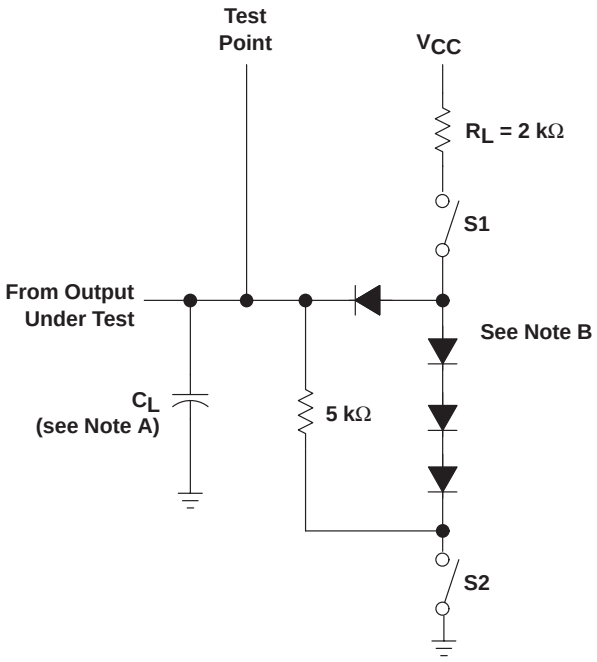


TEST CIRCUIT **VOLTAGE WAVEFORMS**

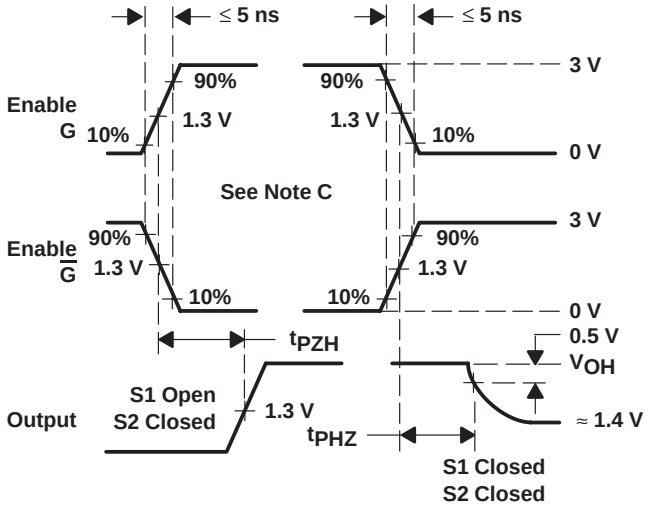
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

Figure 2. t_{PLH} and t_{PHL} Test Circuit and Voltage Waveforms

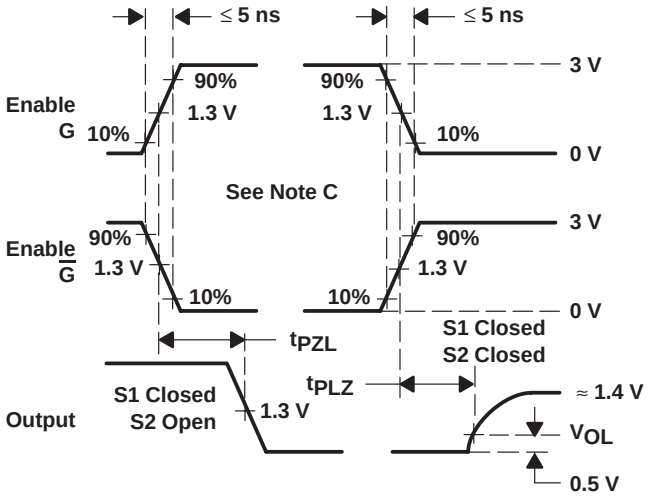
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS FOR t_{PHZ} and t_{PZH}



VOLTAGE WAVEFORMS FOR t_{PLZ} and t_{PZL}

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Enable G is tested with $\overline{G}$ high; $\overline{G}$ is tested with G low.

Figure 3. t_{PHZ}, t_{PZH}, t_{PLZ}, and t_{PZL} Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs ENABLE VOLTAGE

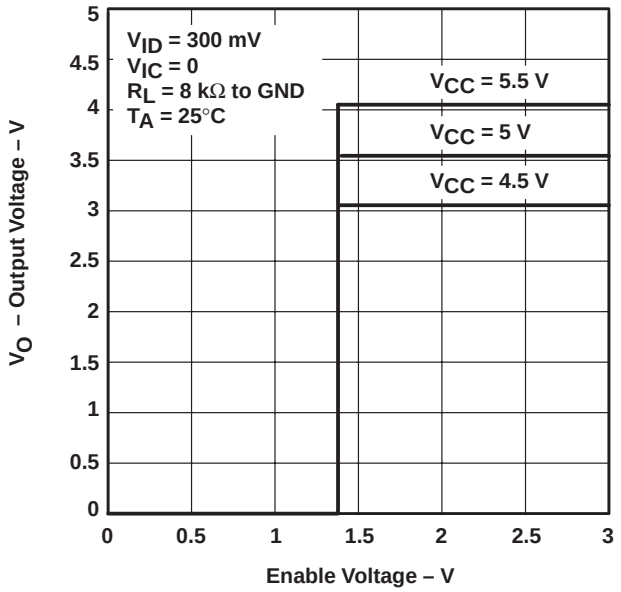


Figure 4

OUTPUT VOLTAGE vs ENABLE VOLTAGE

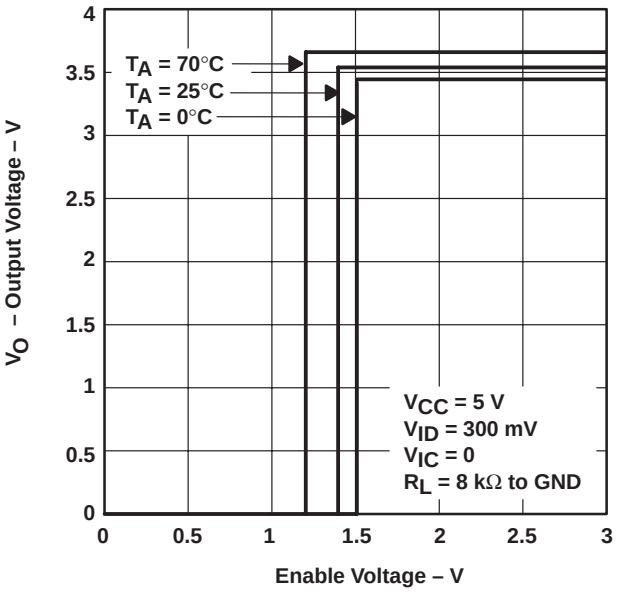


Figure 5

OUTPUT VOLTAGE vs ENABLE VOLTAGE

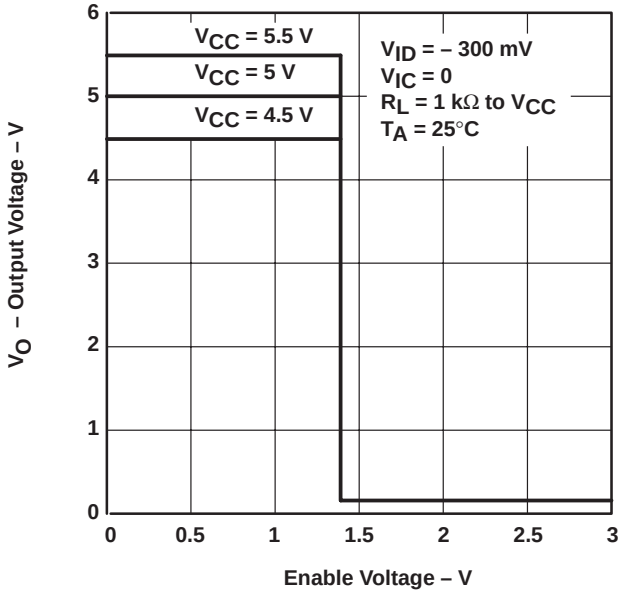


Figure 6

OUTPUT VOLTAGE vs ENABLE VOLTAGE

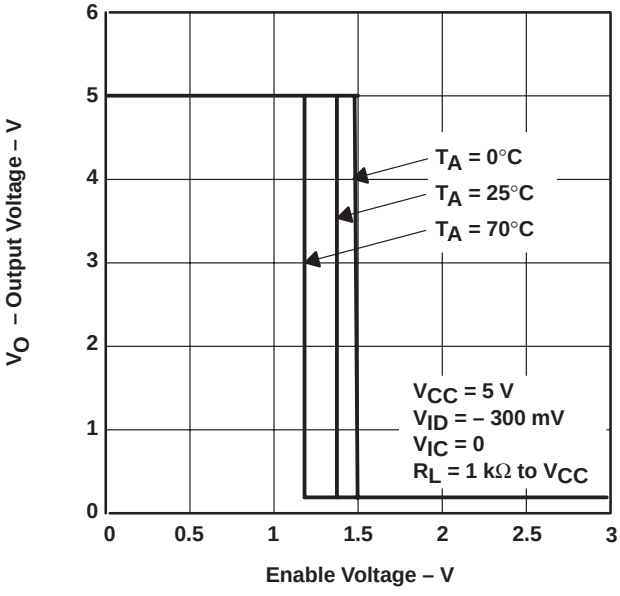


Figure 7

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

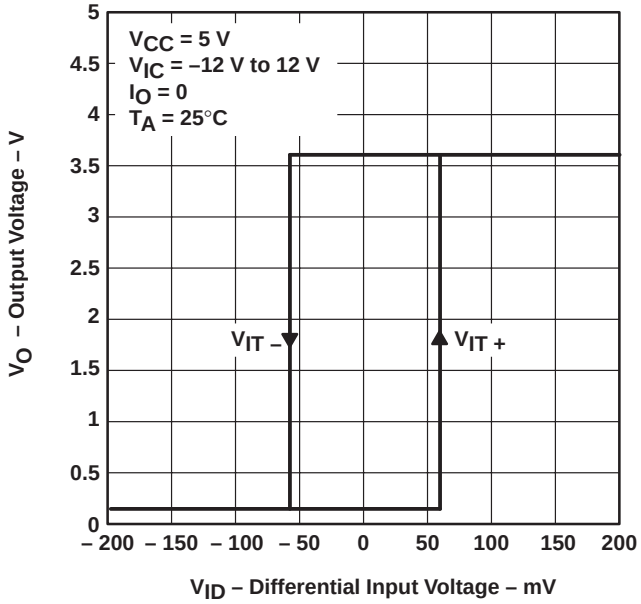


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

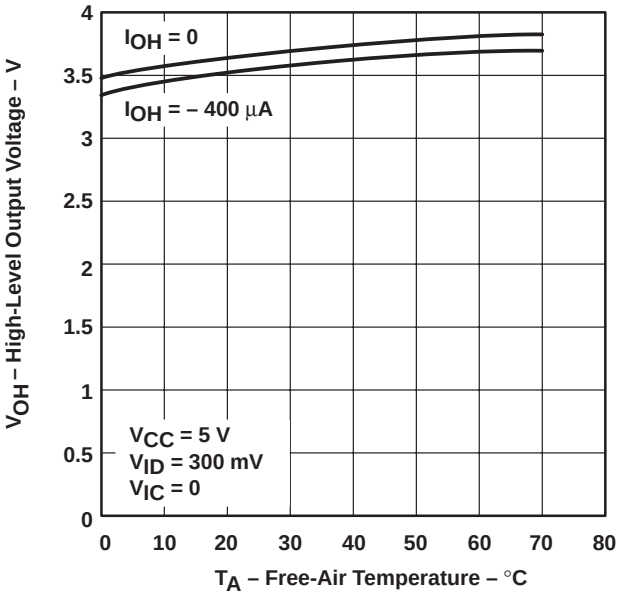


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

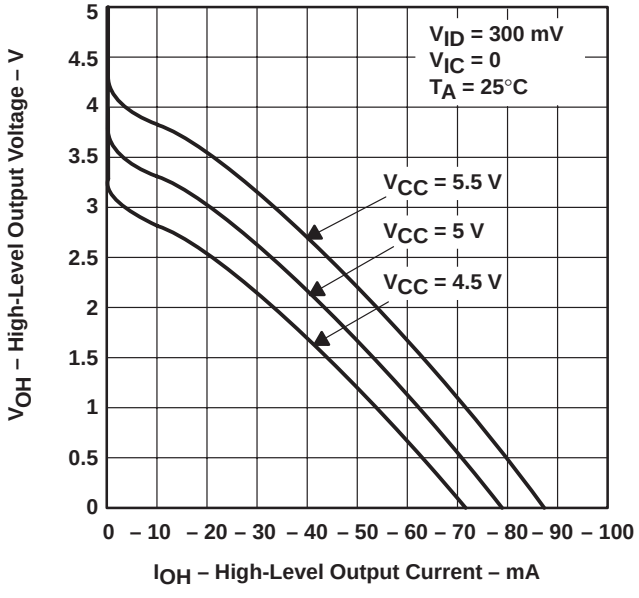


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

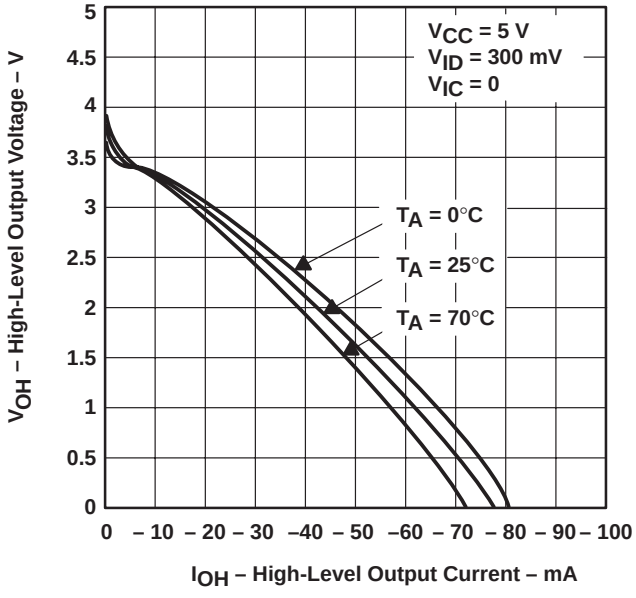


Figure 11

TYPICAL CHARACTERISTICS

**LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE**

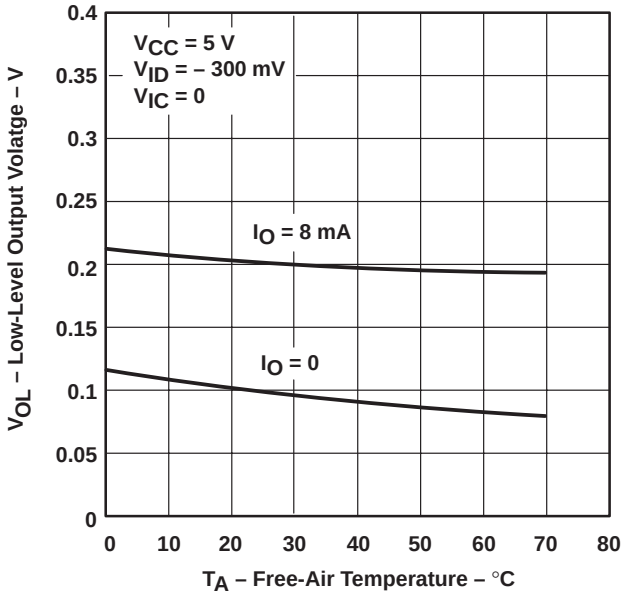


Figure 12

**LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

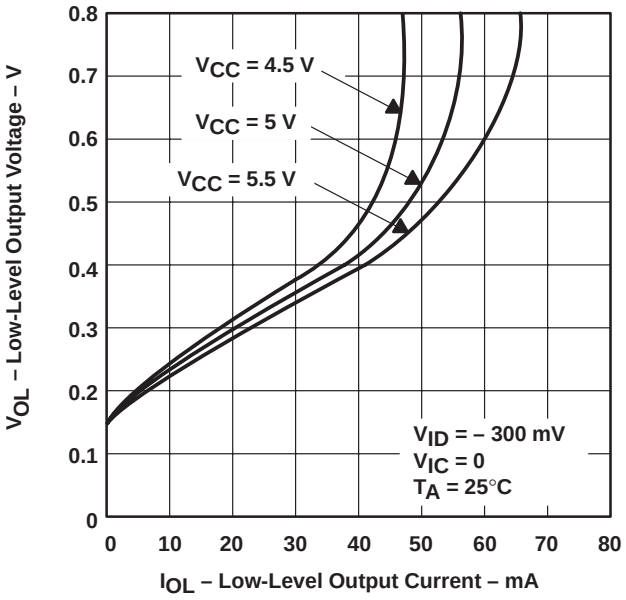


Figure 13

**LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

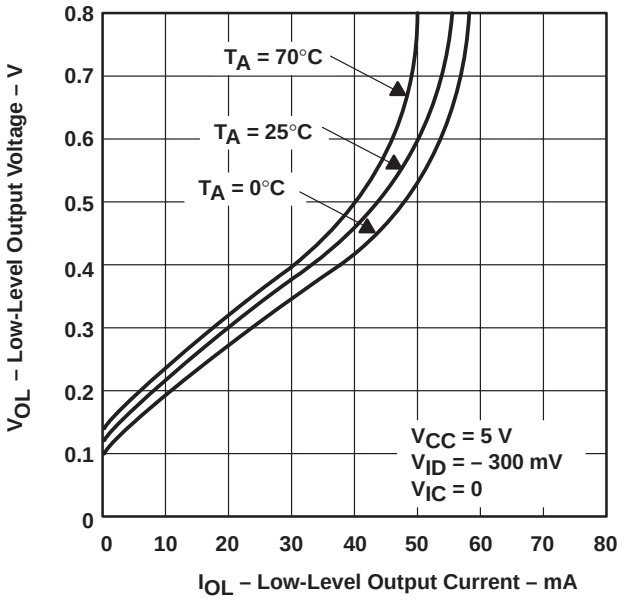


Figure 14

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

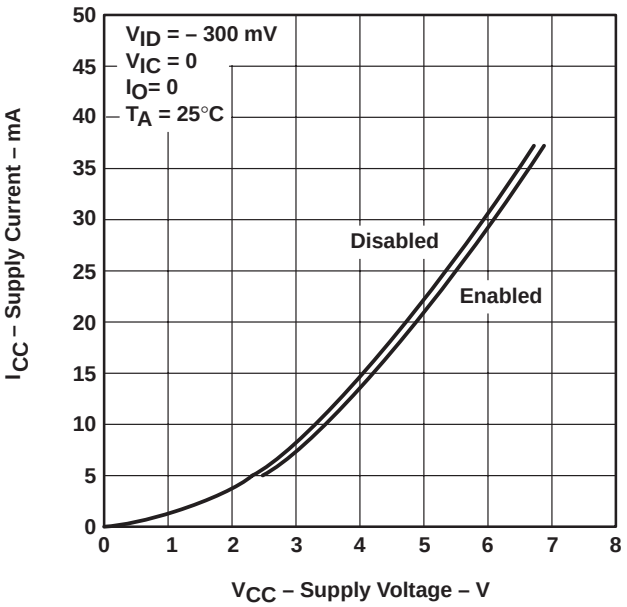


Figure 15

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

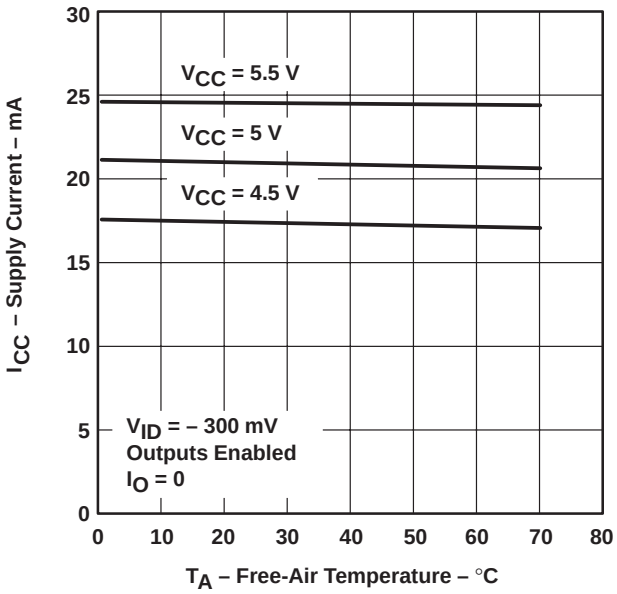


Figure 16

SUPPLY CURRENT vs DIFFERENTIAL INPUT VOLTAGE

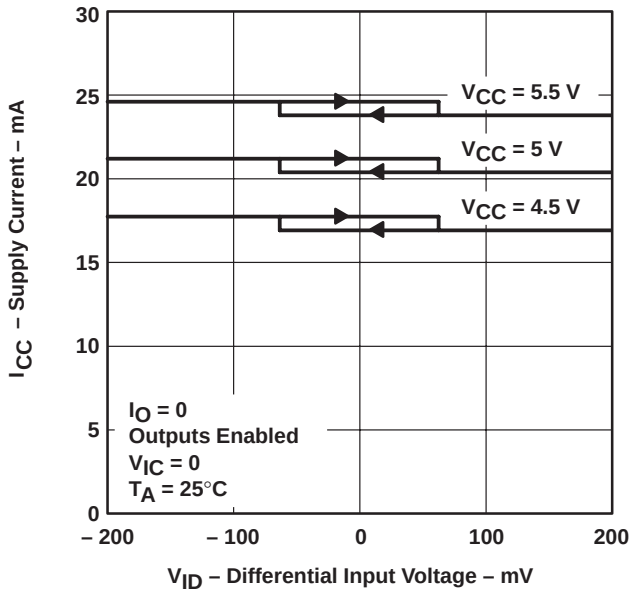


Figure 17

SUPPLY CURRENT vs FREQUENCY

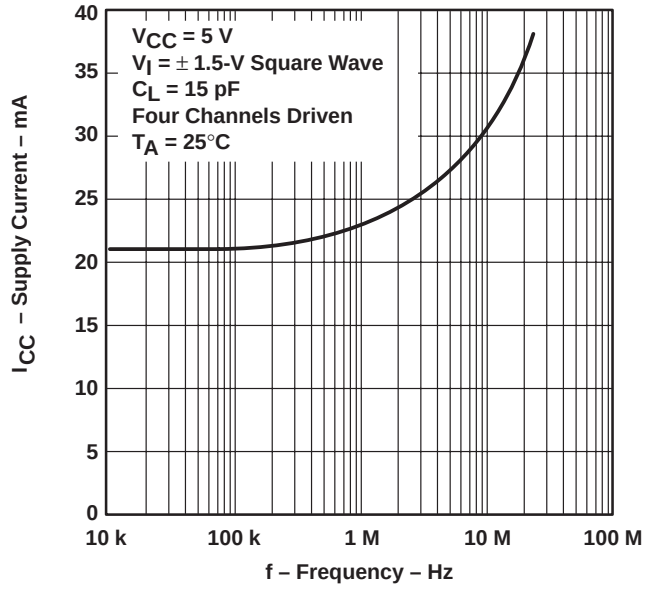


Figure 18

TYPICAL CHARACTERISTICS

INPUT RESISTANCE vs FREE-AIR TEMPERATURE

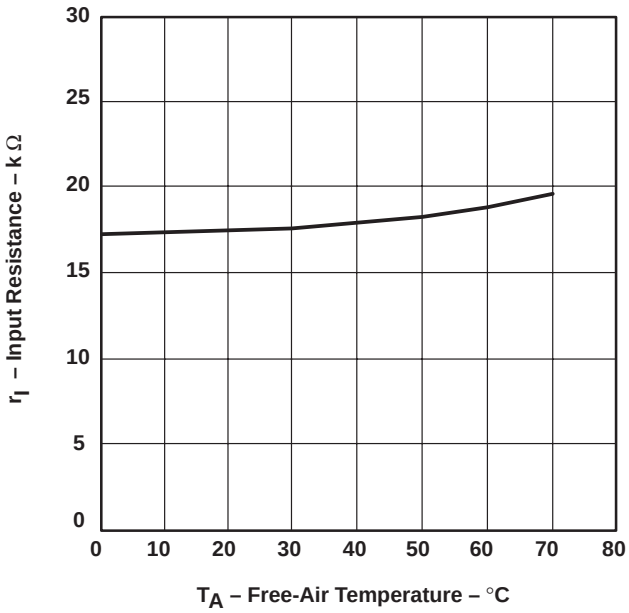


Figure 19

INPUT CURRENT vs INPUT VOLTAGE TO GND

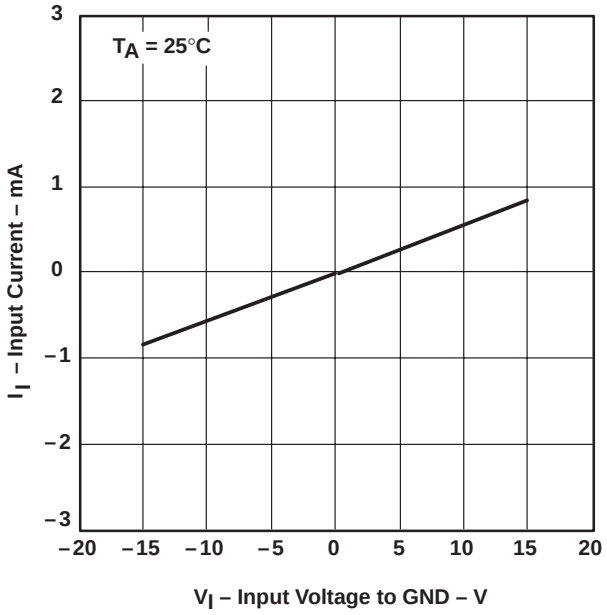


Figure 20

SWITCHING TIME vs FREE-AIR TEMPERATURE

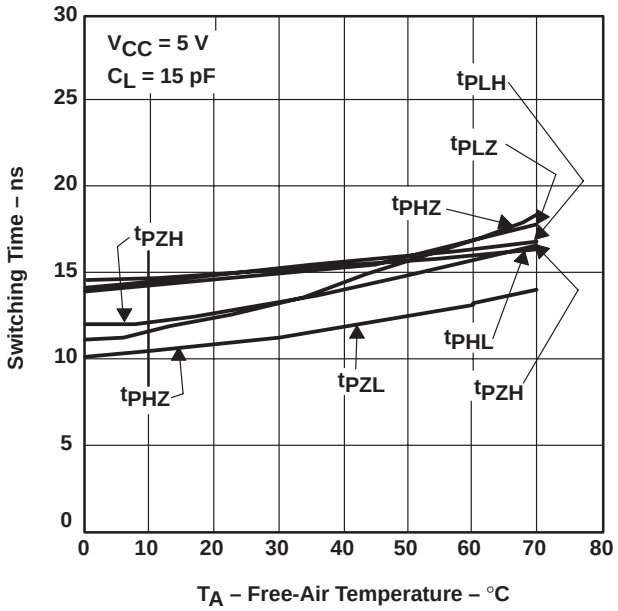


Figure 21

PROPAGATION DELAY TIME vs SUPPLY VOLTAGE

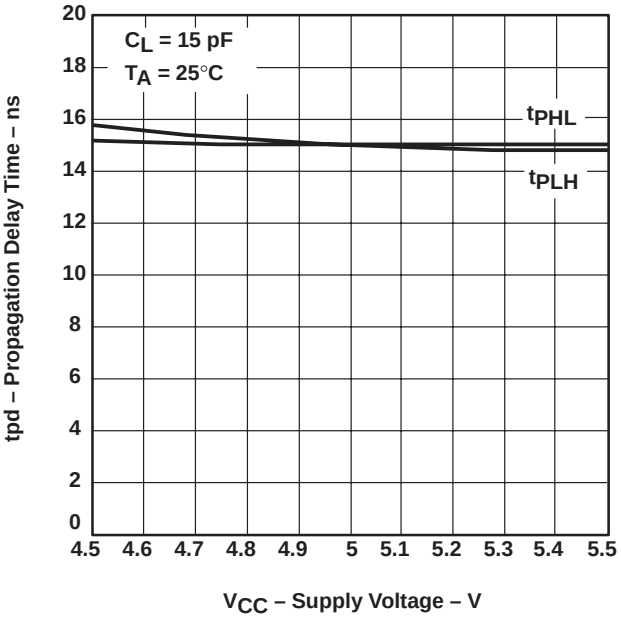


Figure 22

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 1998, Texas Instruments Incorporated