NTR4171P

Power MOSFET

−30 V, −3.5 A, Single P−Channel, SOT−23

Features

- Low $R_{DS(on)}$ at Low Gate Voltage
- Low Threshold Voltage
- High Power and Current Handling Capability
- This is a Pb−Free Device

Applications

- Load Switch
- Optimized for Battery and Load Management Applications in Portable Equipment like Cell Phones, PDA's, Media Players, etc.

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	−30	V
Gate−to−Source Voltage			V_{GS}	±12	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	−2.2	A
		T_A = 85°C		−1.5	
	t ≤ 5 s	T_A = 25°C		−3.5	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	0.48	W
	t ≤ 5 s			1.25	
Pulsed Drain Current	t_p = 10 μs		I_{DM}	−15.0	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to 150	°C
Source Current (Body Diode)			I_S	−1.0	A
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	260	°C/W
Junction−to−Ambient − t ≤ 10 s (Note 1)	$R_{\theta JA}$	100	

1. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)

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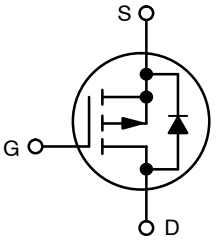
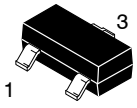
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
−30 V	75 mΩ @ −10 V	−2.2 A
	110 mΩ @ −4.5 V	−1.8 A
	150 mΩ @ −2.5 V	−1.0 A

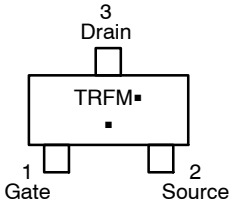
P−CHANNEL MOSFET





SOT−23
CASE 318
STYLE 21

MARKING DIAGRAM/ PIN ASSIGNMENT



TRF = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTR4171PT1G	SOT−23 (Pb−Free)	3000/Tape & Reel
NTR4171PT3G	SOT−23 (Pb−Free)	10000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 μA	−30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}$ /T_J	I_D = −250 μA, Reference to 25°C		24		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −24 V, T_J = 25°C V_{GS} = 0 V, V_{DS} = −24 V, T_J = 85°C			−1.0 −5.0	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±12 V			±0.1	μA
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = −250 μA	−0.7	−1.15	−1.4	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}$/T_J			3.5		mV/°C
Drain−to−Source On−Resistance	$R_{DS(on)}$	V_{GS} = −10 V, I_D = −2.2 A		50	75	mΩ
		V_{GS} = −4.5 V, I_D = −1.8 A		60	110	
		V_{GS} = −2.5 V, I_D = −1.0 A		90	150	
Forward Transconductance	g_{FS}	V_{DS} = −5.0 V, I_D = −2.2 A		7.0		S
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = −15 V		720		pF
Output Capacitance	C_{oss}			95		
Reverse Transfer Capacitance	C_{rss}			65		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −10 V, V_{DS} = −15 V, I_D = −3.5 A		15.6		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.7		
Gate−to−Source Charge	Q_{GS}			1.6		
Gate−to−Drain Charge	Q_{GD}			2.6		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −4.5 V, V_{DS} = −15 V, I_D = −3.5 A		7.4		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.7		
Gate−to−Source Charge	Q_{GS}			1.6		
Gate−to−Drain Charge	Q_{GD}			2.6		
Gate Resistance	R_G			6.1		Ω
SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V (Note 4)						
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = −10 V, V_{DS} = −15 V, I_D = −3.5 A, R_G = 6 Ω		8.0		ns
Rise Time	t_r			11		
Turn−Off Delay Time	$t_{d(off)}$			32		
Fall Time	t_f			14		
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = −4.5 V, V_{DS} = −15 V, I_D = −3.5 A, R_G = 6 Ω		9.0		ns
Rise Time	t_r			16		
Turn−Off Delay Time	$t_{d(off)}$			25		
Fall Time	t_f			22		
DRAIN−SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = −1.0 A, T_J = 25°C		−0.8	−1.2	V
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, I_S = −1.0 A, dI_{SD}/d_t = 100 A/μs		14		ns
Charge Time	t_a			10		
Discharge Time	t_b			4.0		
Reverse Recovery Charge	Q_{RR}			8.0		nC

2. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%
4. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

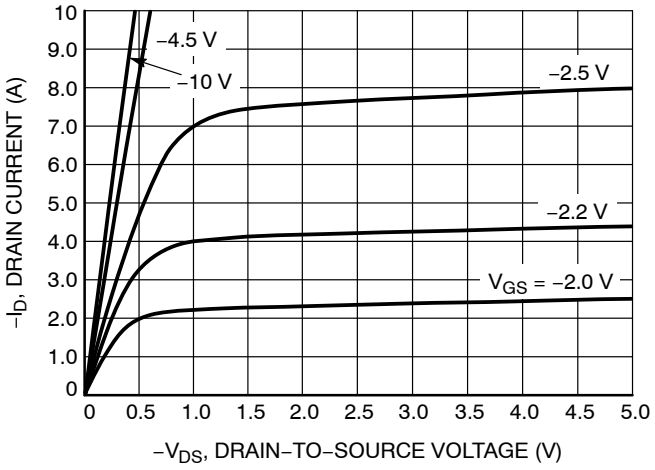


Figure 1. On−Region Characteristics

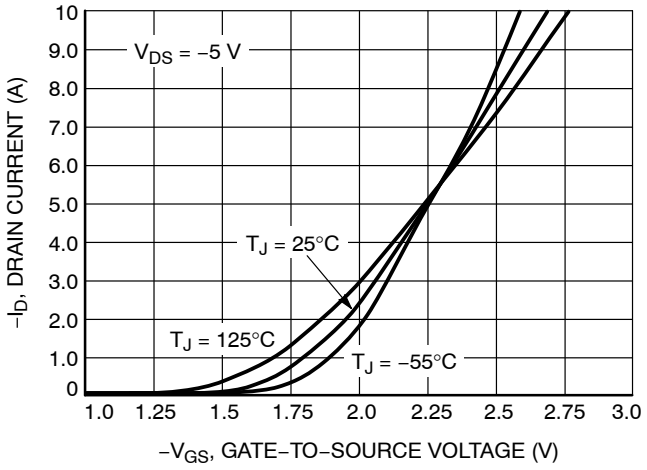


Figure 2. Transfer Characteristics

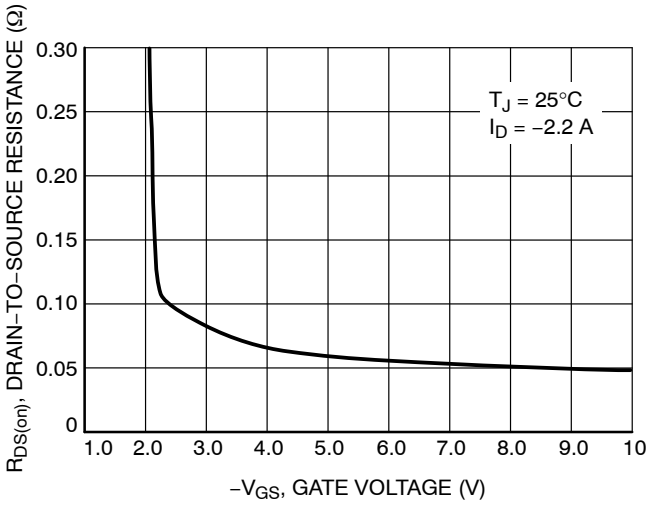


Figure 3. On−Resistance vs. Gate−to−Source Voltage

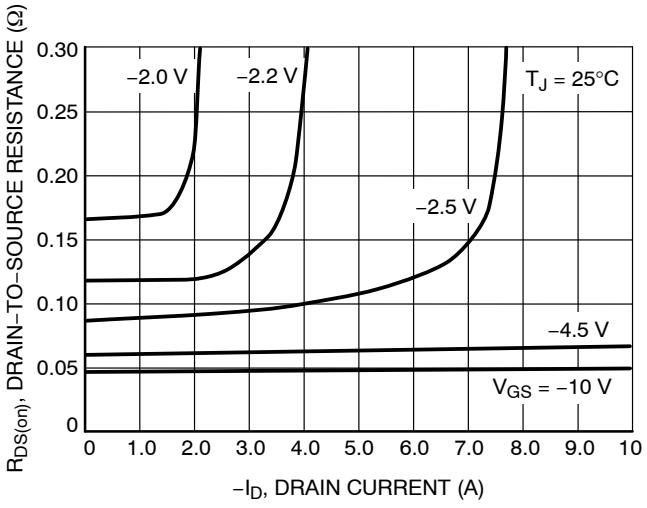


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

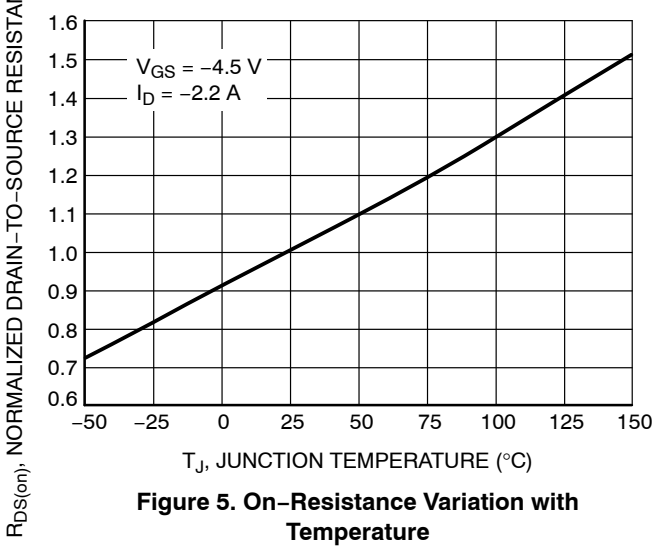


Figure 5. On−Resistance Variation with Temperature

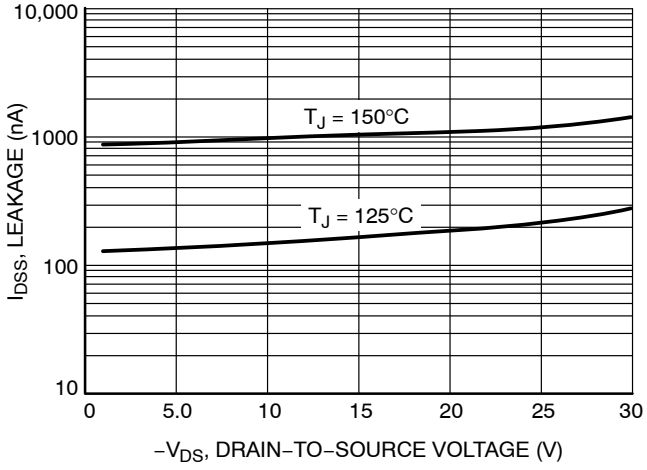


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

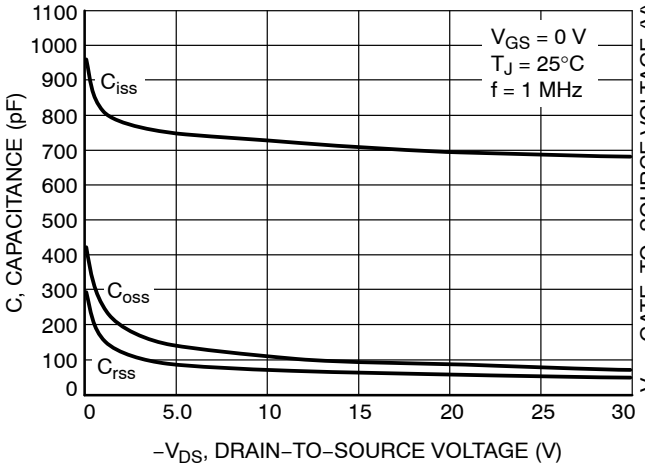


Figure 7. Capacitance Variation

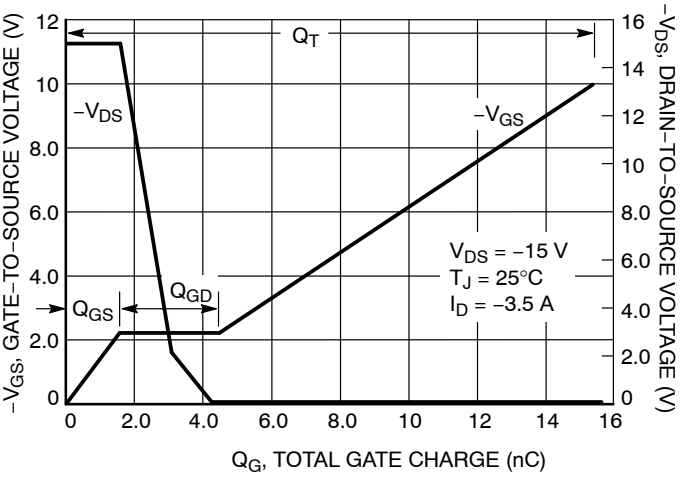


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

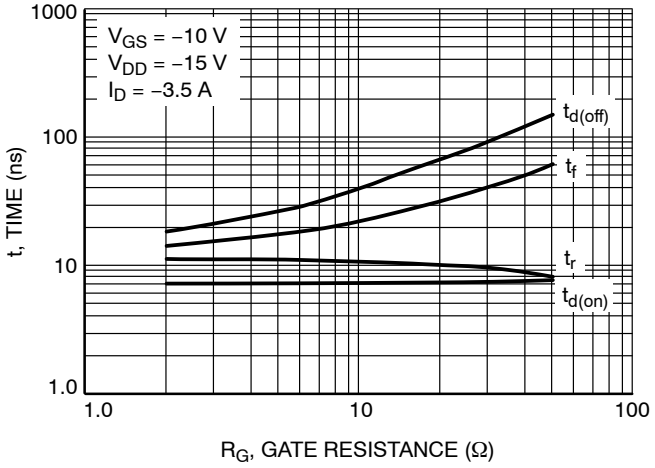


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

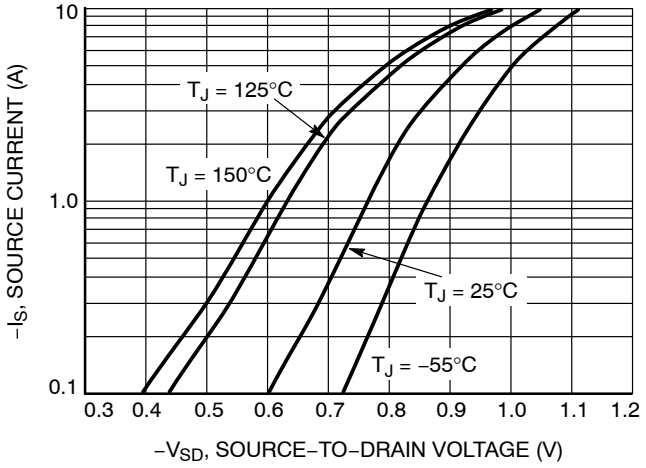


Figure 10. Diode Forward Voltage vs. Current

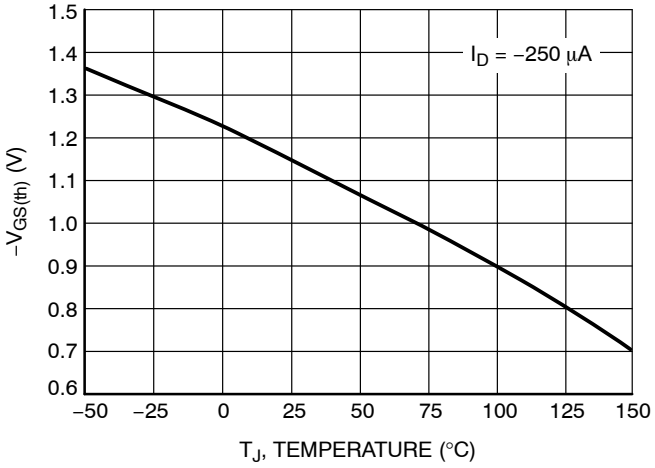


Figure 11. Threshold Voltage

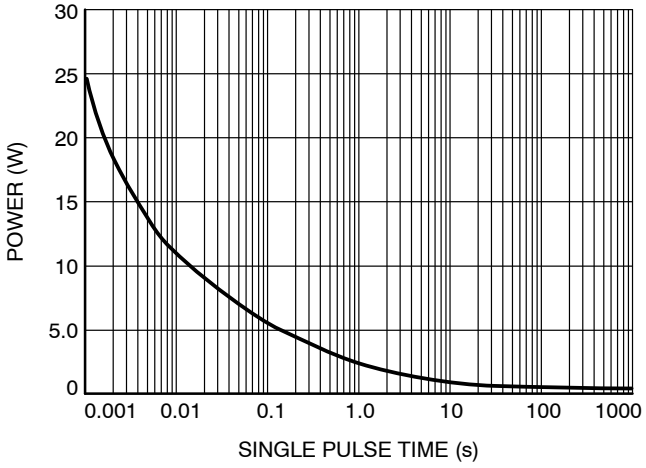


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS

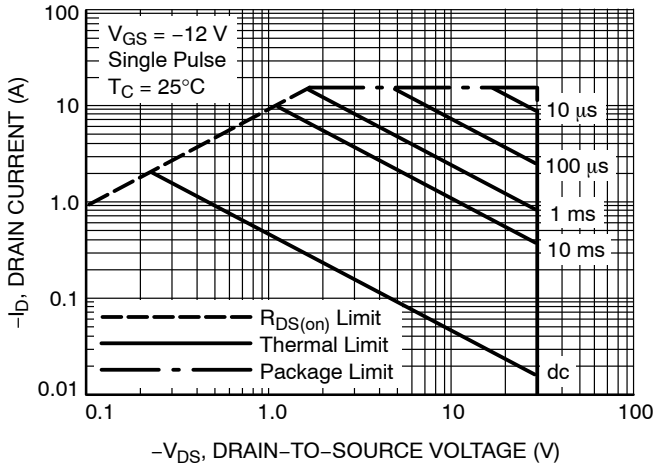


Figure 13. Maximum Rated Forward Biased Safe Operating Area

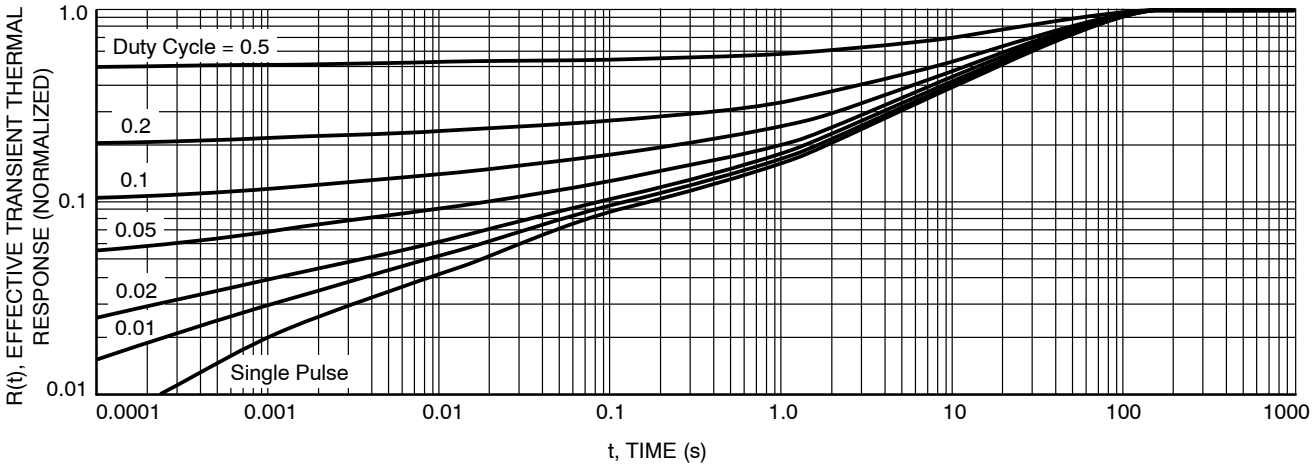
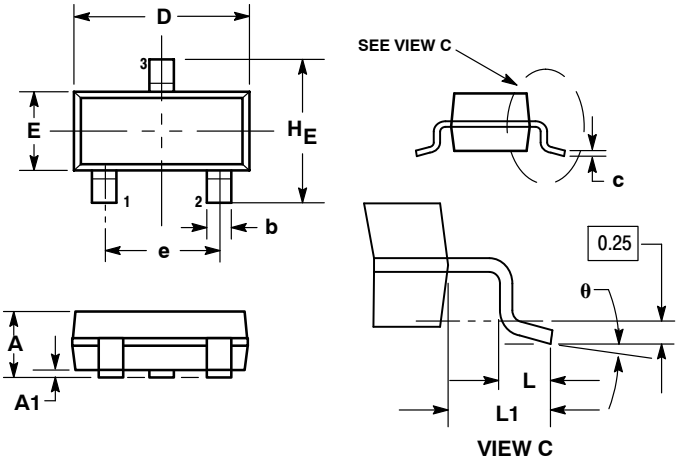


Figure 14. FET Thermal Response

PACKAGE DIMENSIONS

SOT−23 (TO−236)
CASE 318−08
ISSUE AP

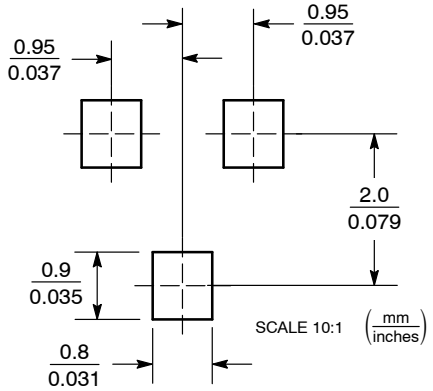


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104
θ	0°	−−−	10°	0°	−−−	10°

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

SOLDERING FOOTPRINT



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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