MC74AC125, MC74ACT125

Quad 3-state Buffer with Low Enable

High−Performance Silicon−Gate CMOS

ON Semiconductor®

Features

- Outputs Source/Sink
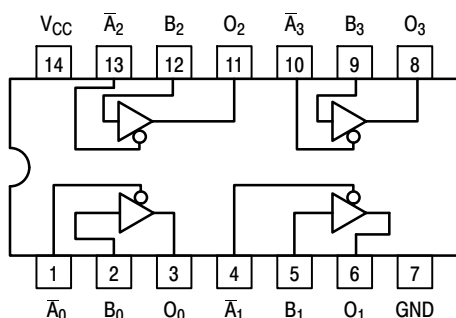- ′ACT125 Has TTL Compatible Inputs
- These are Pb−Free Devices

Figure 1. Pinout: 14−Lead Packages Conductors
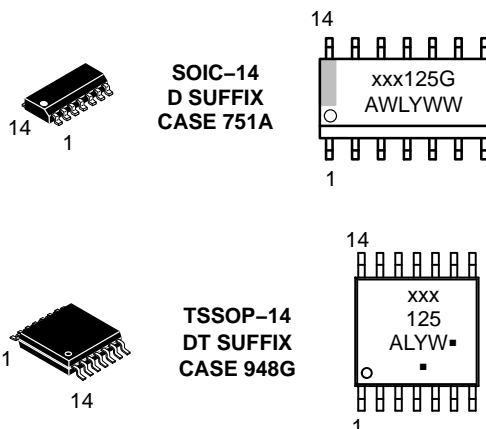(Top View)

PIN ASSIGNMENT

PIN	FUNCTION
$\overline{A}_n$, B_n	Inputs
O_n	Outputs

FUNCTION TABLE

Inputs		Output
$\overline{A}_n$	B_n	O_n
L	L	L
L	H	H
H	X	Z

NOTE: H = High Voltage Level;
        L = Low Voltage Level;
        Z = High Impedance;
        X = Immaterial

MARKING DIAGRAMS

SOIC−14
D SUFFIX
CASE 751A

xxx125G
AWLYWW

TSSOP−14
DT SUFFIX
CASE 948G

xxx
125
ALYW■

xxx	= AC or ACT
A	= Assembly Location
WL or L	= Wafer Lot
Y	= Year
WW or W	= Work Week
G or ■	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MC74AC125, MC74ACT125

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		-0.5 to $+7.0$	V
V_I	DC Input Voltage		$-0.5 \leq V_I \leq V_{CC} +0.5$	V
V_O	DC Output Voltage	(Note 1)	$-0.5 \leq V_O \leq V_{CC} +0.5$	V
I_{IK}	DC Input Diode Current		± 20	mA
I_{OK}	DC Output Diode Current		± 50	mA
I_O	DC Output Sink/Source Current		± 50	mA
I_{CC}	DC Supply Current per Output Pin		± 50	mA
I_{GND}	DC Ground Current per Output Pin		± 50	mA
T_{STG}	Storage Temperature Range		-65 to $+150$	°C
T_L	Lead temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction temperature under Bias		$+150$	°C
θ_{JA}	Thermal Resistance (Note 2)	SOIC TSSOP	125 170	°C/W
P_D	Power Dissipation in Still Air at 85°C	SOIC TSSOP	125 170	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating Oxygen Index: 30% – 35%		UL 94 V–0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)		> 2000 > 200 > 1000	V
$I_{Latch-Up}$	Latch–Up Performance Above V_{CC} and Below GND at 85°C (Note 6)		± 100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. I_O absolute maximum rating must be observed.
2. The package thermal impedance is calculated in accordance with JESD51–7.
3. Tested to EIA/JESD22–A114–A.
4. Tested to EIA/JESD22–A115–A.
5. Tested to JESD22–C101–A.
6. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	'AC	2.0	5.0	6.0	V
		'ACT	4.5	5.0	5.5	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Ref. to GND)		0	–	V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V_{CC} @ 3.0 V	–	150	–	ns/V
		V_{CC} @ 4.5 V	–	40	–	
		V_{CC} @ 5.5 V	–	25	–	
T_J	Junction Temperature (PDIP)		–	–	140	°C
T_A	Operating Ambient Temperature Range		–40	25	85	°C
I_{OH}	Output Current – HIGH		–	–	–24	mA
I_{OL}	Output Current – LOW		–	–	24	mA

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$	74AC $T_A = -40°C$ to $+85°C$	Unit	Conditions
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	V	$V_{OUT} = 0.1$ V or $V_{CC} - 0.1$ V
V_{IL}	Maximum Low Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	V	$V_{OUT} = 0.1$ V or $V_{CC} - 0.1$ V
V_{OH}	Minimum High Level Output Voltage	3.0 4.5 5.5	2.99 4.46 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V	$I_{OUT} = -50$ μA
		3.0 4.5 5.5	– – –	2.56 3.86 4.86	2.46 3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −12 mA − 24 mA − 24 mA
V_{OL}	Minimum Low Level Output Voltage	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V	$I_{OUT} = 50$ μA
		3.0 4.5 5.5	– – –	0.36 0.36 0.36	0.44 0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 12 mA 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	V_I (OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND	5.5	–	±0.5	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5	–	–	75	mA	$V_{OLD} = 1.65$ V Max
I_{OHD}		5.5	–	–	−75	mA	$V_{OHD} = 3.85$ V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	–	8.0	80	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one input loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V.

AC CHARACTERISTICS

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Unit
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Data to Output	3.3 5.0	1.0 1.0	9.0 7.0	1.0 1.0	10 7.5	ns
t_{PHL}	Propagation Delay Data to Output	3.3 5.0	1.0 1.0	9.0 7.0	1.0 1.0	10 7.5	ns
t_{PZH}	Output Enable Time	3.3 5.0	1.0 1.0	10.5 7.0	1.0 1.0	11 8.0	ns
t_{PZL}	Output Enable Time	3.3 5.0	1.0 1.0	10 8.0	1.0 1.0	11 8.5	ns
t_{PHZ}	Output Disable Time	3.3 5.0	1.0 1.0	10 9.0	1.0 1.0	10.5 9.5	ns
t_{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	10.5 9.0	1.0 1.0	11.5 9.5	ns

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
  Voltage Range 5.0 V is 5.0 V ±0.5 V.

DC CHARACTERISTICS

Symbol	Parameter	V$_{CC}$ (V)	74ACT T$_A$ = +25°C		74ACT T$_A$ = −40°C to +85°C	Unit	Conditions
			Typ	Guaranteed Limits			
V$_{IH}$	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.2 2.0	2.0 2.0	V	V$_{OUT}$ = 0.1 V or V$_{CC}$ − 0.1 V
V$_{IL}$	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V$_{OUT}$ = 0.1 V or V$_{CC}$ − 0.1 V
V$_{OH}$	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I$_{OUT}$ = − 50 μA
		4.5 5.5	− −	3.86 4.86	3.76 4.76	V	*V$_{IN}$ = V$_{IL}$ or V$_{IH}$ − 24 mA I$_{OH}$ − 24 mA
V$_{OL}$	Minimum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I$_{OUT}$ = − 50 μA
		4.5 5.5	− −	0.36 0.36	0.44 0.44	V	*V$_{IN}$ = V$_{IL}$ or V$_{IH}$ I$_{OH}$ − 24 mA − 24 mA
I$_{IN}$	Maximum Input Leakage Current	5.5	−	±0.1	±1.0	μA	V$_I$ = V$_{CC}$, GND
I$_{OZ}$	V$_I$ (OE) = V$_{IL}$, V$_{IH}$ V$_I$ = V$_{CC}$, GND V$_O$ = V$_{CC}$, GND	5.5	−	±0.5	±5.0	μA	V$_I$ (OE) = V$_{IL}$, V$_{IH}$ V$_I$ = V$_{CC}$, GND V$_O$ = V$_{CC}$, GND
ΔI$_{CCT}$	Additional Max. I$_{CC}$/Input	5.5	0.6	−	1.5	mA	V$_I$ = V$_{CC}$ − 2.1 V
I$_{OLD}$	†Minimum Dynamic Output Current	5.5	−	−	75	mA	V$_{OLD}$ = 1.65 V Max
I$_{OHD}$		5.5	−	−	−75	mA	V$_{OHD}$ = 3.85 V Min
I$_{CC}$	Maximum Quiescent Supply Current	5.5	−	8.0	80	μA	V$_{IN}$ = V$_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one input loaded at a time.

AC CHARACTERISTICS

Symbol	Parameter	V$_{CC}$* (V)	74ACT T$_A$ = +25°C C$_L$ = 50 pF		74ACT T$_A$ = −40°C to +85°C C$_L$ = 50 pF		Unit
			Min	Max	Min	Max	
t$_{PLH}$	Propagation Delay Data to Output	5.0	1.0	9.0	1.0	10	ns
t$_{PHL}$	Propagation Delay Data to Output	5.0	1.0	9.0	1.0	10	ns
t$_{PZH}$	Output Enable Time	5.0	1.0	8.5	1.0	9.5	ns
t$_{PZL}$	Output Enable Time	5.0	1.0	9.5	1.0	10.5	ns
t$_{PHZ}$	Output Disable Time	5.0	1.0	9.5	1.0	10.5	ns
t$_{PLZ}$	Output Disable Time	5.0	1.0	10	1.0	10.5	ns

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C$_{IN}$	Input Capacitance	4.5	pF	V$_{CC}$ = 5.0 V
C$_{PD}$	Power Dissipation Capacitance	45	pF	V$_{CC}$ = 5.0 V

ORDERING INFORMATION

Device	Package	Shipping†
MC74AC125DG	SOIC−14 (Pb−Free)	55 Units / Rail
MC74AC125DR2G		2500 / Tape & Reel
MC74AC125DTR2G	TSSOP−14 (Pb−Free)	2500 / Tape & Reel
MC74ACT125DR2G	SOIC−14 (Pb−Free)	2500 / Tape & Reel
MC74ACT125DTR2G	TSSOP−14 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

14

1

SCALE 1:1

DETAIL A

A3

L

DETAIL A

h

X 45°

M

⊕ 0.25 Ⓜ B Ⓜ

13X b

⊕ 0.25 Ⓜ C A Ⓢ B Ⓢ

⌓ 0.10

e

A

A1

Ⓒ SEATING PLANE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

SOLDERING FOOTPRINT*

6.50

14X
1.18

1

1.27
PITCH

14X
0.58

DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*

14

XXXXXXXXXG
AWLYWW

1

XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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DESCRIPTION:	SOIC−14 NB		PAGE 1 OF 2

SOIC−14
CASE 751A−03
ISSUE L

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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DESCRIPTION:	SOIC−14 NB		PAGE 2 OF 2

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

14

SCALE 2:1

1

14X **K** REF

⊕ | 0.10 (0.004) Ⓜ | T | U Ⓢ | V Ⓢ

⌓ | 0.15 (0.006) | T | U Ⓢ

2X L/2

L

PIN 1
IDENT.

14

8

B
−U−

1

7

A
−V−

⌓ | 0.15 (0.006) | T | U Ⓢ

N

0.25 (0.010)

M

N

F

DETAIL E

K

K1

J J1

SECTION N−N

C

⌓ | 0.10 (0.004)
−T− SEATING
PLANE

D

G

H

DETAIL E

−W−

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

**GENERIC
MARKING DIAGRAM***

14

XXXX
XXXX
ALYW▪

○   ▪

1

A   = Assembly Location
L   = Wafer Lot
Y   = Year
W   = Work Week
▪   = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

SOLDERING FOOTPRINT

7.06

1

0.65
PITCH

14X
0.36

14X
1.26

DIMENSIONS: MILLIMETERS

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DESCRIPTION:	**TSSOP−14 WB**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

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