PCA9633

4-bit Fm+ I^2C-bus LED driver

Rev. 6.0 — 19 January 2023 **Product data sheet**

1 General description

The PCA9633 is an I^2C-bus controlled 4-bit LED driver optimized for Red/Green/Blue/Amber (RGBA) color mixing applications. Each LED output has its own 8-bit resolution (256 steps) fixed frequency Individual PWM controller that operates at 97 kHz with a duty cycle that is adjustable from 0 % to 99.6 % to allow the LED to be set to a specific brightness value. A fifth 8-bit resolution (256 steps) Group PWM controller has both a fixed frequency of 190 Hz and an adjustable frequency between 24 Hz to once every 10.73 seconds with a duty cycle that is adjustable from 0 % to 99.6 % that is used to either dim or blink all LEDs with the same value.

Each LED output can be off, on (no PWM control), set at its Individual PWM controller value or at both Individual and Group PWM controller values. The LED output driver is programmed to be either open-drain with a 25 mA current sink capability at 5 V or totem pole with a 25 mA sink, 10 mA source capability at 5 V. The PCA9633 operates with a supply voltage range of 2.3 V to 5.5 V and the outputs are 5.5 V tolerant. LEDs can be directly connected to the LED output (up to 25 mA, 5.5 V) or controlled with external drivers and a minimum amount of discrete components for larger current or higher voltage LEDs.

The PCA9633 is one of the first LED controller devices in a new Fast-mode Plus (Fm+) family. Fm+ devices offer higher frequency (up to 1 MHz) and more densely populated bus operation (up to 4000 pF).

The active LOW Output Enable input pin ($\overline{OE}$) allows asynchronous control of the LED outputs and can be used to set all the outputs to a defined I^2C-bus programmable logic state. The $\overline{OE}$ can also be used to externally PWM the outputs, which is useful when multiple devices need to be dimmed or blinked together using software control. This feature is available for the 16-pin version only.

Software programmable LED Group and three Sub Call I^2C addresses allow all or defined groups of PCA9633 devices to respond to a common I^2C address, allowing for example, all red LEDs to be turned on or off at the same time or marquee chasing effect, thus minimizing I^2C-bus commands.

The PCA9633 is offered with 3 different I^2C-bus address options: fixed I^2C-bus address (8-pin version), 4 different I^2C-bus addresses from 2 programmable address pins (10-pin version), and 126 different I^2C-bus addresses from 7 programmable address pins (16-pin version). They are software identical except for the different number of address combinations.

The Software Reset (SWRST) Call allows the controller to perform a reset of the PCA9633 through the I^2C-bus, identical to the Power-On Reset (POR) that initializes the registers to their default state causing the outputs to be set HIGH (LED off). This allows an easy and quick way to reconfigure all device registers to the same condition.

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2 Features

- 4 LED drivers. Each output programmable at:
  - Off
  - On
  - Programmable LED brightness
  - Programmable group dimming/blinking mixed with individual LED brightness
- 1 MHz Fast-mode Plus I²C-bus interface with 30 mA high drive capability on SDA output for driving high capacitive buses
- 256-step (8-bit) linear programmable brightness per LED output varying from fully off (default) to maximum brightness using a 97 kHz PWM signal
- 256-step group brightness control allows general dimming (using a 190 Hz PWM signal) from fully off to maximum brightness (default)
- 256-step group blinking with frequency programmable from 24 Hz to 10.73 s and duty cycle from 0 % to 99.6 %
- Four totem pole outputs (sink 25 mA and source 10 mA at 5 V) with software programmable open-drain LED outputs selection (default at totem pole). No input function.
- Output state change programmable on the Acknowledge or the STOP Command to update outputs byte-by-byte or all at the same time (default to 'Change on STOP').
- Active LOW Output Enable ($\overline{OE}$) input pin. LED outputs programmable to '1', '0' or 'high-impedance' (default at power-up) when $\overline{OE}$ is HIGH, thus allowing hardware blinking and dimming of the LEDs (16-pin version only).
- 2 hardware address pins (10-pin version) and 7 hardware address pins (16-pin version) allow respectively up to 4 and 126 devices to be connected to the same I²C-bus. No hardware address pins in the 8-pin version.
- 4 software programmable I²C-bus addresses (one LED Group Call address and three LED Sub Call addresses) allow groups of devices to be addressed at the same time in any combination (for example, one register used for 'All Call' so that all the PCA9633s on the I²C-bus can be addressed at the same time and the second register used for three different addresses so that ⅓ of all devices on the bus can be addressed at the same time in a group). Software enable and disable for I²C-bus address.
- Software Reset feature (SWRST Call) allows the device to be reset through the I²C-bus
- 25 MHz internal oscillator requires no external components
- Internal power-on reset
- Noise filter on SDA/SCL inputs
- Edge rate control on outputs
- No glitch on power-up
- Supports hot insertion
- Low standby current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 5.5 V tolerant inputs
- -40 °C to +85 °C operation
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: TSSOP8, TSSOP16, HVSON8

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3 Applications

- RGB or RGBA LED drivers
- LED status information
- LED displays
- LCD backlights
- Keypad backlights for cellular phones or handheld devices

4 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCA9633DP1	9633	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1
PCA9633PW	PCA9633	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
PCA9633TK	9633	HVSON8	plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 × 3 × 0.85 mm	SOT908-1

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method [1]	Minimum order quantity	Temperature
PCA9633DP1	PCA9633DP1,118	TSSOP8	REEL 13" Q1 NDP	2500	T_{amb} = -40 °C to +85 °C
PCA9633PW	PCA9633PW,118	TSSOP16	REEL 13" Q1 NDP	2500	T_{amb} = -40 °C to +85 °C
PCA9633TK	PCA9633TK,118	HVSON8	REEL 13" Q1 NDP	6000	T_{amb} = -40 °C to +85 °C

[1] Standard packing quantities and other packaging data are available at www.nxp.com/packages/.

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5 Block diagram

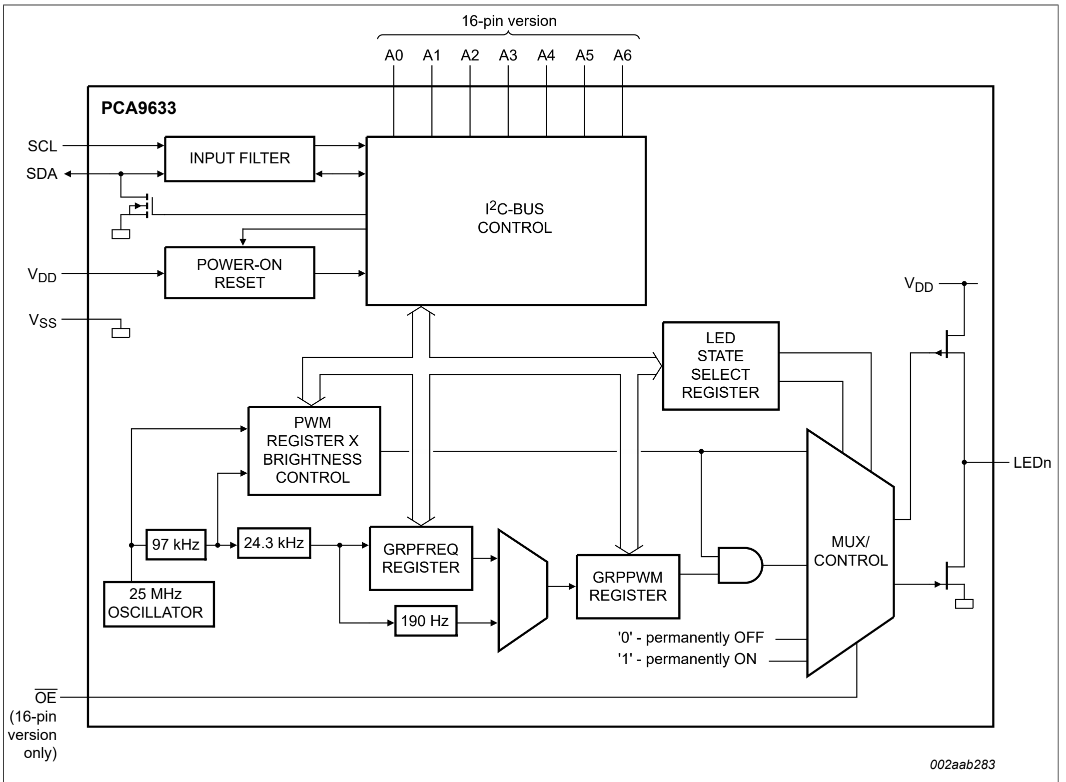

Figure 1. Block diagram of PCA9633

6 Pinning information

6.1 Pinning

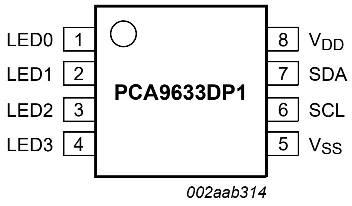

Figure 2. Pin configuration for TSSOP8

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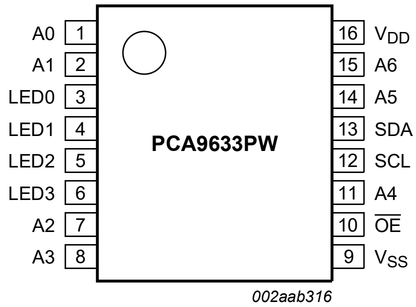

Figure 3. Pin configuration for TSSOP16

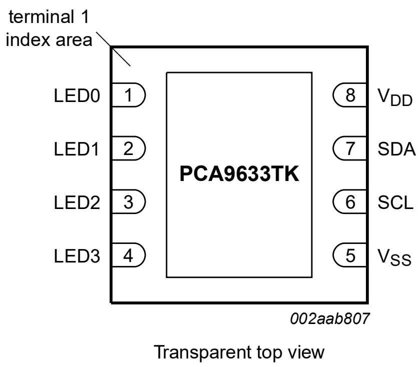

Figure 4. Pin configuration for HVSON8

6.2 Pin description

Table 3. Pin description for TSSOP8 and HVSON8

Symbol	Pin	Type	Description
LED0	1	O	LED driver 0
LED1	2	O	LED driver 1
LED2	3	O	LED driver 2
LED3	4	O	LED driver 3
V_{SS}	5	power supply	supply ground
SCL	6	I	serial clock line
SDA	7	I/O	serial data line
V_{DD}	8	power supply	supply voltage

Table 4. Pin description for TSSOP16

Symbol	Pin	Type	Description
A0	1	I	address input 0
A1	2	I	address input 1
LED0	3	O	LED driver 0
LED1	4	O	LED driver 1
LED2	5	O	LED driver 2

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Table 4. Pin description for TSSOP16...*continued*

Symbol	Pin	Type	Description
LED3	6	O	LED driver 3
A2	7	I	address input 2
A3	8	I	address input 3
V_{SS}	9	power supply	supply ground
$\overline{OE}$	10	I	active LOW Output Enable
A4	11	I	address input 4
SCL	12	I	serial clock line
SDA	13	I/O	serial data line
A5	14	I	address input 5
A6	15	I	address input 6
V_{DD}	16	power supply	supply voltage

7 Functional description

Refer to Figure 1.

7.1 Device addresses

Following a START condition, the bus controller must output the address of the target it is accessing.

There are a maximum of 128 possible programmable addresses using the 7 hardware address pins. Two of these addresses, Software Reset and LED All Call, cannot be used because their default power-up state is ON, leaving a maximum of 126 addresses. Using other reserved addresses, as well as any other subcall address, will reduce the total number of possible addresses even further.

7.1.1 Regular I²C-bus target address

The I²C-bus target address of the PCA9633 is shown in Figure 5. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW (10-pin and 16-pin versions).

Remark: Using reserved I²C-bus addresses will interfere with other devices, but only if the devices are on the bus and/or the bus will be open to other I²C-bus systems at some later date. In a closed system where the designer controls the address assignment these addresses can be used since the PCA9633 treats them like any other address. The LED All Call, Software Reset and PCA9564 or PCA9665 target address (if on the bus) can never be used for individual device addresses.

- PCA9633 LED All Call address (1110 000) and Software Reset (0000 0110) which are active on start-up
- PCA9564 (0000 000) or PCA9665 (1110 000) target address which is active on start-up
- ‘reserved for future use’ I²C-bus addresses (0000 011, 1111 1XX)
- target devices that use the 10-bit addressing scheme (1111 0XX)
- target devices that are designed to respond to the General Call address (0000 000)
- High-speed mode (Hs-mode) controller code (0000 1XX).

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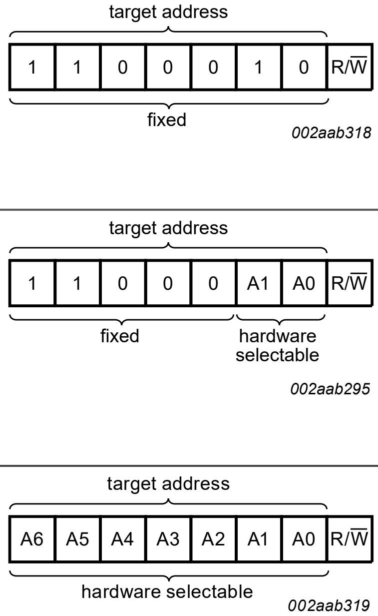

a. 8-pin version

b. 10-pin version

c. 16-pin version

Figure 5. Target address

The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

7.1.2 LED All Call I^{2}C-bus address

- Default power-up value (ALLCALLADR register): E0h or 1110 000X
- Programmable through I^{2}C-bus (volatile programming)
- At power-up, LED All Call I^{2}C-bus address is enabled. PCA9633 sends an ACK when E0h (R/$\overline{W}$ = 0) or E1h (R/$\overline{W}$ = 1) is sent by the controller.

See Section 7.3.8 for more detail.

Remark: The default LED All Call I^{2}C-bus address (E0h or 1110 000X) must not be used as a regular I^{2}C-bus target address since this address is enabled at power-up. All the PCA9633s on the I^{2}C-bus will acknowledge the address if sent by the I^{2}C-bus controller.

7.1.3 LED Sub Call I^{2}C-bus addresses

- Three different I^{2}C-bus addresses can be used
- Default power-up values:
  - SUBADR1 register: E2h or 1110 001X
  - SUBADR2 register: E4h or 1110 010X
  - SUBADR3 register: E8h or 1110 100X
- Programmable through I^{2}C-bus (volatile programming)
- At power-up, Sub Call I^{2}C-bus addresses are disabled. PCA9633 does not send an ACK when E2h (R/$\overline{W}$ = 0) or E3h (R/$\overline{W}$ = 1), E4h (R/$\overline{W}$ = 0) or E5h (R/$\overline{W}$ = 1), or E8h (R/$\overline{W}$ = 0) or E9h (R/$\overline{W}$ = 1) is sent by the controller.

See Section 7.3.7 for more detail.

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Remark: The default LED Sub Call I^{2}C-bus addresses may be used as regular I^{2}C-bus target addresses as long as they are disabled.

7.1.4 Software Reset I^{2}C-bus address

The address shown in Figure 6 is used when a reset of the PCA9633 needs to be performed by the controller. The Software Reset address (SWRST Call) must be used with R/$\overline{W}$ = 0. If R/$\overline{W}$ = 1, the PCA9633 does not acknowledge the SWRST. See Section 7.6"Software Reset" for more detail.

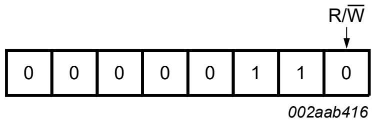

Figure 6. Software Reset address

Remark: The Software Reset I^{2}C-bus address is a reserved address and cannot be used as a regular I^{2}C-bus target address (16-pin version) or as an LED All Call or LED Sub Call address.

7.2 Control register

Following the successful acknowledgement of the target address, LED All Call address or LED Sub Call address, the bus controller will send a byte to the PCA9633, which will be stored in the Control register.

The lowest 4 bits are used as a pointer to determine which register will be accessed (D[3:0]). The highest 3 bits are used as Auto-Increment flag and Auto-Increment options (AI[2:0]). Bit 4 is unused and must be programmed with zero (0) for proper device operation.

reset state = 80h

Remark: The Control register does not apply to the Software Reset I^{2}C-bus address.

Figure 7. Control register

When the Auto-Increment flag is set (AI2 = 1), the four low order bits of the Control register are automatically incremented after a read or write. This allows the user to program the registers sequentially. Four different types of Auto-Increment are possible, depending on AI1 and AI0 values.

Table 5. Auto-Increment options

AI2	AI1	AI0	Function
0	0	0	no Auto-Increment
1	0	0	Auto-Increment for all registers. D3, D2, D1, D0 roll over to ‘0000’ after the last register (1100) is accessed.
1	0	1	Auto-Increment for individual brightness registers only. D3, D2, D1, D0 roll over to ‘0010’ after the last register (0101) is accessed.

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Table 5. Auto-Increment options...*continued*

AI2	AI1	AI0	Function
1	1	0	Auto-Increment for global control registers only. D3, D2, D1, D0 roll over to ‘0110’ after the last register (0111) is accessed.
1	1	1	Auto-Increment for individual and global control registers only. D3, D2, D1, D0 roll over to ‘0010’ after the last register (0111) is accessed.

Remark: Other combinations not shown in Table 5 (AI[2:0] = 001, 010, and 011) are reserved and must not be used for proper device operation.

AI[2:0] = 000 is used when the same register must be accessed several times during a single I^{2}C-bus communication, for example, changes the brightness of a single LED. Data is overwritten each time the register is accessed during a write operation.

AI[2:0] = 100 is used when all the registers must be sequentially accessed, for example, power-up programming.

AI[2:0] = 101 is used when the four LED drivers must be individually programmed with different values during the same I^{2}C-bus communication, for example, changing color setting to another color setting.

AI[2:0] = 110 is used when the LED drivers must be globally programmed with different settings during the same I^{2}C-bus communication, for example, global brightness or blinking change.

AI[2:0] = 111 is used when individual and global changes must be performed during the same I^{2}C-bus communication, for example, changing a color and global brightness at the same time.

Only the 4 least significant bits D[3:0] are affected by the AI[2:0] bits.

When the Control register is written, the register entry point determined by D[3:0] is the first register that will be addressed (read or write operation), and can be anywhere between 0000 and 1100 (as defined in Table 7). When AI[2] = 1, the Auto-Increment flag is set and the rollover value at which the point where the register increment stops and goes to the next one is determined by AI[2:0]. See Table 5 for rollover values. For example, if the Control register = 1110 1000 (E8h), then the register addressing sequence will be (in hex): 08 → … → 0C → 00 → … → 07 → 02 → … → 07 → 02 → … → 07 → 02 → … as long as the controller keeps sending or reading data.

7.3 Register definitions

Table 6. Register summary[1][2]

Register number (hex)	D3	D2	D1	D0	Name	Type	Function
00h	0	0	0	0	MODE1	read/write	Mode register 1
01h	0	0	0	1	MODE2	read/write	Mode register 2
02h	0	0	1	0	PWM0	read/write	brightness control LED0
03h	0	0	1	1	PWM1	read/write	brightness control LED1
04h	0	1	0	0	PWM2	read/write	brightness control LED2
05h	0	1	0	1	PWM3	read/write	brightness control LED3
06h	0	1	1	0	GRPPWM	read/write	group duty cycle control
07h	0	1	1	1	GRPFREQ	read/write	group frequency

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Table 6. Register summary[1][2] ...continued

Register number (hex)	D3	D2	D1	D0	Name	Type	Function
08h	1	0	0	0	LEDOUT	read/write	LED output state
09h	1	0	0	1	SUBADR1	read/write	I^2C-bus subaddress 1
0Ah	1	0	1	0	SUBADR2	read/write	I^2C-bus subaddress 2
0Bh	1	0	1	1	SUBADR3	read/write	I^2C-bus subaddress 3
0Ch	1	1	0	0	ALLCALLADR	read/write	LED All Call I^2C-bus address

[1] Only D[3:0] = 0000 to 1100 are allowed and will be acknowledged. D[3:0] = 1101, 1110, or 1111 are reserved and will not be acknowledged.
[2] When writing to the Control register, bit 4 must be programmed with logic 0 for proper device operation.

7.3.1 Mode register 1, MODE1

Table 7. MODE1 - Mode register 1 (address 00h) bit description
*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	AI2	read only	0	Register Auto-Increment disabled
			1*	Register Auto-Increment enabled
6	AI1	read only	0*	Auto-Increment bit 1 = 0
			1	Auto-Increment bit 1 = 1
5	AI0	read only	0*	Auto-Increment bit 0 = 0
			1	Auto-Increment bit 0 = 1
4	SLEEP	R/W	0	Normal mode[1].
			1*	Low power mode. Oscillator off[2].
3	SUB1	R/W	0*	PCA9633 does not respond to I^2C-bus subaddress 1.
			1	PCA9633 responds to I^2C-bus subaddress 1.
2	SUB2	R/W	0*	PCA9633 does not respond to I^2C-bus subaddress 2.
			1	PCA9633 responds to I^2C-bus subaddress 2.
1	SUB3	R/W	0*	PCA9633 does not respond to I^2C-bus subaddress 3.
			1	PCA9633 responds to I^2C-bus subaddress 3.
0	ALLCALL	R/W	0	PCA9633 does not respond to LED All Call I^2C-bus address.
			1*	PCA9633 responds to LED All Call I^2C-bus address.

[1] It takes 500 μs max. for the oscillator to be up and running once SLEEP bit has been set to logic 0. Timings on LEDn outputs are not guaranteed if PWMx, GRPPWM or GRPFREQ registers are accessed within the 500 μs window.
[2] When the oscillator is off (Sleep mode) the LED outputs cannot be turned on, off or dimmed/blinked.

7.3.2 Mode register 2, MODE2

Table 8. MODE2 - Mode register 2 (address 01h) bit description
*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	-	read only	0*	reserved
6	-	read only	0*	reserved

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Table 8. MODE2 - Mode register 2 (address 01h) bit description *...continued*

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
5	DMBLNK	R/W	0*	Group control = dimming
			1	Group control = blinking
4	INVRT[1]	R/W	0*	Output logic state not inverted. Value to use when no external driver used. Applicable when $\overline{OE}$ = 0 for PCA9633 16-pin version.
			1	Output logic state inverted. Value to use when external driver used. Applicable when $\overline{OE}$ = 0 for PCA9633 16-pin version.
3	OCH	R/W	0*	Outputs change on STOP command.[2]
			1	Outputs change on ACK.
2	OUTDRV[1]	R/W	0	The 4 LED outputs are configured with an open-drain structure.
			1*	The 4 LED outputs are configured with a totem pole structure.
1 to 0	OUTNE[1:0] [3][4]	R/W	00	When $\overline{OE}$ = 1 (output drivers not enabled), LEDn = 0.
			01*	When $\overline{OE}$ = 1 (output drivers not enabled): LEDn = 1 when OUTDRV = 1 LEDn = high-impedance when OUTDRV = 0 (same as OUTNE[1:0] = 10)
			10	When $\overline{OE}$ = 1 (output drivers not enabled), LEDn = high-impedance.
			11	reserved

[1] See Section 7.7 for more details. Normal LEDs can be driven directly in either mode. Some newer LEDs include integrated Zener diodes to limit voltage transients, reduce EMI and protect the LEDs, and these must be driven only in the open-drain mode to prevent overheating the IC.
[2] Change of the outputs at the STOP command allows synchronizing outputs of more than one PCA9633. Applicable to registers from 02h (PWM0) to 08h (LEDOUT) only.
[3] See Section 7.4 for more details.
[4] OUTNE[1:0] is only for PCA9633 16-pin version.

7.3.3 PWM registers 0 to 3, PWMx — Individual brightness control registers

Table 9. PWM0 to PWM3 - PWM registers 0 to 3 (address 02h to 05h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
02h	PWM0	7:0	IDC0[7:0]	R/W	0000 0000*	PWM0 Individual Duty Cycle
03h	PWM1	7:0	IDC1[7:0]	R/W	0000 0000*	PWM1 Individual Duty Cycle
04h	PWM2	7:0	IDC2[7:0]	R/W	0000 0000*	PWM2 Individual Duty Cycle
05h	PWM3	7:0	IDC3[7:0]	R/W	0000 0000*	PWM3 Individual Duty Cycle

A 97 kHz fixed frequency signal is used for each output. Duty cycle is controlled through 256 linear steps from 00h (0 % duty cycle = LED output off) to FFh (99.6 % duty cycle = LED output at maximum brightness). Applicable to LED outputs programmed with LDRx = 10 or 11 (LEDOUT register).

$$duty\ cycle = \frac{IDC[7:0]}{256} \quad (1)$$

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7.3.4 Group duty cycle control, GRPPWM

Table 10. GRPPWM - Group duty cycle control register (address 06h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
06h	GRPPWM	7:0	GDC[7:0]	R/W	1111 1111	GRPPWM register

When DMBLNK bit (MODE2 register) is programmed with 0, a 190 Hz fixed frequency signal is superimposed with the 97 kHz individual brightness control signal. GRPPWM is then used as a global brightness control allowing the LED outputs to be dimmed with the same value. The value in GRPFREQ is then a ‘Don’t care’.

General brightness for the 4 outputs is controlled through 256 linear steps from 00h (0 % duty cycle = LED output off) to FFh (99.6 % duty cycle = maximum brightness). Applicable to LED outputs programmed with LDRx = 11 (LEDOUT register).

When DMBLNK bit is programmed with 1, GRPPWM and GRPFREQ registers define a global blinking pattern, where GRPFREQ contains the blinking period (from 24 Hz to 10.73 s) and GRPPWM the duty cycle (ON/OFF ratio in %).

$$duty\ cycle = \frac{GDC[7:0]}{256} \quad (2)$$

7.3.5 Group frequency, GRPFREQ

Table 11. GRPFREQ - Group Frequency register (address 07h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
07h	GRPFREQ	7:0	GFRQ[7:0]	R/W	0000 0000*	GRPFREQ register

GRPFREQ is used to program the global blinking period when DMBLNK bit (MODE2 register) is equal to 1. Value in this register is a ‘Don’t care’ when DMBLNK = 0. Applicable to LED outputs programmed with LDRx = 11 (LEDOUT register).

Blinking period is controlled through 256 linear steps from 00h (41 ms, frequency 24 Hz) to FFh (10.73 s).

$$global\ blinking\ period = \frac{GFRQ[7:0]+1}{24}\ (in\ seconds) \quad (3)$$

7.3.6 LED driver output state, LEDOUT

Table 12. LEDOUT - LED driver output state register (address 08h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
08h	LEDOUT	7:6	LDR3	R/W	00*	LED3 output state control
		5:4	LDR2	R/W	00*	LED2 output state control
		3:2	LDR1	R/W	00*	LED1 output state control
		1:0	LDR0	R/W	00*	LED0 output state control

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LDRx = 00

LED driver x is off (default power-up state).

LDRx = 01

LED driver x is fully on (individual brightness and group dimming/blinking not controlled).

LDRx = 10

LED driver x individual brightness can be controlled through its PWMx register.

LDRx = 11

LED driver x individual brightness and group dimming/blinking can be controlled through its PWMx register and the GRPPWM registers.

7.3.7 I²C-bus subaddress 1 to 3, SUBADRx

Table 13. SUBADR1 to SUBADR3 - I²C-bus subaddress registers 0 to 3 (address 09h to 0Bh) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
09h	SUBADR1	7:1	A1[7:1]	R/W	1110 001*	I²C-bus subaddress 1
		0	A1[0]	R only	0*	reserved
0Ah	SUBADR2	7:1	A2[7:1]	R/W	1110 010*	I²C-bus subaddress 2
		0	A2[0]	R only	0*	reserved
0Bh	SUBADR3	7:1	A3[7:1]	R/W	1110 100*	I²C-bus subaddress 3
		0	A3[0]	R only	0*	reserved

Subaddresses are programmable through the I²C-bus. Default power-up values are E2h, E4h, E8h, and the device(s) will not acknowledge these addresses right after power-up (the corresponding SUBx bit in MODE1 register is equal to 0).

Once subaddresses have been programmed to their right values, SUBx bits need to be set to 1 in order to have the device acknowledging these addresses (MODE1 register).

Only the 7 MSBs representing the I²C-bus subaddress are valid. The LSB in SUBADRx register is a read-only bit (0).

When SUBx is set to 1, the corresponding I²C-bus subaddress can be used during either an I²C-bus read or write sequence.

7.3.8 LED All Call I²C-bus address, ALLCALLADR

Table 14. ALLCALLADR - LED All Call I²C-bus address register (address 0Ch) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
0Ch	ALLCALLADR	7:1	AC[7:1]	R/W	1110 000*	ALLCALL I²C-bus address register
		0	AC[0]	R only	0*	reserved

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The LED All Call I^{2}C-bus address allows all the PCA9633s in the bus to be programmed at the same time (ALLCALL bit in register MODE1 must be equal to 1, power-up default state). This address is programmable through the I^{2}C-bus and can be used during either an I^{2}C-bus read or write sequence. The register address can be programmed as a sub call.

Only the 7 MSBs representing the All Call I^{2}C-bus address are valid. The LSB in ALLCALLADR register is a Read-only bit (0).

If ALLCALL bit = 0, the device does not acknowledge the address programmed in register ALLCALLADR.

7.4 Active LOW output enable input

The active LOW output enable ($\overline{OE}$) pin, allows to enable or disable all the LED outputs at the same time.

This control signal is only available for the 16-pin version and does not apply to the 8-pin or 10-pin versions.

- When a LOW level is applied to $\overline{OE}$ pin, all the LED outputs are enabled and follow the output state defined in the LEDOUT register with the polarity defined by INVRT bit (MODE2 register).
- When a HIGH level is applied to $\overline{OE}$ pin, all the LED outputs are programmed to the value that is defined by OUTNE[1:0] in the MODE2 register.

Table 15. LED outputs when $\overline{OE}$ = 1

OUTNE1	OUTNE0	LED outputs
0	0	0
0	1	1 if OUTDRV = 1, high-impedance if OUTDRV = 0
1	0	high-impedance
1	1	reserved

The $\overline{OE}$ pin can be used as a synchronization signal to switch on/off several PCA9633 devices at the same time. This requires an external clock reference that provides blinking period and the duty cycle.

The $\overline{OE}$ pin can also be used as an external dimming control signal. The frequency of the external clock must be high enough not to be seen by the human eye, and the duty cycle value determines the brightness of the LEDs.

Remark: Do not use $\overline{OE}$ as an external blinking control signal when internal global blinking is selected (DMBLNK = 1, MODE2 register) since it will result in an undefined blinking pattern. Do not use $\overline{OE}$ as an external dimming control signal when internal global dimming is selected (DMBLNK = 0, MODE2 register) since it will result in an undefined dimming pattern.

7.5 Power-on reset

When power is applied to V_{DD}, an internal Power-on reset holds the PCA9633 in a reset condition until V_{DD} has reached V_{POR}. At this point, the reset condition is released and the PCA9633 registers and I^{2}C-bus state machine are initialized to their default states (all zeroes) causing all the channels to be deselected. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

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7.6 Software Reset

The Software Reset Call (SWRST Call) allows all the devices in the I^2C-bus to be reset to the power-up state value through a specific formatted I^2C-bus command. To be performed correctly, it implies that the I^2C-bus is functional and that there is no device hanging the bus.

The SWRST Call function is defined as the following:

1. A START command is sent by the I^2C-bus controller.
2. The reserved SWRST I^2C-bus address ‘0000 011’ with the R/$\overline{W}$ bit set to 0 (write) is sent by the I^2C-bus controller.
3. The PCA9633 device(s) acknowledge(s) after seeing the SWRST Call address ‘0000 0110’ (06h) only. If the R/$\overline{W}$ bit is set to 1 (read), no acknowledge is returned to the I^2C-bus controller.
4. Once the SWRST Call address has been sent and acknowledged, the controller sends 2 bytes with 2 specific values (SWRST data byte 1 and byte 2):
5. Byte 1 = A5h: the PCA9633 acknowledges this value only. If byte 1 is not equal to A5h, the PCA9633 does not acknowledge it.
6. Byte 2 = 5Ah: the PCA9633 acknowledges this value only. If byte 2 is not equal to 5Ah, then the PCA9633 does not acknowledge it.

If more than 2 bytes of data are sent, the PCA9633 does not acknowledge any more.

1. Once the right 2 bytes (SWRST data byte 1 and byte 2 only) have been sent and correctly acknowledged, the controller sends a STOP command to end the SWRST Call: the PCA9633 then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time (t_{BUF}).

The I^2C-bus controller must interpret a non-acknowledge from the PCA9633 (at any time) as a ‘SWRST Call Abort’. The PCA9633 does not initiate a reset of its registers. This happens only when the format of the SWRST Call sequence is not correct.

7.7 Using the PCA9633 with and without external drivers

The PCA9633 LED output drivers are 5.5 V only tolerant and can sink up to 25 mA at 5 V.

If the device needs to drive LEDs to a higher voltage and/or higher current, use of an external driver is required.

- INVRT bit (MODE2 register) can be used to keep the LED PWM control firmware the same (PWMx and GRPPWM values directly calculated from their respective formulas and the LED output state determined by LEDOUT register value) independently of the type of external driver. This bit allows LED output polarity inversion/non-inversion only when $\overline{OE}$ = 0.
- OUTDRV bit (MODE2 register) allows minimizing the amount of external components required to control the external driver (N-type or P-type device).

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Table 16. Use of INVRT and OUTDRV based on connection to the LEDn outputs when OE = 0[1]

INVRT	OUTDRV	Direct connection to LEDn		External N-type driver		External P-type driver	
		Firmware	External pull-up resistor	Firmware	External pull-up resistor	Firmware	External pull-up resistor
0	0	formulas and LED output state values apply[2]	LED current limiting R[2]	formulas and LED output state values inverted	required	formulas and LED output state values apply	required
0	1	formulas and LED output state values apply[2]	LED current limiting R[2]	formulas and LED output state values inverted	not required	formulas and LED output state values apply[3]	not required[3]
1	0	formulas and LED output state values inverted	LED current limiting R	formulas and LED output state values apply	required	formulas and LED output state values inverted	required
1	1	formulas and LED output state values inverted	LED current limiting R	formulas and LED output state values apply[4]	not required[4]	formulas and LED output state values inverted	not required

[1] $\overline{OE}$ applies to 16-pin version only. When $\overline{OE}$ = 1, LED output state is controlled only by OUTNE[1:0] bits (MODE2 register).
[2] Correct configuration when LEDs directly connected to the LEDn outputs (connection to V_{DD} through current limiting resistor).
[3] Optimum configuration when external P-type (PNP, PMOS) driver used.
[4] Optimum configuration when external N-type (NPN, NMOS) driver used.

Table 17. Output transistors based on LEDOUT registers, INVRT and OUTDRV bits when OE = 0[1]

LEDOUT	INVRT	OUTDRV	Upper transistor (V_{DD} to LEDn)	Lower transistor (LEDn to V_{SS})	LEDn state
00 LED driver off	0	0	off	off	high-Z[2]
	0	1	on	off	V_{DD}
	1	0	off	on	V_{SS}
	1	1	off	on	V_{SS}
01 LED driver on	0	0	off	on	V_{SS}
	0	1	off	on	V_{SS}
	1	0	off	off	high-Z[2]
	1	1	on	off	V_{DD}
10 Individual brightness control	0	0	off	Individual PWM (non-inverted)	V_{SS} or high-Z[2] = PWMx value
	0	1	Individual PWM (non-inverted)	Individual PWM (non-inverted)	V_{SS} or V_{DD} = PWMx value
	1	0	off	Individual PWM (inverted)	high-Z[2] or V_{SS} = 1 - PWMx value
	1	1	Individual PWM (inverted)	Individual PWM (inverted)	V_{DD} or V_{SS} = 1 - PWMx value
11 Individual + Group dimming/ blinking	0	0	off	Individual + Group PWM (non-inverted)	V_{SS} or high-Z[2] = PWMx/GRPPWM values
	0	1	Individual PWM (non-inverted)	Individual PWM (non-inverted)	V_{SS} or V_{DD} = PWMx/GRPPWM values

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Table 17. Output transistors based on LEDOUT registers, INVRT and OUTDRV bits when OE = 0[1] *...continued*

LEDOUT	INVRT	OUTDRV	Upper transistor (V_{DD} to LEDn)	Lower transistor (LEDn to V_{SS})	LEDn state
	1	0	off	Individual + Group PWM (inverted)	high-Z[2] or V_{SS} = (1 - PWMx) or (1 - GRPPWM) values
	1	1	Individual PWM (inverted)	Individual PWM (inverted)	V_{DD} or V_{SS} = (1 - PWMx) or (1 - GRPPWM) values

[1] $\overline{OE}$ applies to 16-pin version only. When $\overline{OE}$ = 1, LED output state is controlled only by OUTNE[1:0] bits (MODE2 register).

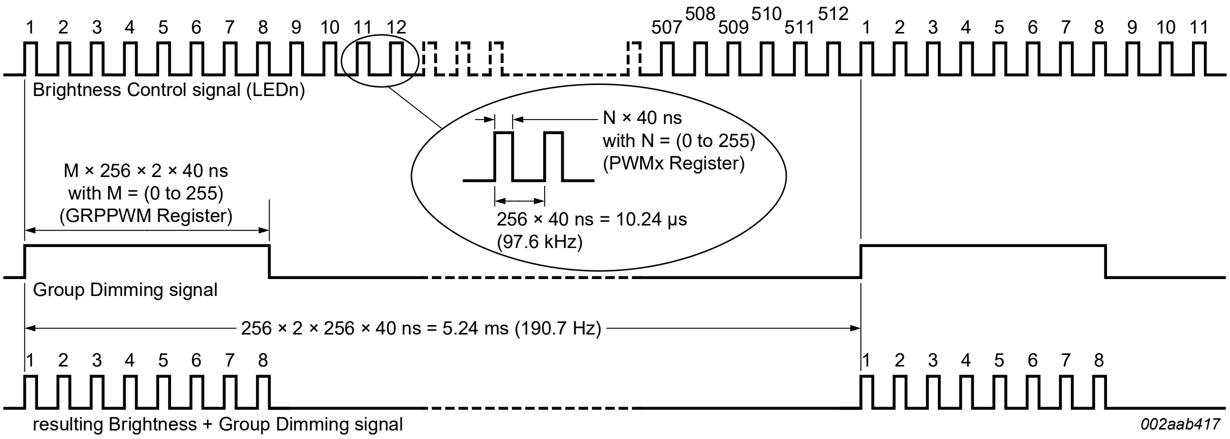
[2] External pull-up or LED current limiting resistor connects LEDn to V_{DD}.

7.8 Individual brightness control with group dimming/blinking

A 97 kHz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to control individually the brightness for each LED.

On top of this signal, one of the following signals can be superimposed (this signal can be applied to the 4 LED outputs):

- A lower 190 Hz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to provide a global brightness control.
- A programmable frequency signal from 24 Hz to $^{1}/_{10.73}$ Hz (8 bits, 256 steps) with programmable duty cycle (8 bits, 256 steps) is used to provide a global blinking control.



Minimum pulse width for LEDn Brightness Control is 40 ns.

Minimum pulse width for Group Dimming is 20.48 μs.

When M = 1 (GRPPWM register value), the resulting LEDn Brightness Control + Group Dimming signal will have 2 pulses of the LED Brightness Control signal (pulse width = N × 40 ns, with 'N' defined in PWMx register).

This resulting Brightness + Group Dimming signal above shows a resulting Control signal with M = 4 (8 pulses).

Figure 8. Brightness + Group Dimming signals

8 Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

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8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 9).

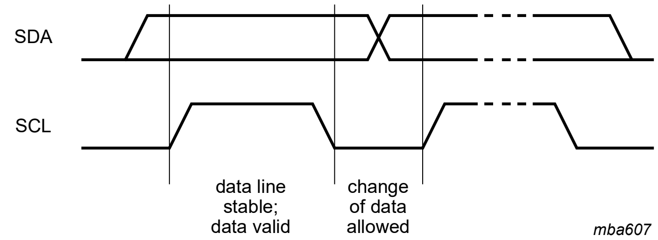

Figure 9. Bit transfer

8.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 10).

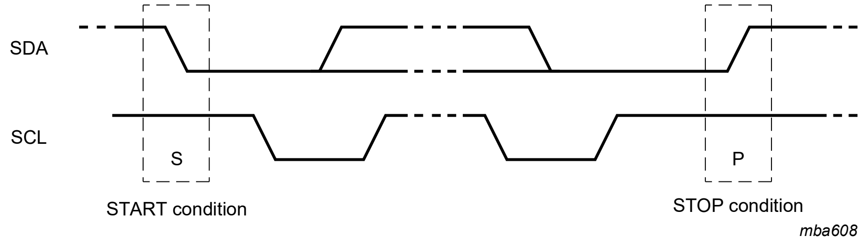

Figure 10. Definition of START and STOP conditions

8.2 System configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'controller' and the devices which are controlled by the controller are the 'targets' (see Figure 11).

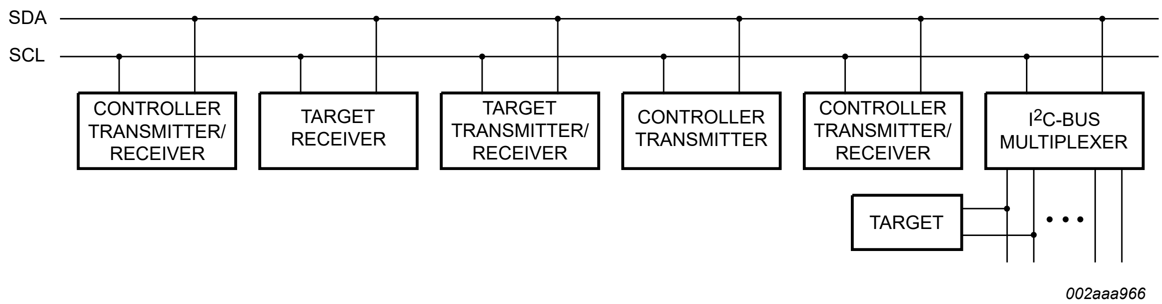

Figure 11. System configuration

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8.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the controller generates an extra acknowledge related clock pulse.

A target receiver which is addressed must generate an acknowledge after the reception of each byte. Also a controller must generate an acknowledge after the reception of each byte that has been clocked out of the target transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

A controller receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the target. In this event, the transmitter must leave the data line HIGH to enable the controller to generate a STOP condition.

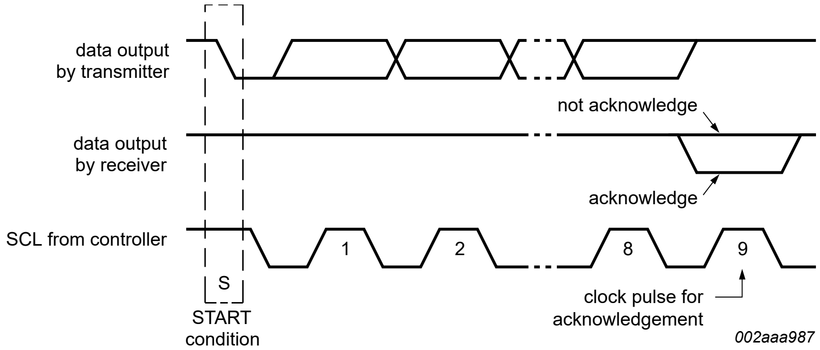
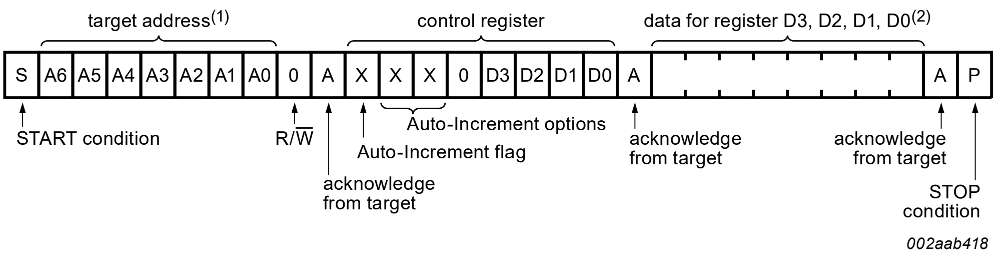


Figure 12. Acknowledgement on the I²C-bus

9 Bus transactions



1. 16-pin version only.
2. See Table 7 for register definition.

Figure 13. Write to a specific register

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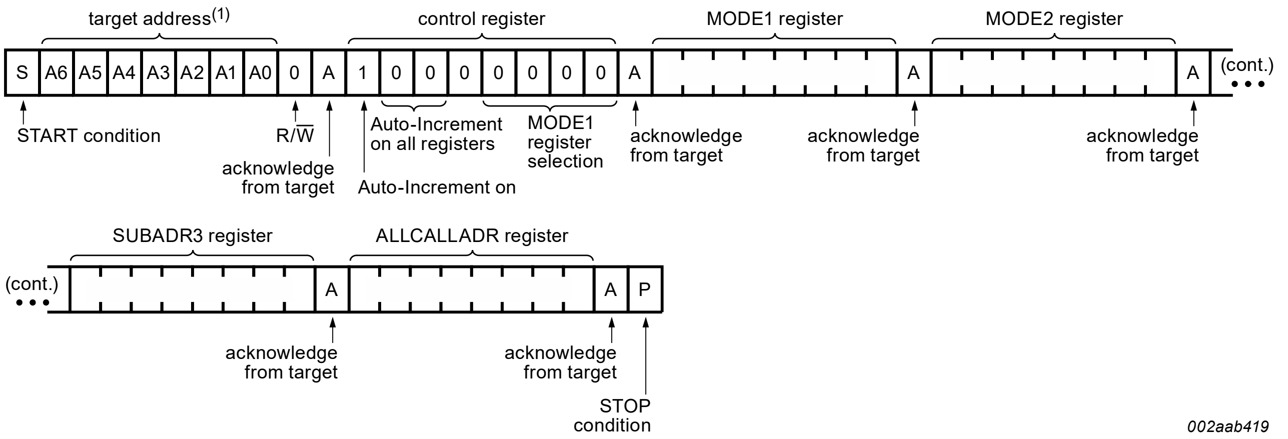
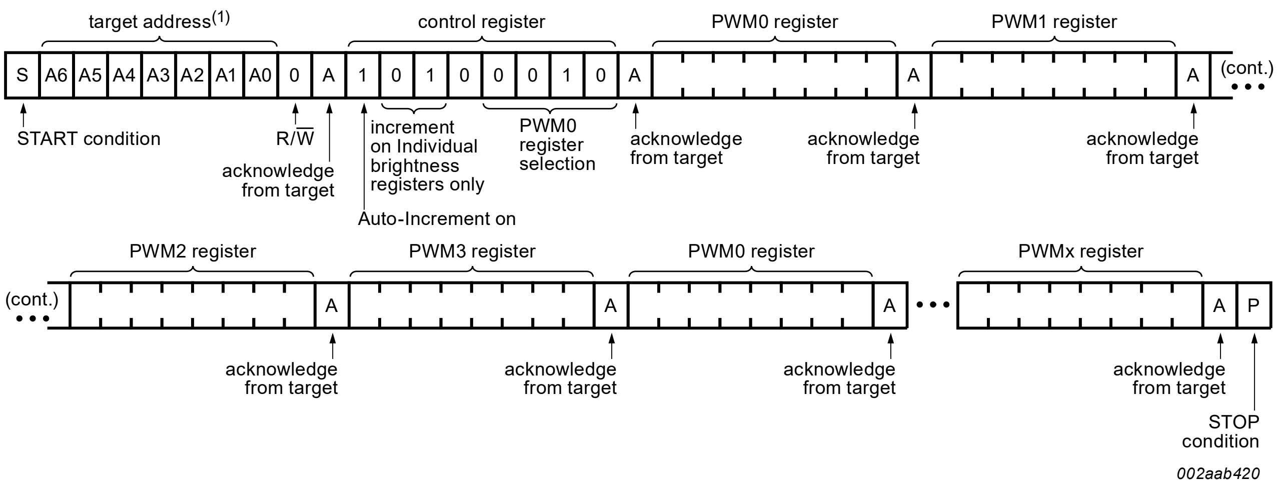


1. 16-pin version only.

Figure 14. Write to all registers using the Auto-Increment feature



1. 16-pin version only.

Figure 15. Multiple writes to Individual Brightness registers only using the Auto-Increment feature

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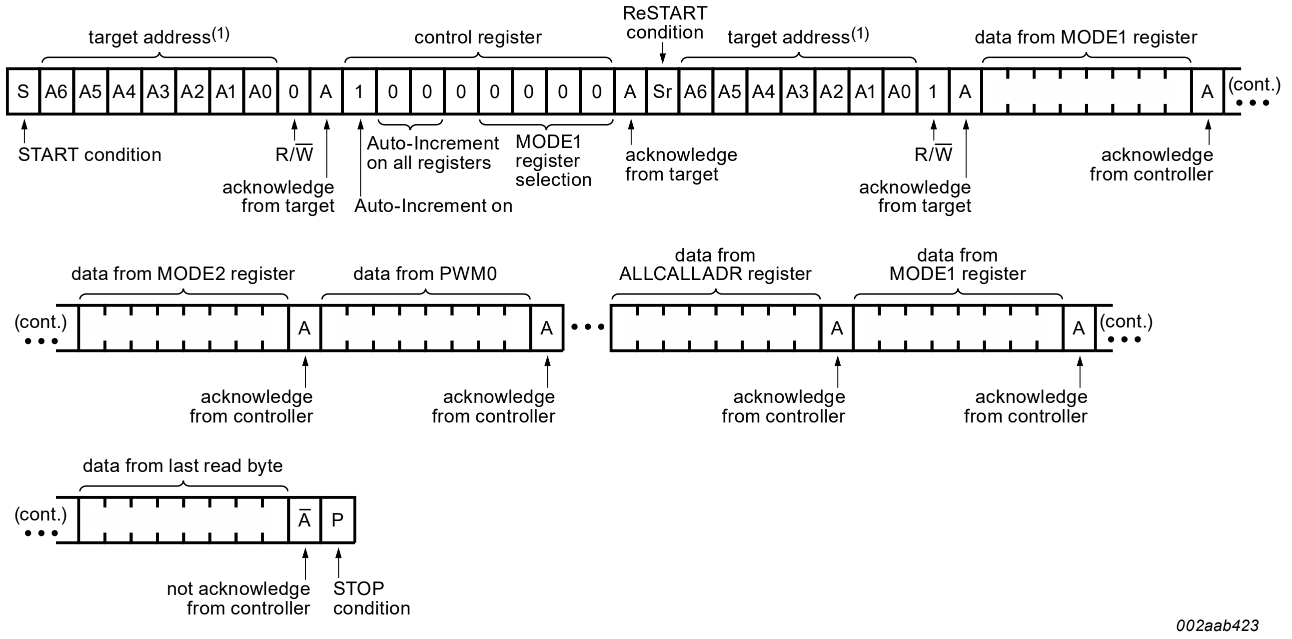
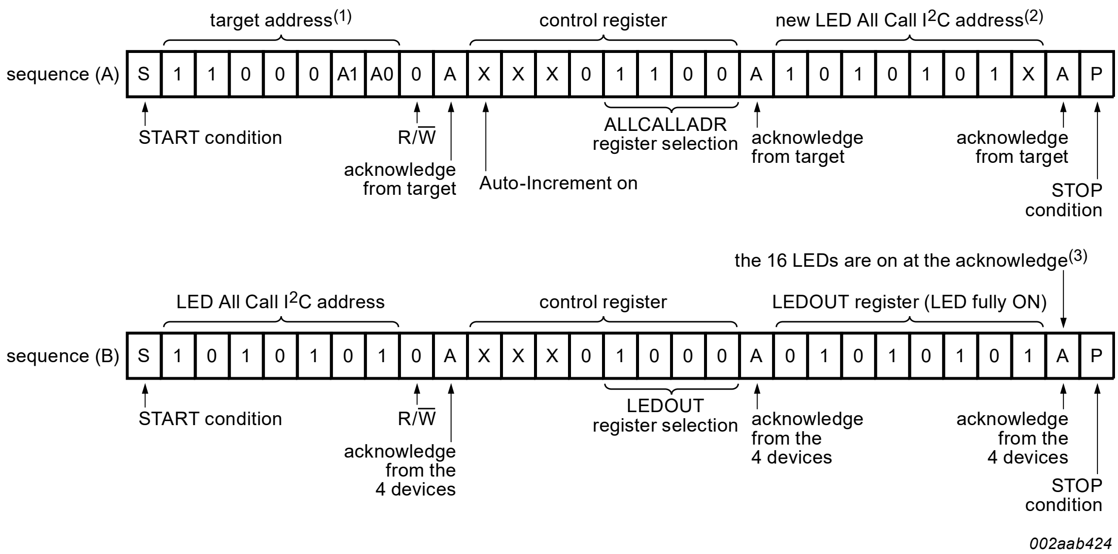


1. 16-pin version only.

Figure 16. Read all registers using the Auto-Increment feature



1. 10-pin version is used for this figure. Four PCA9633DP2s are used and the same sequence (A) (above) is sent to each of them. A[1:0] = 00 to 11.
2. ALLCALL bit in MODE1 register is equal to 1 for this example.
3. OCH bit in MODE2 register is equal to 1 for this example.

Figure 17. LED All Call I²C-bus address programming and LED All Call sequence example

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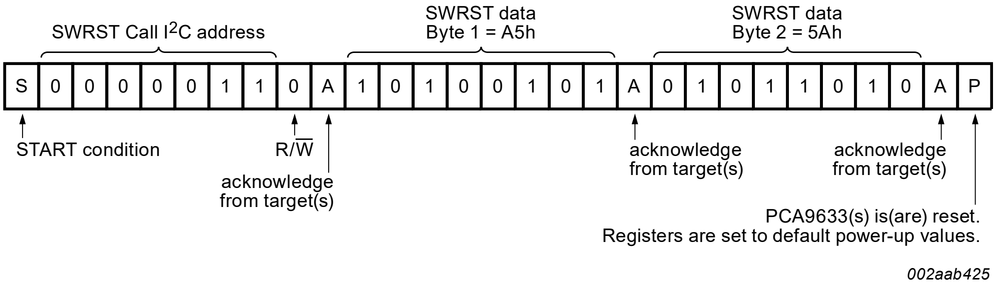
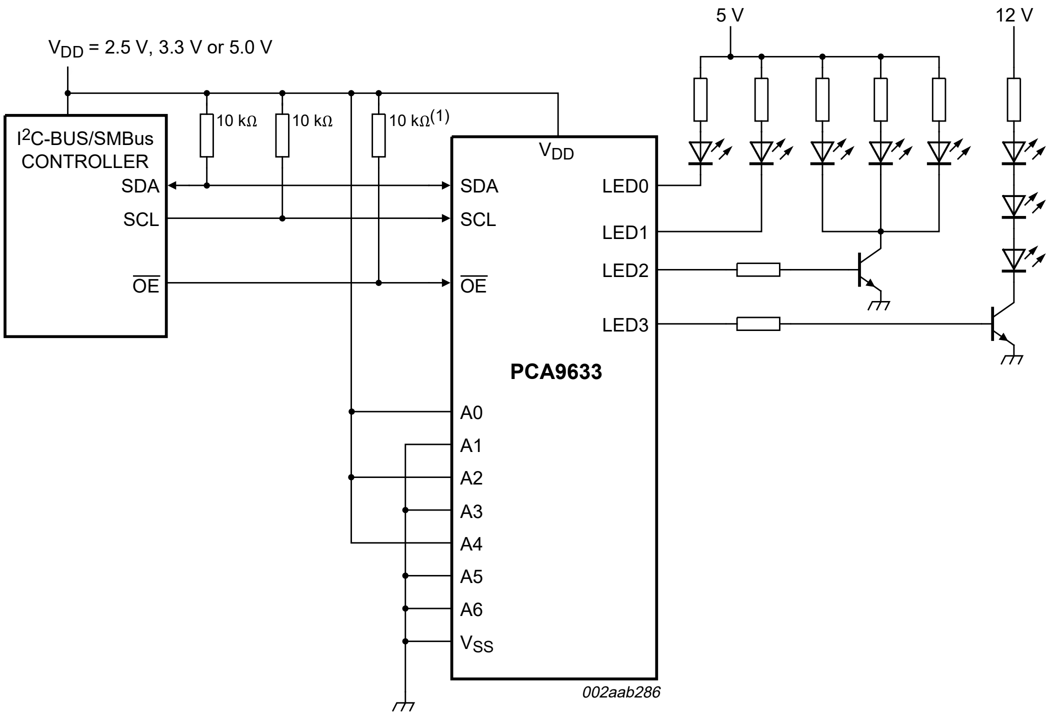


Figure 18. Software Reset (SWRST) Call sequence

10 Application design-in information



I²C-bus address = 0010 101X.

All of the 4 LEDn outputs configurable as either open-drain or totem pole. Mixing of configurations is not possible.

1. OE requires pull-up resistor if control signal from the controller is open-drain.

Figure 19. Typical application

Question 1: What kind of edge rate control is there on the outputs?

- The typical edge rates depend on the output configuration, supply voltage, and the applied load. The outputs can be configured as either open-drain NMOS or totem pole outputs. If the customer is using the part to directly drive LEDs, they should be using it in an open-drain NMOS, if they are concerned about the maximum ISS and ground bounce. The edge rate control was designed primarily to slow down the turn-on of the output device; it turns off rather quickly (~1.5 ns). In simulation, the typical turn-on time for the open-drain NMOS was ~14 ns (V_{DD} = 3.6 V; C_L = 50 pF; R_{PU} = 500 Ω).

Question 2: Is ground bounce possible?

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- Ground bounce is a possibility, especially if all 16 outputs are changed at full current (25 mA each). There is a fair amount of decoupling capacitance on chip (~50 pF), which is intended to suppress some of the ground bounce. The customer will need to determine if additional decoupling capacitance externally placed as close as physically possible to the device is required.

Question 3: Can I really sink 400 mA through the single ground pin on the package and will this cause any ground bounce problem due to the PWM of the LEDs?

- Yes, you can sink 400 mA through a single ground pin on the **package**. Although the package only has one ground pin, there are two ground pads on the die itself connected to this one pin. Although some ground bounce is likely, it will not disrupt the operation of the part and would be reduced by the external decoupling capacitance.

Question 4: I can't turn the LEDs on or off, but their registers are set properly. Why?

- Check the Mode Register 1 bit 4 SLEEP setting. The value needs to be 0 so that the OSC is turn on. If the OSC is turned off, the LEDs cannot be turned on or off and also can't be dimmed or blinked.

Question 5: I'm using LEDs with integrated Zener diodes and the IC is getting very hot. Why?

- The IC outputs can be set to either open-drain or push-pull and default to push-pull outputs. In this application with the Zener diodes, they need to be set to open-drain since in the push-pull architecture there is a low resistance path to GND through the Zener and this is causing the IC to overheat. The PCA9632/33/34/35 ICs all power-up in the push-pull output mode and with the logic state HIGH, so one of the first things that need to be done is to set the outputs to open-drain.

11 Limiting values

Table 18. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			-0.5	+6.0	V
$V_{I/O}$	voltage on an input/output pin			V_{SS} - 0.5	5.5	V
$I_{O(LEDn)}$	output current on pin LEDn			-	25	mA
I_{SS}	ground supply current			-	100	mA
P_{tot}	total power dissipation			-	400	mW
T_{stg}	storage temperature			-65	+150	°C
T_{amb}	ambient temperature	operating		-40	+85	°C

12 Static characteristics

Table 19. Static characteristics

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_{DD}	supply voltage			2.3	-	5.5	V

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Table 19. Static characteristics *...continued*

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DD}	supply current	operating mode; no load; f_{SCL} = 1 MHz					
		V_{DD} = 2.3 V		-	2.5	10	mA
		V_{DD} = 3.3 V		-	2.5	10	mA
		V_{DD} = 5.5 V		-	2.5	10	mA
I_{stb}	standby current	no load; f_{SCL} = 0 Hz; I/O = inputs; V_I = V_{DD}					
		V_{DD} = 2.3 V		-	2.3	11	μA
		V_{DD} = 3.3 V		-	2.9	12	μA
		V_{DD} = 5.5 V		-	3.8	15.5	μA
V_{POR}	power-on reset voltage	no load; V_I = V_{DD} or V_{SS}	[1]	-	1.70	2.0	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage			-0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 2.3 V		20	-	-	mA
		V_{OL} = 0.4 V; V_{DD} = 5.0 V		30	-	-	mA
I_L	leakage current	V_I = V_{DD} or V_{SS}		-1	-	+1	μA
C_i	input capacitance	V_I = V_{SS}		-	6	10	pF
LED driver outputs							
I_{OL}	LOW-level output current	V_{OL} = 0.5 V; V_{DD} = 2.3 V	[2]	12	-	-	mA
		V_{OL} = 0.5 V; V_{DD} = 3.0 V	[2]	17	-	-	mA
		V_{OL} = 0.5 V; V_{DD} = 4.5 V	[2]	25	-	-	mA
$I_{OL(tot)}$	total LOW-level output current	V_{OL} = 0.5 V; V_{DD} = 4.5 V	[2]	-	-	100	mA
I_{OH}	HIGH-level output current	open-drain; V_{OH} = V_{DD}		-50	-	+50	μA
V_{OH}	HIGH-level output voltage	I_{OH} = -10 mA; V_{DD} = 2.3 V		1.6	-	-	V
		I_{OH} = -10 mA; V_{DD} = 3.0 V		2.3	-	-	V
		I_{OH} = -10 mA; V_{DD} = 4.5 V		4.0	-	-	V
C_o	output capacitance			-	2.5	5	pF
$\overline{OE}$ input							
V_{IL}	LOW-level input voltage			-0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage			2	-	5.5	V
I_{LI}	input leakage current			-1	-	+1	μA
C_i	input capacitance			-	3.7	5	pF
Address inputs							
V_{IL}	LOW-level input voltage			-0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	5.5	V

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Table 19. Static characteristics*...continued*

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{LI}	input leakage current			-1	-	+1	μA
C_i	input capacitance			-	3.7	5	pF

[1] V_{DD} must be lowered to 0.2 V in order to reset part.
[2] Each bit must be limited to a maximum of 25 mA and the total package limited to 100 mA due to internal busing limits.

13 Dynamic characteristics

Table 20. Dynamic characteristics

Symbol	Parameter	Conditions		Standard-mode I²C-bus		Fast-mode I²C-bus		Fast-mode Plus I²C-bus		Unit
				Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		[1]	0	100	0	400	0	1000	kHz
t_{BUF}	bus free time between a STOP and START condition			4.7	-	1.3	-	0.5	-	μs
$t_{HD;STA}$	hold time (repeated) START condition			4.0	-	0.6	-	0.26	-	μs
$t_{SU;STA}$	set-up time for a repeated START condition			4.7	-	0.6	-	0.26	-	μs
$t_{SU;STO}$	set-up time for STOP condition			4.0	-	0.6	-	0.26	-	μs
$t_{HD;DAT}$	data hold time			0	-	0	-	0	-	ns
$t_{VD;ACK}$	data valid acknowledge time		[2]	0.3	3.45	0.1	0.9	0.05	0.45	μs
$t_{VD;DAT}$	data valid time		[3]	0.3	3.45	0.1	0.9	0.05	0.45	μs
$t_{SU;DAT}$	data set-up time			250	-	100	-	50	-	ns
t_{LOW}	LOW period of the SCL clock			4.7	-	1.3	-	0.5	-	μs
t_{HIGH}	HIGH period of the SCL clock			4.0	-	0.6	-	0.26	-	μs
t_f	fall time of both SDA and SCL signals		[4][5]	-	300	$20 + 0.1C_b$[6]	300	-	120	ns
t_r	rise time of both SDA and SCL signals			-	1000	$20 + 0.1C_b$[6]	300	-	120	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter		[7]	-	50	-	50	-	50	ns

[1] Minimum SCL clock frequency is limited by the bus time-out feature, which resets the serial bus interface if either SDA or SCL is held LOW for a minimum of 25 ms. Disable bus time-out feature for DC operation.
[2] $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.
[3] $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.
[4] A controller device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.
[5] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time (t_f) for the SDA output stage is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
[6] C_b = total capacitance of one bus line in pF.

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[7] Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns.

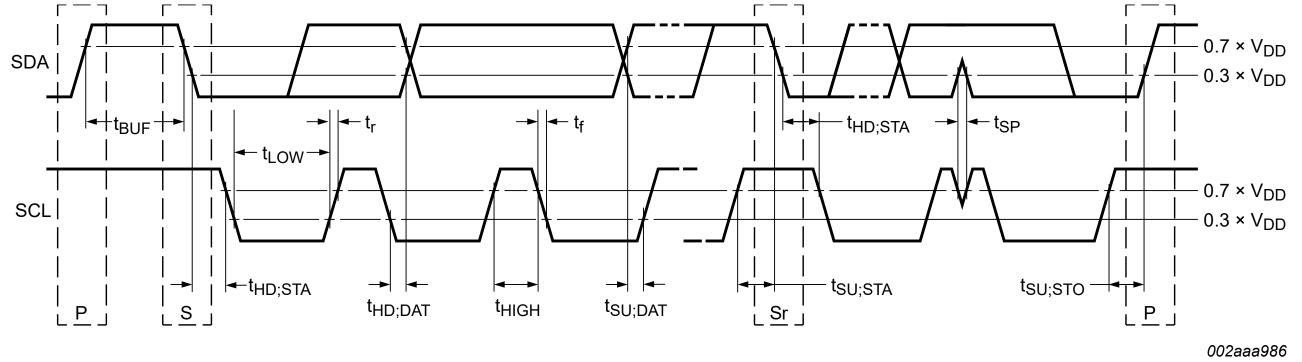
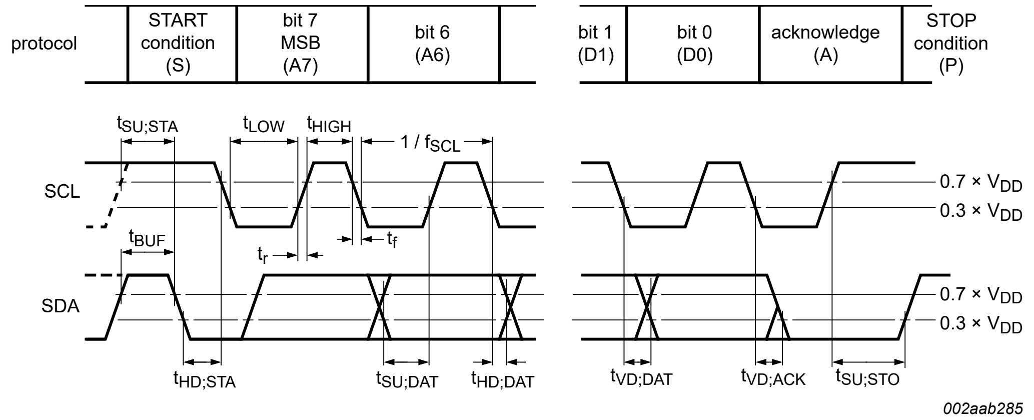


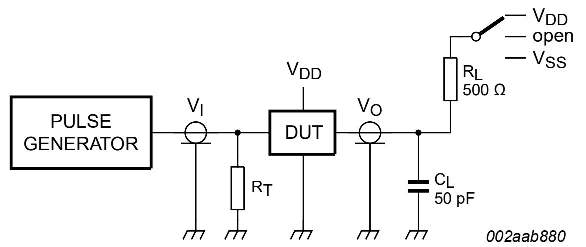
Figure 20. Definition of timing



Rise and fall times refer to V_{IL} and V_{IH}.

Figure 21. I²C-bus timing diagram

14 Test information



R_L = Load resistor for LEDn. R_L for SDA and SCL > 1 kΩ (3 mA or less current).

C_L = Load capacitance includes jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generators.

Figure 22. Test circuitry for switching times

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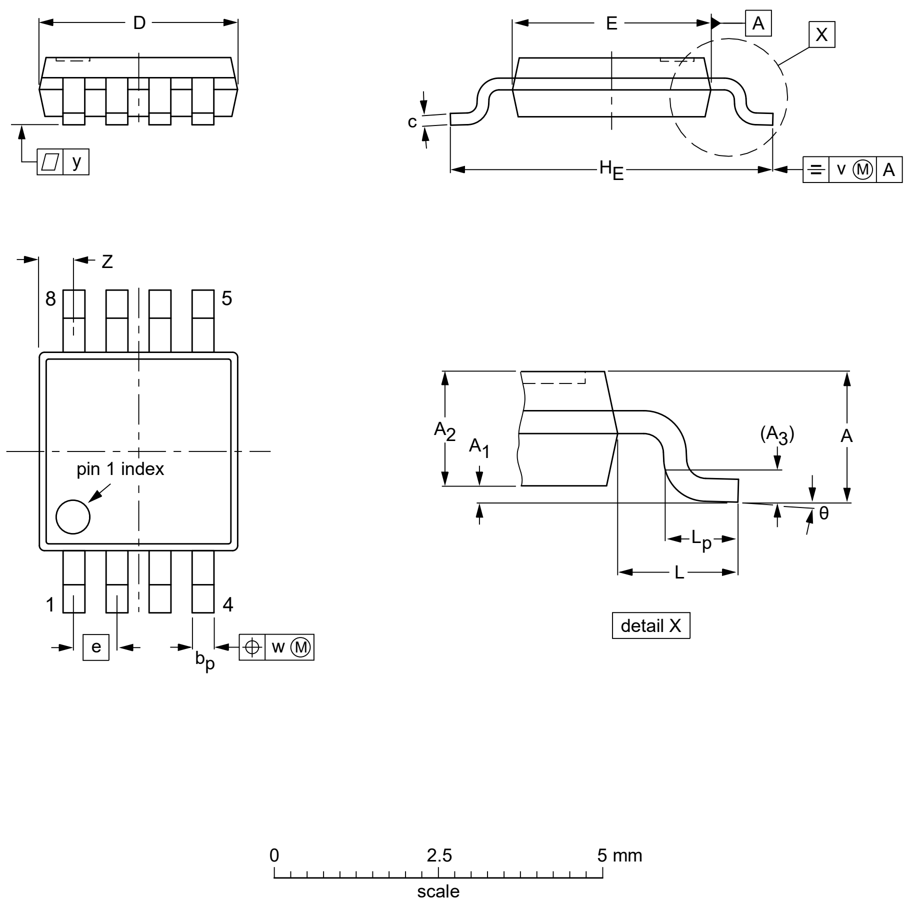
15 Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	v	w	y	Z(1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Figure 23. Package outline SOT505-1 (TSSOP8)

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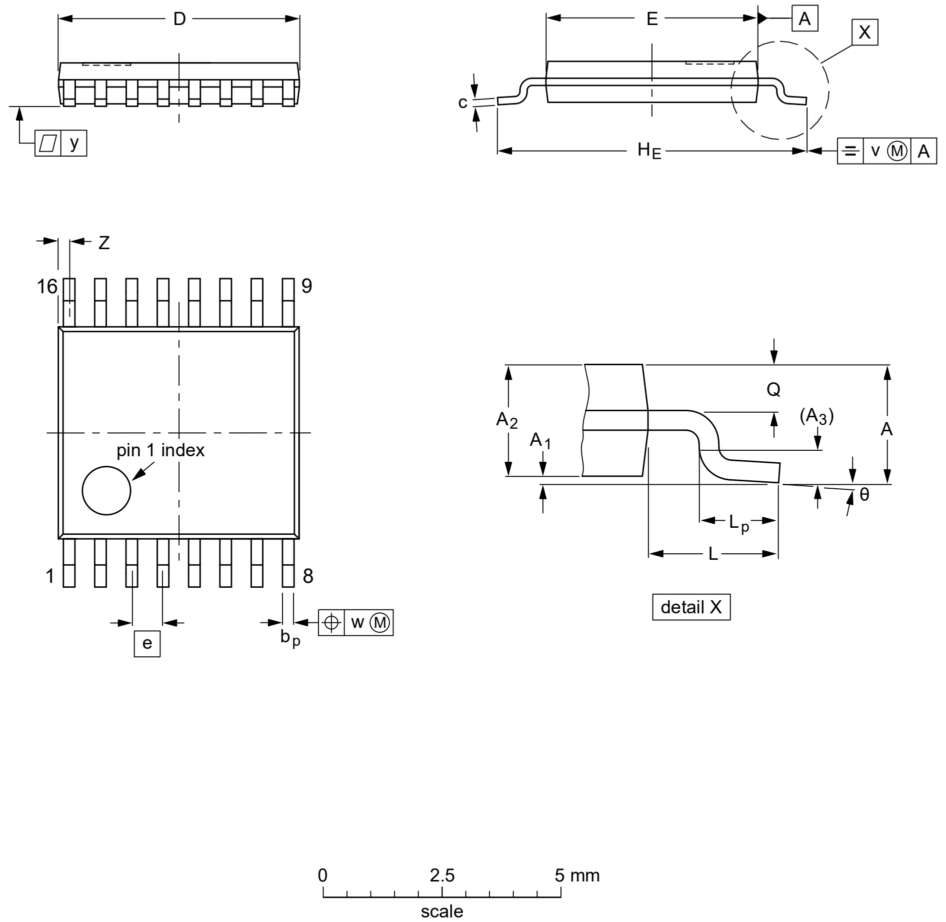
TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Figure 24. Package outline SOT403-1 (TSSOP16)

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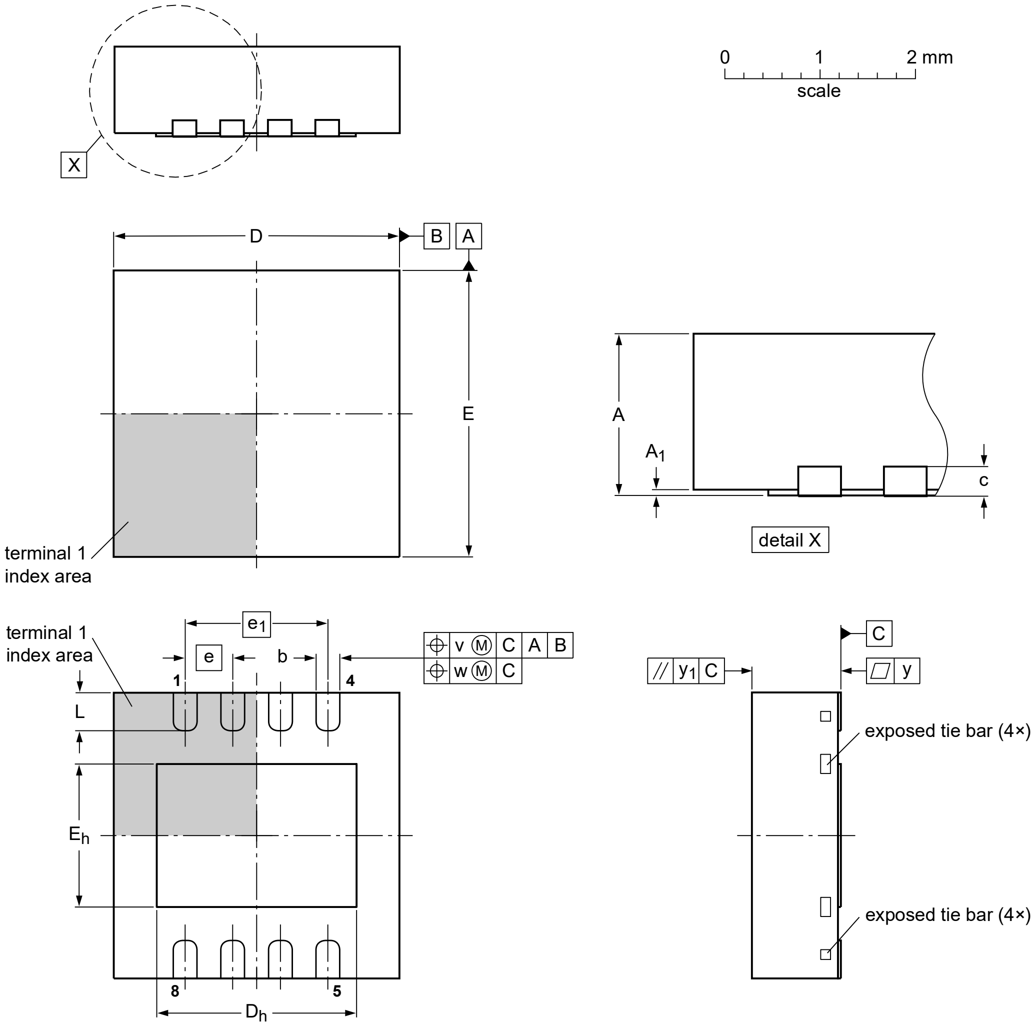
HVSON8: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 x 3 x 0.85 mm **SOT908-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.3 0.2	0.2	3.1 2.9	2.25 1.95	3.1 2.9	1.65 1.35	0.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT908-1		MO-229				~~05-09-26~~ 05-10-05

Figure 25. Package outline SOT908-1 (HVSON8)

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16 Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling integrated circuits.

17 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

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- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 26) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 21 and Table 22

Table 21. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 22. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 26.

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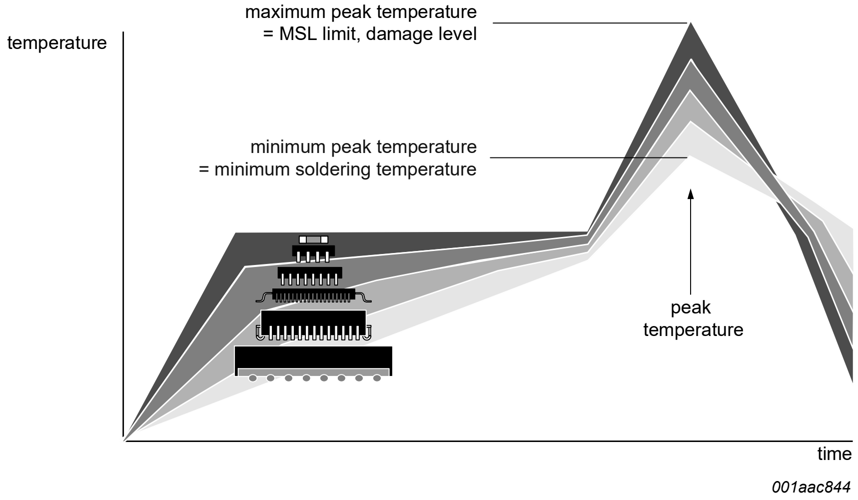

MSL: Moisture Sensitivity Level

Figure 26. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

18 Abbreviations

Table 23. Abbreviations

Acronym	Description
CDM	Charged-Device Model
DUT	Device Under Test
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
HBM	Human Body Model
I^2C-bus	Inter-Integrated Circuit bus
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
NMOS	Negative-channel Metal-Oxide Semiconductor
PCB	Printed-Circuit Board
PMOS	Positive-channel Metal-Oxide Semiconductor
PWM	Pulse Width Modulation
RGB	Red/Green/Blue
RGBA	Red/Green/Blue/Amber
SMBus	System Management Bus

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19 Revision history

Table 24. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9633 v6.0	20230119	Product data sheet	201711018 DNU02 (D16/BS); 202104010DN (DP2)	PCA9633_5
Modifications:	• Removed D16, BS and DP2 package options • Updated Section 4 • Changed terms master/slave to controller/target in accordance with NXP's inclusive language project			
PCA9633_5	20080725	Product data sheet	-	PCA9633_4
PCA9633_4	20080304	Product data sheet	-	PCA9633_3
PCA9633_3	20061220	Product data sheet	-	PCA9633_2
PCA9633_2	20061114	Product data sheet	-	PCA9633_1
PCA9633_1 (9397 750 14614)	20060123	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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