Complementary N & P-Channel Power MOSFET

FEATURES

- Low gate charge for fast power switching
- 100% UIS and R_g tested
- Compliant to RoHS directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

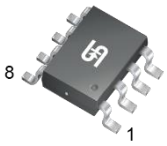
APPLICATIONS

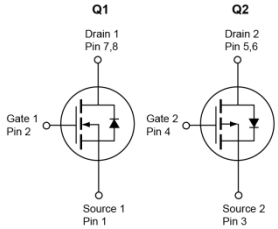
- Building technologies
- DC Fan
- Motor drives

KEY PERFORMANCE PARAMETERS				
PARAMETER		**TYPE**	**VALUE**	**UNIT**
V_{DS}		Q1	60	V
		Q2	-60	
$R_{DS(on)}$ (max)	V_{GS} = 10V	Q1	103	mΩ
	V_{GS} = 4.5V		122	
	V_{GS} = -10V	Q2	180	
	V_{GS} = -4.5V		220	
Q_g		Q1	4.4	nC
		Q2	4.6	

Pb-Free RoHS COMPLIANT HALOGEN FREE

SOP-8





Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)					
PARAMETER		**SYMBOL**	**Q1**	**Q2**	**UNIT**
Drain-Source Voltage		V_{DS}	60	-60	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	T_C = 25°C	I_D	5	-4	A
	T_A = 25°C		2.5	-2	
Pulsed Drain Current (Note 1)		I_{DM}	20	-16	A
Single Pulse Avalanche Current (Note 2)		I_{AS}	6.8	-7	A
Single Pulse Avalanche Energy (Note 2)		E_{AS}	6.9	7.4	mJ
Total Power Dissipation	T_C = 25°C	P_D	5.7	5.7	W
	T_C = 125°C		1.1	1.1	
Total Power Dissipation	T_A = 25°C	P_D	1.4	1.4	W
	T_A = 125°C		0.3	0.3	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150		°C

THERMAL PERFORMANCE			
PARAMETER	**SYMBOL**	**MAXIMUM**	**UNIT**
Thermal Resistance – Junction to Case	$R_{\Theta JC}$	22	°C/W
Thermal Resistance – Junction to Ambient	$R_{\Theta JA}$	88	

Thermal Performance Note: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JC}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. The $R_{\Theta JA}$ limit presented here is based on mounting on a 1 in^2 pad of 2 oz copper.

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)							
PARAMETER	**CONDITIONS**	**SYMBOL**	**TYPE**	**MIN**	**TYP**	**MAX**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	BV_{DSS}	Q1	60	--	--	V
	V_{GS} = 0V, I_D = -250μA		Q2	-60	--	--	
Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	$V_{GS(TH)}$	Q1	1.2	1.8	2.5	V
	V_{GS} = V_{DS}, I_D = -250μA		Q2	-1	-1.5	-2.5	
Gate-Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	Q1	--	--	±100	nA
	V_{GS} = ±20V, V_{DS} = 0V		Q2	--	--	±100	nA
Drain-Source Leakage Current	V_{GS} = 0V, V_{DS} = 60V	I_{DSS}	Q1	--	--	1	μA
	V_{GS} = 0V, V_{DS} = -60V		Q2	--	--	-1	
Drain-Source On-State Resistance (Note 3)	V_{GS} = 10V, I_D = 2.5A	$R_{DS(on)}$	Q1	--	74	103	mΩ
	V_{GS} = 4.5V, I_D = 2.3A			--	86	122	
	V_{GS} = -10V, I_D = -2A		Q2	--	135	180	
	V_{GS} = -4.5V, I_D = -1.7A			--	170	220	
Forward Transconductance (Note 3)	V_{DS} = 10V, I_D = 2.5A	g_{fs}	Q1	--	10	--	S
	V_{DS} = -10V, I_D = -2A		Q2	--	5	--	
Dynamic (Note 4)							
Total Gate Charge	Q1 V_{DS} = 30V, I_D = 2.5A Q2 V_{DS} = -30V, I_D = -2A	$Q_{g(VGS=10V)}$	Q1	--	9.4	--	nC
			Q2	--	9	--	
Total Gate Charge		$Q_{g(VGS=4.5V)}$	Q1	--	4.4	--	
			Q2	--	4.6	--	
Gate-Source Charge		Q_{gs}	Q1	--	1.8	--	
			Q2	--	1.2	--	
Gate-Drain Charge		Q_{gd}	Q1	--	2.3	--	
			Q2	--	2.4	--	
Input Capacitance	Q1 V_{GS} = 0V, V_{DS} = 30V f = 1.0MHz Q2 V_{GS} = 0V, V_{DS} = -30V f = 1.0MHz	C_{iss}	Q1	--	527	--	pF
			Q2	--	436	--	
Output Capacitance		C_{oss}	Q1	--	31	--	
			Q2	--	32	--	
Reverse Transfer Capacitance		C_{rss}	Q1	--	4	--	
			Q2	--	11	--	
Gate Resistance	f = 1.0MHz	R_g	Q1	0.5	1.8	3.6	Ω
			Q2	5	17	34	
Switching (Note 4)							
Turn-On Delay Time	Q1 V_{GS} = 10V, V_{DS} = 30V, I_D = 2.5A, R_G = 2Ω Q2 V_{GS} = -10V, V_{DS} = -30V, I_D = -2A, R_G = 2Ω	$t_{d(on)}$	Q1	--	5	--	ns
			Q2	--	3.4	--	
Turn-On Rise Time		t_r	Q1	--	21	--	
			Q2	--	21	--	
Turn-Off Delay Time		$t_{d(off)}$	Q1	--	10	--	
			Q2	--	21	--	
Turn-Off Fall Time		t_f	Q1	--	17	--	
			Q2	--	26	--	

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)							
PARAMETER	**CONDITIONS**	**SYMBOL**	**TYPE**	**MIN**	**TYP**	**MAX**	**UNIT**
Source-Drain Diode							
Forward Voltage (Note 3)	V_{GS} = 0V, I_S = 2.5A	V_{SD}	Q1	--	--	1	V
	V_{GS} = 0V, I_S = -2A		Q2	--	--	-1	
Reverse Recovery Time	Q1 I_S = 2.5A, dI/dt = 100A/μs	t_{rr}	Q1	--	14	--	ns
			Q2	--	11	--	
Reverse Recovery Charge	Q2 I_S = -2A, dI/dt = 100A/μs	Q_{rr}	Q1	--	10	--	nC
			Q2	--	6	--	

Notes:

1. Current limited by package.
2. Q1 : L = 0.3mH, V_{GS} = 10V, V_{DD} = 30V, R_G = 25Ω, I_{AS} = 6.8A, Starting T_J = 25°C
   Q2 : L = 0.3mH, V_{GS} = -10V, V_{DD} = -30V, R_G = 25Ω, I_{AS} = -7A, Starting T_J = 25°C
3. Pulse test: Pulse Width ≤ 300μs, duty cycle ≤ 2%.
4. Switching time is essentially independent of operating temperature.

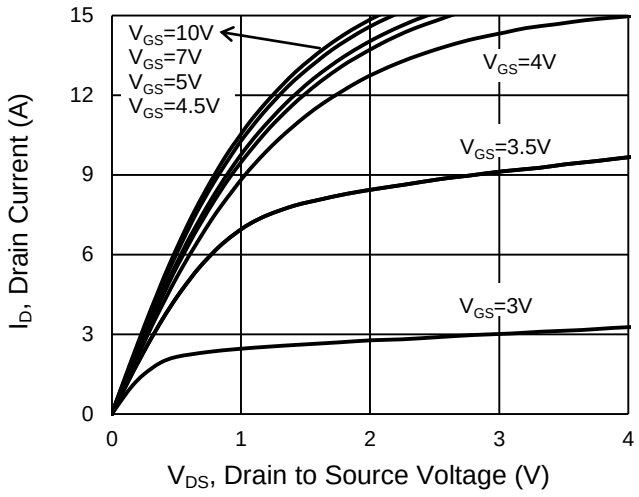
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM8588CS RLG	SOP-8	2,500pcs / 13” Reel

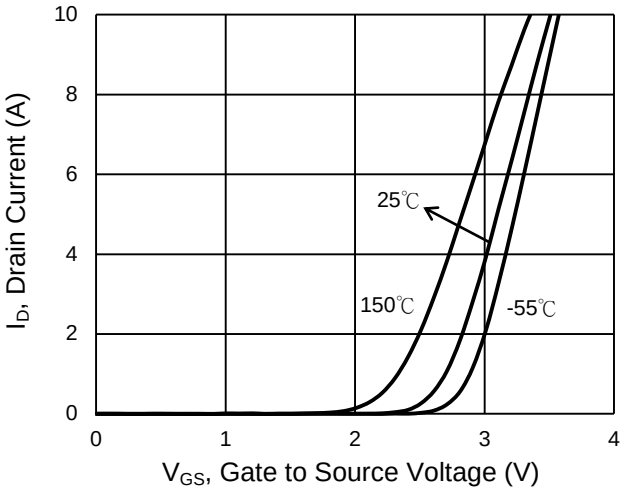
CHARACTERISTICS CURVES (Q1 N-Channel)

(T_A = 25°C unless otherwise noted)

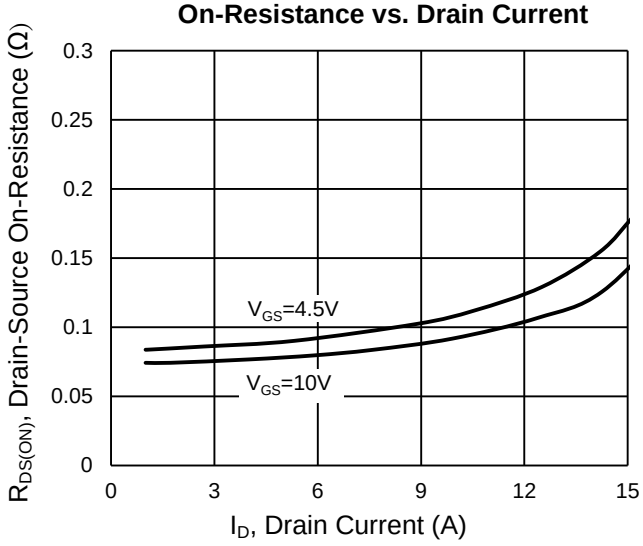
Output Characteristics



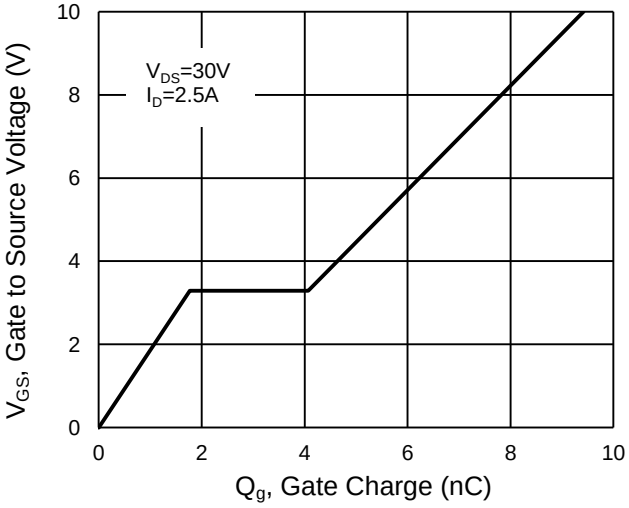
Transfer Characteristics



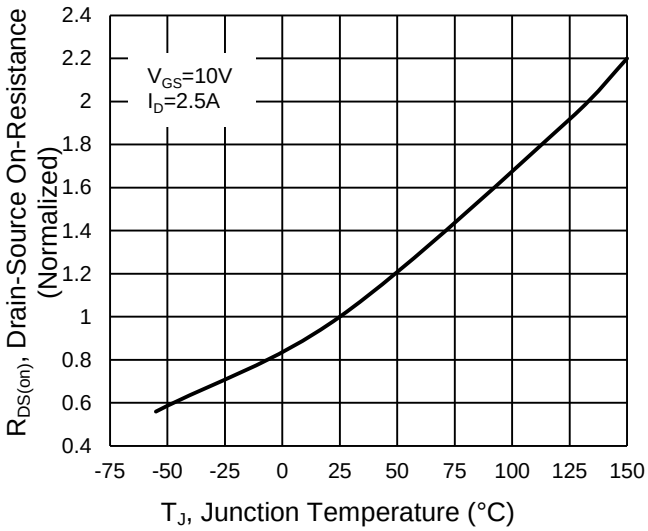
On-Resistance vs. Drain Current



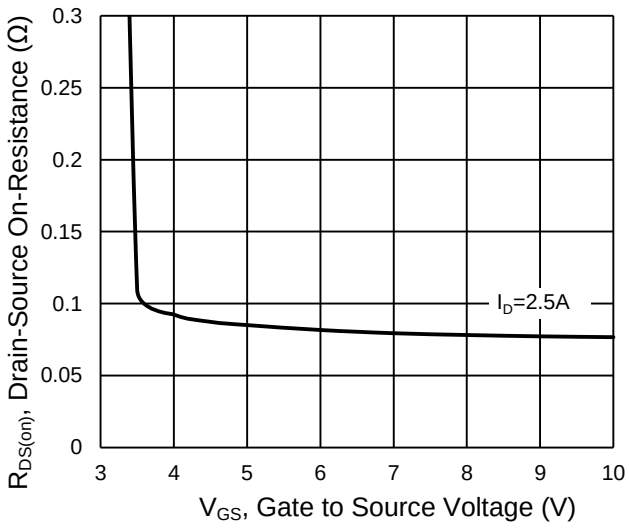
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



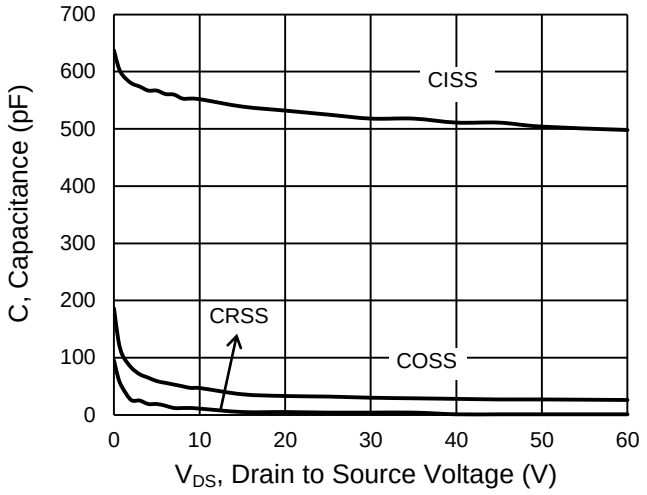
On-Resistance vs. Gate-Source Voltage



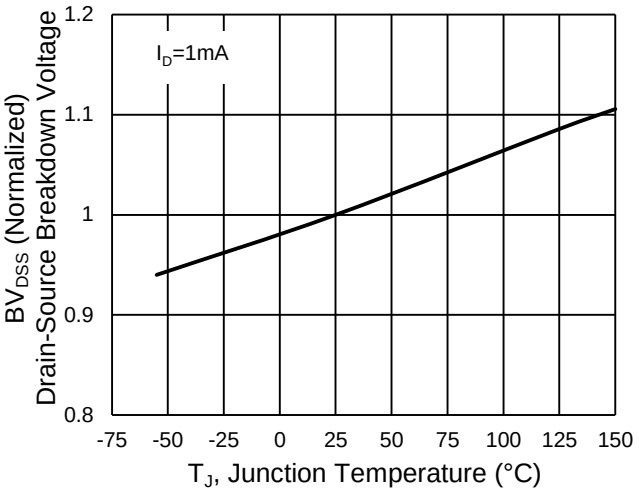
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

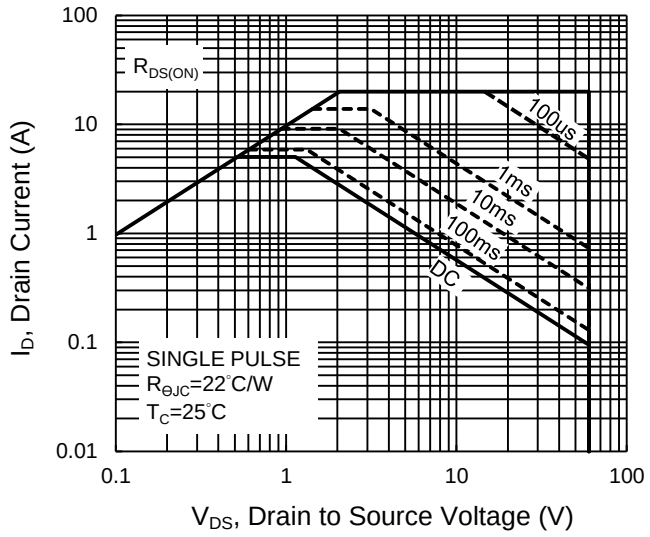
Capacitance vs. Drain-Source Voltage



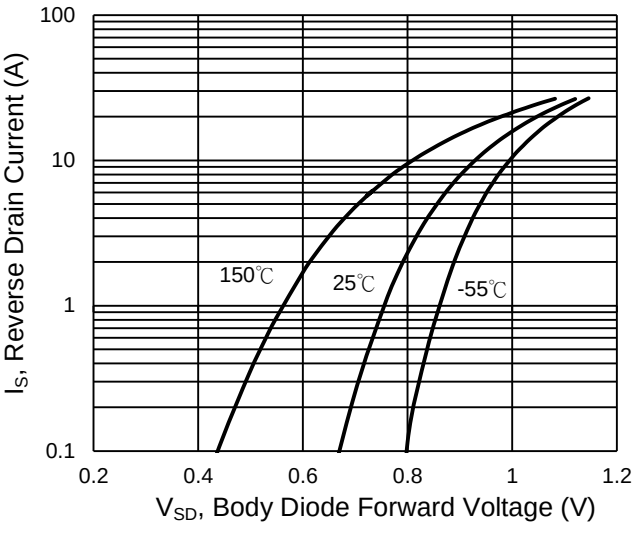
BV_{DSS} vs. Junction Temperature



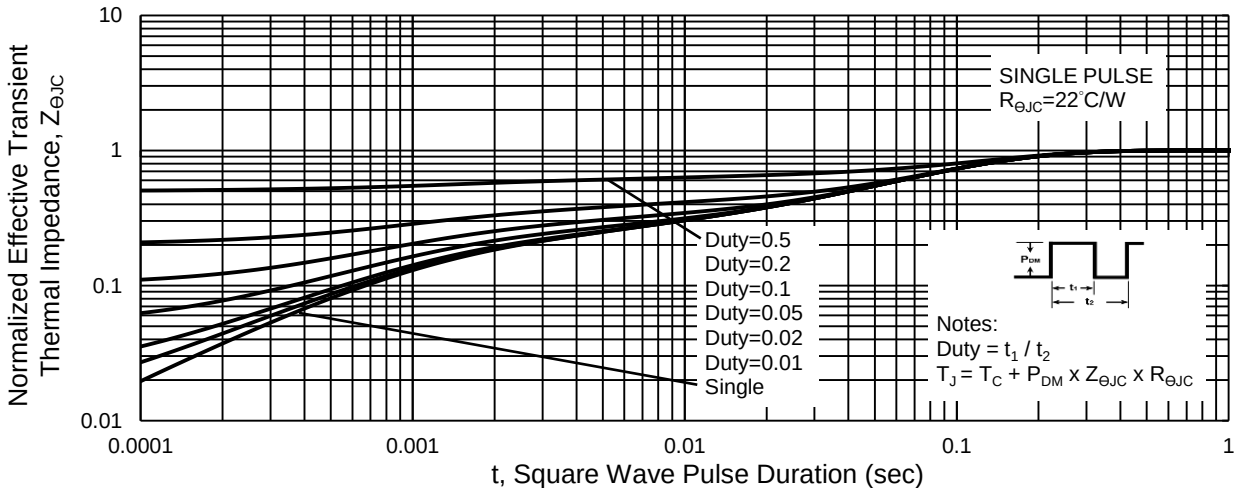
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage



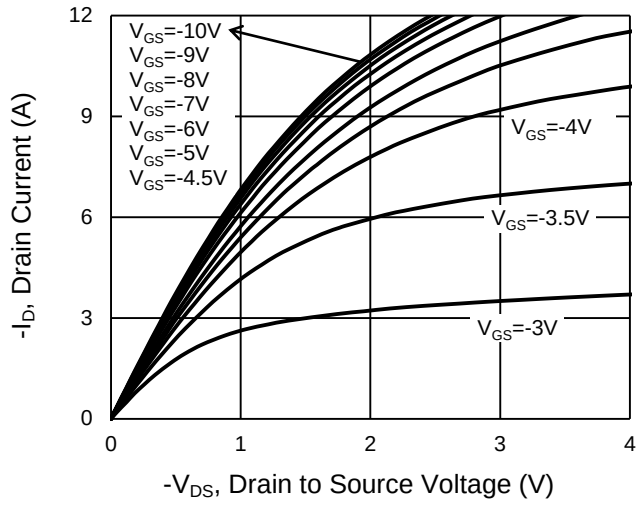
Normalized Thermal Transient Impedance, Junction-to-Case



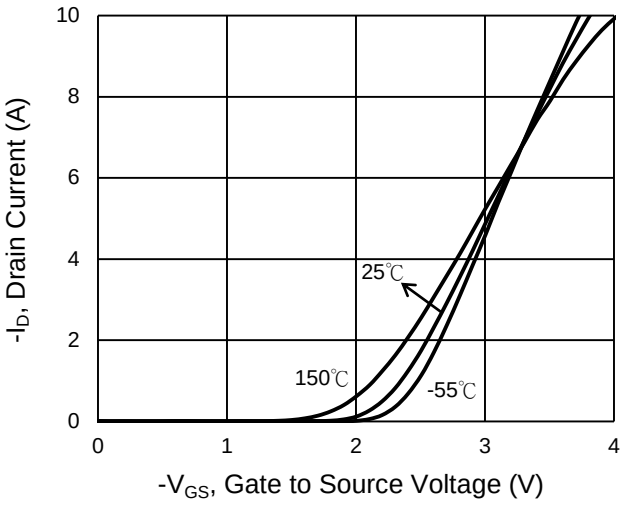
CHARACTERISTICS CURVES (Q2 P-Channel)

(T_A = 25°C unless otherwise noted)

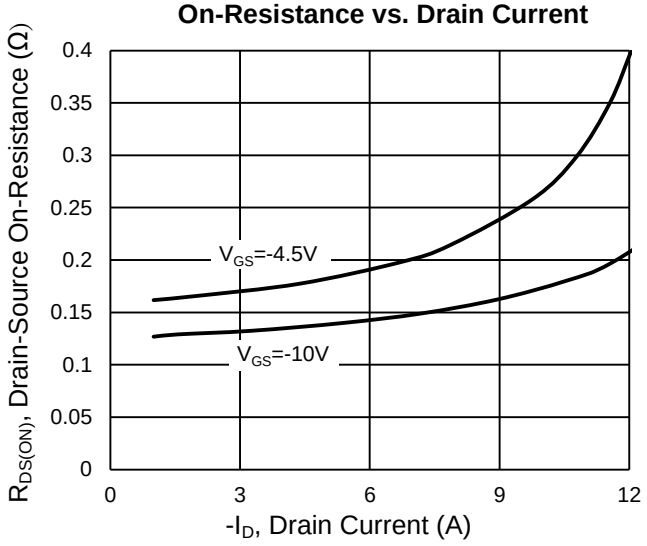
Output Characteristics



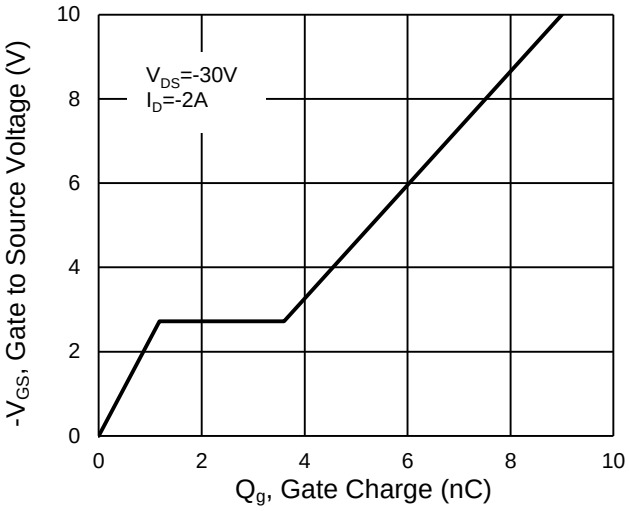
Transfer Characteristics



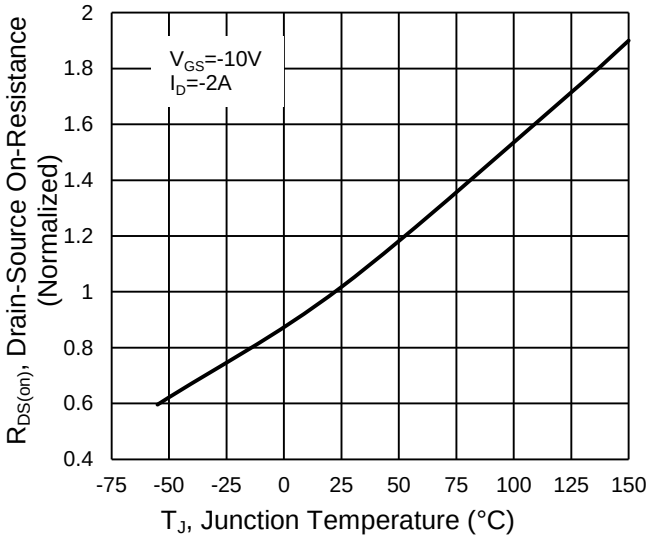
On-Resistance vs. Drain Current



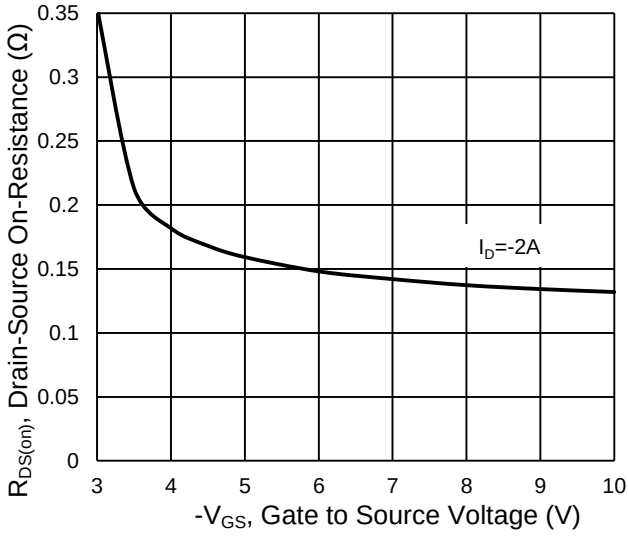
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



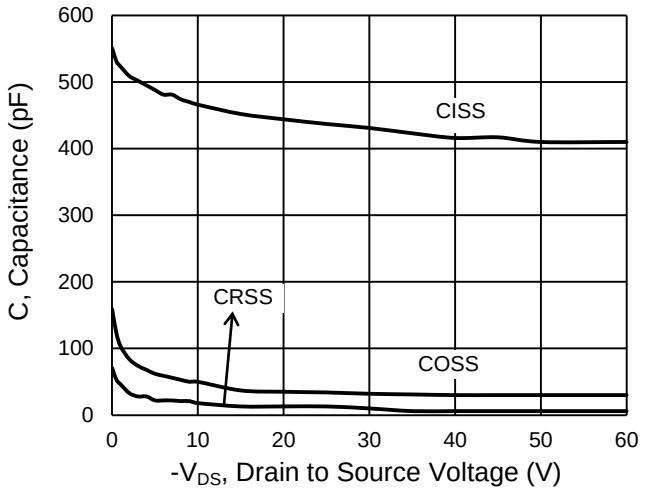
On-Resistance vs. Gate-Source Voltage



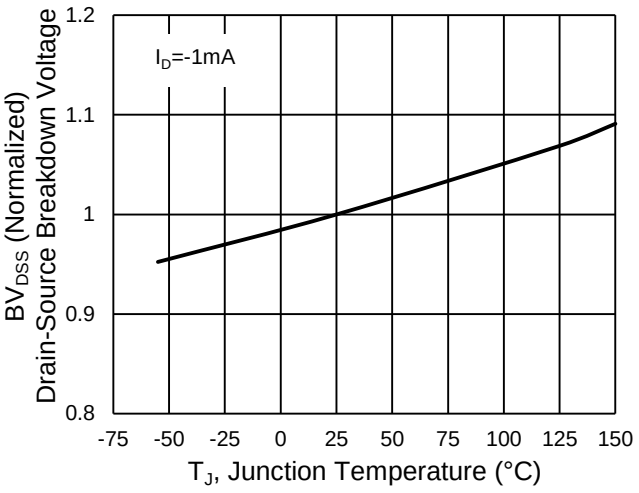
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

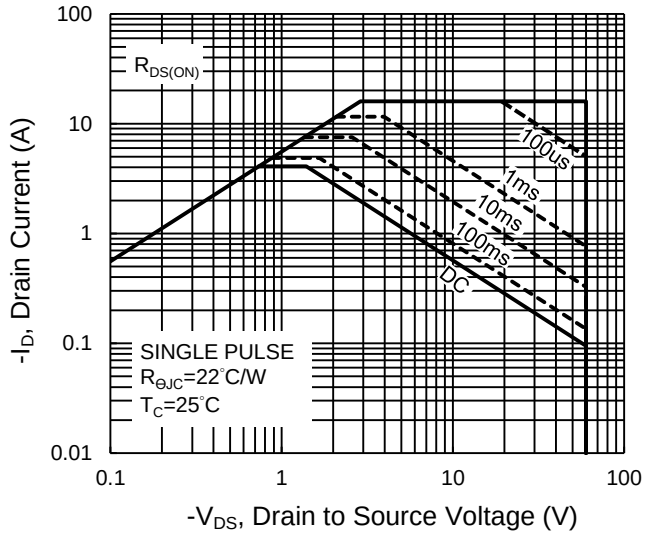
Capacitance vs. Drain-Source Voltage



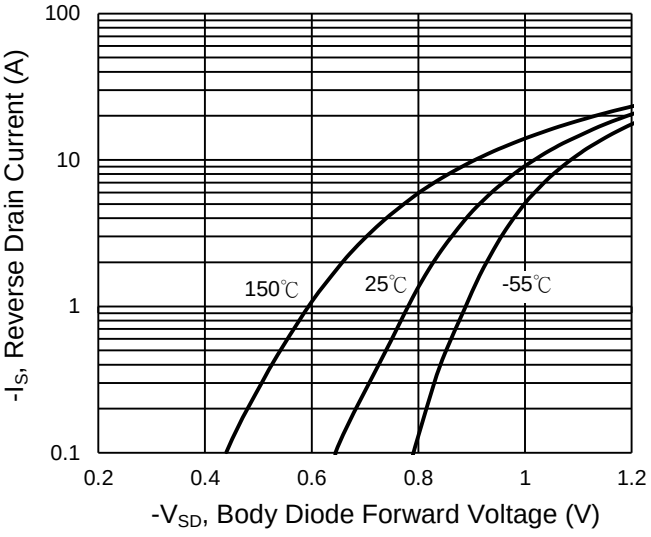
BV_{DSS} vs. Junction Temperature



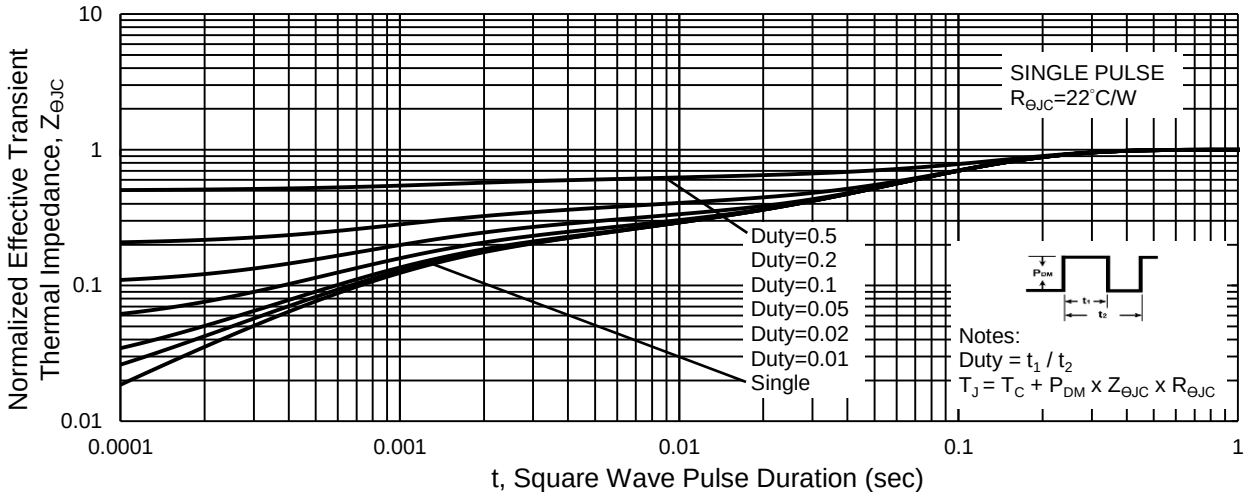
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

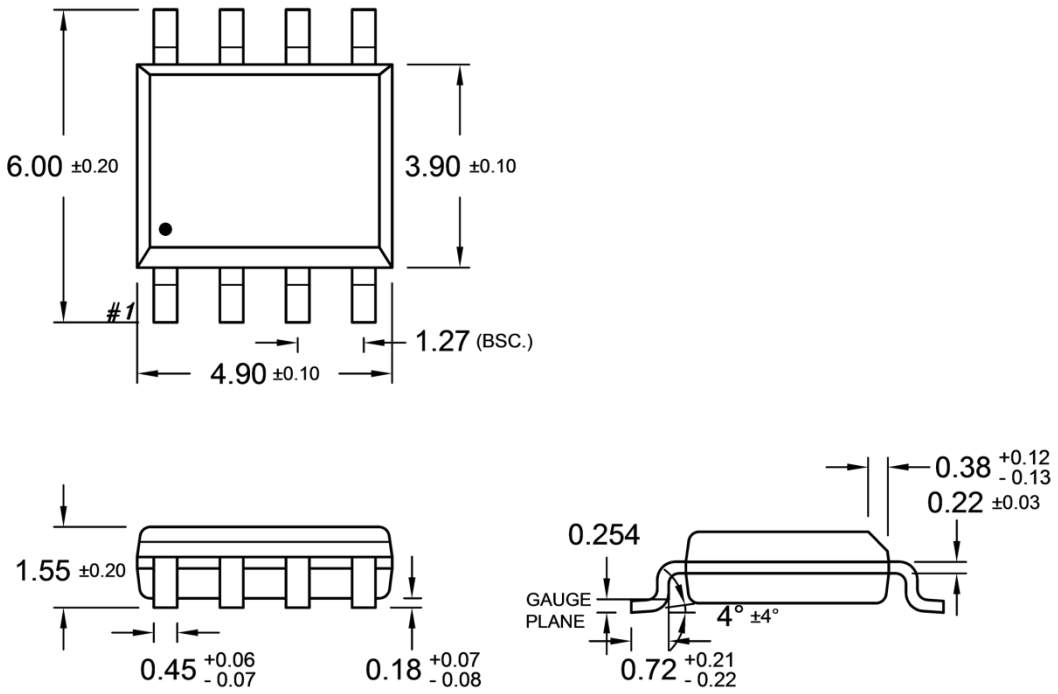


Normalized Thermal Transient Impedance, Junction-to-Case

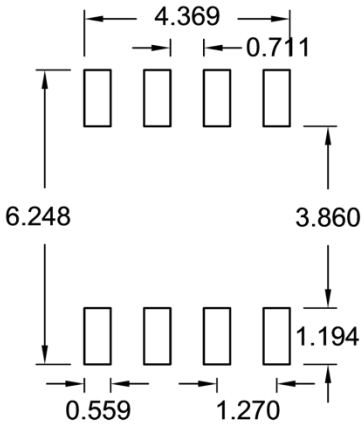


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

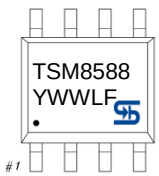
SOP-8



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



Y = Year Code
WW = Week Code (01~52)
L = Lot Code (1~9,A~Z)
F = Factory Code

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