Product Document

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Datasheet

DS000542

4LS

4LS15K, 4LS10K and 4LS5K Line Scan Sensors

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Content Guide

1 General Description

4LS is a family of high-speed line-scan sensors featuring four lines of pixels, spaced with one pixel period line gap. The sensors are provided in Monochrome (B&W) version, allowing amongst other applications 4-To-1 digital TDI or with Red, Green, Blue and Monochrome lines for high quality color line scanning with extended spectral range. Each of the four lines of the sensor has individual gain settings and can be triggered for exposure and reset independently. Moreover, all four lines can be read out simultaneously over bit serial LVDS output taps.

The sensor features a low noise pixel with true CDS and global shutter allowing fully pipelined readout and integration. To enhance dynamic range, multiple nondestructive readouts are possible.

An Invar based sensor chip on board is provided, which features all necessary external decoupling elements and provides mechanical alignment features for high precision self-aligned mounting of the sensors to its optics. Furthermore, the Invar core avoids thermal stress induced bending of the sensors with more important line length.

1.1 Key Benefits, Features and Differentiators

The benefits, features and differentiators of 4LS sensors family (4LS15K, 4LS10K and 4LS5K), are listed below:

Figure 1:
4LS Benefits, Features and Differentiators

Benefits	Features	Differentiators
Allows full RGB color acquisition, plus additional mono channel	Up to four simultaneously and individually operated lines.	Fastest high-resolution sensor on the market operating four lines simultaneously.
Higher machine production speed	High speed up to 119 kLines/s x 4 Lines at full resolution. Up to 238 kLines/s x 4 Lines with ROI feature (1).	Competing four-line sensors only allow simultaneous readout of two lines.
Lower pin count integration for lower speed applications	Configurable output bandwidth.	Cost versus performance trade of possibility.
Configurable full well	Up to 40 ke-	
COB/Invar package	High mechanical stability and planarity of the die.	

(1) 4LS5K main feature, due to reduced readout resolution. For more details, please check section 7.11.5.

1.2 Applications

- Machine vision
- Document scanner
- Print inspection (i.e. glass, PCB, LCD)
- High end web inspection
- Food sorting / inspection
- Battery inspection

1.3 Block Diagram

The functional blocks of the different variants are shown below on Figure 2, Figure 3 and Figure 4. Figure 5 shows a detailed block diagram for a single 2K5 segment.

Figure 2:
4LS15K Sensor's Functional Blocks

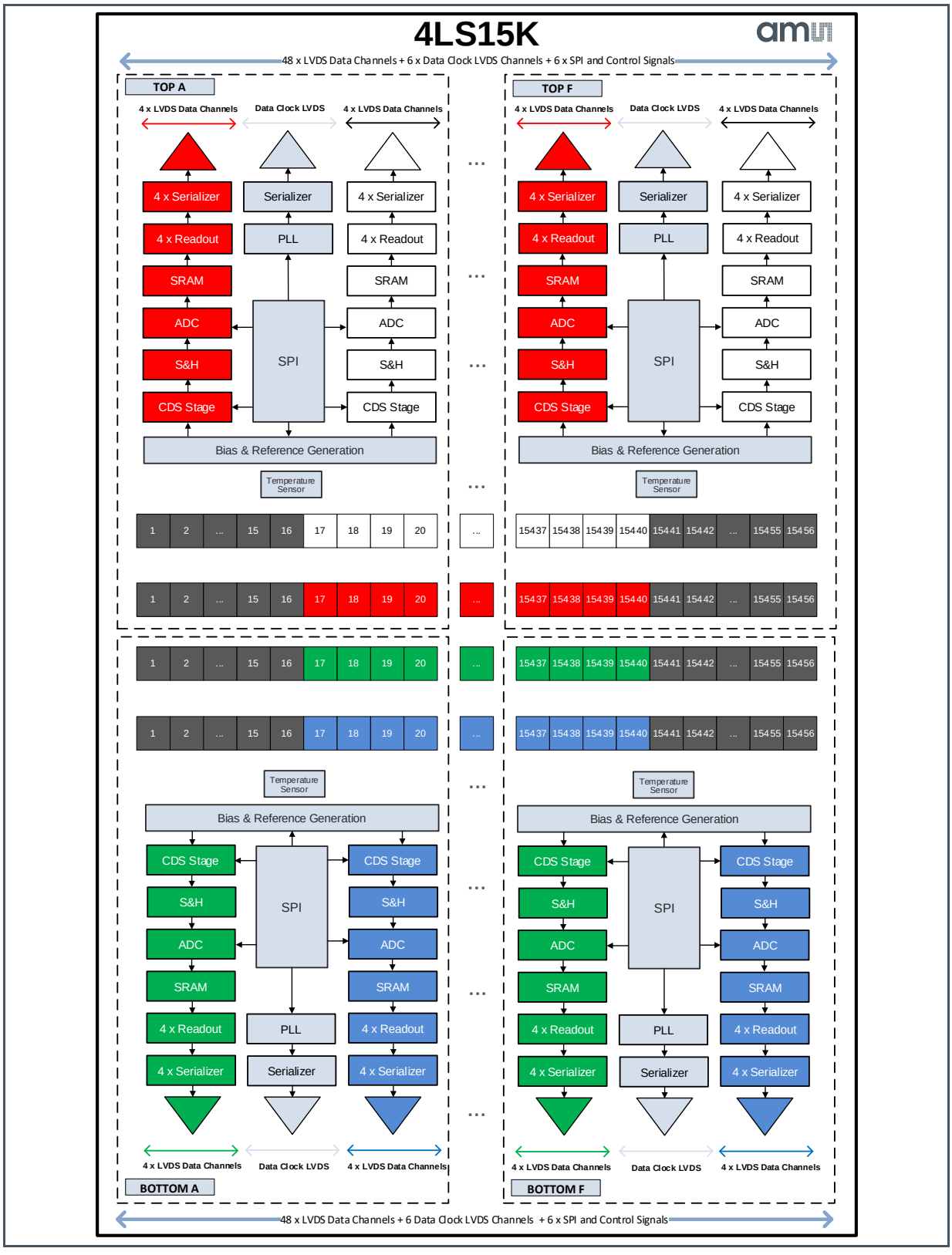


Figure 3:
4LS10K Sensor's Functional Blocks

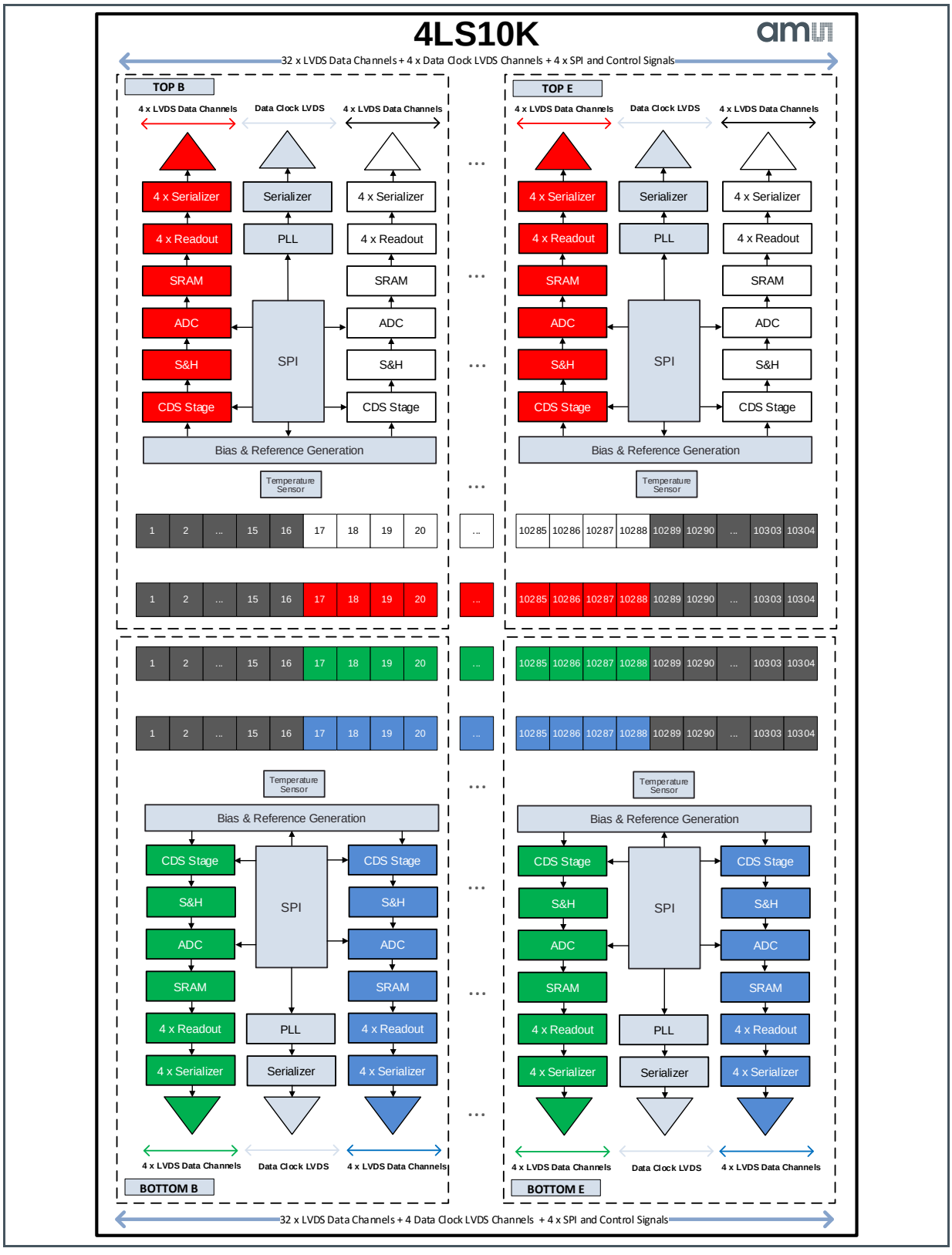


Figure 4:
4LS5K Sensor's Functional Blocks

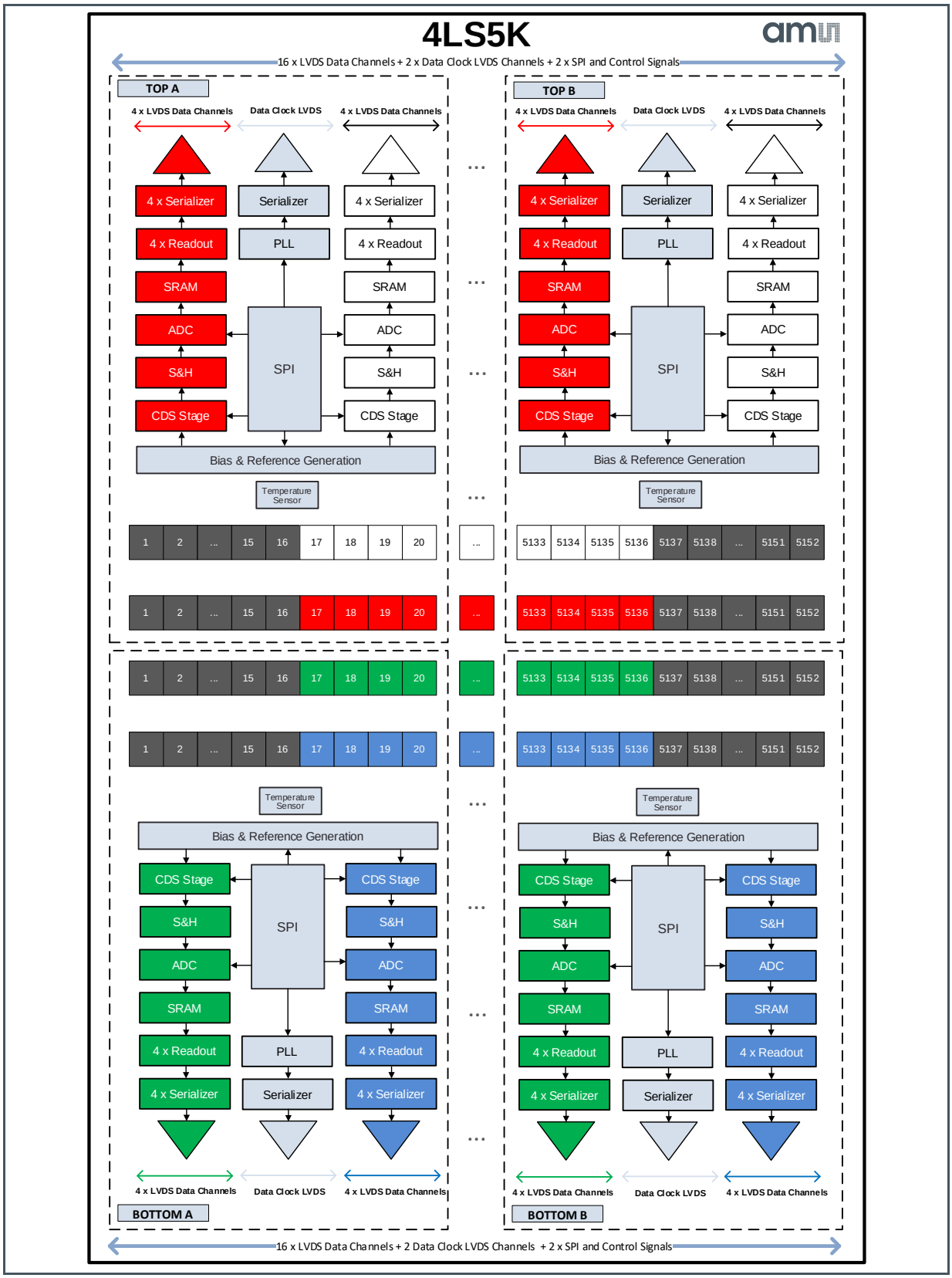
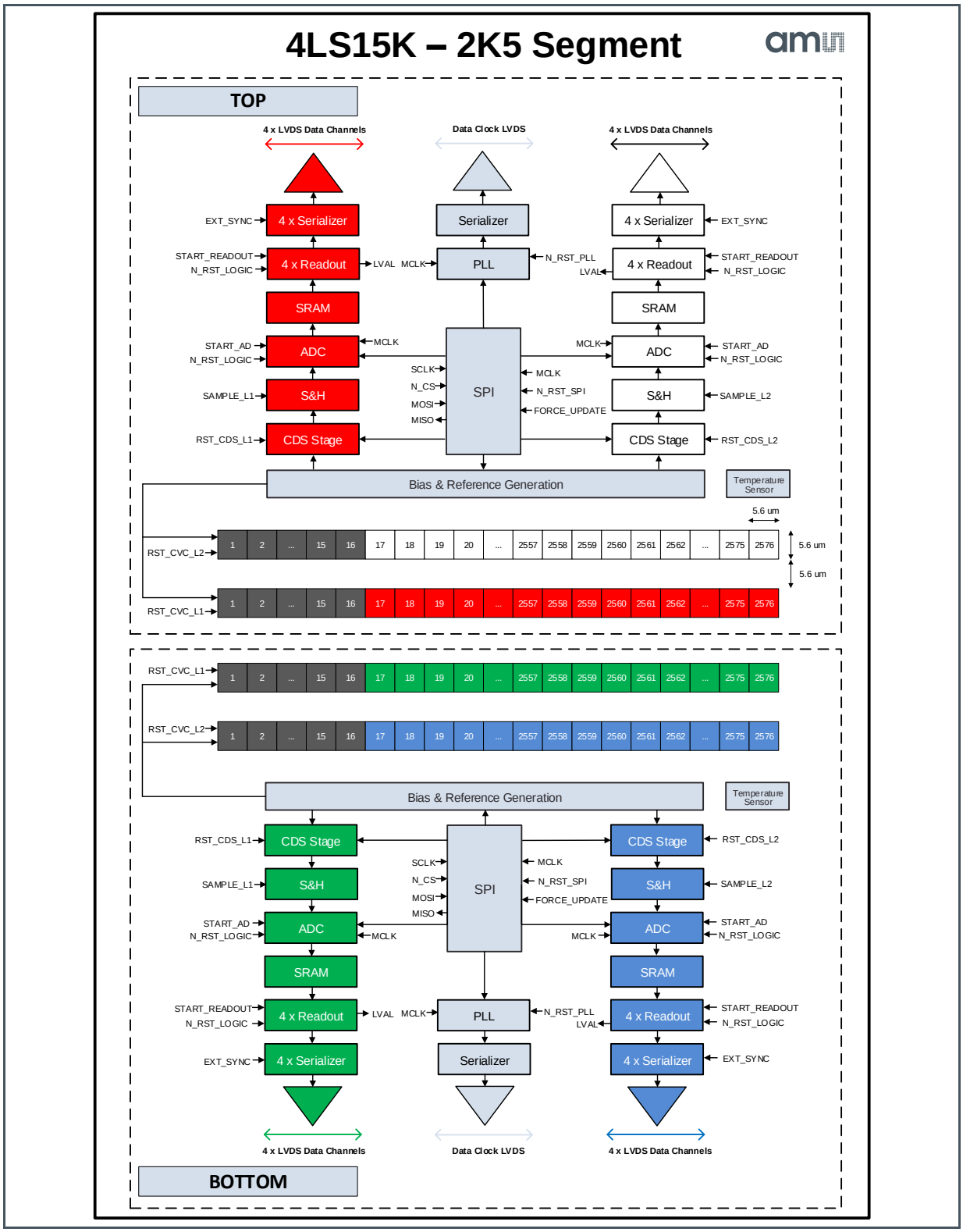


Figure 5:
4LS15K Sensor's Functional Blocks – First 2K5 Segment in Detail



1.4 4LS Device

The images below show the front view of the different 4LS sensor variants.

Figure 6:
4LS15K RGB + Monochrome Variant

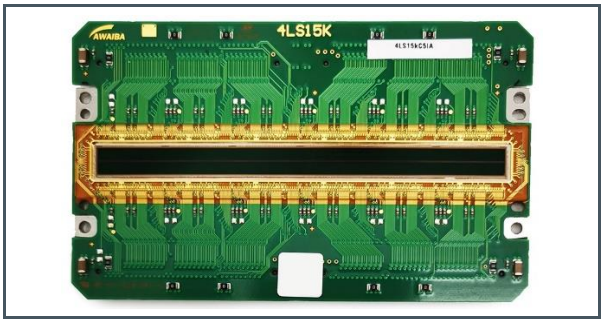


Figure 7:
4LS15K Monochrome Variant

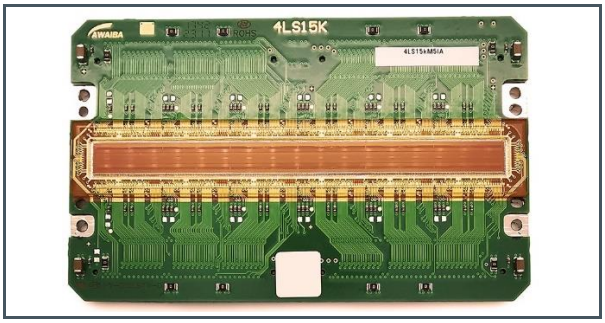


Figure 8:
4LS10K RGB + Monochrome Variant

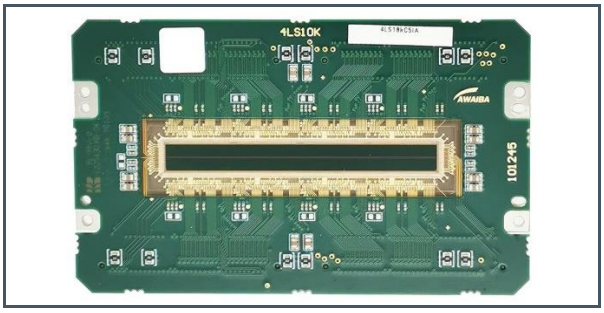


Figure 9:
4LS10K Monochrome Variant

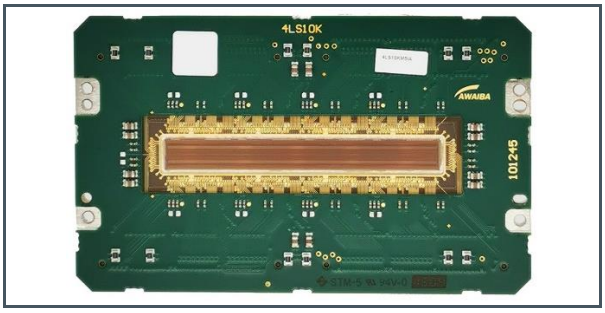


Figure 10:
4LS5K RGB + Monochrome Variant

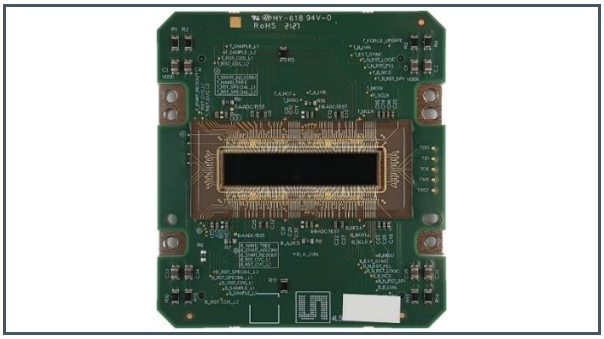
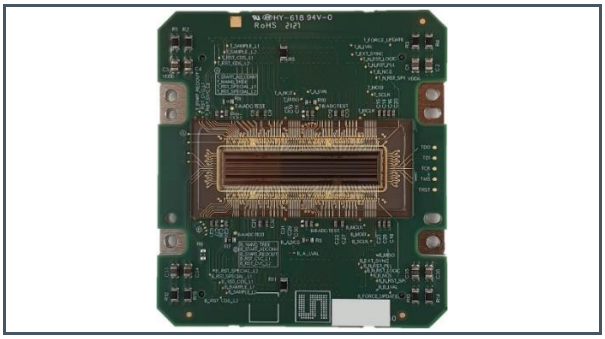


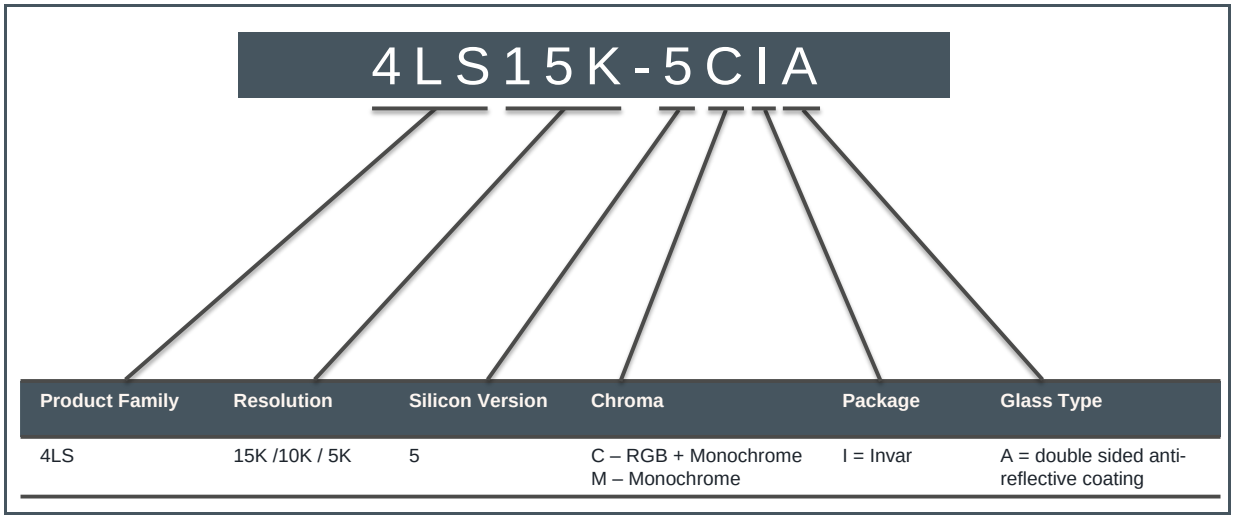
Figure 11:
4LS5K Monochrome Variant



2 Ordering Information

Part #	Ordering Code	Package	Chroma	Delivery Form	Delivery Quantity	Status
508030006	4LS15K-5CIA	Invar	RGB + Monochrome	Tray	2 pcs/tray	Released
507830006	4LS15K-5MIA	Invar	Monochrome	Tray	2 pcs/tray	Released
508080005	4LS10K-5CIA	Invar	RGB + Monochrome	Tray	2 pcs/tray	Released
508070005	4LS10K-5MIA	Invar	Monochrome	Tray	2 pcs/tray	Released
508120002	4LS5K-5CIA	Invar	RGB + Monochrome	Tray	4 pcs/tray	Released
507830007	4LS5K-5MIA	Invar	Monochrome	Tray	4 pcs/tray	Released

Figure 12:
Ordering Code Scheme



3 Pin Assignment

3.1 Pin Diagram

The sensor package for 4LS15K, 4LS10K and 4LS5K resolutions is based on a COB of FR4 material. The die is bonded on an Invar enforcement core through a cavity in the FR4 material. This assembly guarantees high mechanical stability and planarity of the die. Due to the limited heat dissipation capability of the Invar core, a low temperature resistance heat sink should be assembled with maximum contact surface to the back side of the Invar core. The connector (KEL) used on the sensor headboard is DY01-140S and its mating part is DY11-140FS (optionally can be used DY11-140S).

Figure 13:
Pin Numbering for 15K and 10K (Back View)

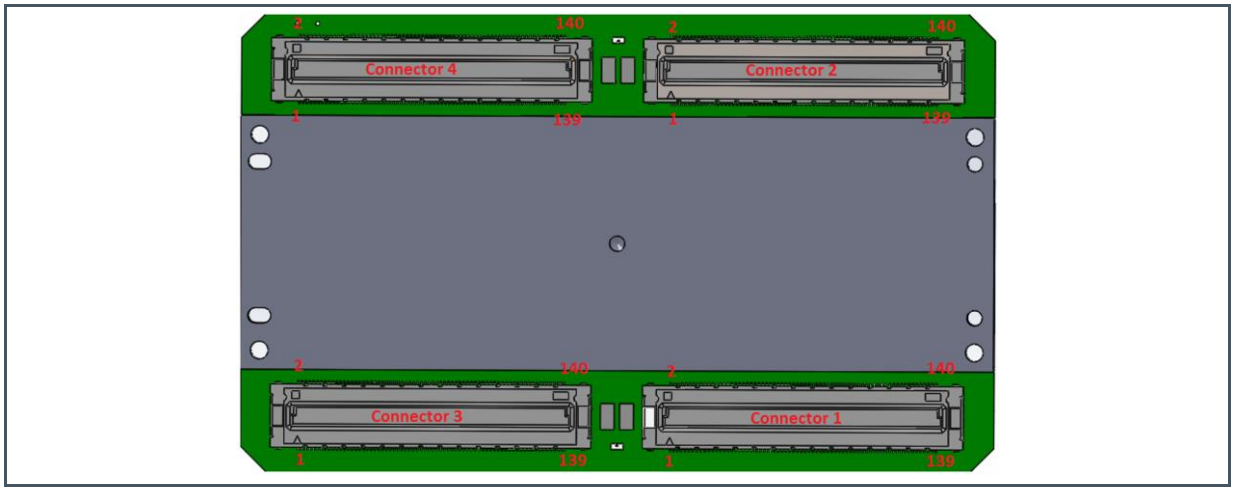


Figure 14:
Pin Numbering for 5K (Back View)

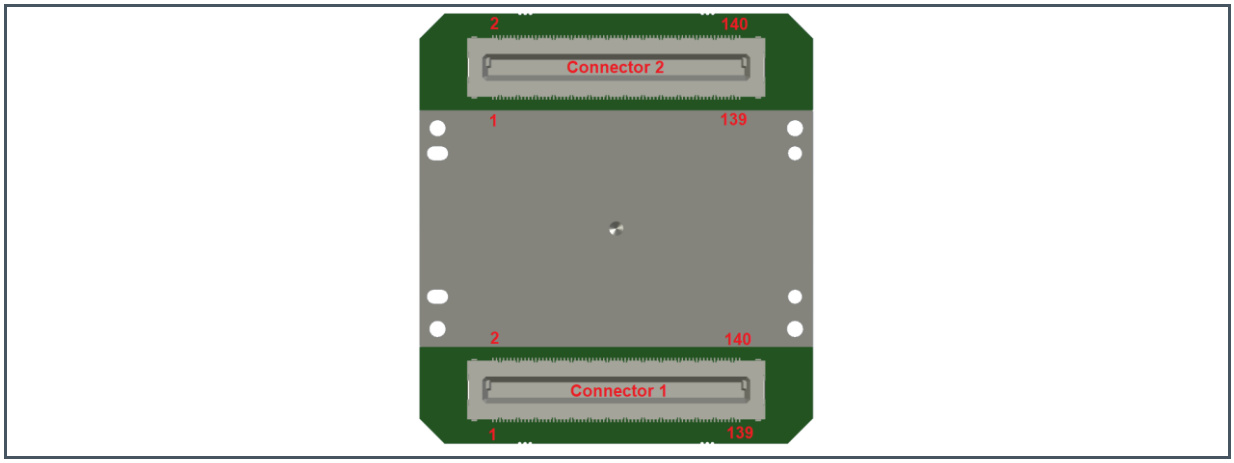


Figure 15:
Segment Usage per Connector

Segment	A	B	C	D	E	F
4LS15K / 4LS10K(1)	Connectors 1 & 2				Connectors 3 & 4	
4LS5K(2)	Connectors 1 & 2				Not used	

(1) 4LS10K uses all four connectors but only reads out data from segment B, C, D and E.
(2) 4LS5K uses only connectors 1 and 2, once only has A and B segments.

Please refer to Pin Description section, to check 4LS15K, 4LS10K and 4LS5K pinout assignment.

4 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 16
Absolute Maximum Ratings of 4LS

Symbol	Parameter		Min	Max	Unit	Comments
Electrical Parameters						
VDDD	Supply voltage to ground		-0.3	2.1	V	
VDDA	Supply voltage to ground		-0.3	3.6	V	
VIO	Input / output pin voltage to digital Inputs		VSSD-0.3	2.4	V	
IIO	Input / output DC forward bias current		-5	100	mA	
I_{SCR}	Input current (latch-up immunity)		±100		mA	JEDEC JESD78-E
Continuous Power Dissipation (at T_J = 85 °C)						
P_{T-15K}	Continuous power dissipation			11.5	W	
P_{T-10K}				7.7	W	
P_{T-5K}				3.85	W	
Electrostatic Discharge						
ESD_{HBM}	Electrostatic discharge HBM		± 2		kV	Class 2 Device - JEDEC JS-001-2017
Temperature Ranges						
T_A	Operating ambient temperature		N/A	N/A	°C	Not applicable. T_A has to be lower than T_J such that, when self-heating (s.h.) is included, T_A + s.h.≤ T_J. T_J must be respected.
$R_{TH, JC}$[1]	Junction to case thermal resistance	4LS15K		0.8	°C/W	See Note[2]
		4LS10K		1.2		
		4LS5K		2.4		
T_J	Operating junction temperature		0	85	°C	
Storage Conditions						
T_{STRG}	Storage temperature range			30	°C	
RH_{NC_STRG}	Long term storage humidity			60	%	
	Shelf life			4	years	

(1) Please refer to section 7.13 to readout the junction temperature in application. This is to ensure proper functioning of the device over lifetime.

(2) **Important:** Thermal resistance of sensor typically is only small contributor to total thermal budget.

5 Electrical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 17:
Electrical Characteristics of 4LS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDA	Analogue power supply		3.2	3.3	3.4	V
V_{nrms}VDDA	RMS noise on VDDA				5	mV
V_{npp}VDDA	Peak to peak noise on VDDA				20	mV
$VDDD_x$	Power supply voltage (Digital, LVDS)		1.7	1.8	1.9	V
$V_{nrms}VDDD_x$	RMS noise on $VDDD_x$				10	mV
$V_{npp}VDDD_x$	Peak to peak noise on $VDDD_x$				40	mV
VDDIO	Power supply voltage on IO's		1.7	1.8	1.9	V
V_{nrms}VDDIO	RMS noise on VDDIO				10	mV
V_{npp}VDDIO	Peak to peak noise on VDDIO				60	mV
VSSA	Ground for analogue power supply			0		V
$VSSD_x$	Ground for digital power supply			0		V
VSSIO	Ground for IO power supply			0		V
MCLK	Input clock frequency				60 @12-bit 80 @8-bit	MHz
T_{MCLK}	Input clock period		16.67 @ 12-bit 12.5 @ 8-bit			ns
Duty Cycle	Input clock duty cycle		45	50	55	%
Jitter Clock	Input clock jitter (peak to peak)				100	ps
C_{Load}	Load capacitance on digital IO's				10	pF
LVDS Output Interface						
V_{CM}	Common mode output voltage	Considering an expected resistor of 100 Ω at the receiver	1		1.2	V
I_o	Output current	Register configurable	0.8		2.8	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{slew, rising}$	Output slew rate of rising edge		250		750	ps
$T_{slew, falling}$	Output slew rate of falling edge		250		750	ps
V_{ODiff}	Differential output voltage		80		350	mV
Characteristics for CMOS-LVTTL Outputs						
V_{OL}	Low level output Voltage		0		0.6	V
V_{OH}	High level output voltage		VDDIO-0.6		VDDIO+0.3	V
$T_{slew, rising}$	Output slew rate of rising edge		2		10	ns
$T_{slew, falling}$	Output slew rate of falling edge		2		10	ns
Characteristics for CMOS-LVTTL Inputs						
V_{IL}	Low level input voltage		0		0.6	V
V_{IH}	High level input voltage		VDDIO-0.6		VDDIO+0.3	V
$T_{slew, rising}$	Input slew rate of rising edge		0		½ MCLK	ns
$T_{slew, falling}$	Input slew rate of falling edge		0		½ MCLK	ns
T_{Setup}	Setup time		2			ns
T_{Hold}	Hold time		4			ns
Power Consumption [(1)(2)]						
$P_{15K\text{-}12\text{-}bit\text{-}1\text{-}To\text{-}1}$	Sensor power consumption for the MCLK frequencies	12-bit @ 60 MHz		9.49	11	W
$P_{10K\text{-}12\text{-}bit\text{-}1\text{-}To\text{-}1}$				6.36	7.4	W
$P_{5K\text{-}12\text{-}bit\text{-}1\text{-}To\text{-}1}$				3.16	3.67	W
$P_{15K\text{-}8\text{-}bit\text{-}1\text{-}To\text{-}1}$		8-bit @ 80 MHz		9.63	11.5	W
$P_{10K\text{-}8\text{-}bit\text{-}1\text{-}To\text{-}1}$				6.45	7.7	W
$P_{5K\text{-}8\text{-}bit\text{-}1\text{-}To\text{-}1}$				3.21	3.85	W
P_{IDLE} [(3)]				0.03	0.15	W

(1) Typical power values, the sensor temperature is approximately at 60 ºC.
(2) Maximum power values considers the sensor working at the maximum line rate for at maximum temperature of 85 ºC.
(3) Idle mode considers the sensor working after the power up of all powers, with all the sensor lines in reset.

When designing the power supply system regulators for 4LS VDDA and VDDD voltages, please take in consideration the below respective recommended values for the current, I_{VDDA} and I_{VDDD}. It is given a safe margin to not be close the minimum required.

- 4LS15K: $I_{VDDD} \geq 2$ A and $I_{VDDA} \geq 3$ A
- 4LS10K: $I_{VDDD} \geq 1.5$ A and $I_{VDDA} \geq 2.5$ A
- 4LS5K: $I_{VDDD} \geq 1$ A and $I_{VDDA} \geq 2$ A

6 Typical Operating Characteristics

6.1 Electro-Optical Characteristics

Below are the typical electro-optical specifications of 4LS.

Figure 18:
Optical Characteristics of 4LS

Parameter	Value	Remark
Pixel size	5.6 x 5.6 µm^2	
Pixel pitch x	5.6 µm	Distance from the center of a pixel to the center of the adjacent pixel (horizontal axis)
Pixel pitch y	11.2 µm	Distance from the center of a pixel to the center of the adjacent pixel (vertical axis)
Pixel type	Global shutter	Low noise pixel with true CDS
Shutter type	Pipelined global shutter	Exposure of next image during readout of the previous image
Number of accessible pixels per line	N x 2576 pixels	N = 2, 4 or 6 pending on the variant
Number of light sensitive pixels per line	(N x 2576 – 32) pixels	Total number of pixels of a line minus 32 electrical black pixels
Fill factor	95%	
Full well capacity (FWC)	10/20/40ke-	Range adjusted over CVC, CDS gain, ADC mode and ADC ramp
Line Rate 12-bit transmission mode	80 k Lines/s	Maximum MCLK = 60 MHz
Line Rate 8-bit transmission mode	119 kLines/s 238 kLines/s	Maximum MCLK = 80 MHz Using ROI feature for 4LS5K @ 80 MHz(1)
Integration time	1 µs	Minimum value
Down Time for Integration (DTI)(2)	1 µs + 8 x T_{MCLK} @ 12-bit 1.25 µs + 12 x T_{MCLK} @ 8-bit	Minimum values for 12-bit@60MHz and 8-bit@80MHz 1 µs and 1.25 µs are the time between rising and falling edge of RST_CDS Additional T_{MCLK} pulses are between falling edge SAMPLE and rising edge RST_CDS
ADC resolution	12-bit or 8-bit	Adjusted in accordance with the line rate and transmission mode
Color filters	Optional	RGB + Mono
Sensor planarity	30 µm	
Cover glass	D263Teco	

(1) 4LS5K main feature, due to reduced readout resolution. For more details, please check section 7.11.5.
(2) Please check Section 7.11.1 for more detailed information.

Figure 19:
Electro-Optical Characteristics of 4LS Monochrome(1)(2)

Parameter	12-bit @ 60 MHz	8-bit @ 80 MHz	Unit	Variant
Full Well Capacity	22.21	10.58	ke-	
QE @ 530 nm	60.81	54.09	%	
Conversion Gain	0.1612	0.0218	DN/e-	
Responsivity	0.098 82.46	0.01179 9.86	DN/ph DN/nJ/cm^2	
Temporal Dark Noise	8.18 50.75	1.01 46.20	DN e-	
FSD	3580	231	DN	
Dynamic Range	52.82	47.20	dB	
SNR_{Max}	43.19	39.35	dB	
DSNU	15.30 9.16 3.68	2.07 1.25 0.71	DN	15K 10K 5K
PRNU	1.02 0.87 0.92	1.2 0.97 0.93	%	15K 10K 5K

(1) The results were obtained using 530 nm illumination. The ADC ramp gain was adjusted to the equivalent of 1 V swing, for 12-bit ADC mode, and 0.5 V swing for 8-bit ADC mode (therefore, approximately half of FWC for 8-bit). The sensors temperature was approximately 60ºC (uncontrolled temperature environment). The values presented are for the default configuration of Full Well around 20 ke- (STS3 Register bits [3:0] = 0x0). Sensor supply levels were the typical ones: VDDA = 3.3 V and VDDD = 1.8 V. The set Readout mode was 1-To-1. DSNU and PRNU results were characterized for each variant. The remaining parameters are valid for all variants, once they all share the same silicon.

(2) The settings used to get these values are those recommended by the European Machine Vision Association standard 1288 from the Machine Vision Sensors and Cameras. https://www.emva.org/standards-technology/emva-1288/

Figure 20:
Electro-Optical Characteristics of 4LS RGB for 12-Bit Transmission Mode(1)(2)

Parameter	Red	Green	Blue	Unit	Variant
Full Well Capacity	21.56	21.12	19.61	ke-	
QE @ nm	55.97	42.69	40.71	%	
Conversion Gain	0.171	0.175	0.1930	DN/e-	
Responsivity	0.094 93.05	0.075 63.11	0.07859 59.55	DN/ph DN/nJ/cm^2	
Temporal Dark Noise	8.17 47.78	7.66 43.77	10.65 55.18	DN e-	
FSD	3687	3696	3785	DN	
Dynamic Range	53.08	53.67	51.01	dB	
SNR_{Max}	42.90	42.87	42.55	dB	
DSNU	13.35 8.05 3.97	13.52 8.57 6.93	15.15 8.24 5.10	DN	15K 10K 5K
PRNU	0.83 0.81 0.68	0.90 0.80 0.69	0.92 0.79 0.73	%	15K 10K 5K

(1) The results were obtained using 625 nm, 530 nm, and 470 nm illumination for the red, green and blue lines, respectively. The ADC ramp gain was adjusted to the equivalent of 1 V swing, for 12-bit ADC mode at 60 MHz (MCLK). The sensors temperature was approximately 60 ºC (uncontrolled temperature environment). The values presented are for the default configuration of Full Well around 20 ke- (STS3 Register bits [3:0] = 0x0). Sensor supply levels were the typical ones: VDDA = 3.3 V and VDDD = 1.8 V. The set Readout mode was 1-To-1. DSNU and PRNU results were characterized for each variant. The remaining parameters are valid for all variants, once they all share the same silicon.

(2) The settings used to get these values are those recommended by the European Machine Vision Association standard 1288 from the Machine Vision Sensors and Cameras. https://www.emva.org/standards-technology/emva-1288/

6.2 Spectral Characteristics

Figure 21:
4LS Monochrome QE(1)(2)

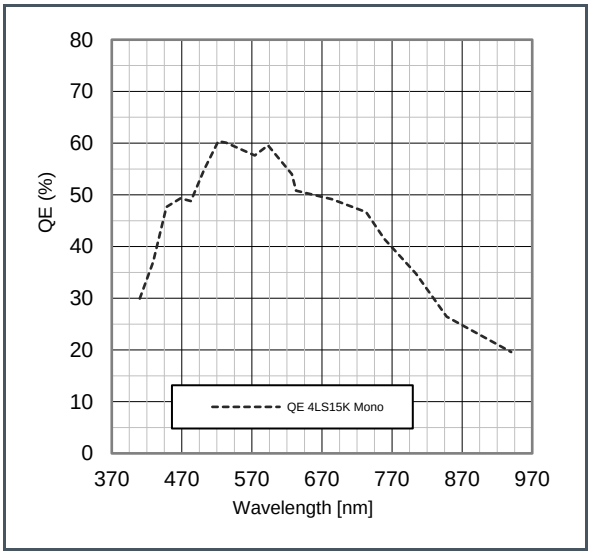
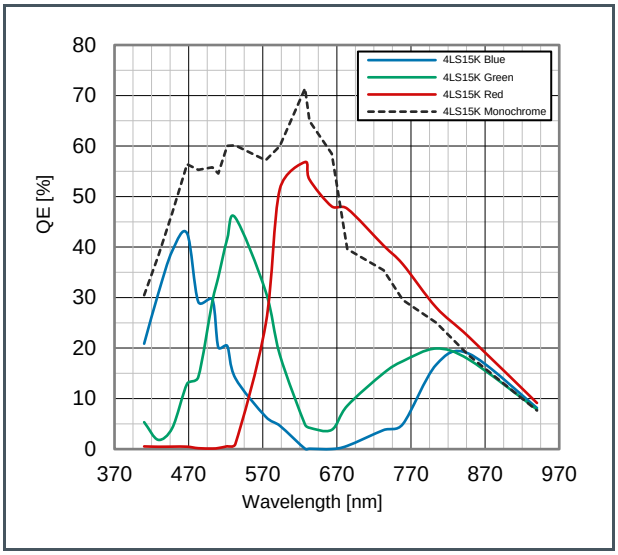


Figure 22:
4LS RGB + Monochrome QE(1)(2)(3)



(1) The results were obtained using a tunable LED light source, with a built-in integrating sphere, covering the range of 410 nm – 940 nm. The ADC ramp gain was adjusted to the equivalent of 1 V swing, for 12-bit ADC mode at 60 MHz (MCLK). The sensors temperature was approximately 60 ºC (uncontrolled temperature environment). The values presented are for the default configuration of Full Well around 20 ke- (STS3 Register bits [3:0] = 0x0). Sensor supply levels were the typical ones: VDDA = 3.3 V and VDDD = 1.8 V. The set Readout mode was 1-To-1. The results are valid for all variants, once they all share the same silicon.

(2) The settings used to get these values are those recommended by the European Machine Vision Association standard 1288 from the Machine Vision Sensors and Cameras. https://www.emva.org/standards-technology/emva-1288/

(3) The RGB sensor QE figure is affected by the coupling of the adjacent lines. There is electrical crosstalk from the Red line to the Monochrome line and from the Green line to the Blue line. This effect causes a “bump” in the PTC which in turn affects the accuracy of the conversion gain calculation and therefore, the QE results. For RGB sensors this effect is more visible on Top as both Red and Monochrome lines are highly responsive to red illumination, while the Bottom lines are response in different spectral ranges. For monochrome sensors this effect is equally visible on both and bottom, once all lines are equally responsive.

Figure 23:
4LS Monochrome Relative Angular Response[1]

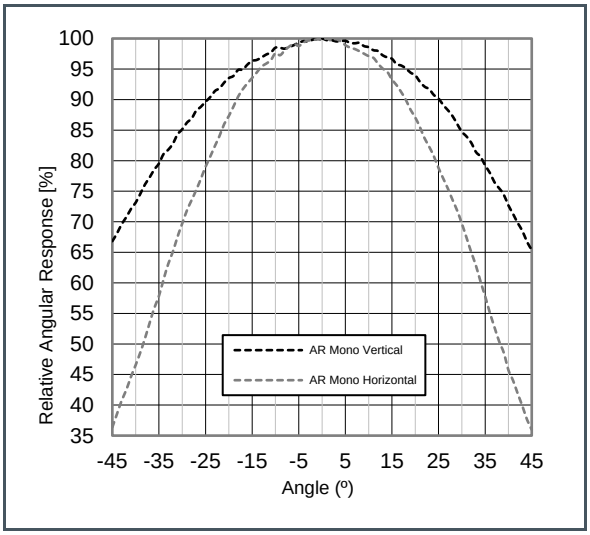
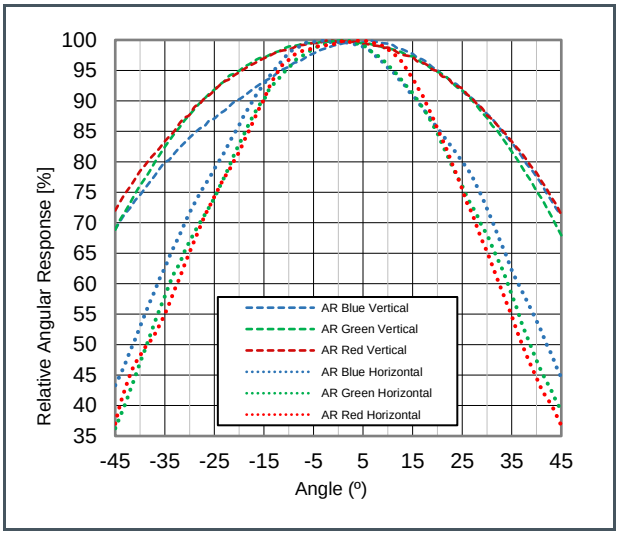


Figure 24:
4LS RGB Relative Angular Response[1][2]



(1) Due to the nature of 4LS pixel and sensor structure, the pixel matrix gets shielded by thick metal barriers, between each pixel line. Therefore it is observed a lower response when the sensor is rotated horizontally, or when the illumination varies horizontally relative to the sensor.

(2) When the sensor is rotated vertically, or the illumination varies vertically relative to the sensor, additional metal barriers on the left side of the pixel will block a part of blue light, while red and green can pass through the metal easier.

7 Functional Description

7.1 General Sensor Description

The 4LS15K, 4LS10K and 4LS5K are stitched multi-segment sensors (Figure 25, Figure 26 and Figure 27), having four lines with a resolution of 15456, 10304 and 5152 pixels, respectively.

Figure 25:
4LS15K Sensor with Six Stitched 2K5 Segments

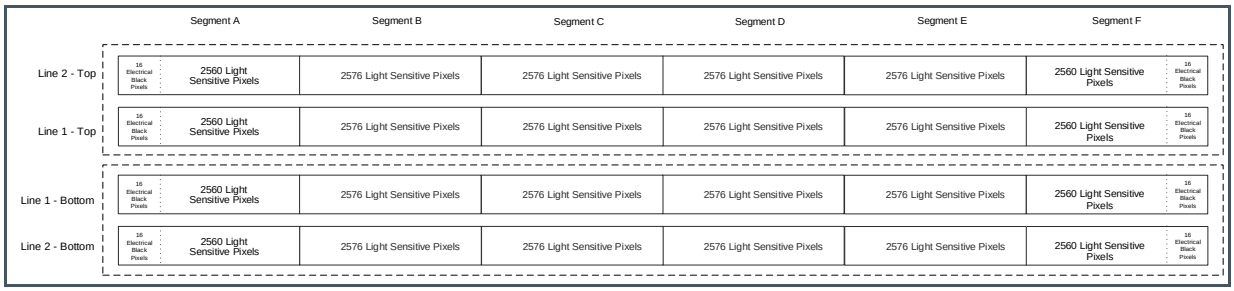


Figure 26:
4LS10K Sensor with Four Stitched 2K5 Segments

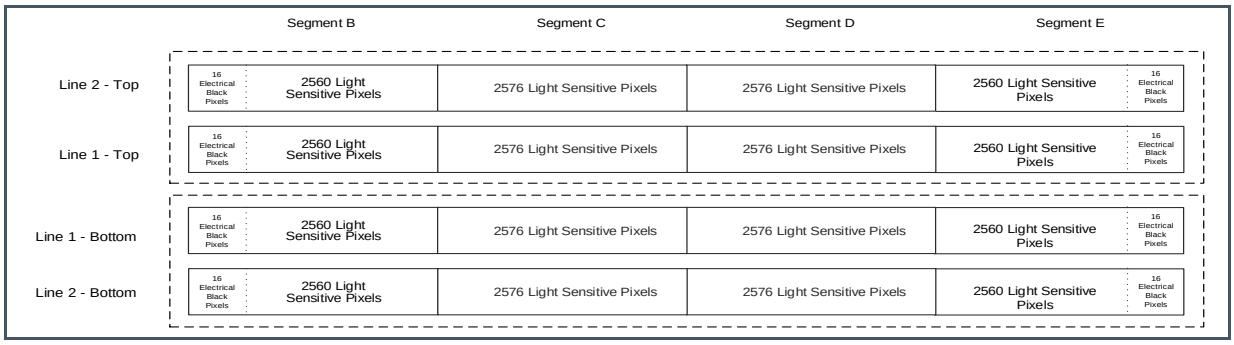
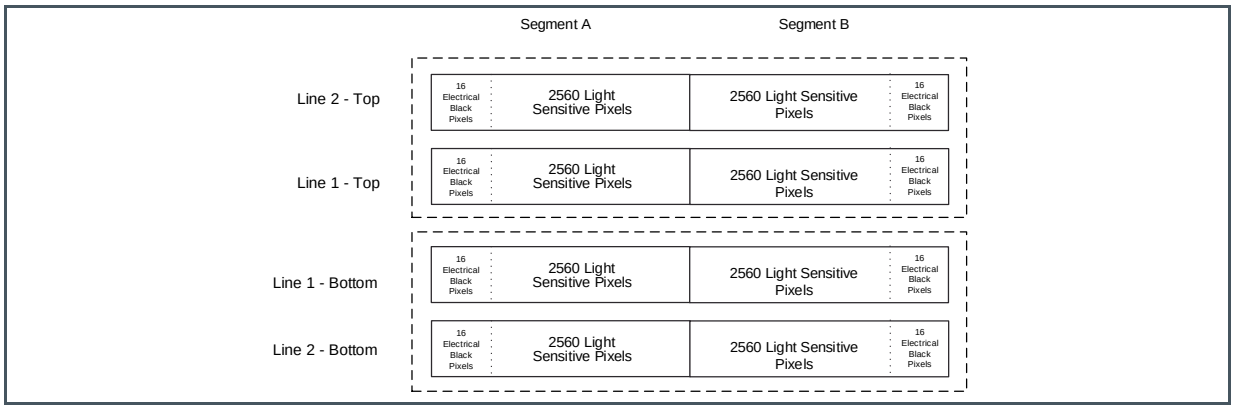


Figure 27:
4LS5K Sensor with Two Stitched 2K5 Segments



- Each segment is divided symmetrically into Top and Bottom, working independently.
- Each Top/ Bottom has:
  - Two lines. Each line has four LVDS outputs
  - Individual SPI and PLL (Dataclock - Differential)
- Each line has 2576 pixels.
  - The middle segments have all light sensitive pixels (Figure 25 and Figure 26).
  - The first and last segments have 16 electrical black pixels located at the very left and very right end of the sensor, respectively. These black pixels are used to give a reference for dark signal offsets.

Once 4LS15K has six segments stitched together (4LS10K has four, 4LS5K has two), it can be seen as 12 individual sensors (eight for 4LS10K, four for 4LS5K) in just one sensor. Having this in consideration, the user needs to provide MCLK individually (for each segment's Top and Bottom) and perform synchronization. Figure 28 presents the pixel distribution on a 15K sensor and its filter organization for color sensor version. Each pixel line is separated with a gap of one pixel period from the next line. The mono version (Figure 29) has no color filter, being all lines the same as Line 2 – Top. For 4LS10K and 4LS5K is the same distribution, with lower resolutions.

Figure 28:
Pixel Distribution on 4LS15K RGB + Monochrome

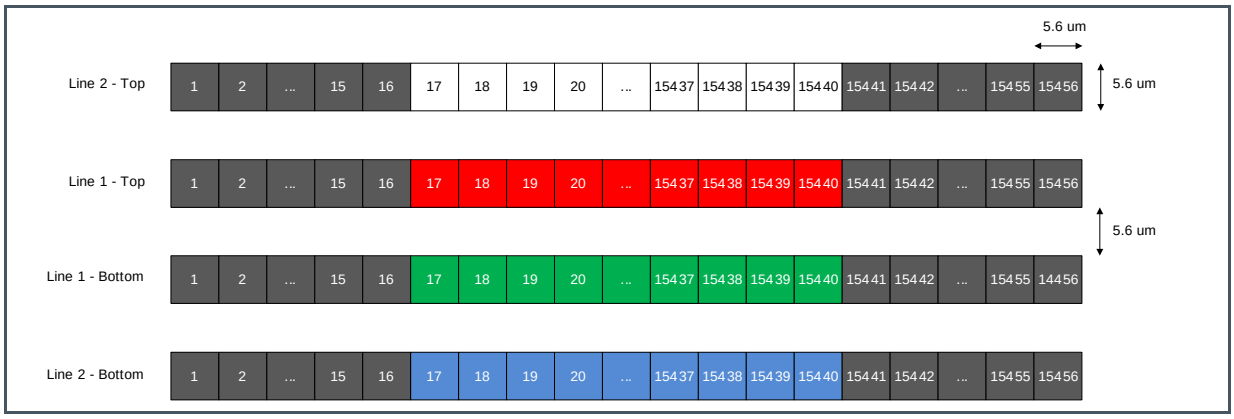
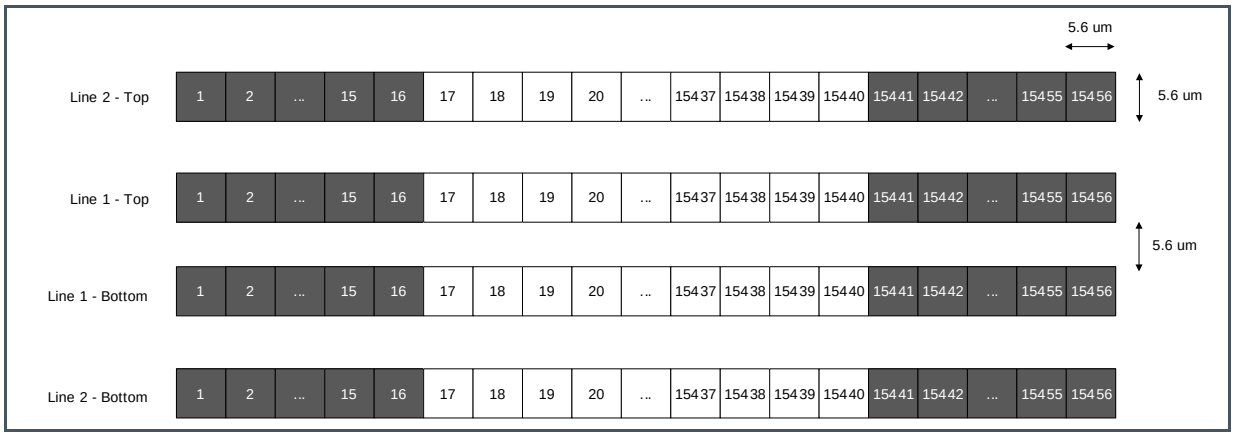


Figure 29:
Pixel Distribution on 4LS15K Monochrome



The sensor has three different operation modes, being the Standard Mode the main setting. The selection between each mode is done using the following configuration bits.

Figure 30:
Sensor Configuration Mode

Status 4 Register Bit 4	Status 4 Register Bit 3	Test Mode Register Bit 0	Operation Mode Selected	Remark
0	1	0	Standard Mode Pixel Size: 5.6 µm x 5.6 µm	Default
1	0	0	Special Mode	**Internal Use Only** Do Not Use.

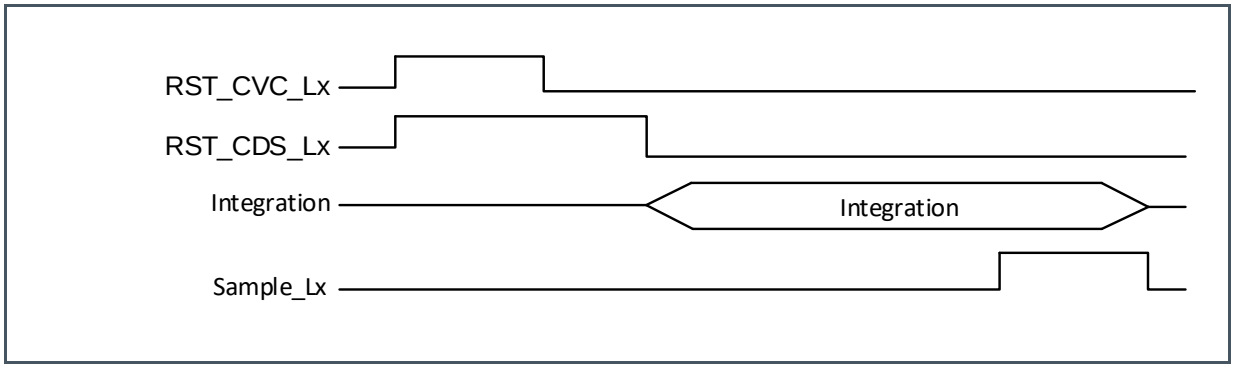
Status 4 Register Bit 4	Status 4 Register Bit 3	Test Mode Register Bit 0	Operation Mode Selected	Remark
0	0	1	ADC Test Mode	**Internal Use Only** Do Not Use.

To operate in standard mode it is necessary to act in:

- RST_CVC_L1 and RST_CVC_L2
- RST_CDS_L1 and RST_CDS_L2
- SAMPLE_L1 and SAMPLE_L2
- Select CVC (Full Well Capacitance is configurable) and CDS gain using registers.

The next figure exemplifies how to act in these signals during this operation mode. For more details, please refer to section 7.11.

Figure 31:
Standard Mode Operation

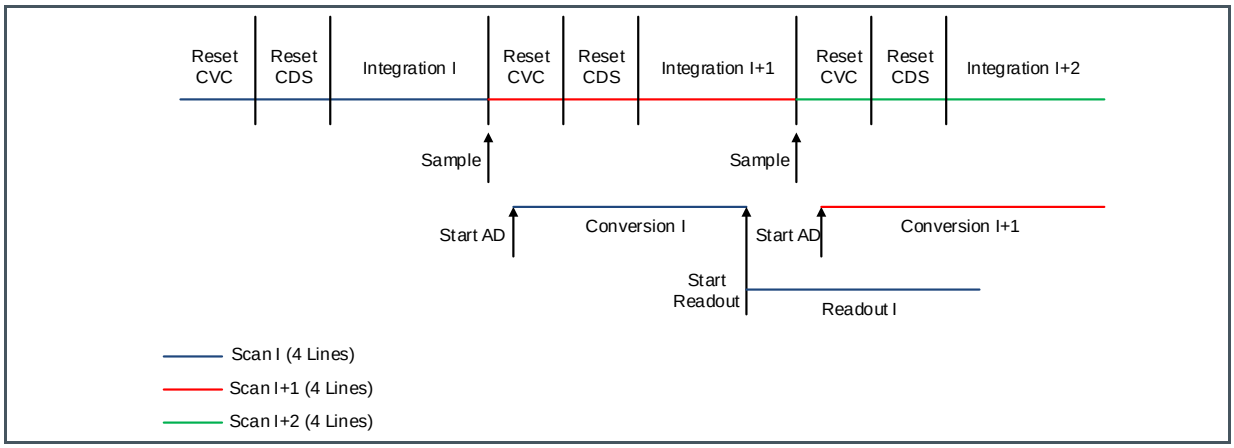


The sensor features a 12-bit ADC with programmable conversion gain and end range. The on chip digital control circuit generates all necessary control signals for conversion and the readout modes. The start of conversion and start of readout for a new line can optionally be triggered by external signals. The ADC conversion range can be programmed over the serial interface. Higher conversion range requires longer ADC conversion time.

"Companding" A/D conversion is presented with a total of four A/D conversion gains, each doubling the conversion step for the next higher signal range. The thresholds for the doubling of the conversion step are programmable over the serial configuration interface.

The sensor enables interleaved integration, A/D conversion and readout, therefore the overall pipeline delay is minimum two line times.

Figure 32:
4LS Pipeline Overview



Regarding the output mode, it is possible to select between two different modes: 12-bit and 8-bit serialization. It is also possible to select between different readout modes: 1-To-1, 2-To-1 and 4-To-1, which allows output multiplexing.

7.2 Startup Sequence

During power up or power down, no signal on any pin shall exceed VDDIO by more than 0.3 V (except for VDDA).

The VDDxx must never be allowed to exceed the VDDA supply by more than 0.5 V during power-up. Therefore, the VDDA supply should always be higher than the lower voltage supply.

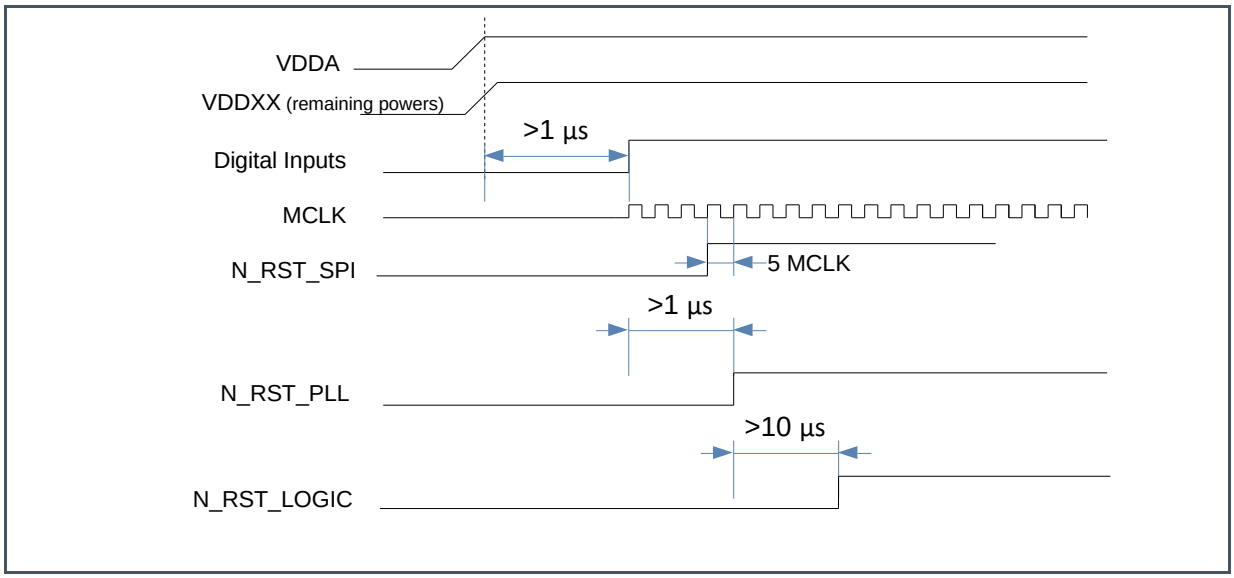
The main clock (MCLK) shall remain low for at least 1 µs after all powers have reached their final values.

The global reset for the PLL, N_RST_PLL, shall remain low for at least 1 µs after MCLK had started.

The global reset for the logic, N_RST_LOGIC, shall remain low for at least 10 µs after the reset of the PLL was released.

Figure 33 shows an example for the power on sequence where the times to be guarded are present.

Figure 33:
Power-On Sequence



Startup Sequence detailed description:

- Until N_RST_SPI remains the same as above.
- Release N_RST_SPI.
- Enable all segments (using FPGA register to control N_CS of each 2K5 segment).
- Write all registers, having in consideration the following:
  - STS2 Register to choose output mode: 0x00 for 12-bit or 0x08 for 8-bit.
  - STS1 = 0x09 – Perform serializer phase sync with each Start_Readout.
  - Choose appropriate CLK phase for PLL clock compensation (STS5 Reg – Bits[5:4]). The chosen value will depend on the user system.
  - Sending remaining registers.
  - STS1 = 0x09 – Update of all registers.
- Release N_RST_PLL.
- Release N_RST_LOGIC.
- Training Sequence tracking to perform the alignment.
- Turn on the timing to start having Data (Training mode or Pixel Data).
- After 1 ms (to guarantee that there is at least one complete LVAL signal) STS1 is set to 0x19 to disable the internal serializer sync (i.e. External Sync with no actual pulse – grounded).

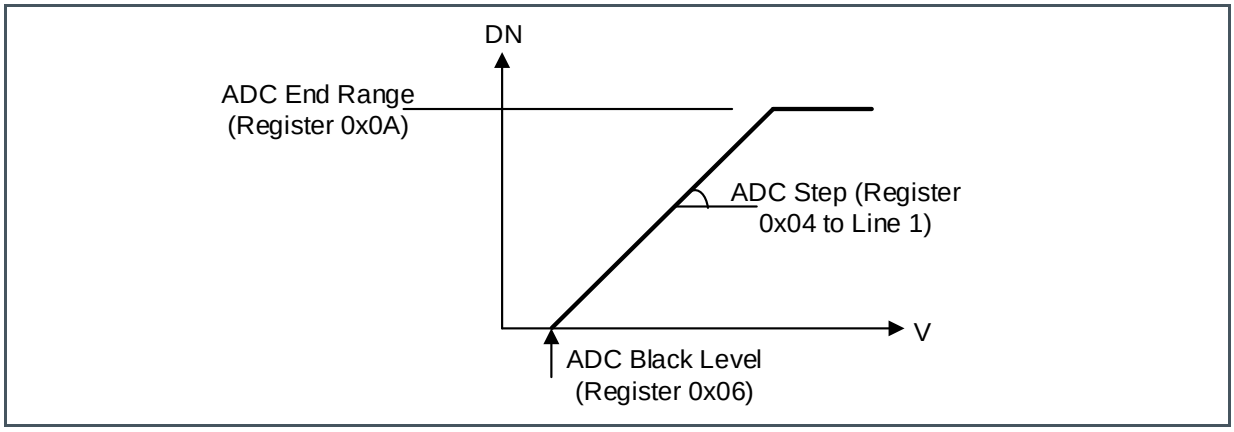
7.3 Conversion Cycle

The A/D conversion starts by sending a pulse on the Start_AD signal. The use of a signal to start the A/D conversion gives the possibility to perform different integration times on the different lines and align the middle of each lines exposure time by starting and ending each lines exposure time individually. However, the start of A/D conversion must always be sent after the falling edge of all Sample signals, since it will be applied to the same ADC on the Sensor. The 12-bit resolution ADC

uses a monotonous linear conversion, or piece wise linear conversion when in companding mode. Prior to A/D conversion, the signal value is stored on a Sample-and-Hold block after CDS block. The result of conversion is stored in SRAM to be processed in digital domain.

7.3.1 ADC Linear Mode

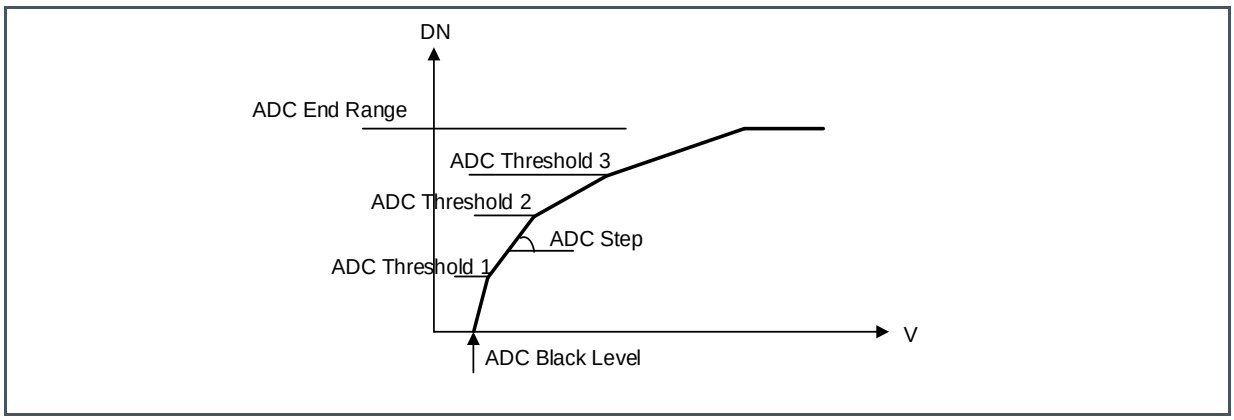
Figure 34:
ADC Transfer Function in Linear Mode



7.3.2 ADC Companding Mode

The "companding" ADC mode allows to adapt the A/D conversion step to the increasing amount of photon shot noise, which is inherent to the impinging optical signal as signal levels increase. This can selectively amplify low light level signals. To ease re-linearization for further image treatment, the A/D conversion step is doubled after each threshold. There are maximum three programmable thresholds available. The thresholds are programmed over the serial configuration interface with a resolution of 8 bits, mapped to the 8 MSB of the conversion range. If using companding ADC mode, the three thresholds must be strictly monotonous and smaller than the end of range register content.

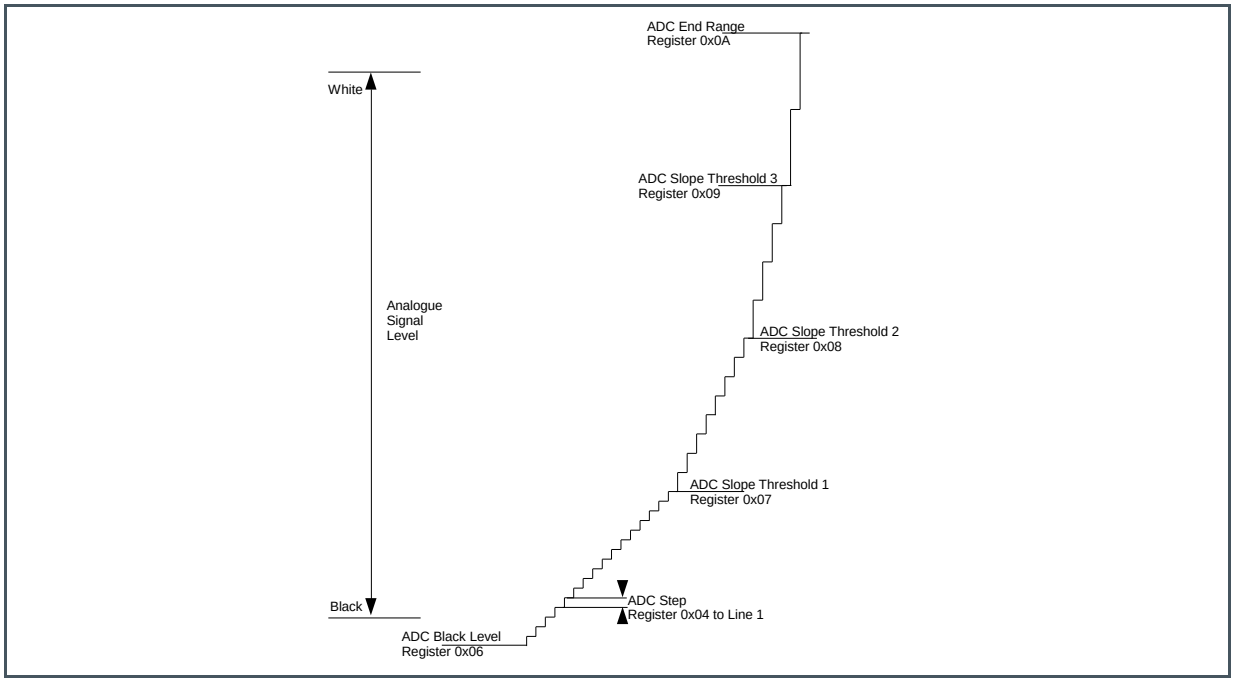
Figure 35:
ADC Transfer Function in Companding Mode



To accommodate for the use of the companding ADC curve, the overall ADC gain can be programmed with 8 bits (255 values) over the serial configuration interface.

For a better understanding on the use of companding mode, please see Figure 36.

Figure 36 :
Principle of ADC Companding Mode



7.3.3 ADC Parameters

The next figure presents the parameters of the ADC.

Figure 37:
ADC Parameters

Parameter	Min	Typ	Max	Unit
Default conversion (full range)	0.8	1	1.2	V
INL		1	2	LSB(1)
DNL		0.5	1	LSB(1)
Programmable V_{Reset} voltage swing	1.65	1.8	1.85	V
Programmable conversion (full range)	0.5		1.38	V

(1) Is defined as LSB as the difference between the binary level N and N+1.

7.4 Readout Cycle

The pixel level ADC signal is stored in an SRAM bench, the digital readout is triggered by the external signal “Start_Readout”. This signal must be sent after the end of A/D conversion, based on the end of range value. When the sensor receives the signal (rising edge), the readout is started from the most left pixel to the right. An LVAL signal (at Start_Readout falling edge) is generated to indicate valid pixel data.

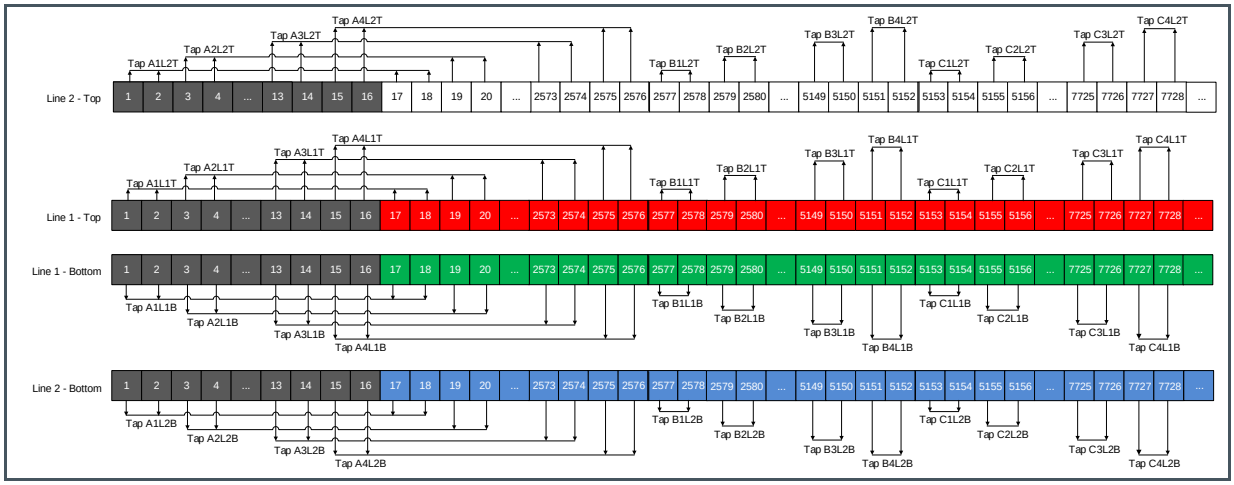
Optionally the start of A/D conversion and start of readout can be triggered automatically from the on chip state machine. This feature can be enabled over a register bit.

7.4.1 Tap Organization

The following figure presents the pixel distribution to three 2K5 segments over different output taps. The tap identification is performed as Tap WXLYZ, where W stands for the each 2K5 segment ID, starting on A as the first and moving on the alphabet for the remaining ones. X stands for each 2K5 segment pixel pair that is read, starting on 1 for the very left (and ending on 4, depending on the readout mode). L stands for Line, where Y identifies the line number. Finally, Z identifies the line’s segment position, being B (Bottom) or T (Top).

Each segment has 18 LVDS channels: 16 for Data (8 top and 8 bottom (4 each line)) and 2 optional for DataClk (1 top and 1 bottom). A 15K sensor, will have a total of 108 LVDS channels available. Depending on the target system, if the user wants to use a 15K sensor with a lower speed, a different readout mode can be chosen: 2-To-1 or 4-To-1, using less LVDS channels (Section 7.10).

Figure 38:
LVDS Outputs Organization on the First Three 4LS15K Segments



7.5 Automatic Start A/D Conversion and Readout

The sensor features the possibility for the user to place it in semi-automatic mode. In this operation mode the user only needs to act over the reset signal for CDS and CVC, and the SAMPLE signal.

The start of A/D conversion and the start for the readout will be performed automatically and the data will be sent to the user with no need for any additional action. To set the sensor to this operation mode it is necessary to set the bits 4 and 5 of register Status 2 to '1'.

It is also possible to set only one of the operations to automatic. As an example, the start of readout can be set to automatic and the conversion set to manual, so the user needs to start the conversion by the START_AD signal, and, as soon the conversion is over, the sensor will start the readout automatically. Also if only the A/D conversion is set to be performed automatically, the sensor will start it as soon as the integration and the readout of previous line is finished, then it is the user's responsibility to trigger the readout by the START_READOUT signal of the converted line.

Despite the fact that these features are available and working, it is recommended to use perform the A/D conversion and readout using external signals, once these were applied for the sensor characterization phase and currently used in the Evaluation Kit (EK) system. For more details, regarding implementation, please refer to section 7.11.

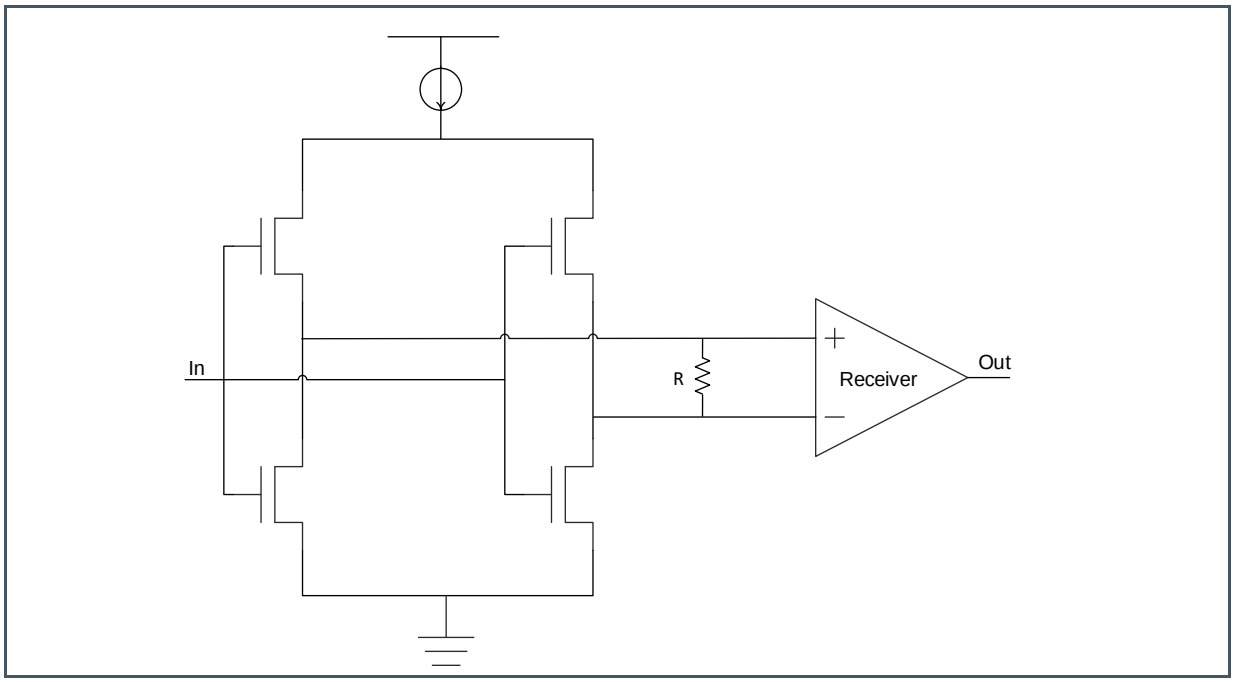
7.6 LVDS Output Data Interface

The data of each segment is communicated off chip via a serial LVDS interface. The LVDS output data interfaces are organized in 16 LVDS data outputs, 4 on each line, on top and on bottom. In addition to the data interface, there are 2 LVDS data clock interface, for deserialization purposes: one on top and another on bottom.

The LVDS output current can be programmable over the SPI interface (register Programmable LVDS register, LVDS bias[4:2]) to grant a safe detection and deserialization. This feature permits to program the current from 400 µA to 2.8 mA with steps of 400 µA. This driving current can be reduced (decreasing the noise coupling to the analogue electronics) or increased based on voltage swing LVDS receiver. Additional, if needed, can also be switched off, drivers setting the configuration bits at '000'.

A schematic, presenting the principle used of the LVDS transmitter, is presented on Figure 39.

Figure 39:
Principle of LVDS Current Steering Interface



The following table shows the LVDS parameters. These parameters were designed and simulated using a 10 pF load and 100 Ω termination.

Figure 40:
LVDS Parameters

Description	Min	Typ	Max	Units
Differential Propagation Delay Low-to-High, t_{PLHD}	150		320	ps
Differential Propagation Delay High-to-Low, t_{PHLD}	150		320	ps
Differential Output Rise Time (20% to 80%), t_{TLHD}	250		400	ps
Differential Output Fall Time (80% to 20%), t_{THLD}	250		400	ps
Pulse Skew, $t_{SK(P)}$		400		ps

7.7 Transmission Mode

The chip has the capability of increasing the output line rate by reducing the transmitted serial word length by configuring the bit-3 of register 0x02.

Figure 41:
Output Bit Rate for Each Transmission Mode

Serial Word Width	Output Bit Rate
8-bit	640 MHz @ 80 MHz MCLK
12-bit	720 MHz @ 60 MHz MCLK

The ADC resolution (End of Range, register 0x0A) should be adjusted to match with the achieved line rate and serial word width.

If using a different MCLK, please check which PLL Division to use, as reference in the below section 7.8.

7.8 Internal Clock

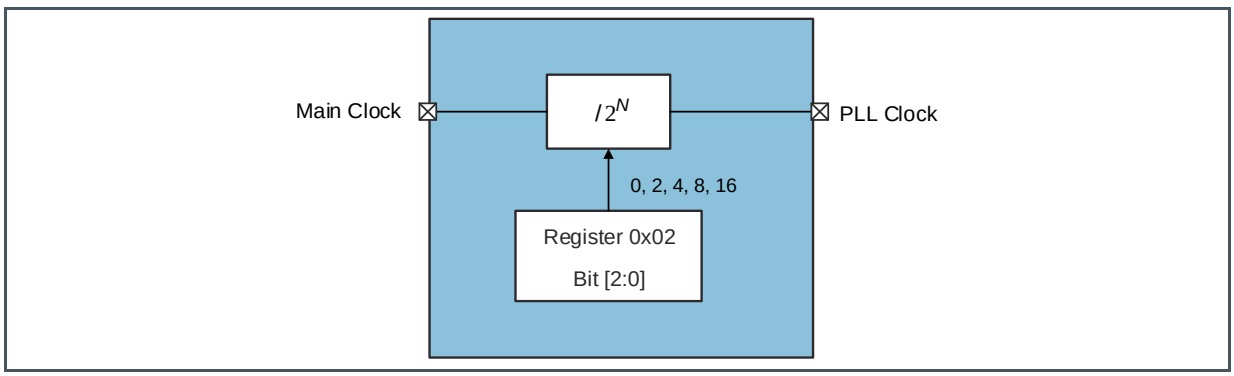
The sensor presents a PLL that will generate a faster clock according to the input main clock frequency (MCLK) and transmission mode.

Figure 42:
Main Clock According to the Transmission Mode

Transmission Mode	Maximum MCLK [MHz]	PLL Clock Frequency [MHz]	PLL Clock Period [ps]	DDR Clock [MHz]
8-bit	80	640	1.56	320
12-bit	60	720	1.39	360

The PLL also includes a division block to promote the possibility of a lower frequency clock.

Figure 43:
Internal Clock Generation



7.9 Training Sequence / Pattern

The use of a Training Sequence/Pattern is implemented on the sensor so that the FPGA can synchronize the receiver for the optimal centered clock edge. The period of each bit is given by the PLL Clock Period, as shown in Figure 42, for the respective MCLK values.

The Training Sequence (TS) is defined by the use of three registers. The tables below gives a representation of the three registers combined together to form the training sequence.

Figure 44:
Transmission of Training Sequence with 8-Bit Resolution

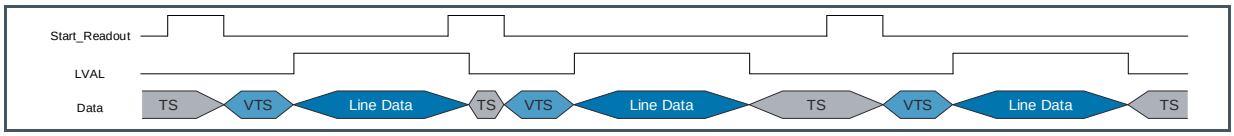
Word	TSA								TSB							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Register	Training Sequence 1						Training Sequence 3		Training Sequence 2						Training Sequence 3	
Register Bits	5	4	3	2	1	0	7	6	5	4	3	2	1	0	3	2

Figure 45:
Transmission of Training Sequence with 12-Bit Resolution

Word	TSA									TSB								
Bit	11	10	…	5	4	3	2	1	0	11	10	…	5	4	3	2	1	0
Register	Training Sequence 1					Training Sequence 3				Training Sequence 2					Training Sequence 3			
Register Bits	7	6	…	1	0	7	6	5	4	7	6	…	1	0	3	2	1	0

Figure 46 presents the transmission for the training pattern over the time, in relation to the LVAL signal. As soon as the sensor is powered (respecting power-on-sequence), starts transmitting the Training Sequence. The TS is always transmitted before the Valid Training Sequence (VTS) and when the FPGA no longer requests for readout. The VTS has the same value as TS but is comprehended between the falling edge of START_READOUT and following LVAL rising edge signals, as represented on Figure 52 and Figure 53.

Figure 46:
Training Pattern Transmission



Pending on the transmission mode (12-bit or 8-bit at 4-To-1, 2-To-1 or 1-To-1), the VTS number of words or clocks (each clock is equal to T_{MCLK}) varies, as shown below. Please note that Word B is always the first word after the START_READOUT falling edge.

Figure 47:
Number of Words Sent for Valid Training Sequence

Number of Outputs	VTS @ 8-Bit Mode Each Word is 8-Bit	VTS @ 12-Bit Mode Each Word is 12-Bit
4 Outputs (1-To-1)	1 x TSB + 11 x (TSA + TSB) = 23 Words = 23 x T_{MCLK}	
2 Outputs (2-To-1)	1 x TSB + 13 x (TSA+ TSB) = 27 Words = 27 x T_{MCLK}	
1 Output (4-To-1)	1 x TSB + 17 x (TSA + TSB) = 35 Words = 35 x T_{MCLK}	

The TS number of words will depend on the pixel timing applied, having a minimum value of three clocks, so the LVAL low period has a minimum of 26, 30 and 38 clocks, for the readout modes of 1-To-1, 2-To-1 and 4-To-1, respectively. This margin of three clocks has to be guaranteed in the pixel timing, in order to avoid timing violations.

Equation 1:

$$LVAL_{Low\_Period}\ (clocks) = TS + VTS$$

Figure 48:
Minimum LVAL Low Period (Clocks)

Number of Outputs	VTS (clocks)	Minimum TS (clocks)	Minimum LVAL Low Period (clocks)
4 Outputs (1-To-1)	23	3	26
2 Outputs (2-To-1)	27	3	30
1 Output (4-To-1)	35	3	38

When performing a synchronization of the serializer to the chip main clock, the phase and bit information gathered from the training sequences must be newly acquired. If the synchronization of the serializer is performed with each start of readout (this can be controlled over register 0x01, bit 4), only the transmission at the beginning of each line of data should be considered as valid.

7.10 Output Mode and Data Transmission

By configuration means it is possible to reduce the number of output taps per line from 2-To-1 (half of LVDS channels) and 4-To-1 (a quarter of LVDS channels). This permits to read the entire lines only by two taps per line, or one tap per line, respectively. However when using this option, the readout speed will be reduced to approximately ½ or ¼ relative to the default 1-To-1 readout mode speed (using four output taps), respectively. It is approximate because the VTS are slightly different between readout modes.

The output data is provided by the sensor according to the following readout modes, considering a 2K5 segment.

Figure 49:
1-To-1 Readout Mode for 12-Bit and 8-Bit Mode

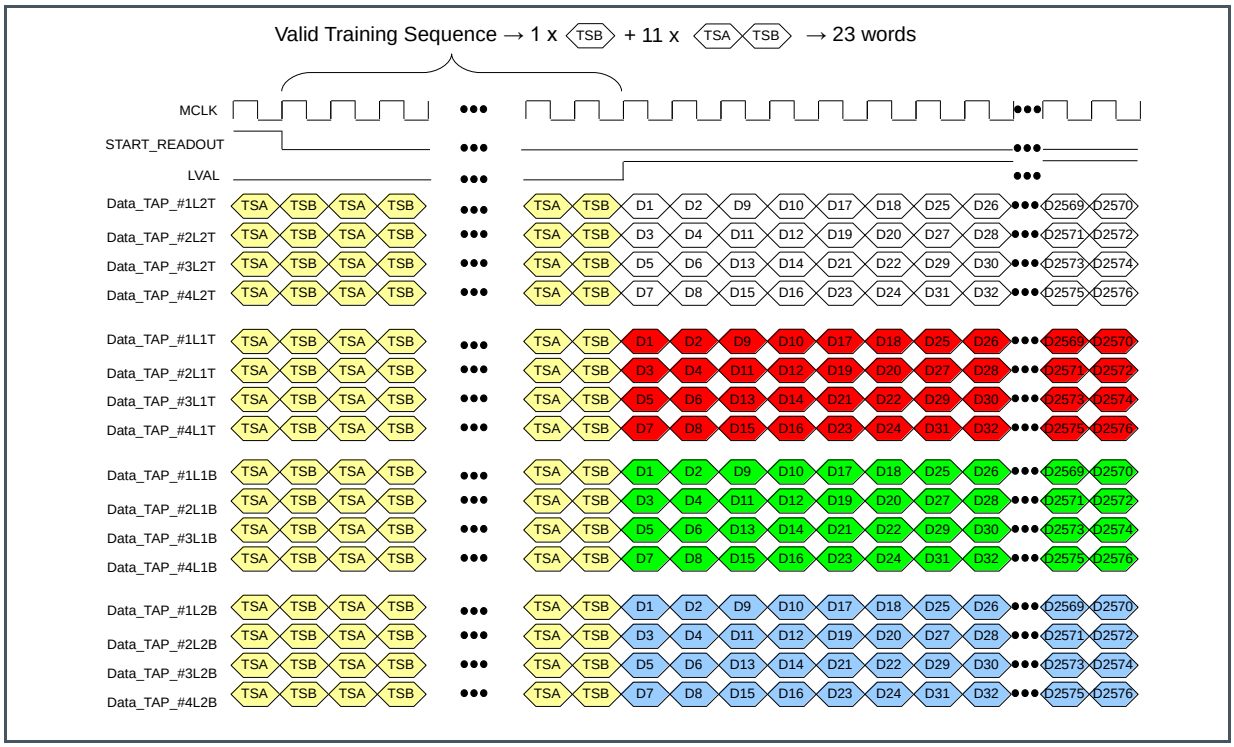


Figure 50:
2-To-1 Readout Mode for 12-Bit and 8-Bit Mode

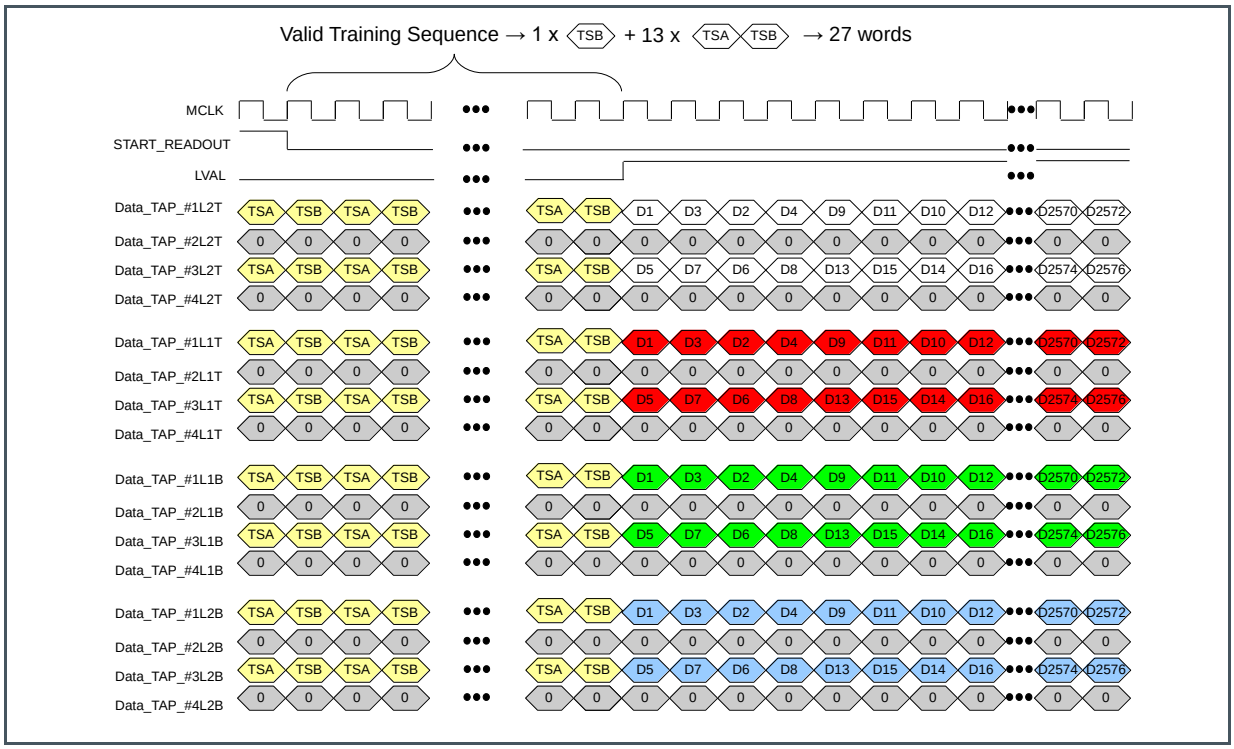


Figure 51:
4-To-1 Readout for 12-Bit and 8-Bit Mode

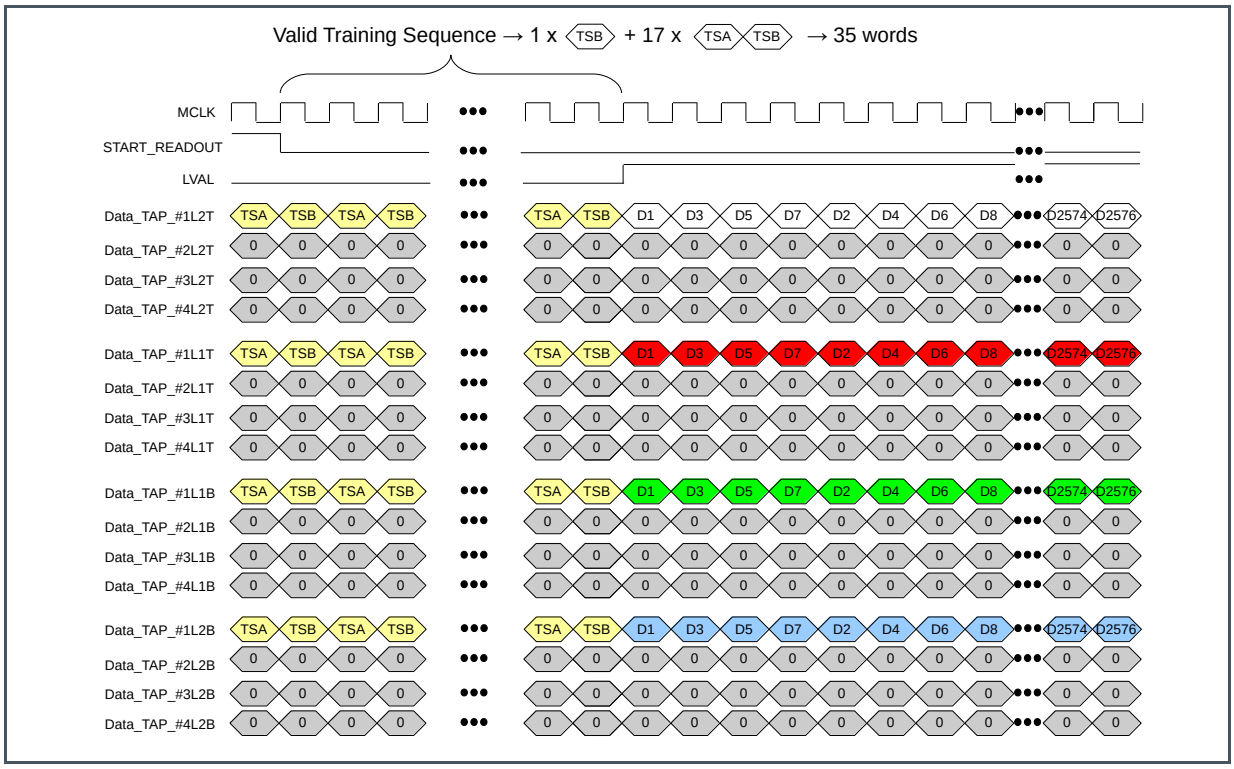


Figure 52, Figure 53, Figure 54 and Figure 55 shows in detail the data being transmitted over the LVDS drivers, with relation to the LVAL signal, for an 8-bit and a 12-bit transmission mode, respectively.

Figure 52:
Readout Sequence for 8-Bit Transmission Mode

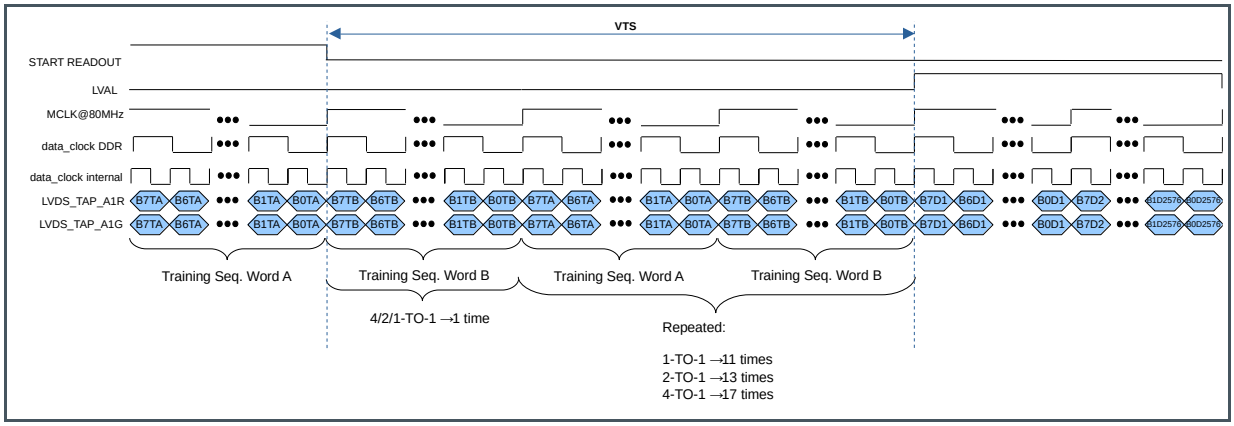


Figure 53:
Readout Sequence for 12-Bit Transmission Mode

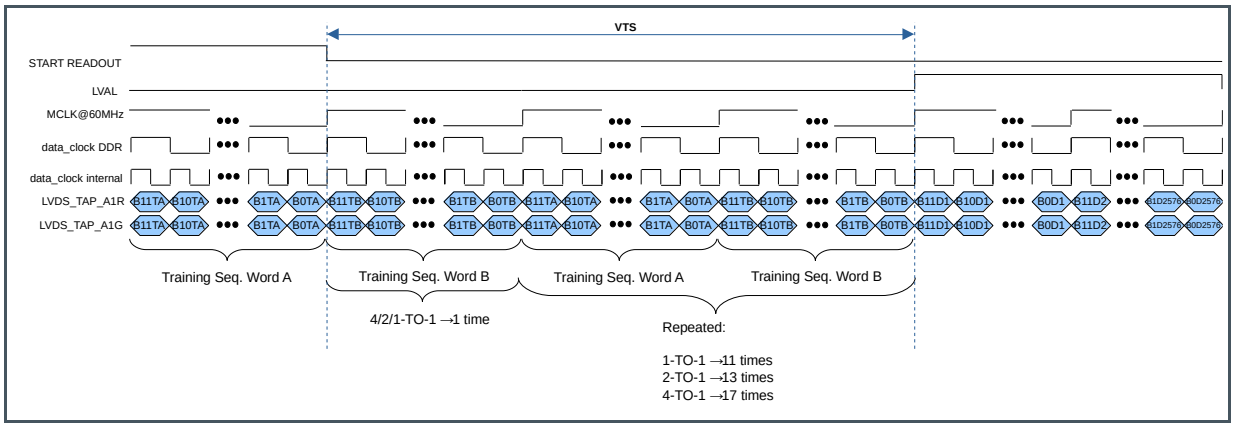


Figure 54:
Three Consecutive Words Readout for 8-Bit Mode

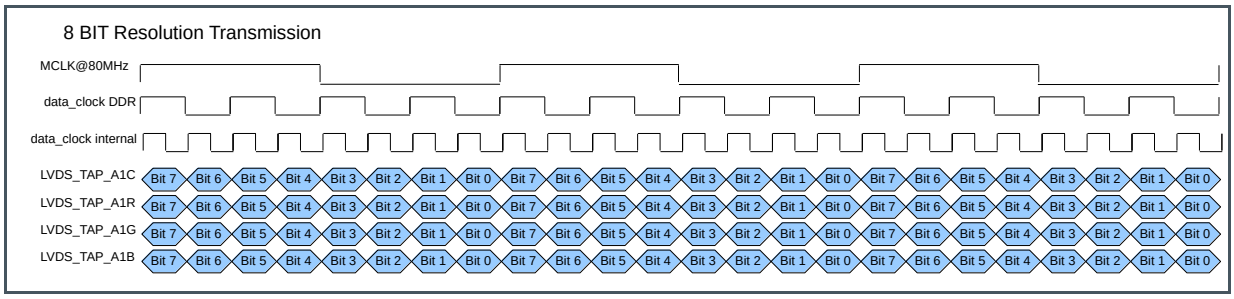
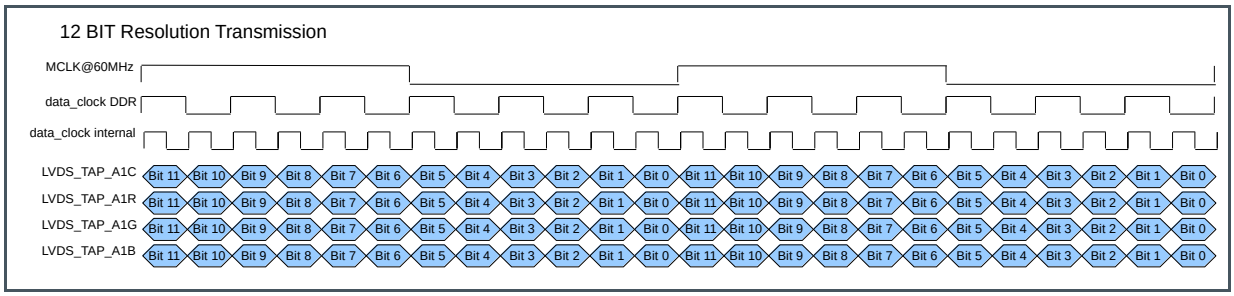


Figure 55:
Two Consecutive Words Readout for 12-Bit Mode



7.11 Timings / State Machine

7.11.1 Pixel Timing Diagram Considerations

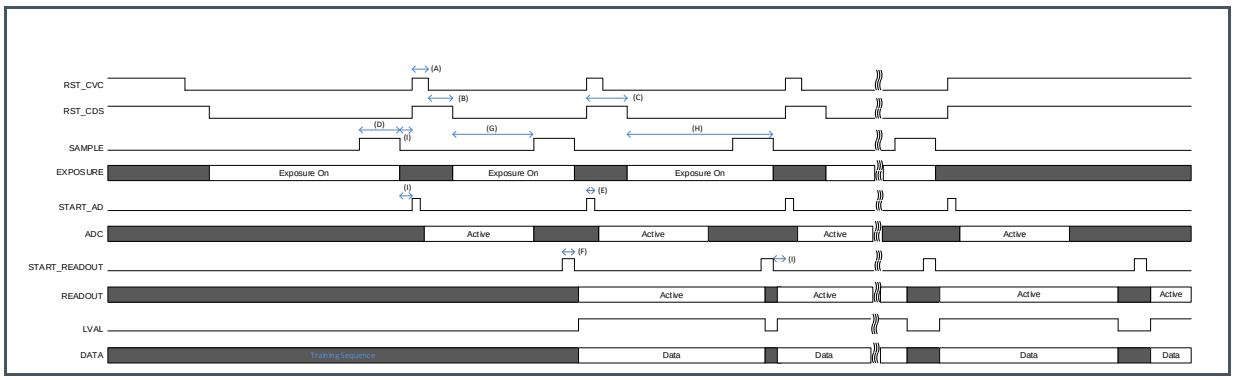
- When stated a value in time (usually ns or µs), this is a fixed or minimum value.
- When stated a time duration in 'X' times T_{MCLK}, this is number of clocks that must be respected, independently of the clock frequency. A clock is equal to T_{MCLK}.
- START_AD signal can only be sent to the sensor, after the falling edge from the last sent SAMPLE signal. It is recommend a minimum number of clocks between SAMPLE falling edge and START_AD rising edge.
  - 8 x T_{MCLK} for 12-bit mode at 60 MHz
  - 12 x T_{MCLK} for 8-bit mode at 80 MHz
- The SAMPLE signal rising edge from the current exposure, can only be sent after A/D conversion period of the previous exposure.
- START READOUT must always be sent before the next A/D conversion (START_AD pulse rising edge).
- For the correct operation of the sensor, the minimum time in T_{MCLK} for START_READOUT pulse is presented in Figure 56.

Figure 56:
START_READOUT Pulse Configuration

Frequency	Auto Start Readout(1)	External Start Readout
Frequency less or equal to 80 MHz	Can use Auto Start Readout	Minimum 20 x T_{MCLK} for 4LS15K Minimum 12 x T_{MCLK} for 4LS10K Minimum 8 x T_{MCLK} for 4LS5K

(1) Can be used, however it is recommended to set the readout using an external pulse, as in Figure 56.

Figure 57:
Timing Diagram Assuming Default Configuration for Standard Mode



According to the bit-mode and frequency, is recommended the below minimum timing values.

Figure 58:
Minimum Timing Periods

Timing ID	Description	12-bit @ 60 MHz	8-bit @ 80 MHz
A	RST_CVC	400 ns	500 ns
B	FE(1) RST_CVC & FE(1) RST_CDS	600 ns	750 ns
C	RST_CDS	1 µs	1.25 µs
D	SAMPLE	500 ns(2)	500 ns(3)
E	START_AD	2 x T_{MCLK}	
F	START_READOUT		20 x T_{MCLK}(4) 12 x T_{MCLK}(5) 8 x T_{MCLK}(6)
G(7)	FE(1)RST_CDS & RE SAMPLE(2)	10.83 µs(8)	6.475 µs(9) 2287.5 µs(10)
H(7)	Integration Time (G + D)	11.33 µs(8)	6.975 µs(9) 2787.5 µs(10)
I	FE(1)SAMPLE & RE(11) START_AD	8 x T_{MCLK}	12 x T_{MCLK}

(1) FE stands for Falling Edge.
(2) Originally, the minimum SAMPLE pulse period is 1 µs. To achieve a higher line rate at 12-bit, the minimum pulse can be 500 µs, maintaining image quality.
(3) When using full resolution, for 8-bit mode, the SAMPLE can be originally 1 µs, because the Readout time is much higher than the ADC conversion time, therefore not affecting the line rate. However, when using the ROI feature for 4LS5K, to achieve a higher line rate, the minimum SAMPLE pulse can be decreased to 500 µs, maintaining the image quality. Please check section 7.11 for details.
(4) 4LS15K
(5) 4LS10K
(6) 4LS5K
(7) In theory, can be zero which means that the Minimum Integration/Exposure can be the same as SAMPLE time, as in D. However, please note that this configuration was never tested. Moreover, when using the sensor with the maximum line rate, does not bring much advantage to reduce this value, because the system would need more illumination power, to illuminate the target, and the line rate is still limited by the ADC time. Please refer to section 7.11 to check the details of the state machine implementation.
(8) For 12-bit, the minimum integration time tested was 11.33 µs (680 clocks for 12-bit @ 60 MHz). Therefore, the minimum G value is 10.83 µs.
(9) For 8-bit, for full resolution, the minimum integration time tested was 6.975 µs (558 clocks @ 80 MHz). Therefore, the minimum G value is 6.475 µs.
(10) When using 4LS5K ROI feature, the minimum integration time tested was 2787.5 µs (223 clocks @ 80 MHz). Therefore, the minimum G value is 2287.5 µs.
(11) RE – Rising Edge

7.11.2 Readout Time

The readout time is calculated by the following formula, taking in consideration the values on Figure 48.

Equation 2:

$$Readout\ Time = Data + TS + VTS = Data + LVAL_{Low\_Period}$$

Figure 59:
Data and VTS Clocks

Readout Mode	Data (clocks)	Minimum LVAL Low Period (clocks)	Minimum Readout Time (clocks)
1-To-1	644	26	670
2-To-1	1288	30	1318
4-To-1	2576	38	2614

7.11.3 ADC Time

The ADC time depends on the sensor configuration (internal or external START_AD, ADC stabilization on or off, ADC end of range, output mode).

Note that End of Range (EOR) value, that gives the maximum EOR level, is performed using 10-bit. Therefore, the two LSBs are hardwired fixed at '1' and the other 8 bits come from the End of Range register value.

Figure 60:
End of Range Value

Value Defined by End of Range Register								Hardwired Fix Values	
x	x	x	x	x	x	x	x	1	1

The following formula presents the relationship between the value on the register and the number of clock cycles.

Equation 3:

$$EOR_{Value} = (End\ of\ Range\ Register\ \times\ 4) + 3$$

Figure 61:
ADC Time According to the Sensor Configuration

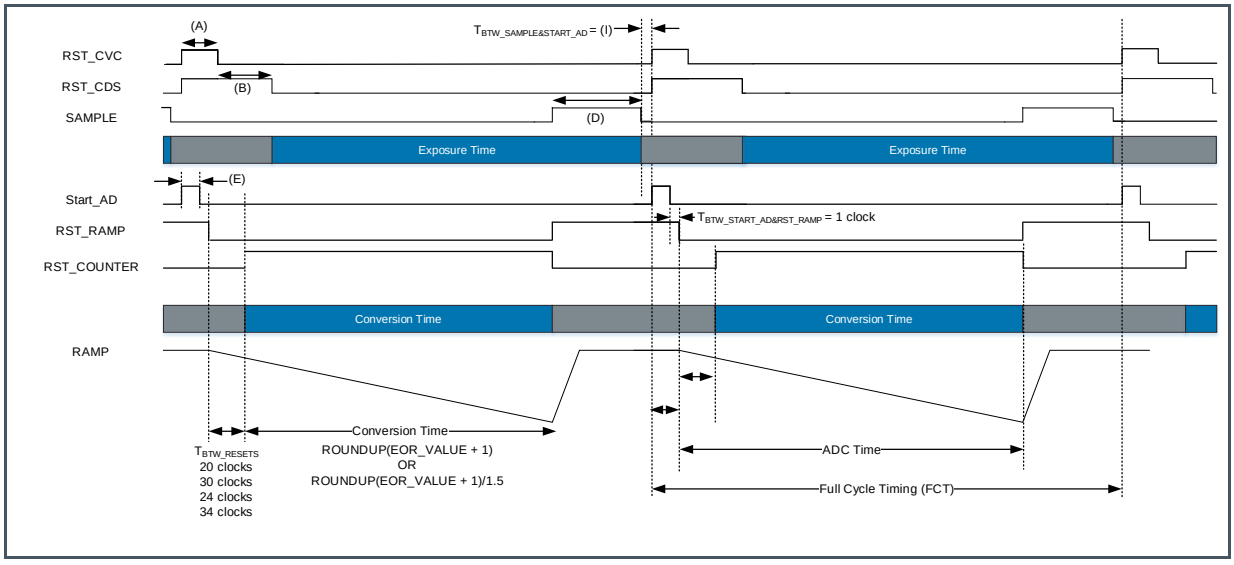
Start AD	ADC Stabilization	Output Mode	ADC Time [clocks]
Auto Start AD OFF Status2Reg[4] = ' 0 '	ADC Response Stabilization OFF Status6Reg[0] = ' 0 '	8-bit mode Status2Reg[3] = ' 1 '	24 + ROUNDUP(EOR_value + 1) = **280**(1)
		12-bit mode Status2Reg[3] = ' 0 '	24 + ROUNDUP((EOR_value + 1) / 1.5) = **707**(1)

Start AD	ADC Stabilization	Output Mode	ADC Time [clocks]
Auto Start AD ON Status2Reg[4] = ' 1 '	ADC Response Stabilization ON Status6Reg[0] = ' 1 '	8-Bit Mode Status2Reg[3] = ' 1 '	34 + ROUNDUP(EOR_value + 1) = **290**
		12-Bit Mode Status2Reg[3] = ' 0 '	34 + ROUNDUP((EOR_value + 1) / 1.5) = **717** (Default)
	ADC Response Stabilization OFF Status6Reg[0] = ' 0 '	8-Bit Mode Status2Reg[3] = ' 1 '	20 + ROUNDUP(EOR_value + 1) = **276**
		12-Bit Mode Status2Reg[3] = ' 0 '	20 + ROUNDUP((EOR_value + 1) / 1.5) = **703**
	ADC Response Stabilization ON Status6Reg[0] = ' 1 '	8-Bit Mode Status2Reg[3] = ' 1 '	30 + ROUNDUP(EOR_value + 1) = **286**
		12-Bit Mode Status2Reg[3] = ' 0 '	30 + ROUNDUP((EOR_value + 1) / 1.5) = **713**

(1) Validation tests were performed using these ADC times, for the respective output modes.

Figure 62 shows in detail the ADC Ramp and all the conversion process. Pending on the ADC configuration, the ADC Time will be different, which may influence the pixel timing minimum number of clocks:

Figure 62:
Sensor Timing According To The ADC Configuration(1)



(1) The times identified by numbers are in line with Figure 58.

Assuming that the ADC Time is much higher than the Readout Time, the sensor Full Cycle Timing (FCT) needs to take in consideration all the diagrams times, to not incur on timing violations.

Equation 4:

$$FCT\ (clocks) = START\_AD + T_{BTW\_START\_AD\&RST\_RAMP} + ADC\ Time + SAMPLE + T_{BTW\_SAMPLE\&START\_AD}$$

Where START_AD is always 2 clocks, $T_{BTW\_START\_AD\&RST\_RAMP}$ is always 1 clock, ADC Time depends of ADC configuration (Figure 61), SAMPLE and $T_{BTW\_SAMPLE\&START\_AD}$ are defined according to Figure 58.

7.11.4 Maximum Line Rate for Full Resolution

The maximum line rate or Minimum Time Allowed (MTA) depends on the bit mode used, ADC Time, exposure time and readout mode, being defined as the highest value from Equation 5.

Equation 5:

$$MTA\ (clocks) = Max(\ FCT\ ;\ Readout\ Time\ ; Exp.Time\ + DTI\ )$$

Where:

Equation 6:

$$DTI = T_{BTW\_SAMPLE\&START\_AD} + RST\_CDS$$

To convert into Hz or Lines/s, it is used Equation 7:

Equation 7:

$$Max\ Line\ Rate\ (Hz) = \frac{MCLK}{MTA}$$

For the following calculations, it is considered that the Exposure Time is lower than other parameters to better understand how to achieve the highest line rate without timing violations, when dependent of the ADC Time and Readout Time. It is also considered the minimum timing values from Figure 58.

12-Bit mode @ 60 MHz

Below described is an example to calculate the maximum line rate for 12-bit mode, for the settings below):

- Output mode: 12-bit @ 60 MHz
- Readout mode: 1-To-1 LVDS
- ADC response stabilization OFF
- Auto-start AD OFF
- Auto-start readout OFF
- End of Range = 0xFF

Once the ADC Time (relative to the FCT) is higher than Readout Time, then the MTA is calculated with the respective Equation 4.

Figure 63:
12-Bit Timing Clocks for Readout Mode 1-To-1

Parameters	Clocks
RST_CDS	60
ADC Time	707
Readout Data	644
Readout Time	670
SAMPLE	30
START_AD	2
$T_{BTW\_START\_AD\&RST\_RAMP}$	1
$T_{BTW\_SAMPLE\&START\_AD}$	8
FCT	748
MTA => Line Rate	FCT = 748 => 80.21 kHz
DTI	68
Max Integration Time(1)	748 – 68 = 680 => 11.33 µs
Minimum $LVAL_{Low\_Period}$	104

(1) To use the sensor at the maximum line rate, this is the maximum integration time possible. When it comes to the minimum integration time, in theory, it is possible to use a lower integration time, but it was not tested on this configuration. From an application perspective, using a lower integration time, does not bring significant advantages, once the line rate cannot be higher and the system would need to increase the illumination power.

The minimum LVAL time at low between two consecutive data streams is:

Equation 8:

$$LVAL_{Low\_Period} = MTA - Data$$

Therefore:

$$LVAL_{Low\_Period} = 748 - 644 = 104\ clocks$$

Below are presented the highest line rate values for readout modes of 2-To-1 and 4-To-1, maintaining the same above sensor configuration. On these specific cases, the Readout Time is higher than the ADC Time, therefore the MTA is calculated by Equation 2. On this case, it is possible to use the original SAMPLE value of 1 µs (60 clocks @ 60 MHz), once will not affect the MTA, because the FCT is only increased by 30 clocks (total of 778).

Figure 64:
12-Bit Timing Clocks for Readout Mode 2-To-1

Parameters	Clocks
Readout Data	1288
Readout Time	1318

Parameters	Clocks
FCT	778
MTA => Max Line Rate	1318 => 45.63 kLines/s
DTI	68
Max Integration Time	1250 => 20.833 µs
Minimum $LVAL_{Low\_Period}$	30

Figure 65:
12-Bit Timing Clocks for Readout Mode 4-To-1

Parameters	Clocks
Readout Data	2576
Readout Time	2614
FCT	778
MTA => Max Line Rate	2614 => 22.95 kLines/s
DTI	68
Max Integration Time	2546 => 42.434 µs
Minimum $LVAL_{Low\_Period}$	38

8-Bit mode @80 MHz

Below described is an example to calculate the maximum line rate for 8-bit @ 80 MHz, with the same sensor configurations for 12-bit, with the exception of End of Range.

- Output mode: 12-bit @ 60 MHz
- Readout mode: 1-To-1 LVDS
- ADC response stabilization OFF
- Auto-start AD OFF
- Auto-start readout OFF
- End of Range = 0x3F

Once the ADC Time (relative to the FCT) is lower than Readout Time, then the MTA is calculated with the respective Equation 2. Moreover, it can be used the original SAMPLE value of 1 µs (80 clocks).

Figure 66:
8-Bit Timing Clocks for Readout Mode 1-To-1

Parameters	Clocks
RST_CDS	100
ADC Time	280
Readout Data	644
Readout Time	670

Parameters	Clocks
SAMPLE	80
START_AD	2
$T_{BTW\_START\_AD\&RST\_RAMP}$	1
$T_{BTW\_SAMPLE\&START\_AD}$	12
FCT	375
MTA => Line Rate	670 => 119.4 kHz
DTI	670 – 558 = 112
Max Integration Time(1)	558 => 6.975 µs
Minimum $LVAL_{Low\_Period}$	26

(1) To use the sensor at the maximum line rate, this is the maximum integration time possible. When it comes to the minimum integration time, in theory, it is possible to use a lower integration time, but it was not tested on this configuration. From an application perspective, using a lower integration time, does not bring significant advantages, once the line rate cannot be higher and the system would need to increase the illumination power.

The minimum LVAL time at low between two consecutive data streams is:

$$LVAL_{Low\_Period} = 670 - 644 = 26\ clocks$$

Figure 67:
8-Bit Timing Clocks for Readout Mode 2-To-1

Parameters	Clocks
Readout Data	1288
Readout Time	1318
FCT	375
MTA => Line Rate	1318 => 60.7 kHz
DTI	112
Max Integration Time	1206 => 15.075 µs
Minimum $LVAL_{Low\_Period}$	30

Figure 68:
8-Bit Timing Clocks for Readout Mode 4-To-1

Parameters	Clocks
Readout Data	2576
Readout Time	2614
FCT	375
MTA => Line Rate	2614 => 30.6 kHz
DTI	112
Max Integration Time	2502 => 31.275 µs

Parameters	Clocks
Minimum $LVAL_{Low\_Period}$	38

7.11.5 Maximum Line Rate for Region of Interest (ROI)

The sensor features the capability to define a Region of Interest to be readout on each 2K5 segment, using bit 7 of register 0x01. Despite the fact this feature works for 4LS15K and 4LS10K, it was only validated for 4LS5K. This ROI is defined by setting a Start Address (ROI_{Start}) on register 0x19 and an End Address (ROI_{End}) on register 0x1A. The region of interest (number of readout pixels) is given by the following equation:

Equation 9:

$$Data\ (clocks) = \left((ROI_{End} - ROI_{Start}) + 1\right) \times (4 \times m)$$

With:

- m = 1 for 1-To-1
- m = 2 for 2-To-1
- m = 4 for 4-To-1

The use of ROI presents some constrains that the user must respect:

- ROI_{End} address (register 0x1A) cannot be smaller than ROI_{Start} address (register 0x19), however it can be the same.
- The ROI always reads a minimum size of 16 columns.
- Each ROI address will generate a jump of 16 columns on readout. ROI_{Start} and ROI_{End} addresses should be programmed between 0 and 160 (0xA0).

Equation 10:

$$First\ Column = ROI_{Start} \times 16$$

Equation 11:

$$Last\ Column = ROI_{End} \times 16 + 16$$

Equation 12:

$$Line\ Resolution_{Segment} = \#_{LVDS} \times Data$$

With:

- $\#_{LVDS}$ = 4 for 1-To-1
- $\#_{LVDS}$ = 2 for 2-To-1
- $\#_{LVDS}$ = 1 for 4-To-1

Equation 13:

$$Line\ Resolution_{Full} = \#_{Segments} \times Line\ Resolution_{Segment}$$

With:

$\#_{Segments}$ = 2 for 4LS5K.

Figure 69:
Data and VTS Clocks Using ROI Feature

Readout Mode	Data [clocks]	Readout Time [clocks]
1-To-1	Equation 5	Data + 26
2-To-1		Data + 30
4-To-1		Data + 38

The following figures present some possible combinations on the use of ROI.

Figure 70:
Centered ROI

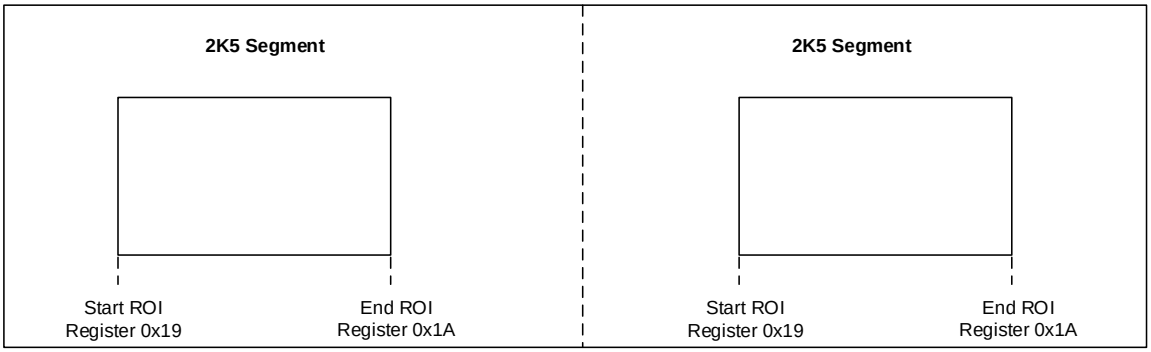
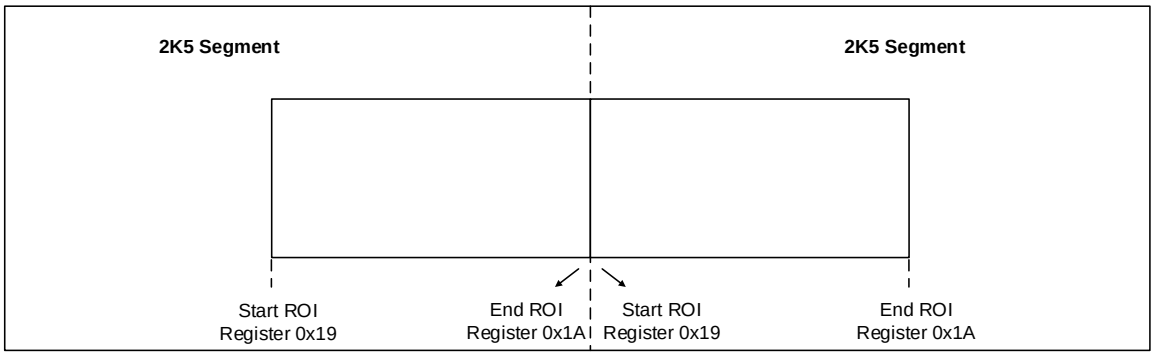


Figure 71:
One ROI Across Two Segments



12-Bit mode @ 60 MHz

Below described is an example to calculate the maximum line rate for 12-bit mode:

- Output mode: 12-bit
- Readout mode: 1-To-1 LVDS
- ADC response stabilization OFF
- Auto-start AD OFF
- Auto-start readout OFF
- End of Range = 0xFF
- Start Region on Interest Register = 0x20
- End Region of interest Register = 0x90

$$Data = \big((144 - 32) + 1\big) \times (4 \times 1) = 452\ clocks$$

$$Readout\ Time = 476 + 26 = 468\ clocks$$

$$Line\ Resolution_{Segment} = 4\ \times 452 = 1808\ pixels$$

$$Line\ Resolution_{Full} = 1808 + 1808 = 3616\ pixels$$

Figure 72:
12-Bit Timing Clocks with ROI On

Parameters	Clocks
RST_CDS	60
ADC Time	707
Readout Data	452
Readout Time	468
SAMPLE	30
START_AD	2
$T_{BTW\_START\_AD\&RST\_RAMP}$	1
$T_{BTW\_SAMPLE\&START\_AD}$	8
FCT	748
MTA => Line Rate	748 => 80.21 kHz
DTI	68
Max Integration Time	680 => 11.33 µs
Minimum $LVAL_{Low\_Period}$	296

The minimum LVAL time at low between two consecutive data streams is:

$$LVAL_{Low\_Period} = 748 - 452 = 296\ clocks$$

Using ROI feature for 12-bit mode, in terms of line rate, it does not bring any advantage, because the ADC time is still much higher than the readout time.

8-Bit mode @ 80 MHz

Below described is an example to calculate the maximum line rate for 8-bit mode, for the below configuration. The region of interested is based on Figure 71.

- Output mode: 8-bit
- Readout mode: 1-To-1 LVDS
- ADC response stabilization OFF
- Auto-start AD OFF
- Auto-start readout OFF
- End of Range = 0x3F

For full resolution, it was verified that the minimum Readout Time is much higher than the ADC time, therefore the maximum line rate was defined by the Readout Time. When performing a ROI in sensor, the goal is to calculate how much the Readout Time can be decreased to achieve the highest line rate possible.

Taking in consideration Equation 4, the MTA and maximum line rate as shown below:

Figure 73:
8-Bit Timing Clocks with ROI On for Readout Mode 1-To-1 – MTA Calculation

Parameters	Clocks
ADC Time	280
SAMPLE	40
START_AD	2
$T_{BTW\_START\_AD\&RST\_RAMP}$	1
$T_{BTW\_SAMPLE\&START\_AD}$	12
DTI	112
MTA	335 => 238.8 kLines/s
Max Integration Time(1)	223 => 2787.5 ns

(1) To use the sensor at the maximum line, this is the maximum integration time possible. When it comes to the minimum integration time, in theory, it is possible to use a lower integration time, but it was not tested on this configuration. From an application perspective, using a lower integration time, does not bring significant advantages, once the line rate cannot be higher and the system would need to increase the illumination power.

Now the Readout Time needs to be calculated in order to achieve the respective line rate and guarantee the minimum LVAL Low Period.

- Start Region of Interest Register Segment A = 0x54 = 84d
- Start Region of Interest Register Segment B = 0x00
- End Region of interest Register Segment A = 0xA0 = 160d
- End Region of Interest Register Segment B = 0x4C = 76d

$$Data = \big((160 - 84) + 1\big) \times (4 \times 1)) = 308\ clocks$$

$$Readout\ Time = 308 + 26 = 334\ clocks$$

$$Line\ Resolution_{Full} = 4\ \times 2\ \times 308 = 2464\ pixels$$

Figure 74:
Complete 8-Bit Timing Clocks with ROI On for Readout Mode 1-To-1

Parameters	Clocks
RST_CDS	100
ADC Time	280
Readout Data	308
Readout Time	334
SAMPLE	40
START_AD	2
$T_{BTW\_START\_AD\&RST\_RAMP}$	1
$T_{BTW\_SAMPLE\&START\_AD}$	12
FCT	335
MTA => Line Rate	335 => 238.8 kHz
DTI	112
Max Integration Time	223 => 2787.5 ns
Minimum $LVAL_{Low\_Period}$	27

$$LVAL_{Low\_Period} = 335 - 308 = 27\ clocks$$

The minimum LVAL time at low between two consecutive data streams is 27 clocks.

For 2-To-1 and 4-To-1 modes, if the goal is still achieve the maximum line rate, the ROI needs to decreased even more, because the number of the output is also lower. Please note that the minimum LVAL low period needs always to be in consideration.

For 2-To-1 mode:

- Start Region of Interest Register Segment A = 0x7B = 123d
- Start Region of Interest Register Segment B = 0x00
- End Region of interest Register Segment A = 0xA0 = 160d
- End Region of Interest Register Segment B = 0x25 = 37d

$$Data = \big((160 - 123) + 1\big) \times (4 \times 2)) = 304\ clocks$$

$$Readout\ Time = 304 + 30 = 334\ clocks$$

$$Line\ Resolution_{Full} = 2\ \times 2 \times 304 = 1216\ pixels$$

Figure 75:
8-Bit Timing Clocks with ROI On for Readout Mode 2-To-1

Parameters	Clocks
Readout Data	304
Readout Time	334
FCT	335
MTA => Line Rate	335 => 238.8 kHz
DTI	112
Max Integration Time	223 => 2787.5 ns
Minimum $LVAL_{Low\_Period}$	31

For 4-To-1 mode:

- Start Region of Interest Register Segment A = 0x8F = 143d
- Start Region of Interest Register Segment B = 0x00
- End Region of interest Register Segment A = 0xA0 = 160d
- End Region of Interest Register Segment B = 0x11 = 17d

$$Data = \big((160 - 123) + 1\big) \times (4 \times 4)) = 288\ clocks$$

$$Readout\ Time = 288 + 38 = 326\ clocks$$

$$Line\ Resolution_{Full} = 1\ \times 2 \times 288 = 576\ pixels$$

Figure 76:
8-Bit Timing Clocks with ROI On for Readout Mode 4-To-1

Parameters	Clocks
Readout Data	208
Readout Time	326
FCT	335
MTA => Line Rate	335 => 238.8 kHz
DTI	112
Max Integration Time	223 => 2787.5 ns
Minimum $LVAL_{Low\_Period}$	47

7.12 Anti-Corona Circuitry

“Corona effect” is a phenomenon sometimes observed under heavy overexposure condition when the most exposed pixels start to become dark again instead of white. This condition can be detected by a special circuitry and saturated pixels are then clamped to the white reference value, before A/D

conversion. This circuitry can be enabled or bypassed by means of register 0x01, bit 6. A '0' will disable the anti-corona circuitry and bypass the signal, while a '1' will enable it.

7.13 Temperature Sensor

The image sensor includes a temperature sensor that will provide the silicon temperature over the MISO line. To retrieve the temperature, the user must perform a read request over the SPI to the register 0x1B. The temperature is converted from analogue to digital value (8-bit representation) on every LVAL falling edge, and stored in the register to be read by the user.

The formula to retrieve the temperature from the read digital values (in decimal) is the following:

Equation 14:

$$Temperature = \frac{(Digital\ Value) - 50.74}{1.42}\ ℃$$

The digital step is approximately 0.7ºC.

The following table presents typical output values for the respective die temperature.

Figure 77:
Temperature and Respective Register Value Read Over SPI

Temperature [ºC]	Value Read [Decimal]
~ 0	51
~ 55	128
~ 120	222

Attention

Please note that the temperature sensor is not a main feature of 4LS. It only monitors the silicon temperature and does not have any influence in data stability and/or image quality. This temperature sensor is only providing an indicative temperature value. This functionality is not part of the core of this product.

8 Digital Interface

The sensor features two different types of control interfaces: SPI interface (using on chip registers) and digital control lines.

8.1 Digital Control Lines

The digital control lines allows a dynamic control that grant maximum flexibility for readout control operations, CVC control, CDS control and test control signals. Most of these signals changes the logic state during pixel integration, A/D conversion and readout that cannot be done using static configuration, due to read and write operation times.

Figure 78 lists all the digital signals used as digital control lines on each 2K5 segment on top and bottom.

Figure 78:
Digital Control Lines

Signal	Function
Ext Sync	By configuration, the serializer can be set to synchronize phase to the rising edge of this signal
LVAL	When at high informs that the line data is valid
N RST Logic	Low active reset for sensor logic
N RST PLL	Low active reset for PLL logic
RST CVC L1	Reset signal to CVC block with respect to Line 1
RST CDS L1	Reset signal to CDS block with respect to Line 1
Sample L1	Performs the signal sampling at the ADC input with respect to Line 1
RST CVC L2	Reset signal to CVC block with respect to Line 2
RST CDS L2	Reset signal to CDS block with respect to Line 2
Sample L2	Performs the signal sampling at the ADC input with respect to Line 2
Start A/D conversion	Starts the A/D conversion for the last integrated line
Start readout	Starts the readout of last converted line

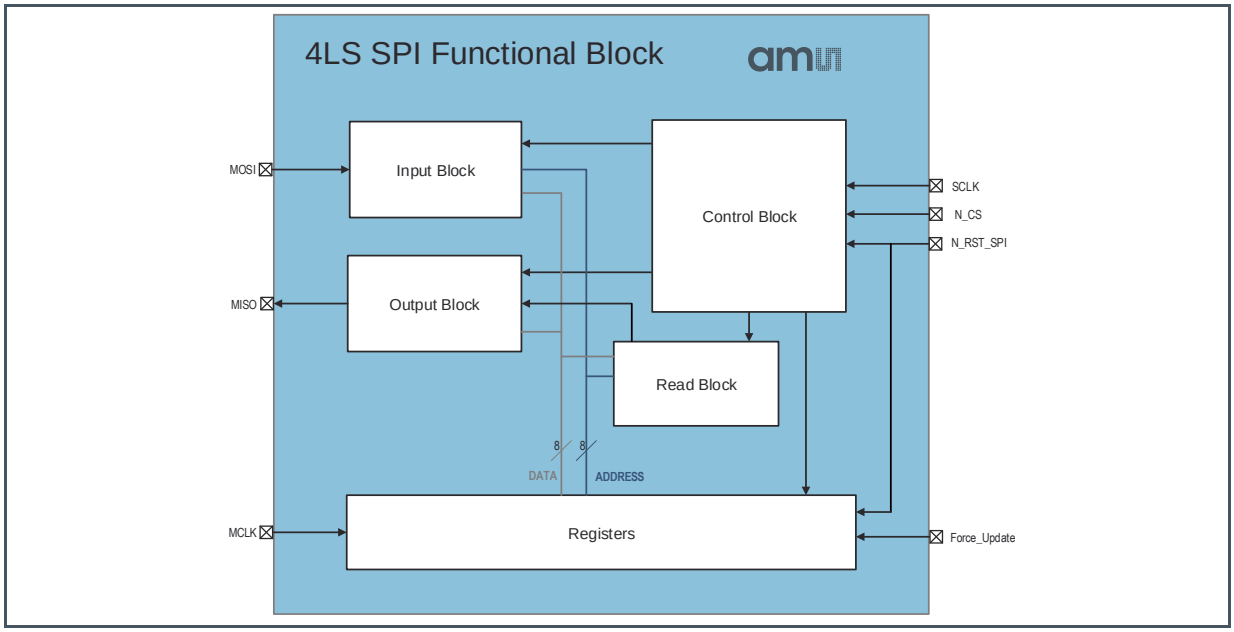
8.2 SPI Interface

8.2.1 General Description

The SPI interface controls static configuration data, such as operation modes, ADC gain, black level, bias currents, etc. It is present in every segment, top and bottom sides. This interface is based on 8-bit registers and addressed using 8-bit addresses.

Figure 79 shows the block diagram of the SPI.

Figure 79:
SPI Functional Block



This interface uses the following signals.

Figure 80:
SPI Signals

Signal	Function
Force Update	Forces the write of the latest data to registers, transferring from shadow to effective memory
MISO	Master In, Slave Out
MOSI	Master Out, Slave In
N_CS	Low active chip select
N_RST_SPI	Low active reset for both SPI interface and all registers
SCLK	Serial interface clock frequency
T_{SCLK}	Serial interface clock period

The command word has a length of 16 bits that contains the address of the register and the data. The SCLK signal frequency, should not be higher than ¼ of main clock up to 12.5 MHz i.e., if MCLK is 10 MHz, SCLK should be defined to a maximum of 2.5 MHz, however if MCLK is >50 MHz, SCLK should not exceed 12.5 MHz.

For read and write operations the data is sent from MSB to LSB.

To use the interface, first the N_CS signal should go low, then the word should be sent synchronous with the SCLK. The data is captured at the MOSI input with the rising edge of SCLK and is sent out on the MISO output on the falling edge of SCLK.

The updating of registers on the sensor can be made using three different methods: update request, immediate update and force update. The update request and immediate update are both set by register 0x01 using the bits 3:0. When update request is set, the read/write operation from shadow memory to effective is only performed with falling edge of LVAL signal. In the case of immediate update the read/write operation from shadow memory to effective is performed immediately, independently if the sensor is performing integration, A/D conversion or readout.

The Force Update[1] method is similar to the immediate update, but is given as an external signal (pulse with 2 x T_{MCLK} minimum). Force Update updates the register values in the moment that pulse is applied. Therefore, when using Force Update signal, please make sure that LVAL is low, avoiding defect lines.

8.2.2 Writing Operation

The writing operation is performed by sending the word containing the data and the address and no acknowledge signal or indication is given back. It can be performed continuously. When writing to the registers, the last word to be sent to the register has to be always the update request or immediate update or force update (STS1Reg – 0x01), otherwise the write is not performed.

After the last word of data is sent to SPI interface, the SCLK should be maintained during 4 x T_{SCLK}.

Figure 81 exemplifies how to perform the operation over the interface.

Figure 81:
Write Cycle Over SPI Interface

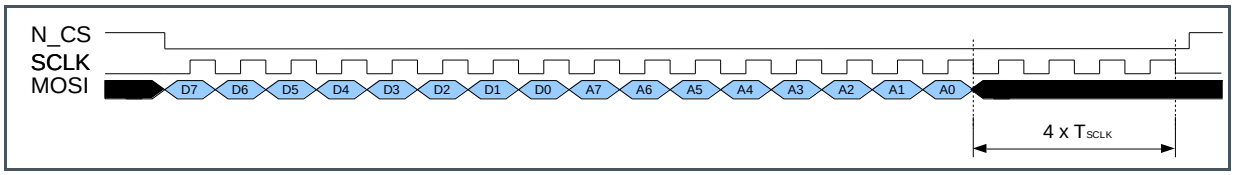
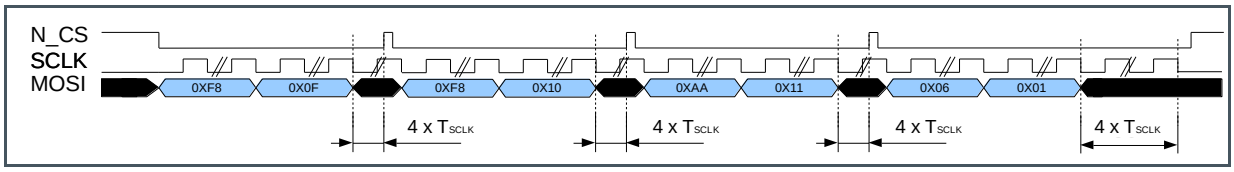


Figure 82 exemplifies a cycle of multiple writing operations.

[1] Despite the fact Force Update works properly, Immediate and Update Request are the recommended ones.

Figure 82:
Write Cycle for Multiple Registers



8.2.3 Reading Operation

The reading operation is performed by sending to read request register (RRQReg - 0x1C) the address of the register to be read. Notice that the read is an immediate operation and if performed between write/update requests and the next falling edge of LVAL, the data read is the one before the update operation. Thus, it is important to read after an update request and wait until the falling edge of next LVAL signal is sent, otherwise the read back can be invalid. Instead of waiting for the next falling edge of the LVAL, an update event can be triggered over the STS1 register by “immediate update” or “update request”.

With respect to read back of registers from the ADC companding threshold registers and ADC end range registers, the register update is only performed once the A/D conversion is completed. Thus, if during the update event (falling edge of LVAL or immediate update request) an A/D conversion is running, the update of those registers is delayed until the end of the A/D conversion. Read back should only be performed afterwards.

The output data of the read will be sent on the MISO line with 3 SCLK delay to the last bit from the address word (MSB first). It is only possible to read one register at a time, but it is possible to perform consecutive reads from the same segment and register. The raise of N_CS signal can be made right after the complete read of the last bit and SCLK should be placed on hold.

Figure 83 presents an example for a read operation.

Figure 83:
Read Cycle Over SPI Interface

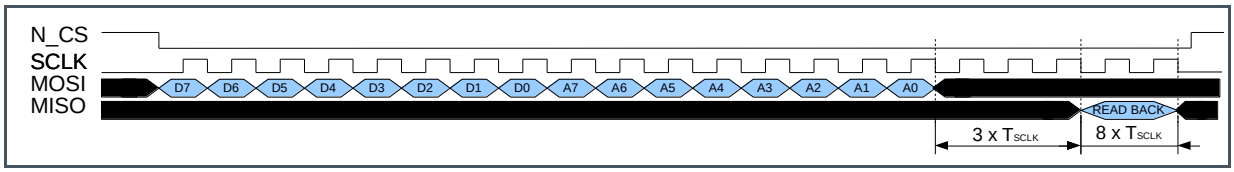


Figure 84:
Read Back Data in Detail

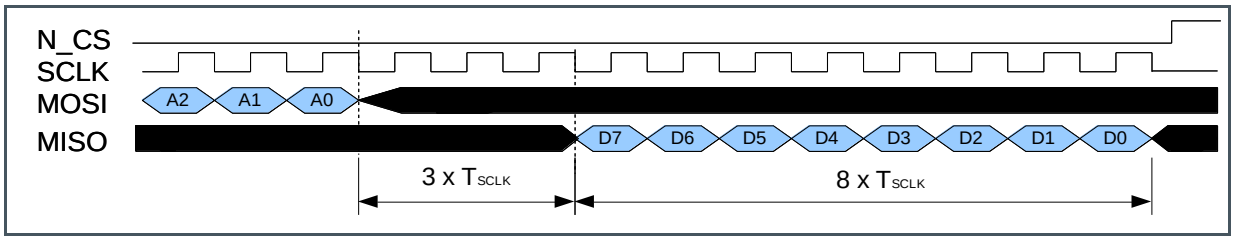
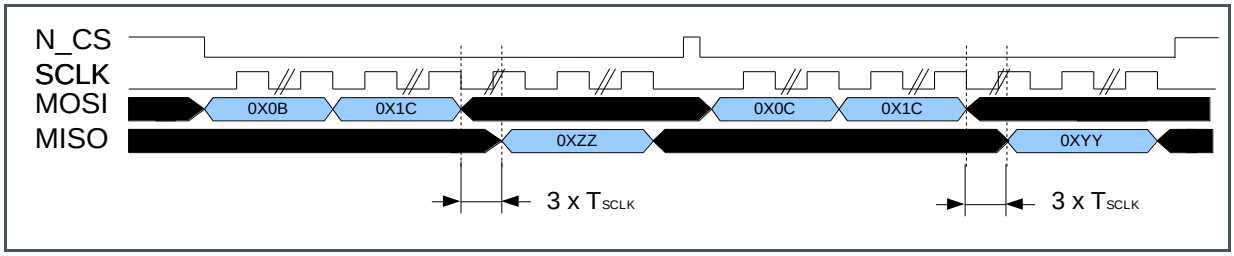


Figure 85 exemplifies a cycle of multiple reading operations.

Figure 85:
Read Cycle For Multiple Registers



8.2.4 Operation Conditions

Functional operation of the SPI is guaranteed under below conditions.

Figure 86:
Power Supply Conditions

Parameter	Description	Min	Typical	Maximum	Unit
VDDIO	Power Supply Voltage (IO)	1.7	1.8	1.9	V
V_{nrms} VDDIO	RMS Noise on VDDIO			10	mV
V_{npp} VDDIO	Peak to Peak Noise on VDDIO			60	mV
VSSIO	Ground for IO Power Supply		0		V

Figure 87:
DC Electrical Conditions

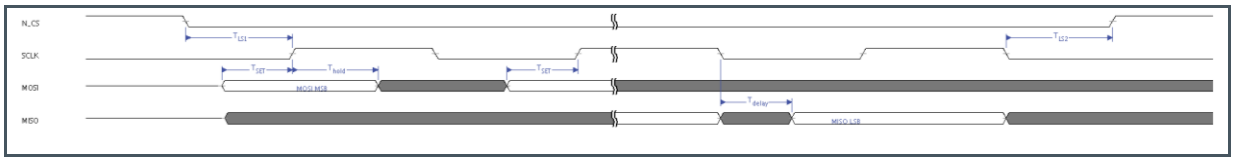
Parameter	Description	Min	Maximum	Unit
V_{OL}	Low Level Output Voltage	0	0.6	V

Parameter	Description	Min	Maximum	Unit
V_{OH}	High Level Output Voltage	VDDIO – 0.6	VDDIO + 0.6	V

Figure 88:
AC Electrical Conditions

Parameter	Description	Min	Maximum	Unit
F_{SCLK}	SCLK Frequency.		< 1/4 of MCLK up to 12.5 MHz	V
T_{LS1}	Time from falling edge of N_CS to first rising edge of SCLK.	50		ns
T_{LS2}	Time form last falling edge of SCLK to the rising edge of N_CS.	50		ns
T_{SET}	Time between MOSI stable and rising edge of SCLK.	10		ns
T_{LH}	Time between SPI cycles (between rising and falling edge of N_CS); minimum SPI idle time.	1		ns
T_{Hold}	Time that MOSI need to be stable after the rising edge of SCLK.	5		ns
T_{Delay}	Time between falling edge of SCLK and stable data on MISO.		10	ns
T_{Rise}	Rise time for SPI signals.	2	20	ns
T_{Fall}	Fall time for SPI signals.	2	20	ns

Figure 89:
Time Guard Between Signals



9 Register Description

The registers are responsible for the static control of the CIS. They are used to set operating values and define states/modes for the sensor. They can also be used to test the sensor, for instance, set dedicated values to the LVDS outputs. Section 9.1 shows the default register setting.

9.1 Detailed Register Description

9.1.1 Chip Revision Register (Address 0x00)

Figure 90:
CRReg

Address: 0x00		Default Value: 0x02	Access: Read Only
Bit	**Bit Name**	**Default**	**Bit Description**
0:7	Revision(1)	00000010b	CIS chip revision

(1) The content of this register can only be modified by metal mask redesign.

9.1.2 Status 1 Register (Address 0x01)

Figure 91:
STS1Reg

Address: 0x01		Default Value: 0x85	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:7	ROI(1)	1b	When set to '1' the ROI is active.
6:6	Anti-corona	0b	When set to '1' enables the anti-corona circuitry.
5:5	Companding Mode	0b	When set to '1' enables the A/D conversion to companding mode.

Address: 0x01		Default Value: 0x85	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
4:4	Sync Bit	0b	When set to '1' the synchronization of the serializer phase to the main clock is performed by an external signal. When set to '0' automatically resynchronize at each rising edge of start of readout.
3:2	Immediate Update	01b	The code 10b request an immediate update on the effective registers. After an update event the bits will be cleared to 01b (no immediate update).
1:0	Update Request	01b	The code 10b request an update from the shadow registers to the effective registers on the next falling edge of the line valid signal. After an update event the bits will be cleared to 01b (no update). These bits have to be written after each complete set of register configurations to make the changes active.

(1) The Region of Interest (ROI) operation is a main feature of 4LS5K. For standard operation, using full line resolution, the bit should be set to ‘0’.

9.1.3 Status 2 Register (Address 0x02)

Figure 92:
STS2Reg

Address: 0x02		Default Value: 0x00	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:7	2-To-1 Output	0b	When set to ’0’, default mode 1-To-1 is used. When set to ‘1’ reduces the number of outputs taps from 4 to 2 per line and per segment.
6:6	4-To-1 Output	0b	When set to ’0’, default mode 1-To-1 is used. When set to ‘1’ reduces the number of output taps from 4 to 1 per line and per segment.
5:5	Auto Start Readout	0b	Activates the automatic start readout when set at ‘1’.
4:4	Auto Start A/D	0b	Activates the automatic start A/D conversion when set at ‘1’.

Address: 0x02		Default Value: 0x00	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
3:3	Output Mode	0b	Sets the output transmission mode. When set to '1' the transmission is performed at 8-bit (maximum MCLK = 80 MHz). When set to '0' the transmission is performed at 12-bit (maximum MCLK = 60 MHz).
2:0	PLL Division	000b	These 3 bits are responsible for the PLL clock division configuration.

Figure 93:
Frequency Range Programmed by PLL Division

Bit 2	Bit 1	Bit 0	Division Value	Frequency Range of MCLK [MHz] for 12-Bit Mode	Frequency Range of MCLK [MHz] for 8-Bit Mode
0	**0**	**0**	**0**	**37.5 – 60**	**75 – 80**
0	0	1	2	19 – 37.5	38 – 75
0	1	0	4	9 –19	18 – 38
0	1	1	8	4.5 – 9	9 – 18
1	0	0	16	2 – 4.5	4 – 9

9.1.4 Status 3 Register (Address 0x03)

Figure 94:
STS3Reg

Address: 0x03		Default Value: 0x00	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:7	VBL Top Bottom Connection	0b	When set to ‘1’ connects the black level voltage between Top and Bottom elements.
6:6	VREF Top Bottom Connection	0b	When set to ‘1’ connects the CDS reference voltage between Top and Bottom elements.
5:5	RAMP L1 L2 Connection	0b	When set to ‘1’ connects Ramp Line 1 to Ramp Line 2 from each segment individually.

Address: 0x03		Default Value: 0x00	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
4:4	Top Bottom Connection	0b	When set to '1' connects the analogue reference signals between Top and Bottom elements. Signals connected when this bit is high: ADC gain ref input, ADC gain ref output, VREF (CDS reference voltage), VBL (ADC offset - black level voltage).
3:3	Gain CDS L2	0b	When set to '1' defines the analogue gain on the CDS stage to be 2x.
2:2	Gain CDS L1	0b	When set to '1' defines the analogue gain on the CDS stage to be 2x.
1:1	CVC L2 Full Well Capacity	0b	When '0' and Gain CDS L2 = '1' the Full Well Capacity is 10 ke- When '0' and Gain CDS L2 = '0' the Full Well Capacity is 20 ke- When '1' and Gain CDS L2 = '0' the Full Well Capacity is 40 ke-
0:0	CVC L1 Full Well Capacity	0b	When '0' and Gain CDS L1 = '1' the Full Well Capacity is 10 ke- When '0' and Gain CDS L1 = '0' the Full Well Capacity is 20 ke- When '1' and Gain CDS L1 = '0' the Full Well Capacity is 40 ke-

9.1.5 Analogue Gain for Line 1 Register (Address 0x04)

Figure 95:
AGL1Reg

Address: 0x04		Default Value: 0x80	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:0	Analogue Gain Level	10000000b	It defines the analogue gain level in the ADC which defines the voltage equivalent to one ADC step (1 DN) applied to the Line 1.

9.1.6 Analogue Gain for Line 2 Register (Address 0x05)

Figure 96:
AGL2Reg

Address: 0x05		Default Value: 0x80	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:0	Analogue Gain Level	10000000b	It defines the analogue gain level in the ADC which defines the voltage equivalent to one ADC step (1 DN) applied to the Line 2.

9.1.7 Black Level Offset Register (Address 0x06)

Figure 97:
BLOReg

Address: 0x06		Default Value: 0x80	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:0	Black Level Offset	10000000b	It defines the analogue black level offset that corresponds to the ADC offset.

The Black Level value is dependent of the Vref value (register 0x0B bits[1:0]), varying 1.4 V around the respective Vref voltage (approximately 36% below and 64% above the reference). For instance, if Vref has a voltage of 1.8 V, and BLOReg is set to (0x00), therefore the Black level is 1.31 V. Similarly, for the maximum value of BLOReg (0xFF), the Black level is 2.57 V. Each register step is equivalent to approximately 5 mV.

9.1.8 Companding Threshold 1 Register (Address 0x07)

Figure 98:
CT1Reg

Address: 0x07		Default Value: 0x00	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:0	Companding Threshold 1	00000000b	It defines, in companding mode, the first ADC step.

9.1.9 Companding Threshold 2 Register (Address 0x08)

Figure 99:
CT2Reg

Address: 0x08		Default Value: 0x80	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:0	Companding Threshold 2	10000000b	It defines, in companding mode, the second ADC step.

9.1.10 Companding Threshold 3 Register (Address 0x09)

Figure 100:
CT3Reg

Address: 0x09		Default Value: 0x00	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:0	Companding Threshold 3	00000000b	It defines, in companding mode, the third ADC step.

9.1.11 End of Range Register (Address 0x0A)

Figure 101:
EORReg

Address: 0x0A		Default Value: 0xFF	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:0	End of Range Level	11111111b	It defines the digital level for the ADC conversion.

This register sets the value for the end of range for the ADC, or the highest value the ADC will compute. It is with this value that the conversion time for the ADC is defined. Since the ADC is 12-bit and the register only holds 8-bit, the register holds the 8 MSB from a 12-bit word.

Figure 102:
End of Range Value According to ADC Resolution

ADC Resolution	Maximum EOR Value
12-bit	0xFF
8-bit	0x3F

9.1.12 Programmable Bias Current Register (Address 0x0B)

Figure 103:
PBCReg

Address: 0x0B		Default Value: 0x55	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:6	Comparator Bias	01b	It defines the comparator bias current multiplier.
5:4	CVC Bias	01b	It defines the CVC bias current multiplier.
3:2	CDS Bias	01b	It defines the CDS bias current multiplier.
1:0	VREF Trimming	01b	It defines the VREF voltage to be used on all CDS on the sensor.

Figure 104:
Comparator Bias Current Programmed by Register

Bit 7	Bit 6	Comparator Bias Current [µA]
0	0	5
0	**1**	**7.5**
1	0	10
1	1	12.5

Figure 105:
CVC Bias Current Programmed by Register

Bit 5	Bit 4	CVC Bias Current [µA]
0	0	2.5
0	**1**	**5**
1	0	7.5

Bit 5	Bit 4	CVC Bias Current [µA]
1	1	10

Figure 106:
CDS Bias Current Programmed by Register

Bit 3	Bit 2	CDS Bias Current [µA]
0	0	5
0	**1**	**10**
1	0	15
1	1	20

Figure 107:
VREF Trimming Current Programmed by Register

Bit 1	Bit 0	Current [µA]	Voltage [V]
0	0	60	1.6
0	**1**	**67.5**	**1.8**
1	0	75	2
1	1	82.5	2.2

9.1.13 Programmable LVDS Register (Address 0x0C)

Figure 108:
PLVDReg

Address: 0x0C		Default Value: 0x8D	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:5	Bandgap Trimming	100b	It defines the bandgap tuning due to devices production variations.
4:2	LVDS Bias	011b	It defines the LVDS driver bias current multiplier.
1:0	VRST Special Trimming	01b	**Internal Debug Purposes** Use default value.

Figure 109:
Bandgap Trimming Current Programmed by Register

Bit 7	Bit 6	Bit 5	Bandgap Trimming Current [µA]
0	0	0	15.8
0	0	1	16.8
0	1	0	18.0
0	1	1	19.6
1	**0**	**0**	**21.4**
1	0	1	23.4
1	1	0	25.8
1	1	1	28.8

Figure 110:
LVDS Bias Current Programmed by Register

Bit 2	Bit 1	Bit 0	LVDS Current [µA]	LVDS Consumption Per Tap [mW] @ 1.8V(1)
0	0	0	0	0
0	0	1	400	0.72
0	1	0	800	1.44
0	**1**	**1**	**1200**	**2.16**
1	0	0	1600	2.88
1	0	1	2000	3.60
1	1	0	2400	4.32
1	1	1	2800	5.09

(1) LVDS consumption for one LVDS driver.

The total LVDS consumption should be calculated assuming the following figure with the number of LVDS enabled for each configuration.

Figure 111
Total Number of LVDS Drivers per 2K5 Segment

	Top Side		Bottom Side		Total Number of LVDS (per 2K5 segment)
	LVDS Driver Data Clock	LVDS Driver Data	LVDS Driver Data Clock	LVDS Driver Data	
1-To-1	**1**	**8**	**1**	**8**	**18**
2-To-1	1	4	1	4	10
4-To-1	1	2	1	2	6

9.1.14 Test Multiplexer Register (Address 0x0D)

This register sets the output of test analogue pad to a certain signal.

Figure 112:
TMXReg

Address: 0x0D		Default Value: 0x00	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:5	N/A	00b	Not used.
4:0	Test Multiplexer output select	000000b	**Internal Debug Purposes** Defines the output of the test multiplexer to a specific test signal.

9.1.15 Test Mode Register (Address 0x0E)

This register sets the CIS to defined states, so that some tests can be performed to debug/check some blocks and operational conditions.

Figure 113:
TMDReg

Address: 0x0E		Default Value: 0x30	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:6	N/A	00b	Not used.
5	Auto Transfer	1b	**Internal Debug Purposes** When set to ‘1’ increases the time to transfer data from shadow to effective memory.

Address: 0x0E		Default Value: 0x30	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
4:4	NAND Tree Mode	1b	**Internal Debug Purposes** When set to '0' places the NAND tree active to perform the test. To disable the NAND tree test mode this bit should be '1'.
3:3	SRAM Mode	0b	**Internal Debug Purposes** When set to '1' defines the SRAM memory test mode. It uses the content of register 0x17 and 0x18.
2:2	Training Mode	0b	When set to '1' defines the training test data mode to be sent by the output LVDS data. It uses the content of register 0x12 and 0x16. When set to '0' the Data is received from the Pixels.
1:1	Counter Test Mode	0b	**Internal Debug Purposes** When set to '1' defines the test mode for counter block.
0:0	ADC Test Mode	0b	**Internal Debug Purposes** When set to '1' defines the test mode for the ADC block.

9.1.16 Training Sequence 1 Line 1 Register (Address 0x0F)

Figure 114:
TSQ1L1Reg

Address: 0x0F		Default Value: 0xFF	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:0	Training sequence 1	11111111b	Defines the 8 MSBs for word A training sequence sent over the LVDS driver of Line 1 for FPGA synchronization purposes.

9.1.17 Training Sequence 2 Line 1 Register (Address 0x10)

Figure 115:
TSQ2L1Reg

Address: 0x10		Default Value: 0xFF	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:0	Training sequence 2	11111111b	Defines the 8 MSBs for word B training sequence sent over the LVDS driver of Line 1 for FPGA synchronization purposes.

9.1.18 Training Sequence 3 Line 1 Register (Address 0x11)

Figure 116:
TSQ3L1Reg

Address: 0x11		Default Value: 0xA9	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:0	Training sequence 3	10101001b	Defines the LSBs for word A and B training sequence sent over the LVDS driver of Line 1 for FPGA synchronization purposes.

9.1.19 Test Data Serializer Line 1 Register (Address 0x12)

Figure 117:
TDSL1Reg

Address: 0x12		Default Value: 0x40	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:0	Training test data	01000000b	When the sensor is in training mode, defines the data pattern to test the serialization / LVDS data output blocks for Line 1. The register value is concatenated with 0x0A (LSB), getting a 12-bit word. For 12-bit mode, test data is the full 12-bit word. For 8-bit mode, the 2 MSB and 2 LSB are discarded to get a 8-bit test data word.

9.1.20 Training Sequence 1 Line 2 Register (Address 0x13)

Figure 118:
TSQ1L2Reg

Address: 0x13		Default Value: 0xFF	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:0	Training sequence 1	11111111b	Defines the 8 MSBs for word A training sequence sent over the LVDS driver of Line 2 for FPGA synchronization purposes.

9.1.21 Training Sequence 2 Line 2 Register (Address 0x14)

Figure 119:
TSQ2L2Reg

Address: 0x14		Default Value: 0xFF	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:0	Training sequence 2	11111111b	Defines the 8 MSBs for word B training sequence sent over the LVDS driver of Line 2 for FPGA synchronization purposes.

9.1.22 Training Sequence 3 Line 2 Register (Address 0x15)

Figure 120:
TSQ3L2Reg

Address: 0x15		Default Value: 0xAA	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:0	Training sequence 3	10101010b	Defines the LSBs for word A and B training sequence sent over the LVDS driver of Line 2 for FPGA synchronization purposes.

9.1.23 Test Data Serializer Line 2 Register (Address 0x16)

Figure 121:
TDSL2Reg

Address: 0x16		Default Value: 0x40	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:0	Training test data	01000000b	When the sensor is in training mode, defines the data pattern to test the serialization / LVDS data output blocks for Line 2. The register value is concatenated with 0x0A (LSB), getting a 12-bit word. For 12-bit mode, test data is the full 12-bit word. For 8-bit mode, the 2 MSB and 2 LSB are discarded to a get 8-bit test data word.

9.1.24 SRAM Mode Test 1 Register (Address 0x17)

Figure 122:
SMT1Reg

Address: 0x17		Default Value: 0x00	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:0	SRAM test data	00000000b	Defines the 8 LSB data to be written on the SRAM.

9.1.25 SRAM Mode Test 2 Register (Address 0x18)

Figure 123:
SMT2Reg

Address: 0x18		Default Value: 0x00	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:5	N/A	000b	Not used.
4:0	SRAM test data	00000b	Defines the 5 MSB data to be written on the SRAM.

9.1.26 Start Region of Interest Register (Address 0x19)

Figure 124:
SROIReg

Address: 0x19		Default Value: 0x00	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:0	ROI_{Start} (1)	00000000b	Defines the start address for the region to be read.

(1) Applicable for 4LS5K. Register related to Region of Interest (ROI) feature on Sections 7.11.5 and 9.1.2. Only valid when ROI is active.

9.1.27 End Region of Interest Register (Address 0x1A)

Figure 125:
EROIReg

Address: 0x1A		Default Value: 0xA0	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:0	ROI_{End} (1)	10100000b	Defines the end address for the region to be read.

(1) Applicable for 4LS5K. Register related to Region of Interest (ROI) feature on Sections 7.11.5 and 9.1.2. Only valid when ROI is active.

9.1.28 Temperature Sensor Register (Address 0x1B)

Figure 126:
TEMPReg

Address: 0x1B		Default Value: 0x00	Access: Read
Bit	**Bit Name**	**Default**	**Bit Description**
7:0	Temperature Sensor	00000000b	Holds the digital value for the silicon temperature.

9.1.29 Read Request Register (Address 0x1C)

Figure 127:
RRQReg

Address: 0x1C		Default Value: 0x00	Access: Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:0	Address to Read	00000000b	Defines the register address to be read in a read back operation over SPI interface.

9.1.30 Status 4 Register (Address 0x1D)

Figure 128:
STS4Reg

Address: 0x1D		Default Value: 0x49	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:7	Enable VRST Special Buffer	0b	**Internal Debug Purposes** Use default value.
6:6	Enable Boost VREF	1b	When set to ‘1’ enables a higher output current on VREF buffer.
5:5	Enable Boost VRST Special	0b	**Internal Debug Purposes** Use default value.
4:4	Special Mode	0b	**Internal Debug Purposes** Use default value.
3:3	Standard Mode	1b	When set to ‘1’ enables readout of regular pixels. Use default value.
2:2	PLL Enhance Current	0b	To be used in case of insufficient current to PLL or process defect.
1:1	Set Counter Reference Voltage	0b	Sets the counter LVDS reference voltage to 0.9 V or 0.5 V when at ‘0’ or ‘1’, respectively.
0:0	Sense Switches ON	1b	When set to ‘1’ enables the Sense Amps switches.

9.1.31 Status 5 Register (Address 0x1E)

Figure 129:
STS5Reg

Address: 0x1E		Default Value: 0x30	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:7	VREF CDS Buff Half Current	0b	When set to '1' reduces the VREF CDS buffer current to half.
6:6	VRST Pixel Buff Half Current	0b	When set to '1' reduces the VRST pixel buffer current to half.
5:4	CLK Phase	11b	It is used to choose between Rise-Edge and Fall-Edge of MLCK to perform the serializer synchronization.
3:2	PLL Resistor	00b	Increases the PLL resistor for stabilization purposes.
1:0	PLL Charge Pump	00b	To be used to configure the current on the PLL charge pump.

Figure 130:
Effect on MLCK Provided to Serializer of 4LS

CLK Phase	Bit 5	Bit 4	Effect on MLCK Provided to Serializer
00	0	0	Copy of MCLK
01	0	1	Inverted copy of MCLK
10	1	0	Copy of MCLK delayed by 1 PLL clock
11	**1**	**1**	**Copy of MCLK delayed by 2 PLL clocks**

Figure 131:
PLL Charge Pump Programmed by Register

Bit 1	Bit 0	Current [µA]
0	**0**	**1.6**
0	1	3.2
1	0	4.9
1	1	6.5

9.1.32 Status 6 Register (Address 0x1F)

Figure 132:
STS6Reg

Address: 0x1F		Default Value: 0x05	Access: Read/Write
Bit	**Bit Name**	**Default**	**Bit Description**
7:7	Slow Clock ON	0b	**Internal Debug Purposes** Use default value.
6:6	Ramp Buff Half Current	0b	When set to ‘1’ reduces the Ramp buffer current to half.
5:4	VREF CVC Trimming	00b	Defines the VREF voltage to be used on all CVC on the sensor.
3:3	RAMP Connection between Segments	0b	When set to ‘1’ ramps reconnected segments, connecting ramp L1 with ramp L2 and then they are connected between each segment.
2:2	Enable Boost VREF CVC Buffer	1b	Enables a higher output current on VREF CVC buffer.
1:1	Enable Pre-charge over SRAM	0b	**Internal Debug Purposes** Use default value.
0:0	ADC Response Stabilization	1b	When set to '1' the ramp have more time to stabilize before start the A/D conversion.

Figure 133:
VREF CVC Trimming

Bit 1	Bit 0	Vref CVC Trimming [V]
0	**0**	**1.1 V**
0	1	1.2 V
1	0	1.3 V
1	1	1.4 V

9.2 Register Mapping

The figure below shows the mapping of all registers (default values) on a 2K5 segment, being applicable for the remaining segments.

Figure 134:
Default Sensor Register Setting

Address	Register ID and Description	Default Value
0x00	CRReg – Holds the CMOS image sensor version	0x02
0x01	STS1Reg – Holds several configuration bits	0x85
0x02	STS2Reg – Holds several configuration bits	0x00
0x03	STS3Reg – Holds several configuration bits	0x00
0x04	AGL1Reg – Sets the analogue gain (step size of ADC) applied on Line 1	0x80
0x05	AGL2Reg – Sets the analogue gain (step size of ADC) applied on Line 2	0x80
0x06	BLOReg – Sets the black level reference for the ADC	0x80
0x07	CT1Reg – Sets the first knee point for companding ADC mode	0x00
0x08	CT2Reg – Sets the second knee point for companding ADC mode	0x80
0x09	CT3Reg – Sets the third knee point for for companding ADC mode	0x00
0x0A	EORReg – Sets the end of range for the ADC (highest ADC code & ADC conversion time)	0xFF
0x0B	PBCReg – Sets the current provided by the bias block	0x55
0x0C	PLVDReg – Sets the current used on LVDS driver	0x8D
0x0D	TMXReg – Sets the output of test multiplexer to the test analogue pad	0x00
0x0E	TMDReg – Sets the CIS mode state for debugging and testing	0x30
0x0F	TSQ1L1Reg – Sets the 8 MSBs for training sequence word A	0xFF
0x10	TSQ2L1Reg – Sets the 8 MSBs for training sequence word B	0xFF
0x11	TSQ3L1Reg – Sets the LSBs for training sequence word A and B	0xA9
0x12	TDSL1Reg – Sets the data pattern to be sent out via Data outputs in training mode	0x40
0x13	TSQ1L2Reg – Sets the 8 MSBs for training sequence word A	0xFF
0x14	TSQ2L2Reg – Sets the 8 MSBs for training sequence word B	0xFF
0x15	TSQ3L2Reg – Sets the LSBs for training sequence word A and B	0xAA
0x16	TDSL2Reg – Sets the data pattern to be sent out via Data outputs in training mode	0x40
0x17	SMT1Reg – Sets the LSB data pattern to be written on the memory for test	0x00
0x18	SMT2Reg – Sets the MSB data pattern to be written on the memory for test	0x00
0x19	SROIReg – Sets the start address for the ROI to be read	0x00
0x1A	EROIReg – Sets the end address for the ROI to be read	0xA0
0x1B	TEMPReg – Holds the temperature value retrieved and converted by the temperature sensor	0x00

Address	Register ID and Description	Default Value
0x1C	RRQReg – Sets the address of the register to be read on a read back operation	0x00
0x1D	STS4Reg- Holds several configuration bits	0x49
0x1E	STS5Reg- Holds several configuration bits	0x30
0x1F	STS6Reg- Holds several configuration bits	0x05

The figure below shows the values of the recommend registers that can be applied to all segments.

Figure 135:
Recommended Sensor Register Setting(1)

Address	Register ID and Description	Recommended Value
0x01	STS1Reg – Holds several configuration bits	0x19(2)
0x02	STS2Reg – Holds several configuration bits	0x00(3)
0x0B	PBCReg – Sets the current provided by the bias block	0x31
0x0C	PLVDReg – Sets the current used on LVDS driver	0x9D(4)
0x1D	STS4Reg- Holds several configuration bits	0x48
0x1E	STS5Reg- Holds several configuration bits	0x30(5)
0x1F	STS6Reg- Holds several configuration bits	0x35

(1) The referred registers are the relevant ones for a stable startup and normal sensor operation.
(2) See the recommended startup sequence recommendation (Section 7.2). Will have different value if using ROI for 4LS5K.
(3) Dependently of Readout mode, ADC mode and MCLK frequency, the user must use the respective register value.
(4) Increase the LVDS bias current for a better signal detection.
(5) This CLK phase configuration is specific for the ams OSRAM test system. CLK phase for PLL clock compensation should be chosen according to the user hardware, in order to have stable sensor operation.

10 Pin Description

10.1 Pinout Assignment for 4LS15K

The Figures below refer the 4LS15K pinout assignment.

Figure 136:
Connector 1 Pinout

Pin Number	Pin Name	Pin Number	Pin Name
1	BOTTOM_C_LVAL	2	BOTTOM_ALL_MCLK
3	FORCE_UPDATE_BOTTOM_L1	4	BOTTOM_C_N_CS
5	BOTTOM_C_LVDS_4_L2-	6	BOTTOM_C_LVDS_4_L2+
7	BOTTOM_ALL_N_RST_SPI	8	1.8V_Digital
9	BOTTOM_C_LVDS_3_L2-	10	BOTTOM_C_LVDS_3_L2+
11	BOTTOM_ALL_N_RST_LOGIC	12	1.8V_Digital
13	BOTTOM_C_LVDS_2_L2-	14	BOTTOM_C_LVDS_2_L2+
15	BOTTOM_ALL_N_RST_PLL	16	1.8V_Digital
17	BOTTOM_C_LVDS_1_L2-	18	BOTTOM_C_LVDS_1_L2+
19	VSS	20	VSS
21	BOTTOM_C_DATA_CLK-	22	BOTTOM_C_DATA_CLK+
23	1.8V_Digital	24	1.8V_Digital
25	BOTTOM_C_LVDS_4_L1-	26	BOTTOM_C_LVDS_4_L1+
27	VSS	28	VSS
29	BOTTOM_C_LVDS_3_L1-	30	BOTTOM_C_LVDS_3_L1+
31	1.8V_Digital	32	1.8V_Digital
33	BOTTOM_C_LVDS_2_L1-	34	BOTTOM_C_LVDS_2_L1+
35	VSS	36	VSS
37	BOTTOM_C_LVDS_1_L1-	38	BOTTOM_C_LVDS_1_L1+
39	VSS	40	BOTTOM_ALL(ABC)_MISO
41	BOTTOM_B_LVAL	42	BOTTOM_ALL_MOSI
43	BOTTOM_ALL_EXT_SYNC	44	BOTTOM_ALL_SCLK
45	1.8V_Digital	46	BOTTOM_B_N_CS
47	BOTTOM_B_LVDS_4_L2-	48	BOTTOM_B_LVDS_4_L2+
49	VSS	50	VSS
51	BOTTOM_B_LVDS_3_L2-	52	BOTTOM_B_LVDS_3_L2+
53	VSS	54	VSS
55	BOTTOM_B_LVDS_2_L2-	56	BOTTOM_B_LVDS_2_L2+
57	1.8V_Digital	58	1.8V_Digital

Pin Number	Pin Name	Pin Number	Pin Name
59	BOTTOM_B_LVDS_1_L2-	60	BOTTOM_B_LVDS_1_L2+
61	VSS	62	VSS
63	BOTTOM_B_DATA_CLK-	64	BOTTOM_B_DATA_CLK+
65	1.8V_Digital	66	1.8V_Digital
67	BOTTOM_B_LVDS_4_L1-	68	BOTTOM_B_LVDS_4_L1+
69	VSS	70	VSS
71	BOTTOM_B_LVDS_3_L1-	72	BOTTOM_B_LVDS_3_L1+
73	1.8V_Digital	74	1.8V_Digital
75	BOTTOM_B_LVDS_2_L1-	76	BOTTOM_B_LVDS_2_L1+
77	VSS	78	VSS
79	BOTTOM_B_LVDS_1_L1-	80	BOTTOM_B_LVDS_1_L1+
81	3.3V_ANALOGUE	82	3.3V_ANALOGUE
83	3.3V_ANALOGUE	84	3.3V_ANALOGUE
85	3.3V_ANALOGUE	86	3.3V_ANALOGUE
87	3.3V_ANALOGUE	88	BOTTOM_A_LVAL
89	3.3V_ANALOGUE	90	BOTTOM_A_N_CS
91	BOTTOM_A_LVDS_4_L2-	92	BOTTOM_A_LVDS_4_L2+
93	VSS	94	VSS
95	BOTTOM_A_LVDS_3_L2-	96	BOTTOM_A_LVDS_3_L2+
97	1.8V_Digital	98	1.8V_Digital
99	BOTTOM_A_LVDS_2_L2-	100	BOTTOM_A_LVDS_2_L2+
101	VSS	102	VSS
103	BOTTOM_A_LVDS_1_L2-	104	BOTTOM_A_LVDS_1_L2+
105	1.8V_Digital	106	1.8V_Digital
107	BOTTOM_A_DATA_CLK-	108	BOTTOM_A_DATA_CLK+
109	VSS	110	VSS
111	BOTTOM_A_LVDS_4_L1-	112	BOTTOM_A_LVDS_4_L1+
113	1.8V_Digital	114	1.8V_Digital
115	BOTTOM_A_LVDS_3_L1-	116	BOTTOM_A_LVDS_3_L1+
117	VSS	118	VSS
119	BOTTOM_A_LVDS_2_L1-	120	BOTTOM_A_LVDS_2_L1+
121	1.8V_Digital	122	1.8V_Digital
123	BOTTOM_A_LVDS_1_L1-	124	BOTTOM_A_LVDS_1_L1+
125	VSS	126	VSS
127	BOTTOM_ALL_SAMPLE_L2	128	BOTTOM_ALL_RST_CVC_L2
129	BOTTOM_ALL_SAMPLE_L1	130	BOTTOM_ALL_RST_CVC_L1
131	BOTTOM_ALL_RST_CDS_L2	132	BOTTOM_ALL_START_READOUT
133	BOTTOM_ALL_RST_CDS_L1	134	BOTTOM_ALL_START_AD_CONV
135	3.3V_ANALOGUE	136	Internal Use Only [1]

Pin Number	Pin Name	Pin Number	Pin Name
137	3.3V_ANALOGUE	138	Internal Use Only (1)
139	3.3V_ANALOGUE	140	Internal Use Only (1)

(1) Leave floating or connected to 1.8 V.

Figure 137:
Connector 2 Pinout

Pin Number	Pin Name	Pin Number	Pin Name
1	TOP_ALL_MCLK	2	TOP_C_LVAL
3	TOP_C_N_CS	4	FORCE_UPDATE_TOP_L1
5	TOP_C_LVDS_4_L2+	6	TOP_C_LVDS_4_L2-
7	1.8V_Digital	8	TOP_ALL_N_RST_PLL
9	TOP_C_LVDS_3_L2+	10	TOP_C_LVDS_3_L2-
11	1.8V_Digital	12	TOP_ALL_N_RST_SPI
13	TOP_C_LVDS_2_L2+	14	TOP_C_LVDS_2_L2-
15	1.8V_Digital	16	TOP_ALL_N_RST_LOGIC
17	TOP_C_LVDS_1_L2+	18	TOP_C_LVDS_1_L2-
19	VSS	20	VSS
21	TOP_C_DATA_CLK+	22	TOP_C_DATA_CLK-
23	1.8V_Digital	24	1.8V_Digital
25	TOP_C_LVDS_4_L1+	26	TOP_C_LVDS_4_L1-
27	VSS	28	VSS
29	TOP_C_LVDS_3_L1+	30	TOP_C_LVDS_3_L1-
31	1.8V_Digital	32	1.8V_Digital
33	TOP_C_LVDS_2_L1+	34	TOP_C_LVDS_2_L1-
35	VSS	36	VSS
37	TOP_C_LVDS_1_L1+	38	TOP_C_LVDS_1_L1-
39	TOP_ALL(ABC)_MISO	40	VSS
41	TOP_ALL_MOSI	42	TOP_B_LVAL
43	TOP_ALL_SCLK	44	TOP_ALL_EXT_SYNC
45	TOP_B_N_CS	46	1.8V_Digital
47	TOP_B_LVDS_4_L2+	48	TOP_B_LVDS_4_L2-
49	VSS	50	VSS
51	TOP_B_LVDS_3_L2+	52	TOP_B_LVDS_3_L2-
53	VSS	54	VSS
55	TOP_B_LVDS_2_L2+	56	TOP_B_LVDS_2_L2-
57	1.8V_Digital	58	1.8V_Digital
59	TOP_B_LVDS_1_L2+	60	TOP_B_LVDS_1_L2-
61	VSS	62	VSS

Pin Number	Pin Name	Pin Number	Pin Name
63	TOP_B_DATA_CLK+	64	TOP_B_DATA_CLK-
65	1.8V_Digital	66	1.8V_Digital
67	TOP_B_LVDS_4_L1+	68	TOP_B_LVDS_4_L1-
69	VSS	70	VSS
71	TOP_B_LVDS_3_L1+	72	TOP_B_LVDS_3_L1-
73	1.8V_Digital	74	1.8V_Digital
75	TOP_B_LVDS_2_L1+	76	TOP_B_LVDS_2_L1-
77	VSS	78	VSS
79	TOP_B_LVDS_1_L1+	80	TOP_B_LVDS_1_L1-
81	3.3V_ANALOGUE	82	3.3V_ANALOGUE
83	3.3V_ANALOGUE	84	3.3V_ANALOGUE
85	3.3V_ANALOGUE	86	3.3V_ANALOGUE
87	TOP_A_LVAL	88	3.3V_ANALOGUE
89	TOP_A_N_CS	90	3.3V_ANALOGUE
91	TOP_A_LVDS_4_L2+	92	TOP_A_LVDS_4_L2-
93	VSS	94	VSS
95	TOP_A_LVDS_3_L2+	96	TOP_A_LVDS_3_L2-
97	1.8V_Digital	98	1.8V_Digital
99	TOP_A_LVDS_2_L2+	100	TOP_A_LVDS_2_L2-
101	VSS	102	VSS
103	TOP_A_LVDS_1_L2+	104	TOP_A_LVDS_1_L2-
105	1.8V_Digital	106	1.8V_Digital
107	TOP_A_DATA_CLK+	108	TOP_A_DATA_CLK-
109	VSS	110	VSS
111	TOP_A_LVDS_4_L1+	112	TOP_A_LVDS_4_L1-
113	1.8V_Digital	114	1.8V_Digital
115	TOP_A_LVDS_3_L1+	116	TOP_A_LVDS_3_L1-
117	VSS	118	VSS
119	TOP_A_LVDS_2_L1+	120	TOP_A_LVDS_2_L1-
121	1.8V_Digital	122	1.8V_Digital
123	TOP_A_LVDS_1_L1+	124	TOP_A_LVDS_1_L1-
125	VSS	126	VSS
127	TOP_All_RST_CVC_L2	128	TOP_All_SAMPLE_L2
129	TOP_All_RST_CVC_L1	130	TOP_All_SAMPLE_L1
131	TOP_ALL_START_READOUT	132	TOP_All_RST_CDS_L2
133	TOP_ALL_START_AD_CONV	134	TOP_All_RST_CDS_L1
135	Internal Use Only (1)	136	3.3V_ANALOGUE
137	Internal Use Only (1)	138	3.3V_ANALOGUE
139	Internal Use Only (1)	140	3.3V_ANALOGUE

(1) Leave floating or connected to 1.8 V.

Figure 138:
Connector 3 Pinout(1)

Pin Number	Pin Name	Pin Number	Pin Name
1	FORCE_UPDATE_BOTTOM_L2	2	TDI(2)
3	TCK(3)	4	TDO(4)
5	Dig_IO	6	TMS(5)
7	Dig_IO	8	TRST(6)
9	BOTTOM_F_LVAL	10	BOTTOM_ALL(DEF)_MISO
11	3.3V_ANALOGUE	12	BOTTOM_F_N_CS
13	3.3V_ANALOGUE	14	3.3V_ANALOGUE
15	3.3V_ANALOGUE	16	3.3V_ANALOGUE
17	BOTTOM_F_LVDS_4_L2-	18	BOTTOM_F_LVDS_4_L2+
19	VSS	20	VSS
21	BOTTOM_F_LVDS_3_L2-	22	BOTTOM_F_LVDS_3_L2+
23	VSS	24	VSS
25	BOTTOM_F_LVDS_2_L2-	26	BOTTOM_F_LVDS_2_L2+
27	1.8V_Digital	28	1.8V_Digital
29	BOTTOM_F_LVDS_1_L2-	30	BOTTOM_F_LVDS_1_L2+
31	1.8V_Digital	32	1.8V_Digital
33	BOTTOM_F_DATA_CLK-	34	BOTTOM_F_DATA_CLK+
35	VSS	36	VSS
37	BOTTOM_F_LVDS_4_L1-	38	BOTTOM_F_LVDS_4_L1+
39	VSS	40	VSS
41	BOTTOM_F_LVDS_3_L1-	42	BOTTOM_F_LVDS_3_L1+
43	1.8V_Digital	44	1.8V_Digital
45	BOTTOM_F_LVDS_2_L1-	46	BOTTOM_F_LVDS_2_L1+
47	1.8V_Digital	48	1.8V_Digital
49	BOTTOM_F_LVDS_1_L1-	50	BOTTOM_F_LVDS_1_L1+
51	VSS	52	VSS
53	BOTTOM_E_LVAL	54	BOTTOM_E_N_CS
55	VSS	56	VSS
57	BOTTOM_E_LVDS_4_L2-	58	BOTTOM_E_LVDS_4_L2+
59	VSS	60	VSS
61	BOTTOM_E_LVDS_3_L2-	62	BOTTOM_E_LVDS_3_L2+
63	1.8V_Digital	64	1.8V_Digital
65	BOTTOM_E_LVDS_2_L2-	66	BOTTOM_E_LVDS_2_L2+
67	1.8V_Digital	68	1.8V_Digital
69	BOTTOM_E_LVDS_1_L2-	70	BOTTOM_E_LVDS_1_L2+
71	1.8V_Digital	72	1.8V_Digital
73	BOTTOM_E_DATA_CLK-	74	BOTTOM_E_DATA_CLK+

Pin Number	Pin Name	Pin Number	Pin Name
75	VSS	76	VSS
77	BOTTOM_E_LVDS_4_L1-	78	BOTTOM_E_LVDS_4_L1+
79	VSS	80	VSS
81	BOTTOM_E_LVDS_3_L1-	82	BOTTOM_E_LVDS_3_L1+
83	VSS	84	VSS
85	BOTTOM_E_LVDS_2_L1-	86	BOTTOM_E_LVDS_2_L1+
87	VSS	88	VSS
89	BOTTOM_E_LVDS_1_L1-	90	BOTTOM_E_LVDS_1_L1+
91	3.3V_ANALOGUE	92	3.3V_ANALOGUE
93	3.3V_ANALOGUE	94	3.3V_ANALOGUE
95	3.3V_ANALOGUE	96	BOTTOM_D_LVAL
97	3.3V_ANALOGUE	98	BOTTOM_D_N_CS
99	BOTTOM_D_LVDS_4_L2-	100	BOTTOM_D_LVDS_4_L2+
101	VSS	102	VSS
103	BOTTOM_D_LVDS_3_L2-	104	BOTTOM_D_LVDS_3_L2+
105	1.8V_Digital	106	1.8V_Digital
107	BOTTOM_D_LVDS_2_L2-	108	BOTTOM_D_LVDS_2_L2+
109	VSS	110	VSS
111	BOTTOM_D_LVDS_1_L2-	112	BOTTOM_D_LVDS_1_L2+
113	1.8V_Digital	114	1.8V_Digital
115	BOTTOM_D_DATA_CLK-	116	BOTTOM_D_DATA_CLK+
117	VSS	118	VSS
119	BOTTOM_D_LVDS_4_L1-	120	BOTTOM_D_LVDS_4_L1+
121	1.8V_Digital	122	1.8V_Digital
123	BOTTOM_D_LVDS_3_L1-	124	BOTTOM_D_LVDS_3_L1+
125	VSS	126	VSS
127	BOTTOM_D_LVDS_2_L1-	128	BOTTOM_D_LVDS_2_L1+
129	1.8V_Digital	130	1.8V_Digital
131	BOTTOM_D_LVDS_1_L1-	132	BOTTOM_D_LVDS_1_L1+
133	VSS	134	VSS (connected Dig_IO pin)
135	3.3V_ANALOGUE	136	Dig_IO
137	3.3V_ANALOGUE	138	Dig_IO
139	3.3V_ANALOGUE	140	Dig_IO

(1) Dig_IO → Not connected to the silicon. For FPGA debug test point purposes.
(2) Leave floating or connected to 1.8 V.
(3) Leave floating or connected to VSS.
(4) Leave floating.

Figure 139:
Connector 4 Pinout(1)

Pin Number	Pin Name	Pin Number	Pin Name
1	Dig_IO	2	FORCE_UPDATE_TOP_L2
3	Dig_IO	4	Dig_IO
5	Dig_IO	6	Dig_IO
7	Dig_IO	8	Dig_IO
9	TOP_ALL(DEF)_MISO	10	TOP_F_LVAL
11	TOP_F_N_CS	12	3.3V_ANALOGUE
13	3.3V_ANALOGUE	14	3.3V_ANALOGUE
15	3.3V_ANALOGUE	16	3.3V_ANALOGUE
17	TOP_F_LVDS_4_L2+	18	TOP_F_LVDS_4_L2-
19	VSS	20	VSS
21	TOP_F_LVDS_3_L2+	22	TOP_F_LVDS_3_L2-
23	VSS	24	VSS
25	TOP_F_LVDS_2_L2+	26	TOP_F_LVDS_2_L2-
27	1.8V_Digital	28	1.8V_Digital
29	TOP_F_LVDS_1_L2+	30	TOP_F_LVDS_1_L2-
31	1.8V_Digital	32	1.8V_Digital
33	TOP_F_DATA_CLK+	34	TOP_F_DATA_CLK-
35	VSS	36	VSS
37	TOP_F_LVDS_4_L1+	38	TOP_F_LVDS_4_L1-
39	VSS	40	VSS
41	TOP_F_LVDS_3_L1+	42	TOP_F_LVDS_3_L1-
43	1.8V_Digital	44	1.8V_Digital
45	TOP_F_LVDS_2_L1+	46	TOP_F_LVDS_2_L1-
47	1.8V_Digital	48	1.8V_Digital
49	TOP_F_LVDS_1_L1+	50	TOP_F_LVDS_1_L1-
51	VSS	52	VSS
53	TOP_E_N_CS	54	TOP_E_LVAL
55	VSS	56	VSS
57	TOP_E_LVDS_4_L2+	58	TOP_E_LVDS_4_L2-
59	VSS	60	VSS
61	TOP_E_LVDS_3_L2+	62	TOP_E_LVDS_3_L2-
63	1.8V_Digital	64	1.8V_Digital
65	TOP_E_LVDS_2_L2+	66	TOP_E_LVDS_2_L2-
67	1.8V_Digital	68	1.8V_Digital
69	TOP_E_LVDS_1_L2+	70	TOP_E_LVDS_1_L2-
71	1.8V_Digital	72	1.8V_Digital
73	TOP_E_DATA_CLK+	74	TOP_E_DATA_CLK-

Pin Number	Pin Name	Pin Number	Pin Name
75	VSS	76	VSS
77	TOP_E_LVDS_4_L1+	78	TOP_E_LVDS_4_L1-
79	VSS	80	VSS
81	TOP_E_LVDS_3_L1+	82	TOP_E_LVDS_3_L1-
83	VSS	84	VSS
85	TOP_E_LVDS_2_L1+	86	TOP_E_LVDS_2_L1-
87	VSS	88	VSS
89	TOP_E_LVDS_1_L1+	90	TOP_E_LVDS_1_L1-
91	3.3V_ANALOGUE	92	3.3V_ANALOGUE
93	3.3V_ANALOGUE	94	3.3V_ANALOGUE
95	TOP_D_LVAL	96	3.3V_ANALOGUE
97	TOP_D_N_CS	98	3.3V_ANALOGUE
99	TOP_D_LVDS_4_L2+	100	TOP_D_LVDS_4_L2-
101	VSS	102	VSS
103	TOP_D_LVDS_3_L2+	104	TOP_D_LVDS_3_L2-
105	1.8V_Digital	106	1.8V_Digital
107	TOP_D_LVDS_2_L2+	108	TOP_D_LVDS_2_L2-
109	VSS	110	VSS
111	TOP_D_LVDS_1_L2+	112	TOP_D_LVDS_1_L2-
113	1.8V_Digital	114	1.8V_Digital
115	TOP_D_DATA_CLK+	116	TOP_D_DATA_CLK-
117	VSS	118	VSS
119	TOP_D_LVDS_4_L1+	120	TOP_D_LVDS_4_L1-
121	1.8V_Digital	122	1.8V_Digital
123	TOP_D_LVDS_3_L1+	124	TOP_D_LVDS_3_L1-
125	VSS	126	VSS
127	TOP_D_LVDS_2_L1+	128	TOP_D_LVDS_2_L1-
129	1.8V_Digital	130	1.8V_Digital
131	TOP_D_LVDS_1_L1+	132	TOP_D_LVDS_1_L1-
133	VSS (connected Dig_IO pin)	134	VSS
135	Dig_IO	136	3.3V_ANALOGUE
137	Dig_IO	138	3.3V_ANALOGUE
139	Dig_IO	140	3.3V_ANALOGUE

(1) Dig_IO → Not connected to the silicon. For FPGA debug test point purposes.

10.2 Pinout Assignment for 4LS10K

Figure 140:
Connector 1 Pinout(1)

Pin Number	Pin Name	Pin Number	Pin Name
1	BOTTOM_C_LVAL	2	BOTTOM_ALL_MCLK
3	FORCE_UPDATE_BOTTOM_L1	4	BOTTOM_C_N_CS
5	BOTTOM_C_LVDS_4_L2-	6	BOTTOM_C_LVDS_4_L2+
7	BOTTOM_ALL_N_RST_SPI	8	1.8V_Digital
9	BOTTOM_C_LVDS_3_L2-	10	BOTTOM_C_LVDS_3_L2+
11	BOTTOM_ALL_N_RST_LOGIC	12	1.8V_Digital
13	BOTTOM_C_LVDS_2_L2-	14	BOTTOM_C_LVDS_2_L2+
15	BOTTOM_ALL_N_RST_PLL	16	1.8V_Digital
17	BOTTOM_C_LVDS_1_L2-	18	BOTTOM_C_LVDS_1_L2+
19	VSS	20	VSS
21	BOTTOM_C_DATA_CLK-	22	BOTTOM_C_DATA_CLK+
23	1.8V_Digital	24	1.8V_Digital
25	BOTTOM_C_LVDS_4_L1-	26	BOTTOM_C_LVDS_4_L1+
27	VSS	28	VSS
29	BOTTOM_C_LVDS_3_L1-	30	BOTTOM_C_LVDS_3_L1+
31	1.8V_Digital	32	1.8V_Digital
33	BOTTOM_C_LVDS_2_L1-	34	BOTTOM_C_LVDS_2_L1+
35	VSS	36	VSS
37	BOTTOM_C_LVDS_1_L1-	38	BOTTOM_C_LVDS_1_L1+
39	VSS	40	BOTTOM_ALL(ABC)_MISO
41	BOTTOM_B_LVAL	42	BOTTOM_ALL_MOSI
43	BOTTOM_ALL_EXT_SYNC	44	BOTTOM_ALL_SCLK
45	1.8V_Digital	46	BOTTOM_B_N_CS
47	BOTTOM_B_LVDS_4_L2-	48	BOTTOM_B_LVDS_4_L2+
49	VSS	50	VSS
51	BOTTOM_B_LVDS_3_L2-	52	BOTTOM_B_LVDS_3_L2+
53	VSS	54	VSS
55	BOTTOM_B_LVDS_2_L2-	56	BOTTOM_B_LVDS_2_L2+
57	1.8V_Digital	58	1.8V_Digital
59	BOTTOM_B_LVDS_1_L2-	60	BOTTOM_B_LVDS_1_L2+
61	VSS	62	VSS
63	BOTTOM_B_DATA_CLK-	64	BOTTOM_B_DATA_CLK+
65	1.8V_Digital	66	1.8V_Digital
67	BOTTOM_B_LVDS_4_L1-	68	BOTTOM_B_LVDS_4_L1+
69	VSS	70	VSS

Pin Number	Pin Name	Pin Number	Pin Name
71	BOTTOM_B_LVDS_3_L1-	72	BOTTOM_B_LVDS_3_L1+
73	1.8V_Digital	74	1.8V_Digital
75	BOTTOM_B_LVDS_2_L1-	76	BOTTOM_B_LVDS_2_L1+
77	VSS	78	VSS
79	BOTTOM_B_LVDS_1_L1-	80	BOTTOM_B_LVDS_1_L1+
81	3.3V_ANALOGUE	82	3.3V_ANALOGUE
83	3.3V_ANALOGUE	84	3.3V_ANALOGUE
85	3.3V_ANALOGUE	86	3.3V_ANALOGUE
87	3.3V_ANALOGUE	88	NC
89	3.3V_ANALOGUE	90	NC
91	NC	92	NC
93	VSS	94	VSS
95	NC	96	NC
97	1.8V_Digital	98	1.8V_Digital
99	NC	100	NC
101	VSS	102	VSS
103	NC	104	NC
105	1.8V_Digital	106	1.8V_Digital
107	NC	108	NC
109	VSS	110	VSS
111	NC	112	NC
113	1.8V_Digital	114	1.8V_Digital
115	NC	116	NC
117	VSS	118	VSS
119	NC	120	NC
121	1.8V_Digital	122	1.8V_Digital
123	NC	124	NC
125	VSS	126	VSS
127	BOTTOM_ALL_SAMPLE_L2	128	BOTTOM_All_RST_CVC_L2
129	BOTTOM_ALL_SAMPLE_L1	130	BOTTOM_All_RST_CVC_L1
131	BOTTOM_ALL_RST_CDS_L2	132	BOTTOM_ALL_START_READOUT
133	BOTTOM_ALL_RST_CDS_L1	134	BOTTOM_ALL_START_AD_CONV
135	3.3V_ANALOGUE	136	Internal Use Only (2)
137	3.3V_ANALOGUE	138	Internal Use Only (2)
139	3.3V_ANALOGUE	140	Internal Use Only (2)

(1) NC → Not connected.
(2) Leave floating or connected to 1.8 V.

Figure 141:
Connector 2 Pinout(1)

Pin Number	Pin Name	Pin Number	Pin Name
1	TOP_ALL_MCLK	2	TOP_C_LVAL
3	TOP_C_N_CS	4	FORCE_UPDATE_TOP_L1
5	TOP_C_LVDS_4_L2+	6	TOP_C_LVDS_4_L2-
7	1.8V_Digital	8	TOP_ALL_N_RST_PLL
9	TOP_C_LVDS_3_L2+	10	TOP_C_LVDS_3_L2-
11	1.8V_Digital	12	TOP_ALL_N_RST_SPI
13	TOP_C_LVDS_2_L2+	14	TOP_C_LVDS_2_L2-
15	1.8V_Digital	16	TOP_ALL_N_RST_LOGIC
17	TOP_C_LVDS_1_L2+	18	TOP_C_LVDS_1_L2-
19	VSS	20	VSS
21	TOP_C_DATA_CLK+	22	TOP_C_DATA_CLK-
23	1.8V_Digital	24	1.8V_Digital
25	TOP_C_LVDS_4_L1+	26	TOP_C_LVDS_4_L1-
27	VSS	28	VSS
29	TOP_C_LVDS_3_L1+	30	TOP_C_LVDS_3_L1-
31	1.8V_Digital	32	1.8V_Digital
33	TOP_C_LVDS_2_L1+	34	TOP_C_LVDS_2_L1-
35	VSS	36	VSS
37	TOP_C_LVDS_1_L1+	38	TOP_C_LVDS_1_L1-
39	TOP_ALL(ABC)_MISO	40	VSS
41	TOP_ALL_MOSI	42	TOP_B_LVAL
43	TOP_ALL_SCLK	44	TOP_ALL_EXT_SYNC
45	TOP_B_N_CS	46	1.8V_Digital
47	TOP_B_LVDS_4_L2+	48	TOP_B_LVDS_4_L2-
49	VSS	50	VSS
51	TOP_B_LVDS_3_L2+	52	TOP_B_LVDS_3_L2-
53	VSS	54	VSS
55	TOP_B_LVDS_2_L2+	56	TOP_B_LVDS_2_L2-
57	1.8V_Digital	58	1.8V_Digital
59	TOP_B_LVDS_1_L2+	60	TOP_B_LVDS_1_L2-
61	VSS	62	VSS
63	TOP_B_DATA_CLK+	64	TOP_B_DATA_CLK-
65	1.8V_Digital	66	1.8V_Digital
67	TOP_B_LVDS_4_L1+	68	TOP_B_LVDS_4_L1-
69	VSS	70	VSS
71	TOP_B_LVDS_3_L1+	72	TOP_B_LVDS_3_L1-
73	1.8V_Digital	74	1.8V_Digital

Pin Number	Pin Name	Pin Number	Pin Name
75	TOP_B_LVDS_2_L1+	76	TOP_B_LVDS_2_L1-
77	VSS	78	VSS
79	TOP_B_LVDS_1_L1+	80	TOP_B_LVDS_1_L1-
81	3.3V_ANALOGUE	82	3.3V_ANALOGUE
83	3.3V_ANALOGUE	84	3.3V_ANALOGUE
85	3.3V_ANALOGUE	86	3.3V_ANALOGUE
87	NC	88	3.3V_ANALOGUE
89	NC	90	3.3V_ANALOGUE
91	NC	92	NC
93	VSS	94	VSS
95	NC	96	NC
97	1.8V_Digital	98	1.8V_Digital
99	NC	100	NC
101	VSS	102	VSS
103	NC	104	NC
105	1.8V_Digital	106	1.8V_Digital
107	NC	108	NC
109	VSS	110	VSS
111	NC	112	NC
113	1.8V_Digital	114	1.8V_Digital
115	NC	116	NC
117	VSS	118	VSS
119	NC	120	NC
121	1.8V_Digital	122	1.8V_Digital
123	NC	124	NC
125	VSS	126	VSS
127	TOP_ALL_RST_CVC_L2	128	TOP_ALL_SAMPLE_L2
129	TOP_ALL_RST_CVC_L1	130	TOP_ALL_SAMPLE_L1
131	TOP_ALL_START_READOUT	132	TOP_ALL_RST_CDS_L2
133	TOP_ALL_START_AD_CONV	134	TOP_ALL_RST_CDS_L1
135	Internal Use Only (2)	136	3.3V_ANALOGUE
137	Internal Use Only (2)	138	3.3V_ANALOGUE
139	Internal Use Only (2)	140	3.3V_ANALOGUE

(1) NC → Not connected.
(2) Leave floating or connected to 1.8 V.

Figure 142:
Connector 3 Pinout(1)(2)

Pin Number	Pin Name	Pin Number	Pin Name
1	FORCE_UPDATE_BOTTOM_L2	2	TDI(3)
3	TCK(4)	4	TDO(5)
5	Dig_IO	6	TMS(6)
7	Dig_IO	8	TRST(7)
9	NC	10	BOTTOM_ALL(DEF)_MISO
11	3.3V_ANALOGUE	12	NC
13	3.3V_ANALOGUE	14	3.3V_ANALOGUE
15	3.3V_ANALOGUE	16	3.3V_ANALOGUE
17	NC	18	NC
19	VSS	20	VSS
21	NC	22	NC
23	VSS	24	VSS
25	NC	26	NC
27	1.8V_Digital	28	1.8V_Digital
29	NC	30	NC
31	1.8V_Digital	32	1.8V_Digital
33	NC	34	NC
35	VSS	36	VSS
37	NC	38	NC
39	VSS	40	VSS
41	NC	42	NC
43	1.8V_Digital	44	1.8V_Digital
45	NC	46	NC
47	1.8V_Digital	48	1.8V_Digital
49	NC	50	NC
51	VSS	52	VSS
53	BOTTOM_E_LVAL	54	BOTTOM_E_N_CS
55	VSS	56	VSS
57	BOTTOM_E_LVDS_4_L2-	58	BOTTOM_E_LVDS_4_L2+
59	VSS	60	VSS
61	BOTTOM_E_LVDS_3_L2-	62	BOTTOM_E_LVDS_3_L2+
63	1.8V_Digital	64	1.8V_Digital
65	BOTTOM_E_LVDS_2_L2-	66	BOTTOM_E_LVDS_2_L2+
67	1.8V_Digital	68	1.8V_Digital
69	BOTTOM_E_LVDS_1_L2-	70	BOTTOM_E_LVDS_1_L2+
71	1.8V_Digital	72	1.8V_Digital
73	BOTTOM_E_DATA_CLK-	74	BOTTOM_E_DATA_CLK+

Pin Number	Pin Name	Pin Number	Pin Name
75	VSS	76	VSS
77	BOTTOM_E_LVDS_4_L1-	78	BOTTOM_E_LVDS_4_L1+
79	VSS	80	VSS
81	BOTTOM_E_LVDS_3_L1-	82	BOTTOM_E_LVDS_3_L1+
83	VSS	84	VSS
85	BOTTOM_E_LVDS_2_L1-	86	BOTTOM_E_LVDS_2_L1+
87	VSS	88	VSS
89	BOTTOM_E_LVDS_1_L1-	90	BOTTOM_E_LVDS_1_L1+
91	3.3V_ANALOGUE	92	3.3V_ANALOGUE
93	3.3V_ANALOGUE	94	3.3V_ANALOGUE
95	3.3V_ANALOGUE	96	BOTTOM_D_LVAL
97	3.3V_ANALOGUE	98	BOTTOM_D_N_CS
99	BOTTOM_D_LVDS_4_L2-	100	BOTTOM_D_LVDS_4_L2+
101	VSS	102	VSS
103	BOTTOM_D_LVDS_3_L2-	104	BOTTOM_D_LVDS_3_L2+
105	1.8V_Digital	106	1.8V_Digital
107	BOTTOM_D_LVDS_2_L2-	108	BOTTOM_D_LVDS_2_L2+
109	VSS	110	VSS
111	BOTTOM_D_LVDS_1_L2-	112	BOTTOM_D_LVDS_1_L2+
113	1.8V_Digital	114	1.8V_Digital
115	BOTTOM_D_DATA_CLK-	116	BOTTOM_D_DATA_CLK+
117	VSS	118	VSS
119	BOTTOM_D_LVDS_4_L1-	120	BOTTOM_D_LVDS_4_L1+
121	1.8V_Digital	122	1.8V_Digital
123	BOTTOM_D_LVDS_3_L1-	124	BOTTOM_D_LVDS_3_L1+
125	VSS	126	VSS
127	BOTTOM_D_LVDS_2_L1-	128	BOTTOM_D_LVDS_2_L1+
129	1.8V_Digital	130	1.8V_Digital
131	BOTTOM_D_LVDS_1_L1-	132	BOTTOM_D_LVDS_1_L1+
133	VSS	134	VSS (connected Dig_IO pin)
135	3.3V_ANALOGUE	136	Dig_IO
137	3.3V_ANALOGUE	138	Dig_IO
139	3.3V_ANALOGUE	140	Dig_IO

(1) Dig_IO → Not connected to the silicon. For FPGA debug test point purposes.
(2) NC → Not connected.
(3) Leave floating or connected to 1.8 V.
(4) Leave floating or connected to VSS.
(5) Leave floating.

Figure 143:
Connector 4 Pinout(1)(2)

Pin Number	Pin Name	Pin Number	Pin Name
1	Dig_IO	2	FORCE_UPDATE_TOP_L2
3	Dig_IO	4	Dig_IO
5	Dig_IO	6	Dig_IO
7	Dig_IO	8	Dig_IO
9	TOP_ALL(DEF)_MISO	10	NC
11	NC	12	3.3V_ANALOGUE
13	3.3V_ANALOGUE	14	3.3V_ANALOGUE
15	3.3V_ANALOGUE	16	3.3V_ANALOGUE
17	NC	18	NC
19	VSS	20	VSS
21	NC	22	NC
23	VSS	24	VSS
25	NC	26	NC
27	1.8V_Digital	28	1.8V_Digital
29	NC	30	NC
31	1.8V_Digital	32	1.8V_Digital
33	NC	34	NC
35	VSS	36	VSS
37	NC	38	NC
39	VSS	40	VSS
41	NC	42	NC
43	1.8V_Digital	44	1.8V_Digital
45	NC	46	NC
47	1.8V_Digital	48	1.8V_Digital
49	NC	50	NC
51	VSS	52	VSS
53	TOP_E_N_CS	54	TOP_E_LVAL
55	VSS	56	VSS
57	TOP_E_LVDS_4_L2+	58	TOP_E_LVDS_4_L2-
59	VSS	60	VSS
61	TOP_E_LVDS_3_L2+	62	TOP_E_LVDS_3_L2-
63	1.8V_Digital	64	1.8V_Digital
65	TOP_E_LVDS_2_L2+	66	TOP_E_LVDS_2_L2-
67	1.8V_Digital	68	1.8V_Digital
69	TOP_E_LVDS_1_L2+	70	TOP_E_LVDS_1_L2-
71	1.8V_Digital	72	1.8V_Digital
73	TOP_E_DATA_CLK+	74	TOP_E_DATA_CLK-

Pin Number	Pin Name	Pin Number	Pin Name
75	VSS	76	VSS
77	TOP_E_LVDS_4_L1+	78	TOP_E_LVDS_4_L1-
79	VSS	80	VSS
81	TOP_E_LVDS_3_L1+	82	TOP_E_LVDS_3_L1-
83	VSS	84	VSS
85	TOP_E_LVDS_2_L1+	86	TOP_E_LVDS_2_L1-
87	VSS	88	VSS
89	TOP_E_LVDS_1_L1+	90	TOP_E_LVDS_1_L1-
91	3.3V_ANALOGUE	92	3.3V_ANALOGUE
93	3.3V_ANALOGUE	94	3.3V_ANALOGUE
95	TOP_D_LVAL	96	3.3V_ANALOGUE
97	TOP_D_N_CS	98	3.3V_ANALOGUE
99	TOP_D_LVDS_4_L2+	100	TOP_D_LVDS_4_L2-
101	VSS	102	VSS
103	TOP_D_LVDS_3_L2+	104	TOP_D_LVDS_3_L2-
105	1.8V_Digital	106	1.8V_Digital
107	TOP_D_LVDS_2_L2+	108	TOP_D_LVDS_2_L2-
109	VSS	110	VSS
111	TOP_D_LVDS_1_L2+	112	TOP_D_LVDS_1_L2-
113	1.8V_Digital	114	1.8V_Digital
115	TOP_D_DATA_CLK+	116	TOP_D_DATA_CLK-
117	VSS	118	VSS
119	TOP_D_LVDS_4_L1+	120	TOP_D_LVDS_4_L1-
121	1.8V_Digital	122	1.8V_Digital
123	TOP_D_LVDS_3_L1+	124	TOP_D_LVDS_3_L1-
125	VSS	126	VSS
127	TOP_D_LVDS_2_L1+	128	TOP_D_LVDS_2_L1-
129	1.8V_Digital	130	1.8V_Digital
131	TOP_D_LVDS_1_L1+	132	TOP_D_LVDS_1_L1-
133	VSS (connected Dig_IO pin)	134	VSS
135	Dig_IO	136	3.3V_ANALOGUE
137	Dig_IO	138	3.3V_ANALOGUE
139	Dig_IO	140	3.3V_ANALOGUE

(1) Dig_IO → Not connected to the silicon. For FPGA debug test point purposes.
(2) NC → Not connected.

10.3 Pinout Assignment for 4LS5K

Figure 144:
Connector 1 Pinout(1)

Pin Number	Pin Name	Pin Number	Pin Name
1	BOTTOM_A_TEST_OUT	2	BOTTOM_ALL_MCLK
3	FORCE_UPDATE_BOTTOM_L1	4	BOTTOM_B_TEST_OUT
5	NC	6	NC
7	BOTTOM_ALL_N_RST_SPI	8	1.8V_Digital
9	NC	10	NC
11	BOTTOM_ALL_N_RST_LOGIC	12	1.8V_Digital
13	NC	14	NC
15	BOTTOM_ALL_N_RST_PLL	16	1.8V_Digital
17	NC	18	NC
19	VSS	20	VSS
21	NC	22	NC
23	1.8V_Digital	24	1.8V_Digital
25	NC	26	NC
27	VSS	28	VSS
29	NC	30	NC
31	1.8V_Digital	32	1.8V_Digital
33	NC	34	NC
35	VSS	36	VSS
37	NC	38	NC
39	VSS	40	BOTTOM_ALL(ABC)_MISO
41	BOTTOM_B_LVAL	42	BOTTOM_ ALL _MOSI
43	BOTTOM_ ALL _EXT_SYNC	44	BOTTOM_ ALL _SCLK
45	1.8V_Digital	46	BOTTOM_B_N_CS
47	BOTTOM_B_LVDS_4_L2-	48	BOTTOM_B_LVDS_4_L2+
49	VSS	50	VSS
51	BOTTOM_B_LVDS_3_L2-	52	BOTTOM_B_LVDS_3_L2+
53	VSS	54	VSS
55	BOTTOM_B_LVDS_2_L2-	56	BOTTOM_B_LVDS_2_L2+
57	1.8V_Digital	58	1.8V_Digital
59	BOTTOM_B_LVDS_1_L2-	60	BOTTOM_B_LVDS_1_L2+
61	VSS	62	VSS
63	BOTTOM_B_DATA_CLK-	64	BOTTOM_B_DATA_CLK+
65	1.8V_Digital	66	1.8V_Digital
67	BOTTOM_B_LVDS_4_L1-	68	BOTTOM_B_LVDS_4_L1+
69	VSS	70	VSS

Pin Number	Pin Name	Pin Number	Pin Name
71	BOTTOM_B_LVDS_3_L1-	72	BOTTOM_B_LVDS_3_L1+
73	1.8V_Digital	74	1.8V_Digital
75	BOTTOM_B_LVDS_2_L1-	76	BOTTOM_B_LVDS_2_L1+
77	VSS	78	VSS
79	BOTTOM_B_LVDS_1_L1-	80	BOTTOM_B_LVDS_1_L1+
81	3.3V_ANALOGUE	82	3.3V_ANALOGUE
83	3.3V_ANALOGUE	84	3.3V_ANALOGUE
85	3.3V_ANALOGUE	86	3.3V_ANALOGUE
87	3.3V_ANALOGUE	88	BOTTOM_A_LVAL
89	3.3V_ANALOGUE	90	BOTTOM_A_N_CS
91	BOTTOM_A_LVDS_4_L2-	92	BOTTOM_A_LVDS_4_L2+
93	VSS	94	VSS
95	BOTTOM_A_LVDS_3_L2-	96	BOTTOM_A_LVDS_3_L2+
97	1.8V_Digital	98	1.8V_Digital
99	BOTTOM_A_LVDS_2_L2-	100	BOTTOM_A_LVDS_2_L2+
101	VSS	102	VSS
103	BOTTOM_A_LVDS_1_L2-	104	BOTTOM_A_LVDS_1_L2+
105	1.8V_Digital	106	1.8V_Digital
107	BOTTOM_A_DATA_CLK-	108	BOTTOM_A_DATA_CLK+
109	VSS	110	VSS
111	BOTTOM_A_LVDS_4_L1-	112	BOTTOM_A_LVDS_4_L1+
113	1.8V_Digital	114	1.8V_Digital
115	BOTTOM_A_LVDS_3_L1-	116	BOTTOM_A_LVDS_3_L1+
117	VSS	118	VSS
119	BOTTOM_A_LVDS_2_L1-	120	BOTTOM_A_LVDS_2_L1+
121	1.8V_Digital	122	1.8V_Digital
123	BOTTOM_A_LVDS_1_L1-	124	BOTTOM_A_LVDS_1_L1+
125	VSS	126	VSS
127	BOTTOM_ ALL _SAMPLE_L2	128	BOTTOM_All_RST_CVC_L2
129	BOTTOM_ ALL _SAMPLE_L1	130	BOTTOM_All_RST_CVC_L1
131	BOTTOM_ ALL _RST_CDS_L2	132	BOTTOM_ ALL _START_READOUT
133	BOTTOM_ ALL _RST_CDS_L1	134	BOTTOM_ ALL _START_AD_CONV
135	3.3V_ANALOGUE	136	Internal Use Only (2)
137	3.3V_ANALOGUE	138	Internal Use Only (2)
139	3.3V_ANALOGUE	140	Internal Use Only (2)

(1) NC → Not connected.
(2) Leave floating or connected to 1.8 V.

Figure 145:
Connector 2 Pinout(1)

Pin Number	Pin Name	Pin Number	Pin Name
1	TOP_ ALL _MCLK	2	TOP_A_TEST_OUT
3	TOP_B_TEST_OUT	4	FORCE_UPDATE_TOP_L1
5	NC	6	NC
7	1.8V_Digital	8	TOP_ ALL _N_RST_PLL
9	NC	10	NC
11	1.8V_Digital	12	TOP_ ALL _N_RST_SPI
13	NC	14	NC
15	1.8V_Digital	16	TOP_ ALL _N_RST_LOGIC
17	NC	18	NC
19	VSS	20	VSS
21	NC	22	NC
23	1.8V_Digital	24	1.8V_Digital
25	NC	26	NC
27	VSS	28	VSS
29	NC	30	NC
31	1.8V_Digital	32	1.8V_Digital
33	NC	34	NC
35	VSS	36	VSS
37	NC	38	NC
39	TOP_ALL(ABC)_MISO	40	VSS
41	TOP_ALL_MOSI	42	TOP_B_LVAL
43	TOP_ALL_SCLK	44	TOP_ ALL _EXT_SYNC
45	TOP_B_N_CS	46	1.8V_Digital
47	TOP_B_LVDS_4_L2+	48	TOP_B_LVDS_4_L2-
49	VSS	50	VSS
51	TOP_B_LVDS_3_L2+	52	TOP_B_LVDS_3_L2-
53	VSS	54	VSS
55	TOP_B_LVDS_2_L2+	56	TOP_B_LVDS_2_L2-
57	1.8V_Digital	58	1.8V_Digital
59	TOP_B_LVDS_1_L2+	60	TOP_B_LVDS_1_L2-
61	VSS	62	VSS
63	TOP_B_DATA_CLK+	64	TOP_B_DATA_CLK-
65	1.8V_Digital	66	1.8V_Digital
67	TOP_B_LVDS_4_L1+	68	TOP_B_LVDS_4_L1-
69	VSS	70	VSS
71	TOP_B_LVDS_3_L1+	72	TOP_B_LVDS_3_L1-
73	1.8V_Digital	74	1.8V_Digital

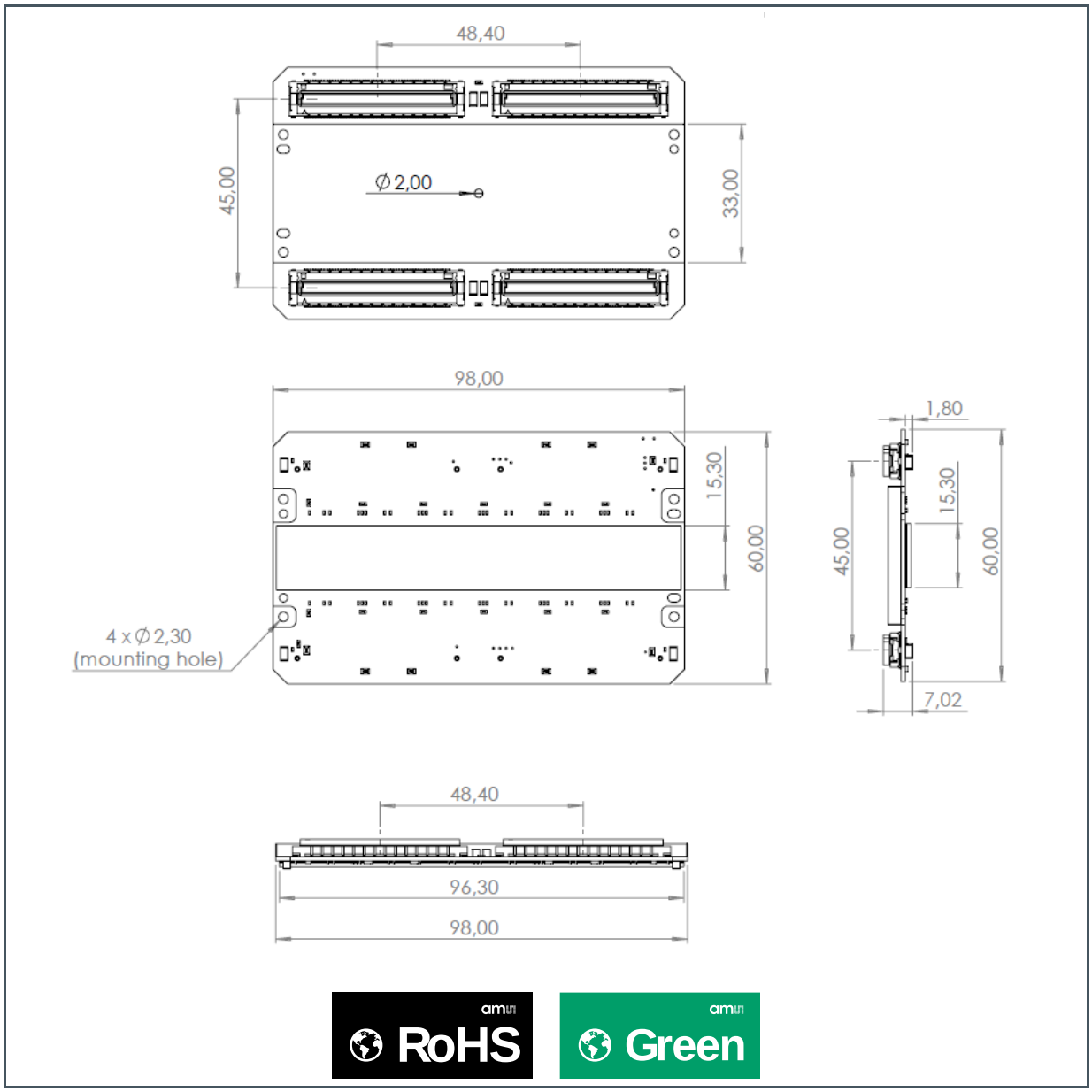
Pin Number	Pin Name	Pin Number	Pin Name
75	TOP_B_LVDS_2_L1+	76	TOP_B_LVDS_2_L1-
77	VSS	78	VSS
79	TOP_B_LVDS_1_L1+	80	TOP_B_LVDS_1_L1-
81	3.3V_ANALOGUE	82	3.3V_ANALOGUE
83	3.3V_ANALOGUE	84	3.3V_ANALOGUE
85	3.3V_ANALOGUE	86	3.3V_ANALOGUE
87	TOP_A_LVAL	88	3.3V_ANALOGUE
89	TOP_A_N_CS	90	3.3V_ANALOGUE
91	TOP_A_LVDS_4_L2+	92	TOP_A_LVDS_4_L2-
93	VSS	94	VSS
95	TOP_A_LVDS_3_L2+	96	TOP_A_LVDS_3_L2-
97	1.8V_Digital	98	1.8V_Digital
99	TOP_A_LVDS_2_L2+	100	TOP_A_LVDS_2_L2-
101	VSS	102	VSS
103	TOP_A_LVDS_1_L2+	104	TOP_A_LVDS_1_L2-
105	1.8V_Digital	106	1.8V_Digital
107	TOP_A_DATA_CLK+	108	TOP_A_DATA_CLK-
109	VSS	110	VSS
111	TOP_A_LVDS_4_L1+	112	TOP_A_LVDS_4_L1-
113	1.8V_Digital	114	1.8V_Digital
115	TOP_A_LVDS_3_L1+	116	TOP_A_LVDS_3_L1-
117	VSS	118	VSS
119	TOP_A_LVDS_2_L1+	120	TOP_A_LVDS_2_L1-
121	1.8V_Digital	122	1.8V_Digital
123	TOP_A_LVDS_1_L1+	124	TOP_A_LVDS_1_L1-
125	VSS	126	VSS
127	TOP_ ALL _RST_CVC_L2	128	TOP_ ALL _SAMPLE_L2
129	TOP_ ALL _RST_CVC_L1	130	TOP_ ALL _SAMPLE_L1
131	TOP_ ALL _START_READOUT	132	TOP_ ALL _RST_CDS_L2
133	TOP_ ALL _START_AD_CONV	134	TOP_ ALL _RST_CDS_L1
135	Internal Use Only (1)	136	3.3V_ANALOGUE
137	Internal Use Only (1)	138	3.3V_ANALOGUE
139	Internal Use Only (1)	140	3.3V_ANALOGUE

(1) NC → Not connected.
(2) Leave floating or connected to 1.8 V.

11 Package Drawings & Markings

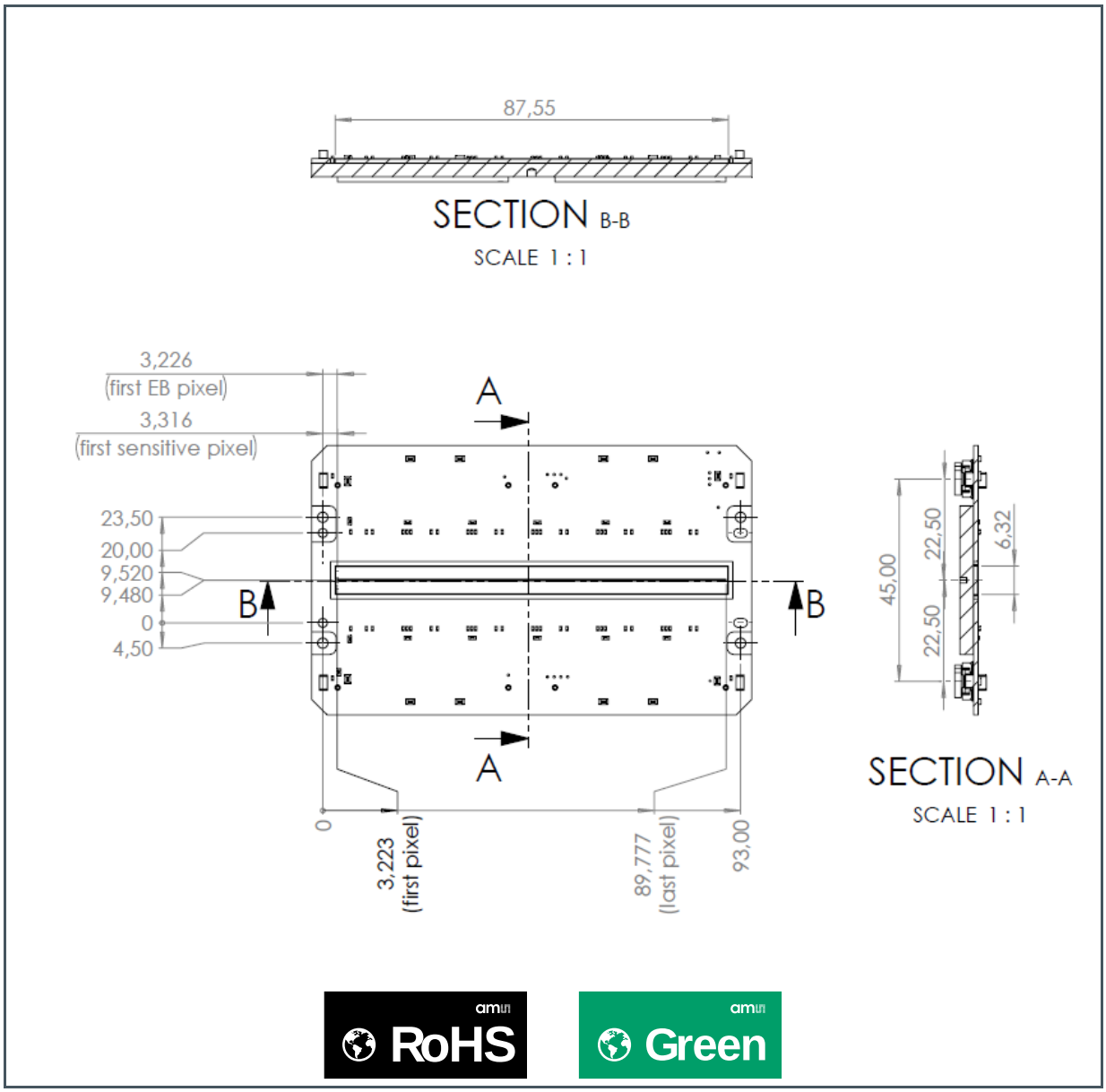
11.1 4LS15K Mechanical Drawing

Figure 146:
4LS15K Invar Package Outline Drawing – General Overview (1)(2)(3)(4)



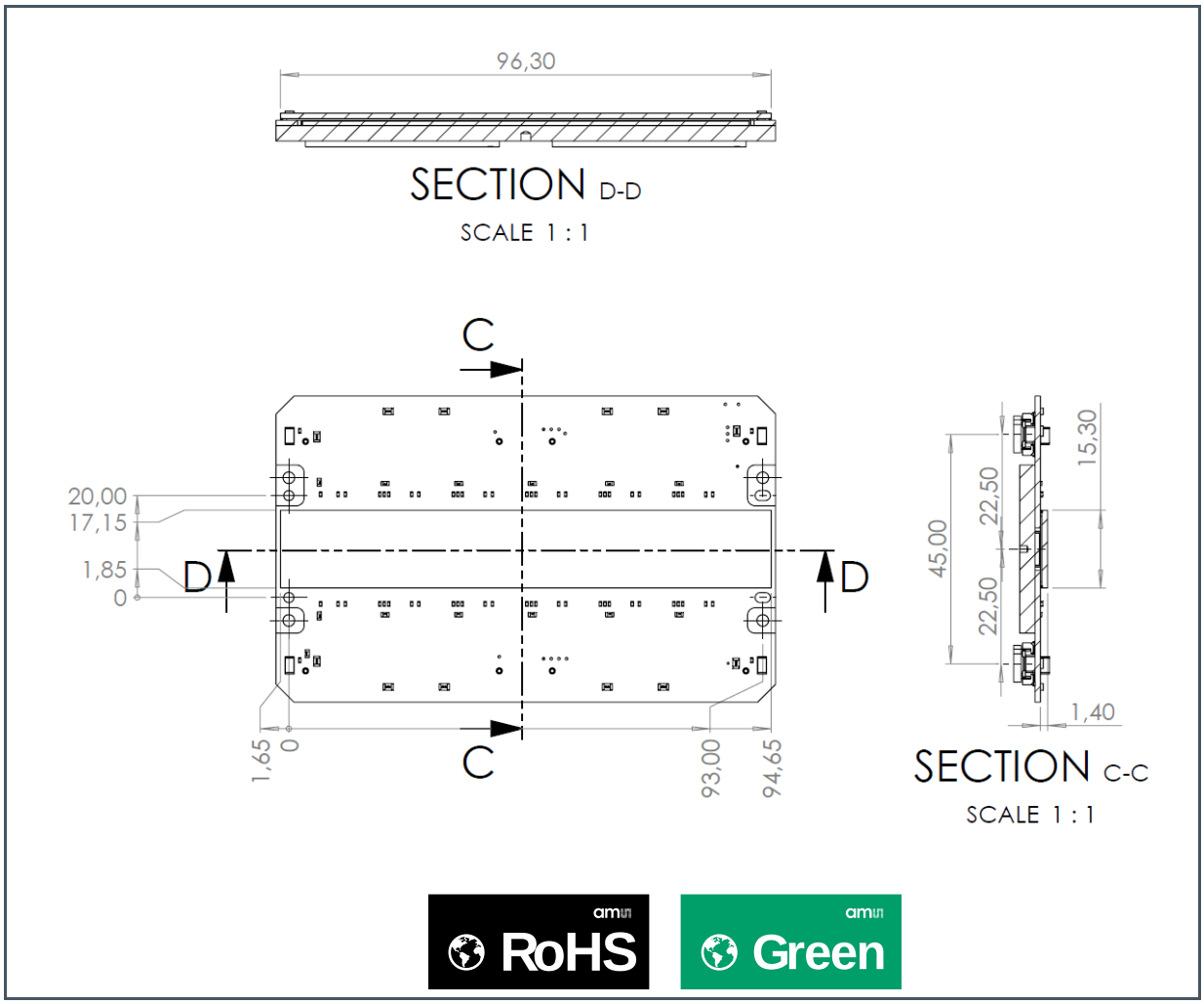
(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are ±0.1 mm.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

Figure 147:
4LS15K Invar Package Outline Drawing – Section A-A and Section B-B(1)(2)(3)(4)



(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are ±0.1 mm.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

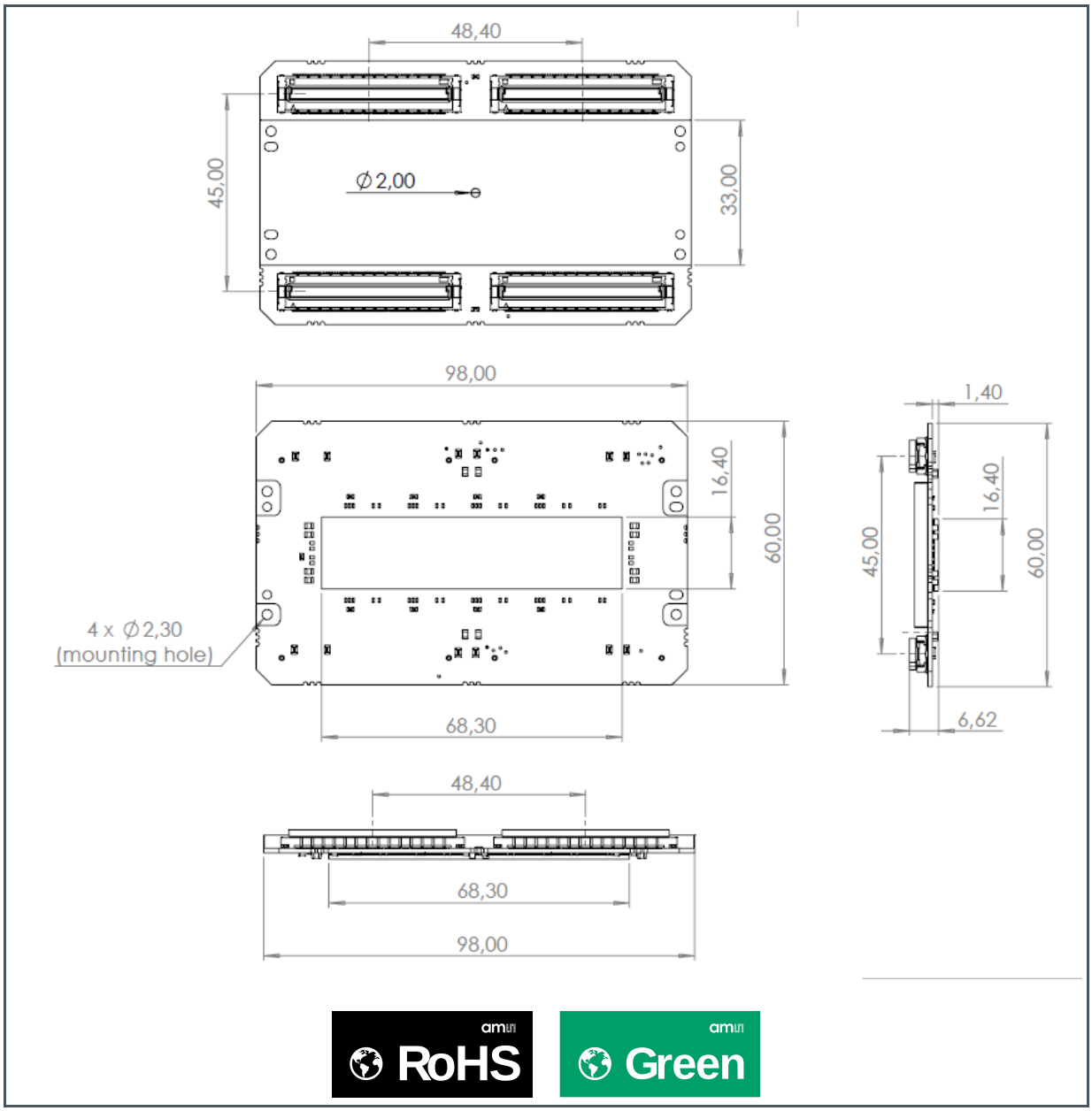
Figure 148:
4LS15K- Invar Package Outline Drawing – Section C-C and Section D-D(1)(2)(3)(4)



(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are ±0.1 mm.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

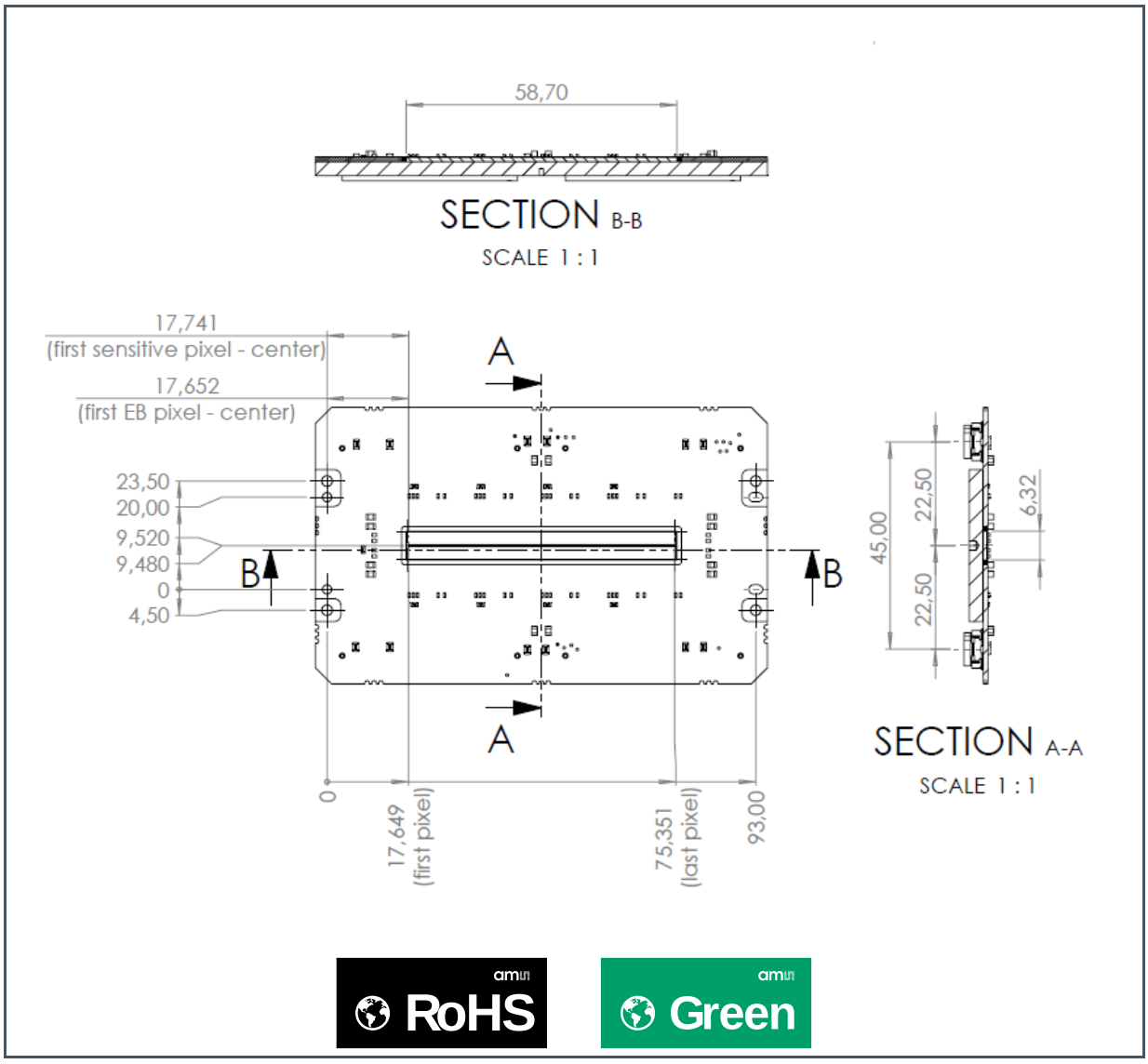
11.2 4LS10K Mechanical Drawing

Figure 149:
4LS10K Invar Package Outline Drawing – General Overview (1)(2)(3)(4)



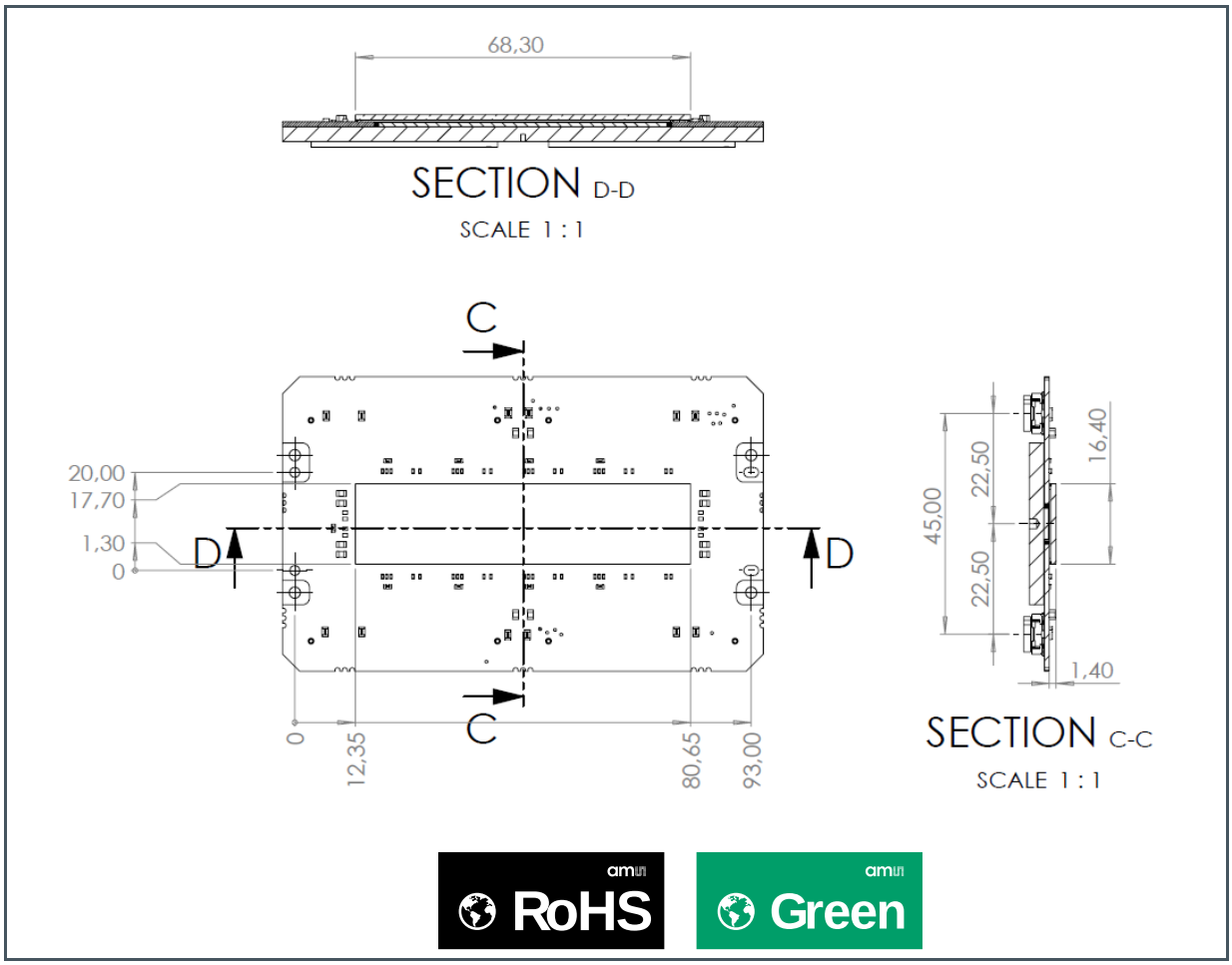
(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are ±0.1 mm.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

Figure 150:
4LS10K Invar Package Outline Drawing – Section A-A and Section B-B(1)(2)(3)(4)



(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are ±0.1 mm.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

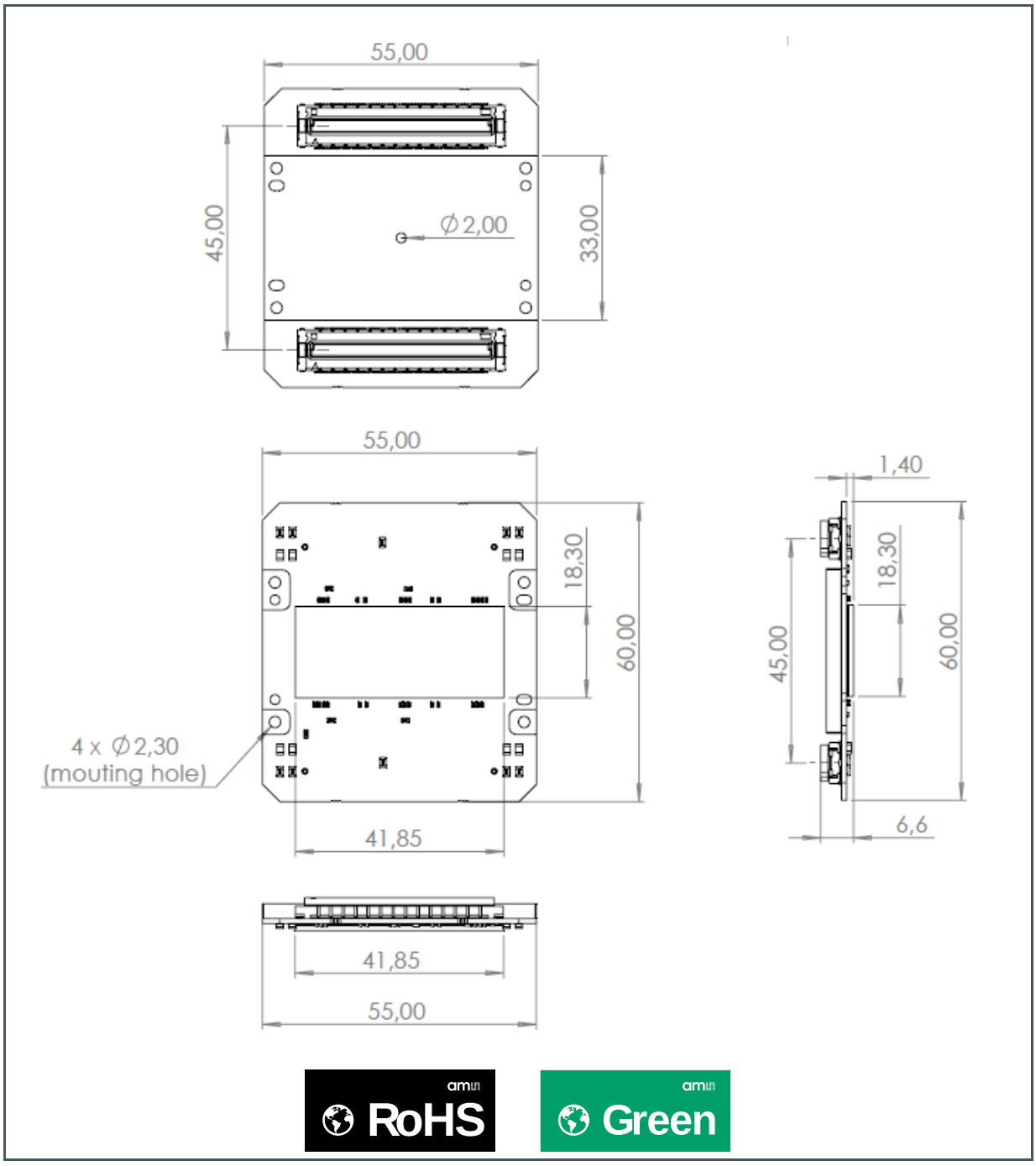
Figure 151:
4LS10K Invar Package Outline Drawing – Section C-C and Section D-D(1)(2)(3)(4)



(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are ±0.1 mm.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

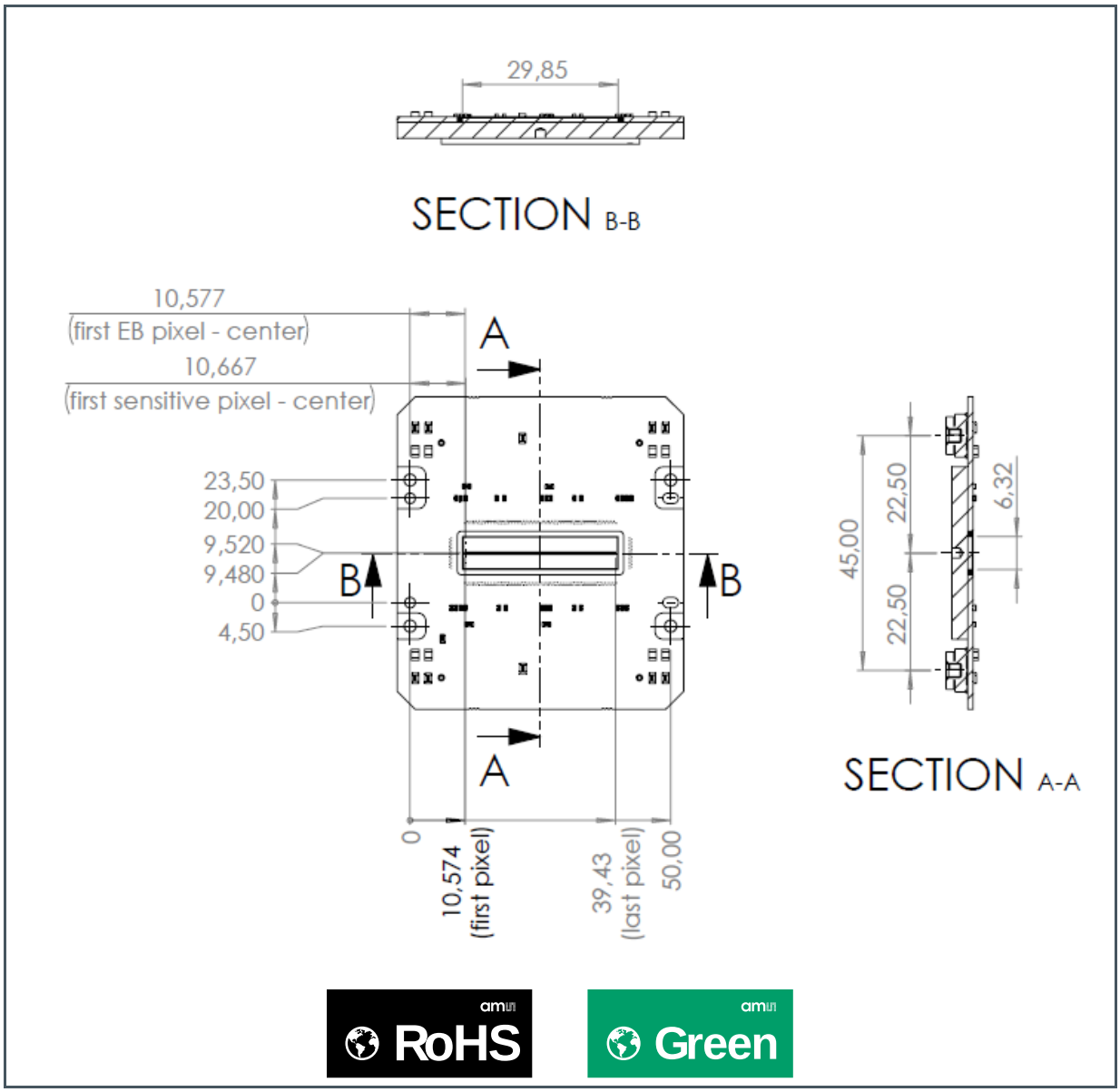
11.3 4LS5K Mechanical Drawing

Figure 152:
4LS5K Invar Package Outline Drawing – General Overview (1)(2)(3)(4)



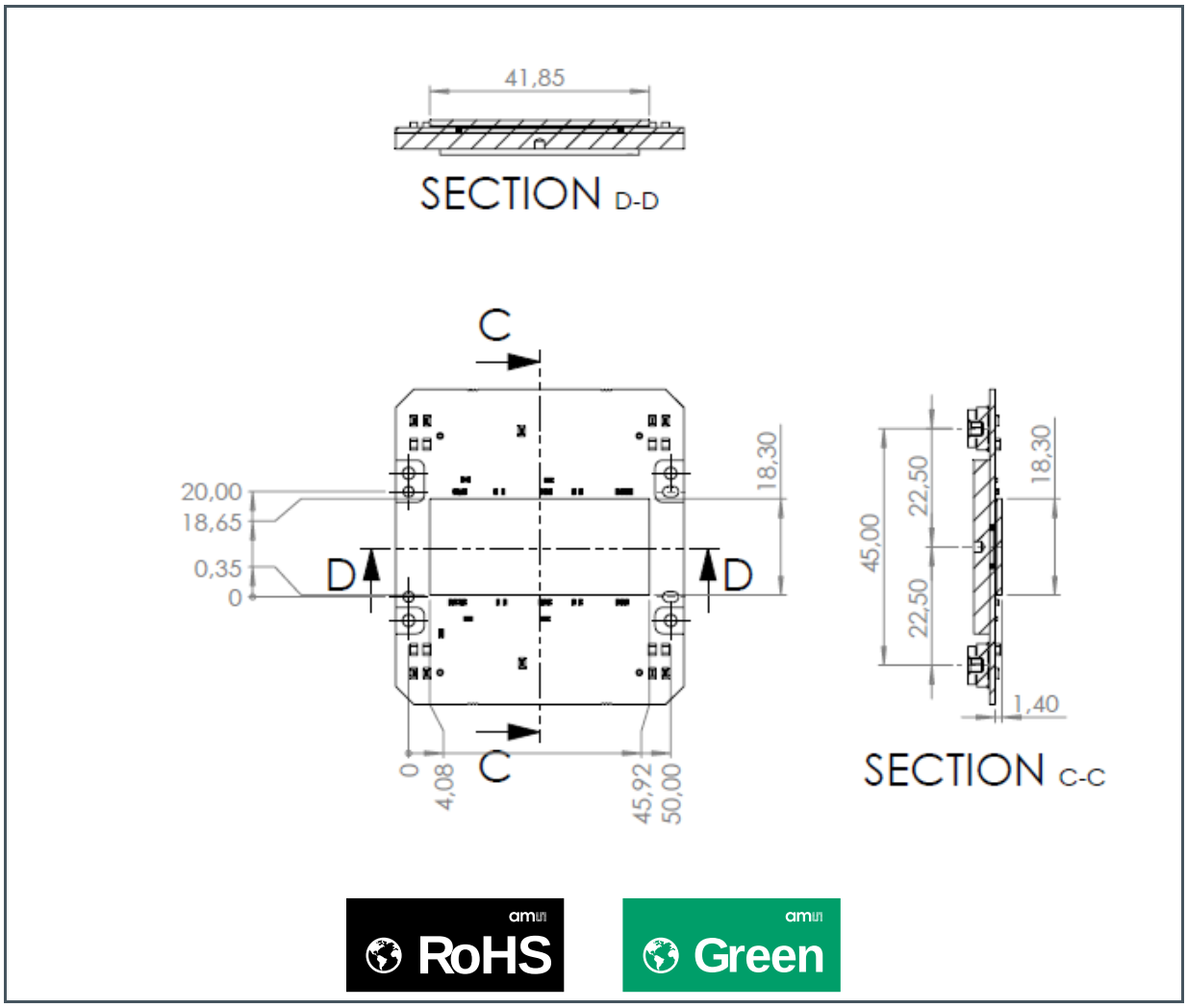
(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are ±0.1 mm.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

Figure 153:
4LS5K Invar Package Outline Drawing – Section A-A and Section B-B(1)(2)(3)(4)



(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are ±0.1 mm.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

Figure 154:
4LS5K Invar Package Outline Drawing – Section C-C and Section D-D(1)(2)(3)(4)



(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are ±0.1 mm.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

Information

For additional support on mechanical drawings (e.g. STEP files), please contact the Technical Support Team.

12 Evaluation System

ams OSRAM provides an Evaluation System for the 4LS sensors family. It supports all variants and has a USB3 interface to the 4LS Viewer Software, for video transmission and 4LS sensor control: For more information, please check the EK user guide, 4LS_Evaluation_Kit_UG001010.

13 Acronyms and Abbreviations

Figure 155:
Acronyms and Abbreviations

Abbreviation / Acronym	Definition
ADC	Analog to Digital Conversion
B&W	Black and White
CDS	Correlated Double Sampling
CLK	Clock
CMOS	Complementary Metal-Oxide Semiconductor
COB	Chip On Board
CVC	Charge to Voltage Converter
DDR	Double Data Rate
DNL	Differential Non-Linearity
DSNU	Dark Signal Non Uniformity
DTI	Down Time for Integration
EB	Electrical Black
EK	Evaluation Kit
EOR	End of Range
ESD	Electrostatic Discharge
FCT	Full Cycle Timing
FWC	Full Well Capacity
FE	Falling Edge
FPGA	Field Programmable Gate Array
FSD	Full Scale Deviation
HBM	Human Body Model
INL	Integral Non-Linearity
LCD	Liquid Crystal Display
LVAL	Line Valid
LVDS	Low-Voltage Differential Signaling
LSB	Least Significant Bit
MCLK	Main Clock Frequency
MISO	Master In Slave Out
MOSI	Master Out Slave In
MSB	Most Significant Bit
MTA	Minimum Timings Allowed
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
PRNU	Pixel Response Non-Uniformity

Abbreviation / Acronym	Definition
QE	Quantum Efficiency
RE	Rising Edge
RGB	Red Green Blue
RH	Relative Humidity
RMS	Root Mean Square
ROI	Region of Interest
SCLK	Serial Clock
S&H	Sample and Hold
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface
SQC	Statistical Quality Control
SRAM	Static Random Access Memory
TDI	Test Data In
TDI	Time Delay and Integration
TDO	Test Data Out
TMS	Test Mode Select
TRST	Test Reset
TS	Training Sequence
TSA	Training Sequence Word A
TSB	Training Sequence Word B
VTS	Valid Training Sequence

14 Revision Information

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams-OSRAM AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams-OSRAM AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

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- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

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