MP2002

Low Input Voltage 500mA Linear Regulator

NOT RECOMMENDED FOR NEW DESIGNS

DESCRIPTION

The MP2002 is a low-current, low-dropout linear regulator operating over a single input supply between 1.35V to 6.5V. The output voltage of the MP2002 is adjustable via an external resistor divider. The MP2002 can supply up to 500mA of load current. The enable pin (EN) allows the part to be put into a low current shutdown mode (EN=0). The MP2002 features thermal overload and current limit protection. It is available in an 8-pin QFN (2 x 3mm) package

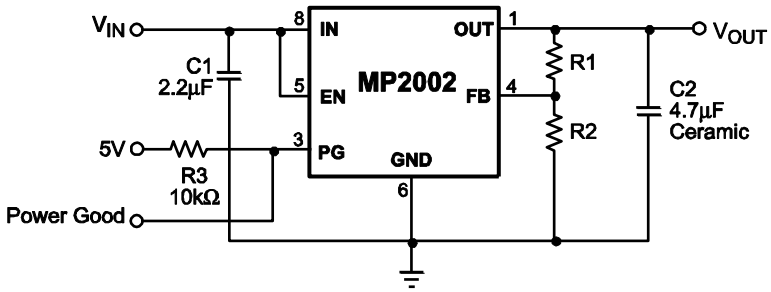
FEATURES

- Power Good Open Collector Output
- Operates from 1.35V – 6.5V Input
- Low 300mV Dropout at 500mA Output
- Stable with Very Small Ceramic Capacitors
- 2% Feedback Reference
- Adjustable Output Voltage Option from 0.5V to 5V using an External Resistor Divider
- Better Than 0.001%/mA Load Regulation
- Low 100µA Ground Current
- Internal Thermal Protection
- Current Limit Protection
- 6µA Typical Quiescent Current at Shutdown
- Available in a Tiny 2 x 3mm 8-pin QFN Package

APPLICATIONS

- Low Current Regulators
- Battery Powered Systems
- Cellular Phones

TYPICAL APPLICATION

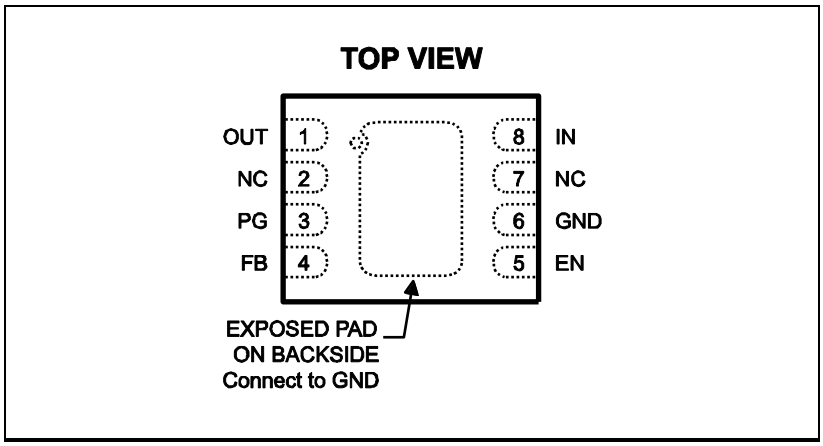


ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP2002DD	QFN8 (2 x 3mm)	L7	-40°C to +85°C

* For Tape & Reel, add suffix –Z (eg. MP2002DD–Z)
For RoHS Compliant Packaging, add suffix –LF (eg. MP2002DD–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

IN, PG, FB to GND.....-0.3V to +7V
EN to GND.....-0.3V to V_{IN} +0.3V
OUT .....-0.3V to V_{IN} + 0.3V
Continuous Power Dissipation (T_A = +25°C)(2)
.....2.27W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Input Voltage V_{IN}.....1.35V to 6.5V
Output Voltage.....0.5V to 5V
Load Current.....500mA Maximum
Maximum Junction Temp. (T_J)..... +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN8 (2 x 3mm) .....55 ..... 12 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature TA. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7 4-layer board.

ELECTRICAL CHARACTERISTICS

V_{IN} = 1.8V, V_{OUT} = 1.2V, C_{OUT} = 4.7µF, C_{IN} = 2.2µF, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ (5)	Max	Units
Operating Voltage		I_{OUT} = 1mA	1.35		6.5	V
Ground Pin Current		I_{OUT} = 1mA (7)		100		µA
		I_{OUT} = 500mA		5		mA
Shutdown Current		V_{EN} = 1.45V, V_{IN} = 5V		7		µA
FB Regulation Voltage			0.482	0.500	0.508	V
		–40°C ≤ T_A ≤ +85°C	0.477	0.495	0.513	
Dropout Voltage (8)		I_{OUT} = 500mA		290		mV
Line Regulation		I_{OUT} = 1mA, V_{IN} = (V_{OUT} + 0.5V) to 6.5V (8)		0.005		%/V
Load Regulation		I_{OUT} = 1mA to 500mA, V_{IN} = V_{OUT} + 0.5V		0.001		%/mA
Power Good Output Voltage Low(9)	V_{OL}	I_{sink} = 0.5mA		0.5		V
EN Input High Voltage			1.2			V
EN Input Low Voltage					0.4	V
EN Input Bias Current		V_{EN} = 1.5V, 5V		0.01	1	µA
Thermal Protection				155		°C
Current Limit			550	730		mA

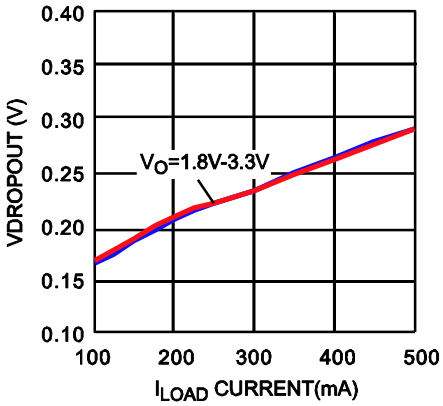
Notes:

5) Parameter is guaranteed by design, not production tested.
6) Resistors for V_{OUT} measurement are 10k, 14k, 1%
7) The ground current does not include current through feedback current
8) Dropout Voltage is defined as the input to output differential when the output voltage drops 1% below its nominal value
9) VFEEDBACK is 90% of the regulated value with 10k pull-up to 5V

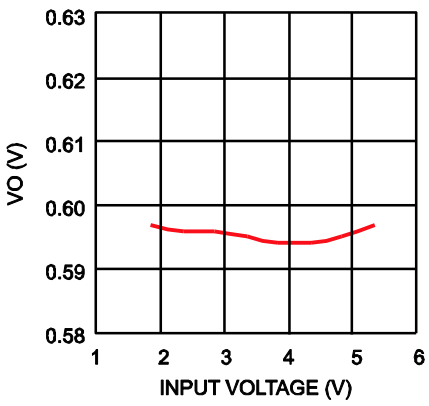
TYPICAL PERFORMANCE CHARACTERISTICS

C1=2.2µF, C2 =4.7µF, C3=1nF, T_A = +25°C, unless otherwise noted. (Reference Figure 2)

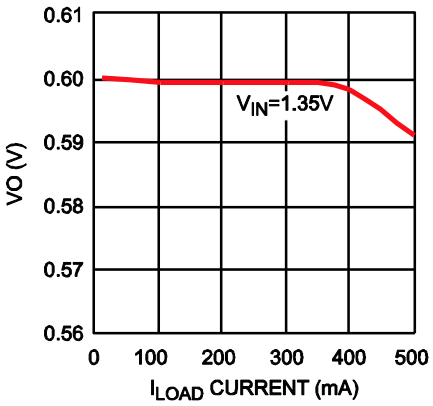
Voltage Dropout vs Current



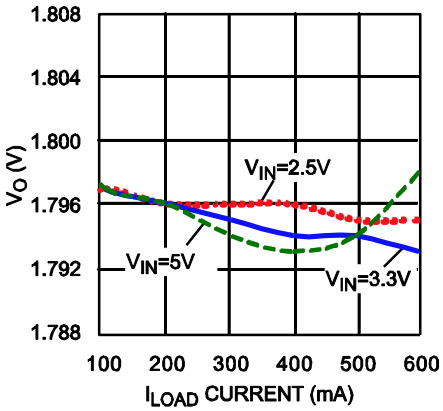
Line Regulation



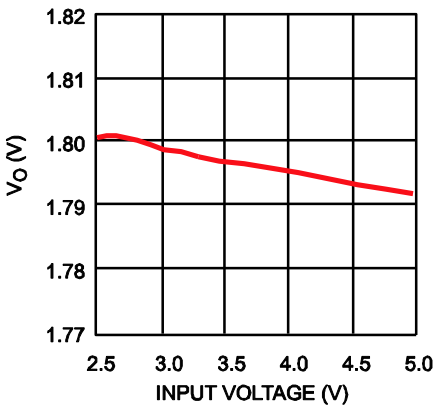
Load Regulation



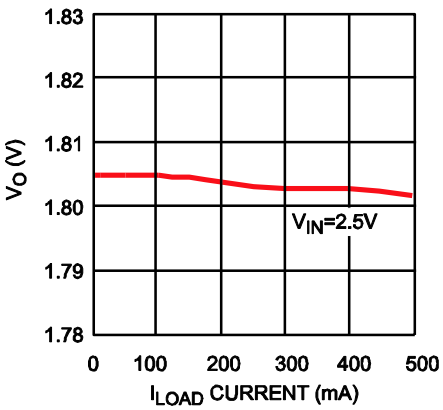
85 °C Load Regulation



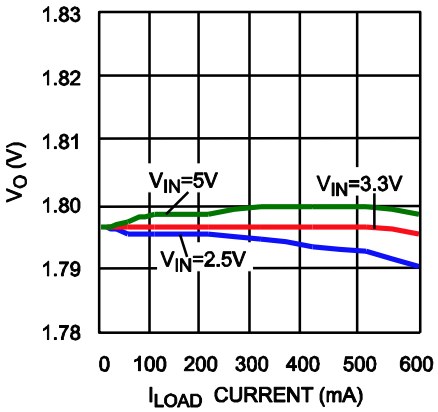
Line Regulation



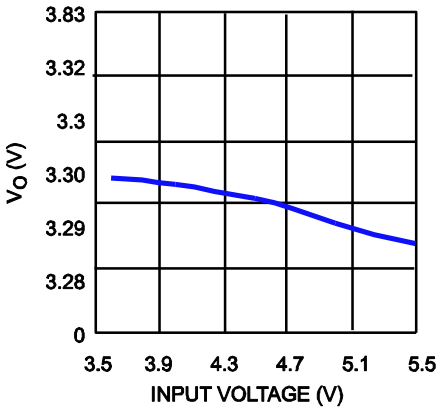
Load Regulation



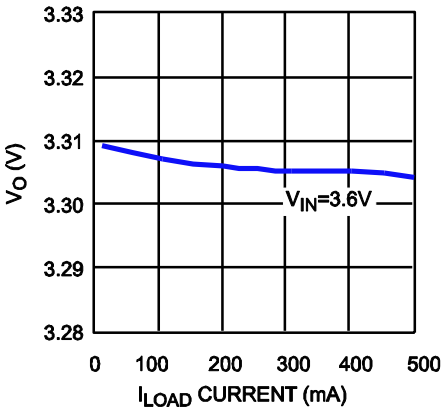
-40 °C Load Regulation



Line Regulation



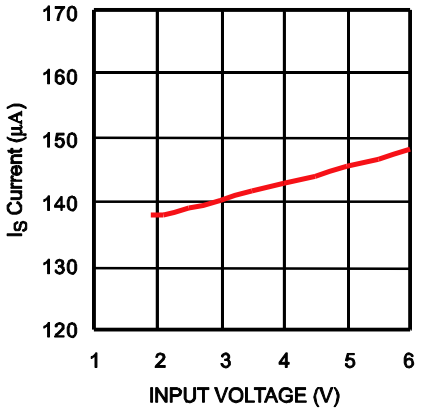
Load Regulation



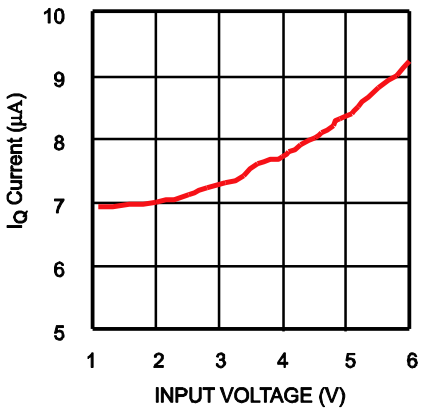
TYPICAL PERFORMANCE CHARACTERISTICS

C1=2.2µF, C2 =4.7µF, C3=1nF, T_A = +25°C, unless otherwise noted. (Reference Figure 2)

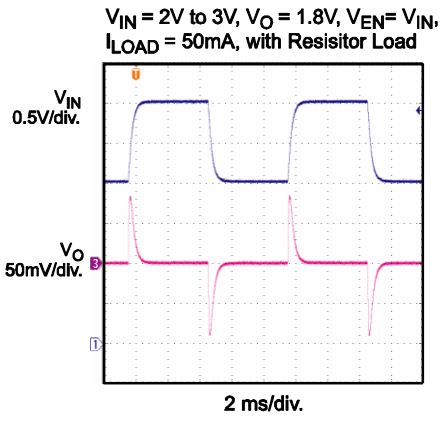
Supply Current



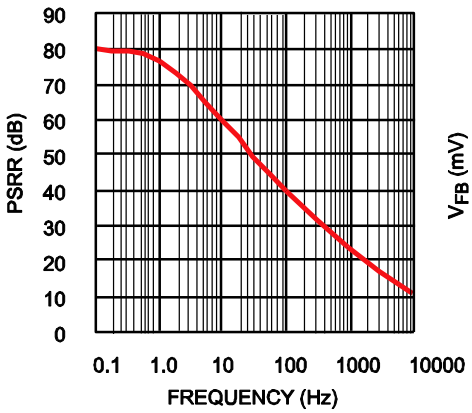
Shut Down Current



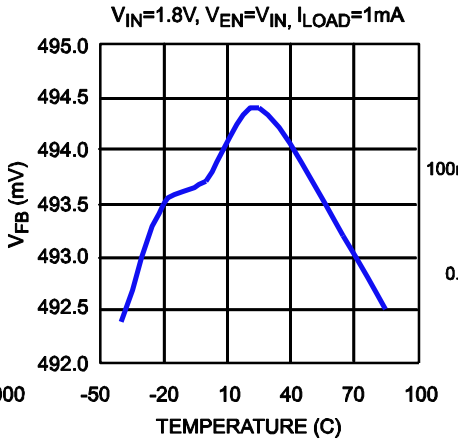
Line Transient



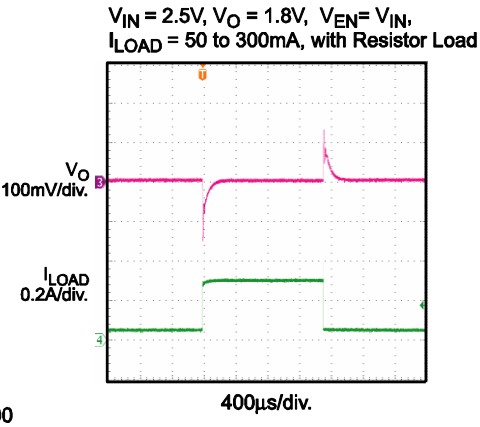
PSRR vs Frequency



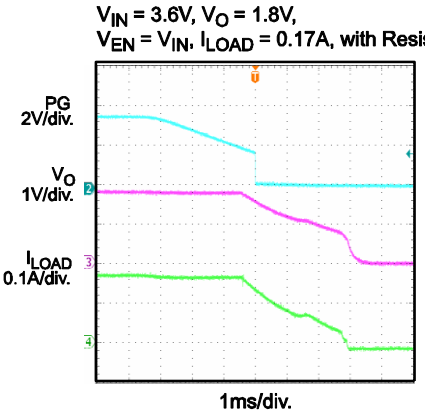
V_{FB} vs Temperature



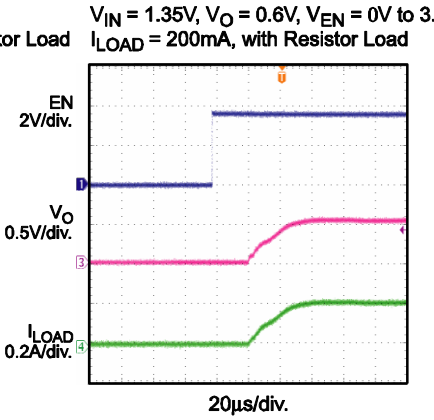
Load Transient



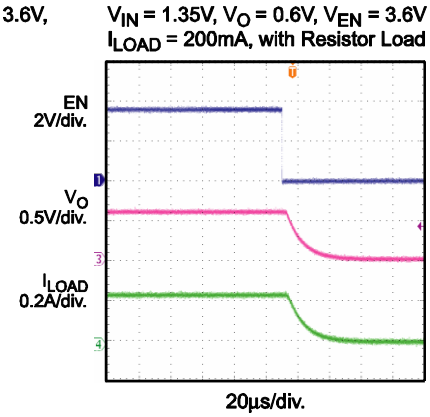
Power Good OFF



Enable Turn On



Enable Turn Off

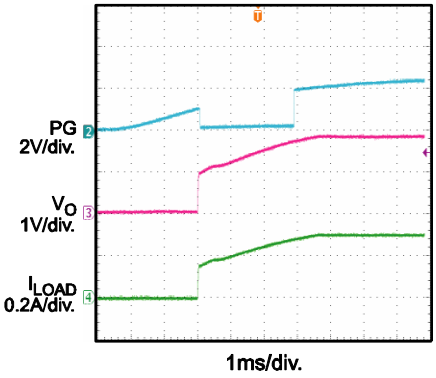


TYPICAL PERFORMANCE CHARACTERISTICS

C1=2.2µF, C2 =4.7µF, C3=1nF, T_A = +25°C, unless otherwise noted. (Reference Figure 2)

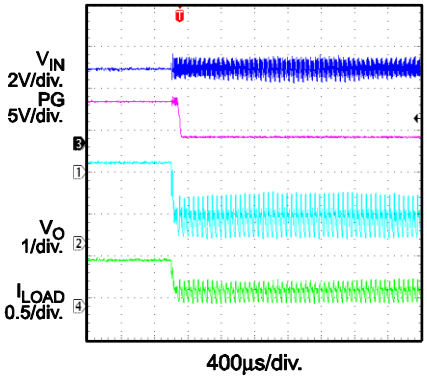
Power Good ON

V_{IN} = 2.5V, V_O = 1.8V, V_{EN} = V_{IN}, I_{LOAD} = 0.3A, with Resistor Load



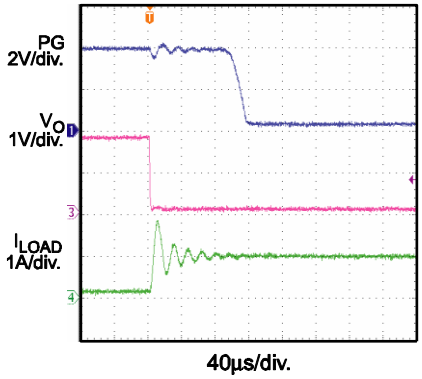
Thermal Protection

V_{IN} = V_{EN} = 5V, V_O = 1.8V, I_{LOAD} = 0.5A



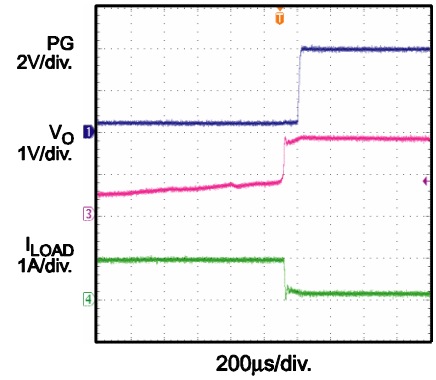
Short Circuit Protection

V_{IN} = 4V, V_O = 1.8V, V_{EN} = V_{IN}



Short Circuit Recovery

V_{IN} = 4V, V_O = 1.8V, V_{IN} = V_{EN}



PIN FUNCTIONS

Pin #	Name	Description
1	OUT	Regulator Output. OUT is the output of the linear regulator. Bypass OUT to GND with a 4.7μF or greater capacitor.
2	NC	No connect.
3	PG	Power Good Open Collector Output
4	FB	Feedback Input. Connect a resistive voltage divider from OUT to FB to set the output voltage. OUT feedback threshold is 0.5V.
5	EN	Enable Input. Drive EN higher than 1.2V to turn on the MP2002, drive EN lower than 0.4V to turn it off.
6	GND, Exposed pad	Ground. Exposed pad must be connected to GND plane.
7	NC	No connect.
8	IN	Power Source Input. IN supplies the internal power to the MP2002 and is the source of the pass transistor. Bypass IN to GND with a 2.2μF or greater capacitor.

OPERATION

The MP2002 is a low-current, low-voltage, high-PSRR, low-dropout, linear regulator. It is intended for use in devices that require very low voltage, low quiescent current power and high PSRR such as wireless modems, pagers, and cellular phones.

The MP2002 uses a PNP pass element and features internal thermal shutdown and an internal current limit circuit.

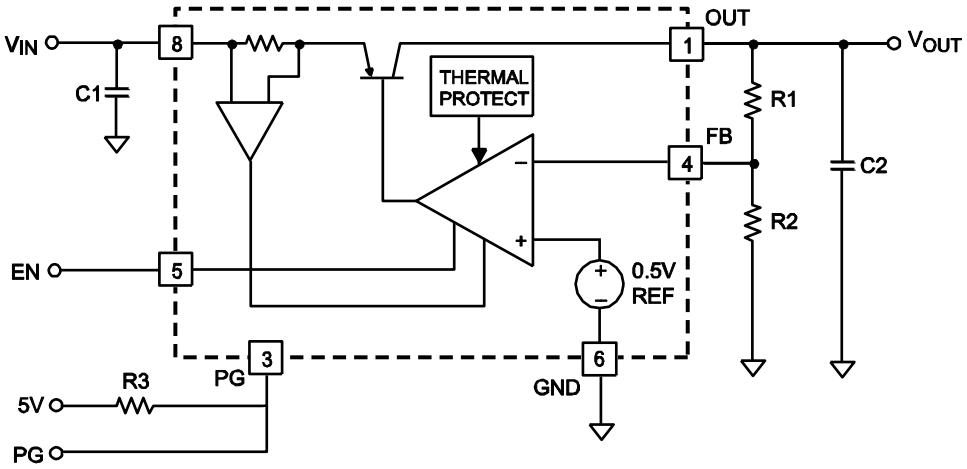


Figure 1—Block Diagram of Ultra Low Noise Adjustable Output Regulator

APPLICATION INFORMATION

Setting the Output Voltage

The MP2002 has an adjustable output voltage, set via an external resistor divider (R1 and R2 in Figure 2).

$$R1 = R2 \times \left(\frac{V_{OUT} - V_{FB}}{V_{FB}} \right)$$

where V_{FB} = 0.5V (The OUT feedback threshold voltage.)

Example: For 2.5V Output and R2=10kΩ

$$R1 = 10k \times \left(\frac{2.5 - 0.5}{0.5} \right) = 40k\Omega$$

A standard 40kΩ (±1%) resistor can be selected for R1.

Table 1 lists the selected R1 values for some typical output voltages (assuming R2 = 10kΩ).

Power Good

The power good pin is an open collector output completed with a pull up resistor (10kΩ recommended). The pull up resistor can be tied to a supply within the voltage range of the pin (0V to 5.5V). For example, the pull up resistor can be tied to the input voltage when it is being monitored by an IC powered from this input voltage. It monitors the output voltage, and if the output voltage is 10% below its regulation point, the PG pin becomes low.

Table 1—Adjustable Output Voltage R1 Values (R2=10kΩ)

V_{OUT} (V)	R1 (Ω)
1.25	15k
1.5	20k
1.8	26k
2	30k
2.5	40k
2.8	46k
3	50k
3.3	56k
4	70k
5	90k

Bypass Capacitors

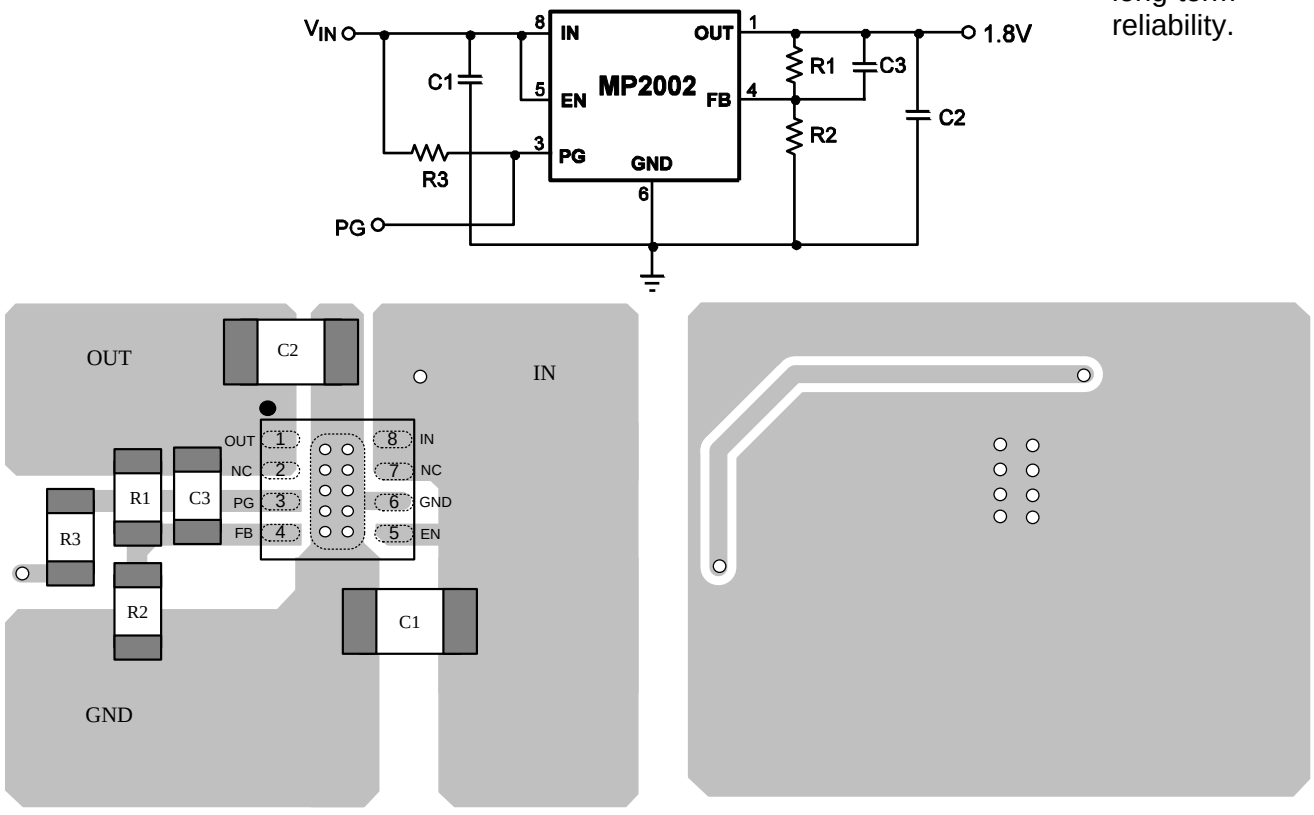
For lower noise, the reference voltage can be bypassed by an external capacitor. A low ESR capacitor, such as the ceramic type, will provide the best performance.

PCB Layout Guide

PCB layout is very important to achieve good regulation, ripple rejection, transient response and thermal performance. It is highly recommended to duplicate EVB layout for optimum performance.

If change is necessary, please follow these guidelines and take Figure 2 for reference.

1) Input and output bypass ceramic capacitors are suggested to be put close to the IN Pin and OUT Pin respectively.
2) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
3) Connect IN, OUT and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.



Top Layer **Bottom Layer**

Figure 2—PCB Layout

TYPICAL APPLICATION CIRCUIT

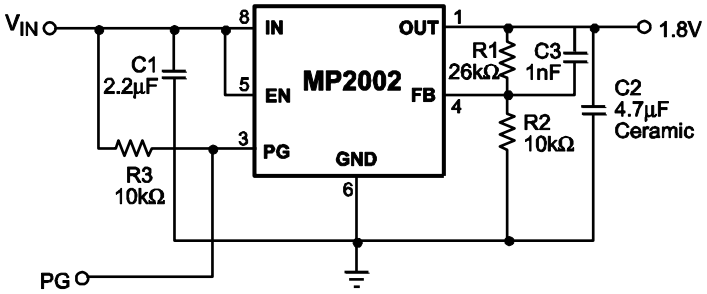
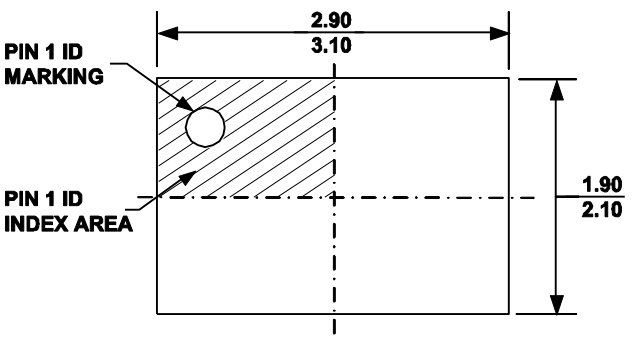


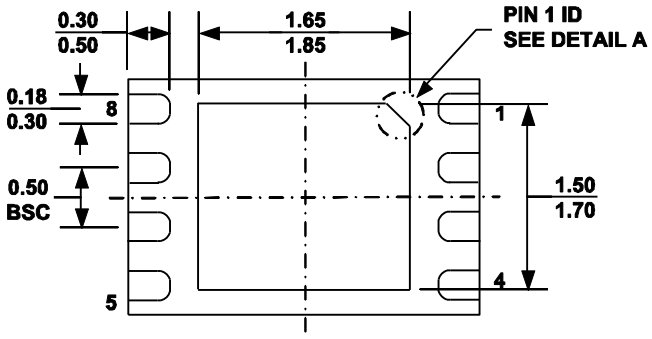
Figure 3—Typical Application Circuit with Fix Pinout

PACKAGE INFORMATION

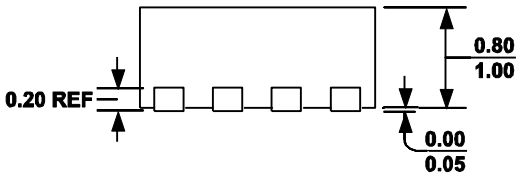
QFN8 (2mm x 3mm)



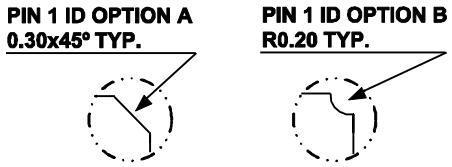
TOP VIEW



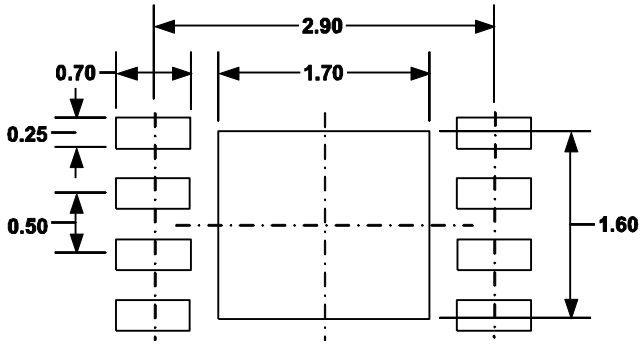
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VCED-2.
5) DRAWING IS NOT TO SCALE.