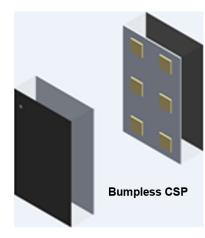
MLPF-WB55-02E3

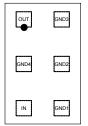


Datasheet

2.4 GHz low pass filter matched to STM32WB55Vx



Top view (pads down)



Product status link MLPF-WB55-02E3

Features

- Integrated impedance matching to STM32WB55Vx
- LGA footprint compatible
- 50 Ω nominal impedance on antenna side
- Deep rejection harmonics filter
- Low insertion loss
- Small footprint

•

- Low thickness ≤ 450 µm
- High RF performance
- RF BOM and area reduction
- ECOPACK2 compliant component

Applications

- Bluetooth 5
- OpenThread
- Zigbee®
- IEEE 802.15.4
- Optimized for STM32WB55Vx

Description

The MLPF-WB55-02E3 integrates an impedance matching network and harmonics filter. The matching impedance network has been tailored to maximize the RF performance of STM32WB55Vx. This device uses STMicroelectronics IPD technology on non-conductive glass substrate which optimizes RF performance.

1 Characteristics

Symbol	Parameter	Value	Unit
P _{IN}	Input power RF _{IN}	10	dBm
V _{ESD}	ESD ratings human body model (JESD22-A114-C), all I/O one at a time while others connected to GND	2000 V	
ESD ratings machine model, all I/O		200	
T _{OP}	Maximum operating temperature	-40 to +105	°C

Table 2. Impedances(T_{amb} = 25 °C)

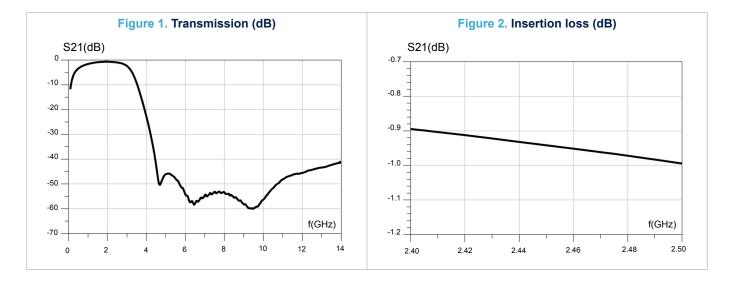
Symbol	Parameter		Unit		
Symbol	Farameter	Min.	Тур.	Max.	Onit
Z _{IN}	STM32WB55xx single-ended impedance	-	matched to STM32WB55Vx	-	Ω
Z _{OUT}	Antenna impedance	-	50	-	Ω

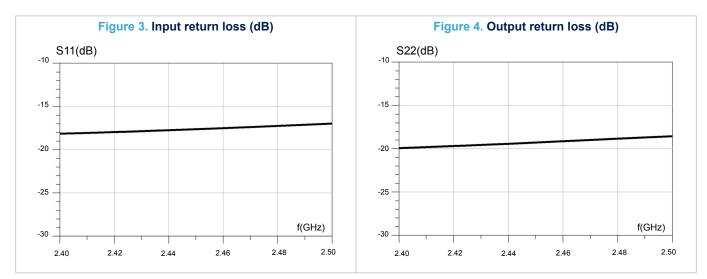
Table 3. Electrical characteristics and RF performance (T_{amb} = 25 °C)

Cumhal	Parameter -		Value			Unit
Symbol			Min.	Тур.	Max.	Onit
f	Frequency range	Frequency range			2500	MHz
IL	Insertion loss IS ₂₁ I			1.0	1.2	dB
RL _{IN}	Input return loss IS ₁₁	l	13	17		dB
RL _{OUT}	Output return loss IS ₂₂ I		15	18		dB
	Harmonic rejection	Attenuation at 2fo (4800-5825) MHz	43	45		dB
Att		Attenuation at 3fo (7200 – 7500) MHz	47	53		dB
Au levels	levels IS ₂₁ I	Attenuation at 4fo (9600 – 10000) MHz	41	56		dB
		Attenuation at 5fo (12000 – 12500) MHz	38	44		dB



1.1 RF measurement





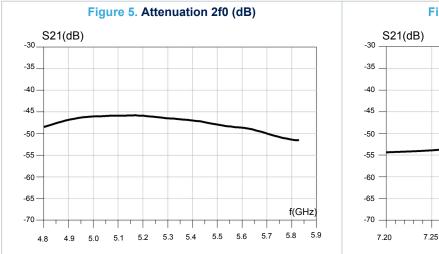


Figure 6. Attenuation 3f0 (dB) (dB)

7.35

7.30

7.40

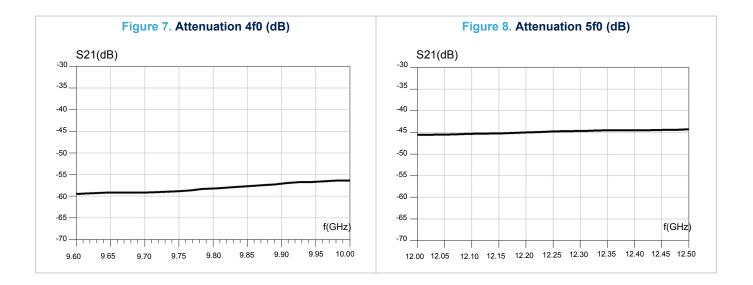
f(GHz)

7.45

7.50







Coating 25µm

Package information 2

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Bumpless CSP package information 2.1

Figure 9. Bumpless CSP package outline

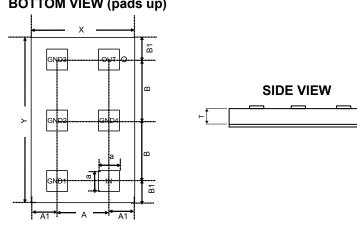


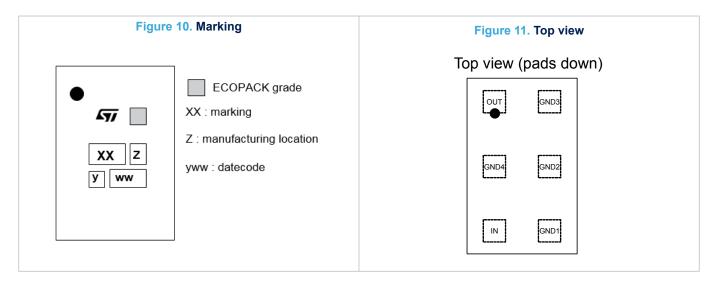
Table 4. Bumpless CSP package mechanical data

Parameter	Description	Min.	Тур.	Max.	Unit
Х	X dimension of the die	975	1000	1025	μm
Y	Y dimension of the die	1575	1600	1625	μm
А	X pitch		500		μm
В	Y pitch		587		μm
A1	Distance from bump to edge of die on X axis		250		μm
B1	Distance from pad to edge of die on Y axis		213		μm
а	Pad dimension		200		μm
Т	Substrate thickness	375	400	425	μm

BOTTOM VIEW (pads up)



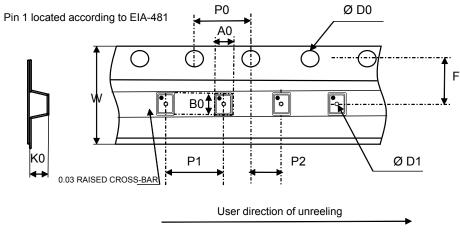




More packing information is available in the application note:

AN2348 Flip-Chip: "Package description and recommendations for use

Figure 12. Tape and reel outline



Note:

Pocket dimensions are not on scale Pocket shape may vary depending on package

	Dimensions Millimeters				
Ref					
	Min	Тур	Мах		
A0	1.04	1.09	1.14		
B0	1.64	1.69	1.74		
КО	0.47	0.52	0.57		
P1	3.9	4.0	4.1		
P0	3.9	4.0	4.1		
Ø D0	1.4	1.5	1.6		
Ø D1	0.35	0.40	0.45		
F	3.45	3.50	3.55		
P2	1.95	2.00	2.05		
W	7.9	8.0	8.3		

Table 5. Tape and reel mechanical data

Table 6. Pad description top view (pads down)

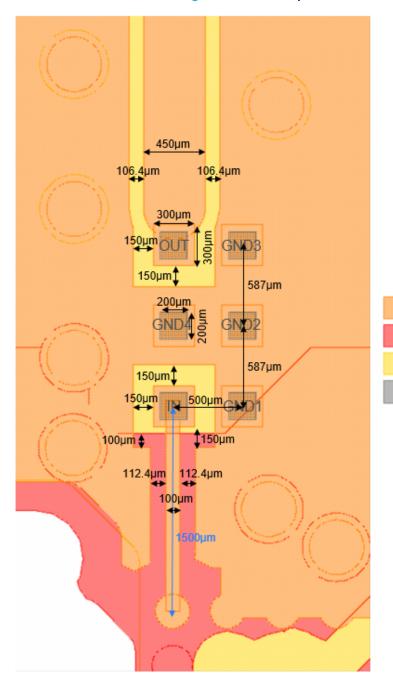
Pad ref	Pad name	Description
A1	OUT	Antenna
A2	GND4	Ground
A3	IN	STM32WB55 RF out
B1	GND3	Ground
B2	GND2	Ground
В3	GND1	Ground



3 Recommendation on PCB assembly

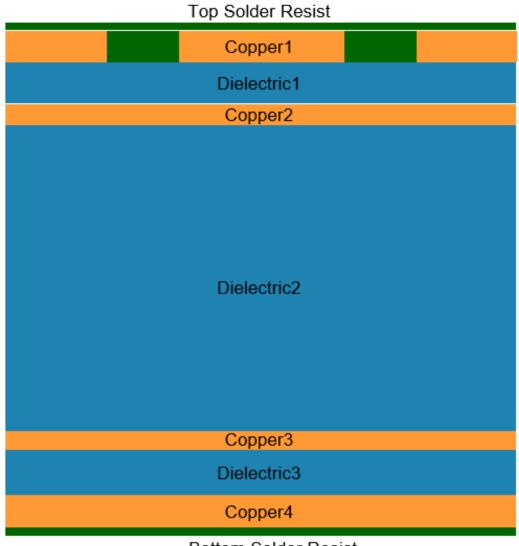
3.1 Land pattern

Figure 13. PCB land pattern recommendations



Top_Layer_L1 Buried_Layer_L2 Buried_Layer_L3 Top_Solder_Mask

Figure 14. PCB stack-up recommendations

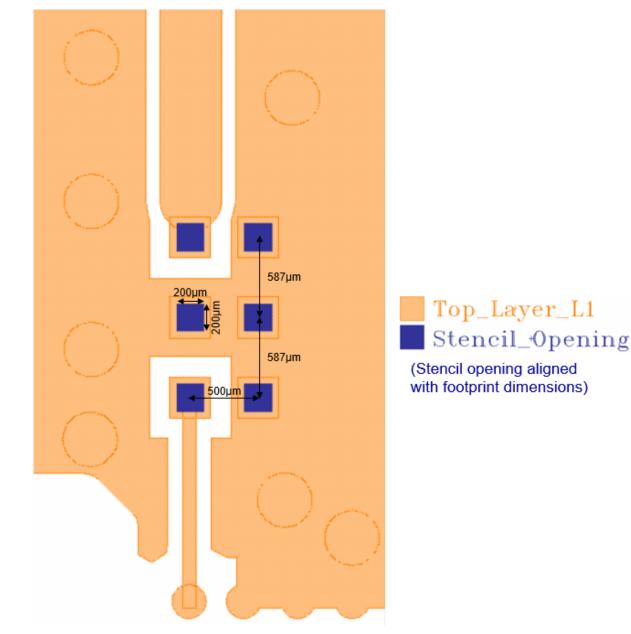


Bottom Solder Resist

Material	Thickness	Dielectric constant
Copper1	62 µm	
Dielectric1	82 µm	3.69
Copper2	41 µm	
Dielectric2	1180 µm	3.69
Copper3	42 µm	
Dielectric3	87 µm	3.69
Copper4	66 µm	

3.2 Stencil opening design





3.3 Solder paste

- 1. 100 µm solder stencil thickness is recommended
- 2. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
- 3. "No clean" solder paste is recommended.
- 4. Offers a high tack force to resist component movement during PCB movement.
- 5. Solder paste with fine particles: powder particle size is 20-45 $\mu m.$

3.4 Placement

- 1. Manual positioning is not recommended.
- 2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
- 3. Standard tolerance of ±0.05 mm is recommended.
- 4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
- 5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
- 6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.5 PCB design preference

- 1. To control the solder paste amount, the closed via is recommended instead of open vias.
- 2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.



4 Ordering information

Figure 16. Ordering information scheme

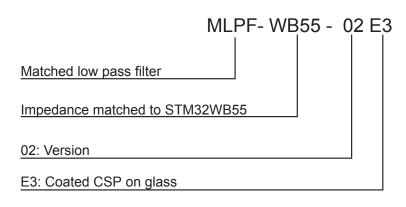


Table 7. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
MLPF-WB55-02E3	TT	CSP Bumpless	1.546 mg	5000	Tape and reel (7")

Revision history

Table 8. Document revision history

Date	Version	Changes
28-Nov-2019	1	Initial release.



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