

# MOSFET – N-Channel, Shielded Gate, POWERTRENCH®

150 V, 2.3 A, 144 mΩ

## FDC86244

### General Description

This N-Channel MOSFET is produced using ON Semiconductor's advanced POWERTRENCH process that incorporates Shielded Gate technology. This process has been optimized for  $r_{DS(on)}$ , switching performance and ruggedness.

### Features

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 144 mΩ at  $V_{GS} = 10$  V,  $I_D = 2.3$  A
- Max  $r_{DS(on)}$  = 188 mΩ at  $V_{GS} = 6$  V,  $I_D = 1.9$  A
- High Performance Trench Technology for Extremely Low  $r_{DS(on)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- Fast Switching Speed
- 100% UIL Tested
- This Device is Pb-Free, Halogen Free/BFR Free and is RoHS Compliant

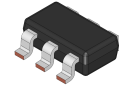
### Applications

- Load Switch
- Synchronous Rectifier
- Primary Switch



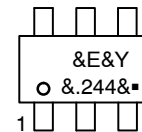
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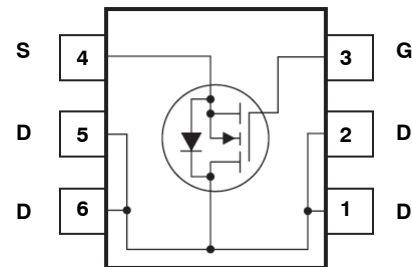
TSOT23 6-Lead  
CASE 419BL

### MARKING DIAGRAM



XXX = Specific Device Code  
 &E = Space Designator  
 &Y = Year of Production  
 &. = Pin One Identifier  
 ▪ = Pb-Free Package

### PINOUT



SuperSOT™-6

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# FDC86244

## MOSFET MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	150	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current – Continuous (Note 1a) – Pulsed	2.3 10	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	12	mJ
$P_D$	Power Dissipation (Note 1a)	1.6	W
	Power Dissipation (Note 1b)	0.8	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	30	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	78	

## PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
0.244	FDC86244	SSOT-6	7"	8 mm	3000 Units

# FDC86244

## ELECTRICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}$ , $V_{GS} = 0 \text{V}$	150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$		103		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 120 \text{V}$ , $V_{GS} = 0 \text{V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{V}$ , $V_{DS} = 0 \text{V}$			$\pm 100$	nA

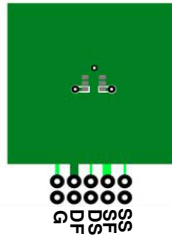
<b>ON CHARACTERISTICS</b>						
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250 \mu\text{A}$	2.0	2.5	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$		-9		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{V}$ , $I_D = 2.3 \text{A}$		113	144	m $\Omega$
		$V_{GS} = 6 \text{V}$ , $I_D = 1.9 \text{A}$		128	188	
		$V_{GS} = 10 \text{V}$ , $I_D = 2.3 \text{A}$ , $T_J = 125^\circ\text{C}$		214	273	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5 \text{V}$ , $I_D = 2.3 \text{A}$		6		S

<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 75 \text{V}$ , $V_{GS} = 0 \text{V}$ , $f = 1 \text{MHz}$		260	345	pF
$C_{oss}$	Output Capacitance			32	45	pF
$C_{rss}$	Reverse Transfer Capacitance			1.7	5	pF
$R_g$	Gate Resistance			1.3		$\Omega$

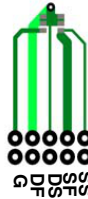
<b>SWITCHING CHARACTERISTICS</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75 \text{V}$ , $I_D = 2.3 \text{A}$ , $V_{GS} = 10 \text{V}$ , $R_{GEN} = 6 \Omega$		4.7	10	ns
$t_r$	Rise Time			1.4	10	ns
$t_{d(off)}$	Turn-Off Delay Time			10	20	ns
$t_f$	Fall Time			3.1	10	ns
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0 \text{V}$ to $10 \text{V}$	$V_{DD} = 75 \text{V}$	4.2	6
	Total Gate Charge	$V_{GS} = 0 \text{V}$ to $5 \text{V}$	2.4		4	nC
$Q_{gs}$	Total Gate Charge	$I_D = 2.3 \text{A}$		1.0		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			1.0		nC

<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>						
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{V}$ , $I_S = 2.3 \text{A}$ (Note 2)		0.8	1.3	V
$t_{rr}$	Reverse Recovery Time	$I_F = 2.3 \text{A}$ , $di/dt = 100 \text{A}/\mu\text{s}$		45	73	ns
$Q_{rr}$	Reverse Recovery Charge			33	53	nC

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $78^\circ\text{C}/\text{W}$  when mounted on a  $1 \text{in}^2$  pad of 2 oz copper



b.  $175^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width <  $300 \mu\text{s}$ , Duty cycle < 2.0 %.  
3. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 1.0 \text{mH}$ ,  $I_{AS} = 5.0 \text{A}$ ,  $V_{DD} = 135 \text{V}$ ,  $V_{GS} = 10 \text{V}$ .

TYPICAL CHARACTERISTICS  $T_J = 25^\circ\text{C}$  Unless Otherwise Noted

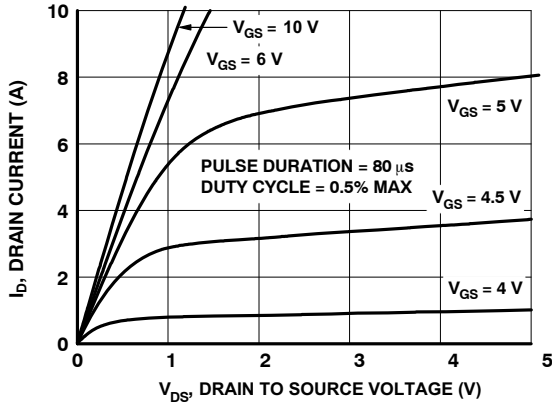


Figure 1. On-Region Characteristics

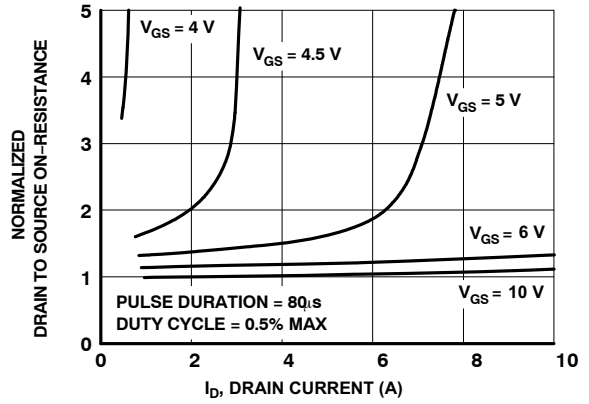


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

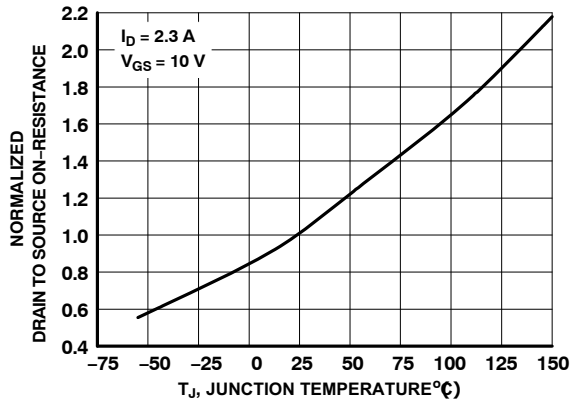


Figure 3. Normalized On-Resistance vs Junction Temperature

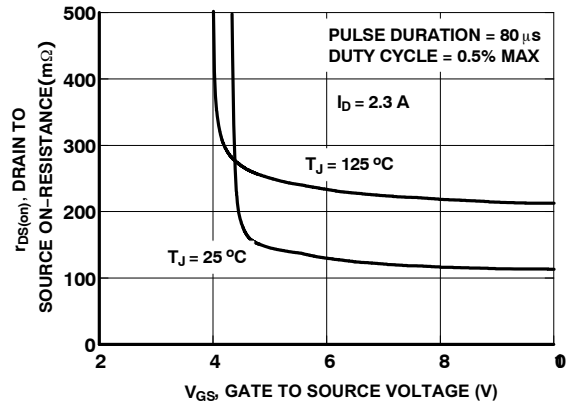


Figure 4. On-Resistance vs Gate to Source Voltage

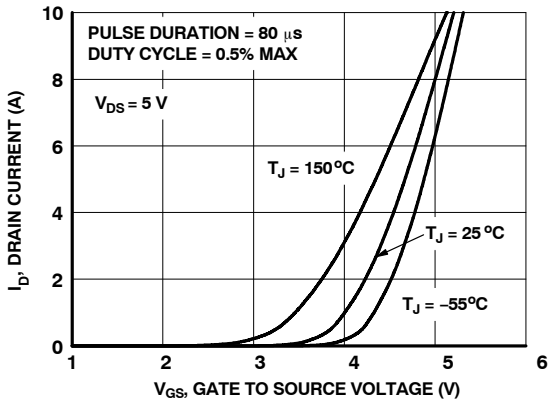


Figure 5. Transfer Characteristics

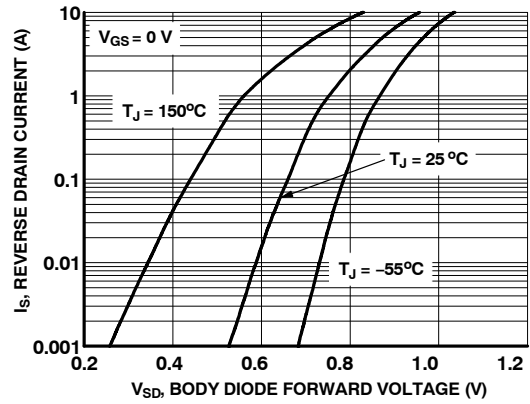


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS  $T_J = 25^\circ\text{C}$  Unless Otherwise Noted (continued)

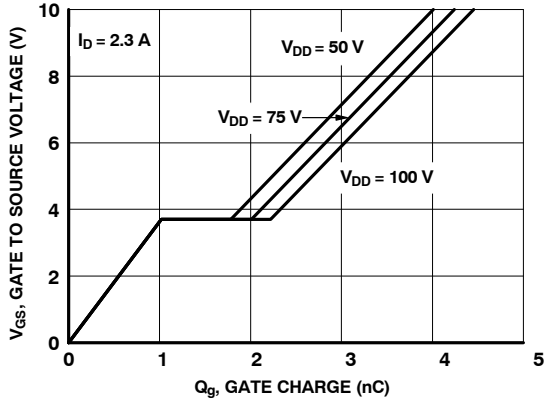


Figure 7. Gate Charge Characteristics

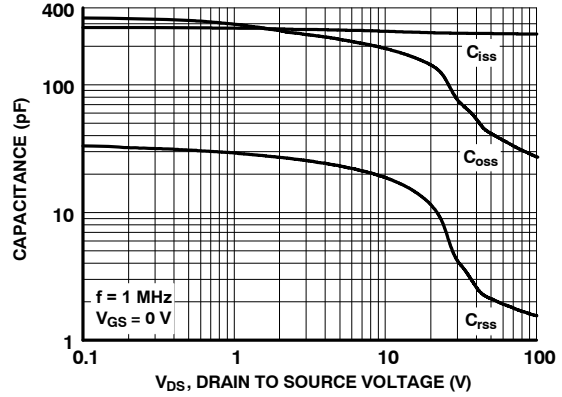


Figure 8. Capacitance vs Drain to Source Voltage

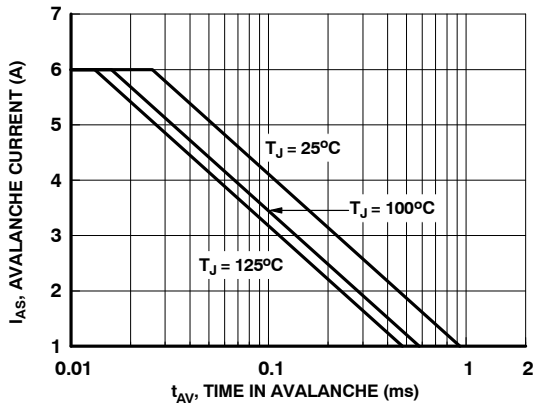


Figure 9. Unclamped Inductive Switching Capability

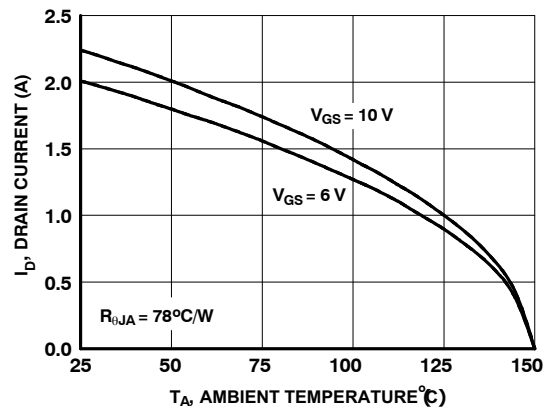


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

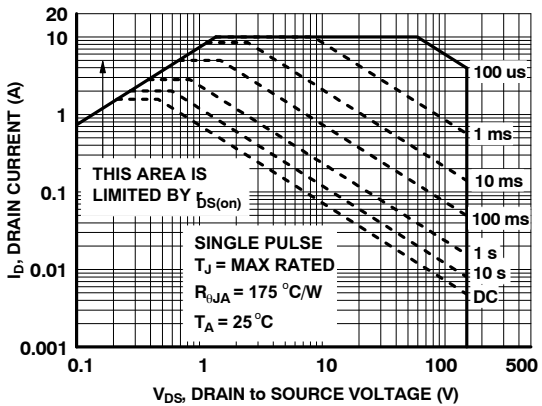


Figure 11. Forward Bias Safe Operating Area

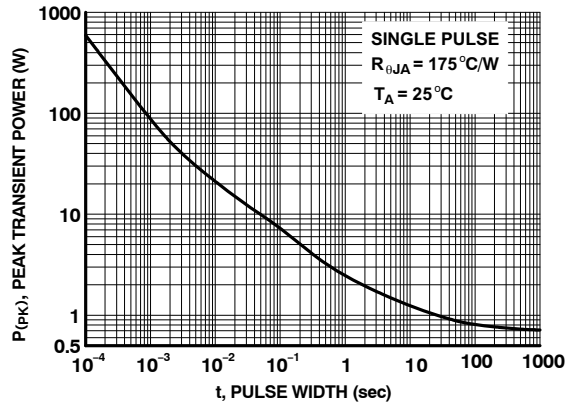


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS  $T_J = 25^\circ\text{C}$  unless otherwise noted (continued)

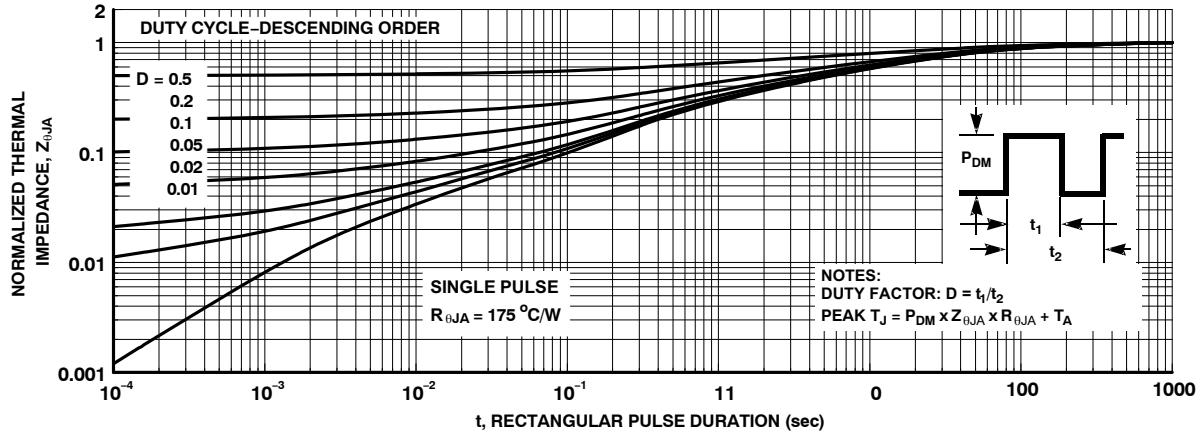


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

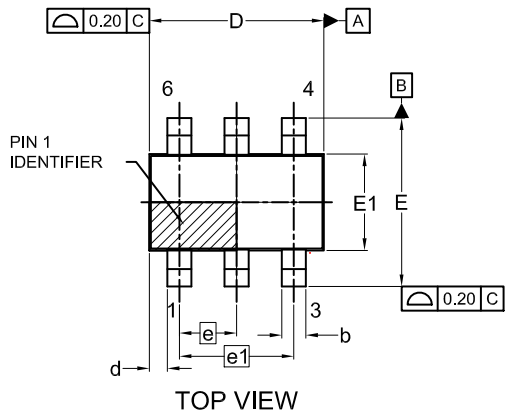
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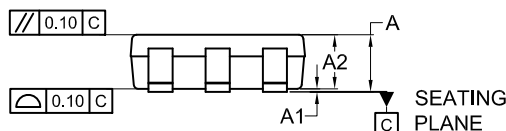
1  
SCALE 2:1

## TSOT23 6-Lead CASE 419BL ISSUE A

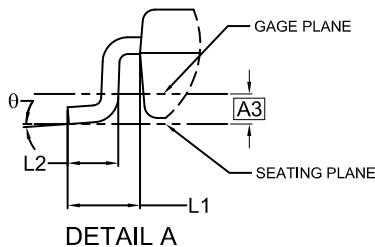
DATE 31 AUG 2020



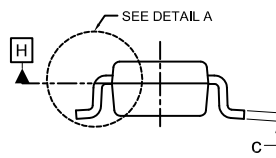
TOP VIEW



FRONT VIEW

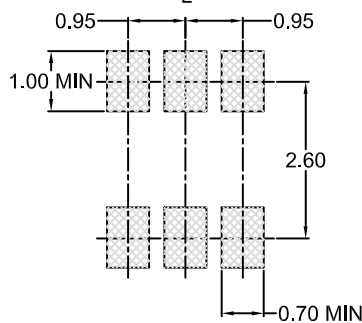


DETAIL A



SIDE VIEW

SYMM  
⌀



LAND PATTERN  
RECOMMENDATION

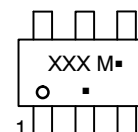
\*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDDERRM/D.

NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- CONTROLLING DIMENSION: MILLIMETERS
- DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
- SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3	0.25 BSC		
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d	0.30 REF		
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.95 BSC		
e1	1.90 BSC		
L1	0.60 REF		
L2	0.20	0.40	0.60
⊖	0°	--	10°

### GENERIC MARKING DIAGRAM\*



XXX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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<b>DESCRIPTION:</b>	<b>TSOT23 6-Lead</b>	<b>PAGE 1 OF 1</b>

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