TEXAS INSTRUMENTS

SN54HC273, SN74HC273

SCLS136E – DECEMBER 1982 – REVISED JULY 2016

SNx4HC273 Octal D-Type Flip-Flops With Clear

1 Features

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up to 10 LSTTL Loads
- Low Power Consumption, 80-µA Maximum I_{CC}
- Typical t_{pd} = 12 ns
- ±4-mA Output Drive at 5 V
- Low Input Current of 1-µA Maximum
- Contain Eight Flip-Flops With Single-Rail Outputs
- Direct Clear Input
- Individual Data Input to Each Flip-Flop
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Buffer or Storage Registers
- Shift Registers
- Pattern Generators

3 Description

The SNx4HC273 devices are positive-edge-triggered D-type flip-flops with a direct active low clear (CLR) input.

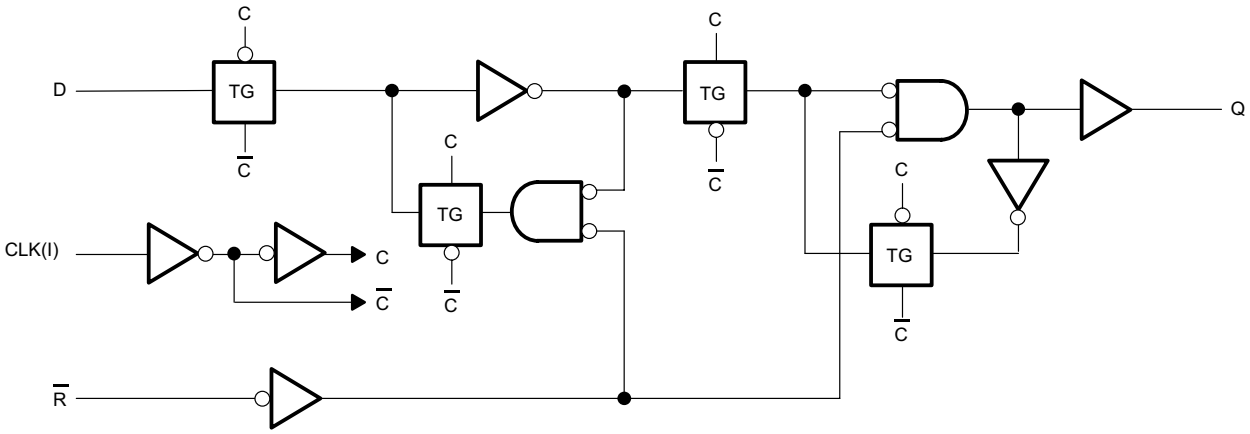
Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not related directly to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output.

Device Information(1)

PART NUMBER	PACKAGE (PINS)	BODY SIZE (NOM)
SN54HC273J	CDIP (20)	24.20 mm × 6.92 mm
SN54HC273W	CFP (20)	13.09 mm × 6.92 mm
SN54HC273FK	LCCC (20)	8.89 mm × 8.89 mm
SN74HC273D	SOIC (20)	12.80 mm × 7.50 mm
SN74HC273DB	SSOP (20)	7.20 mm × 5.30 mm
SN74HC273NS	SO (20)	12.60 mm × 5.30 mm
SN74HC273N	PDIP (20)	24.33 mm × 6.35 mm
SN74HC273PW	TSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram, Each Flip-Flop (Positive Logic)



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4 Revision History

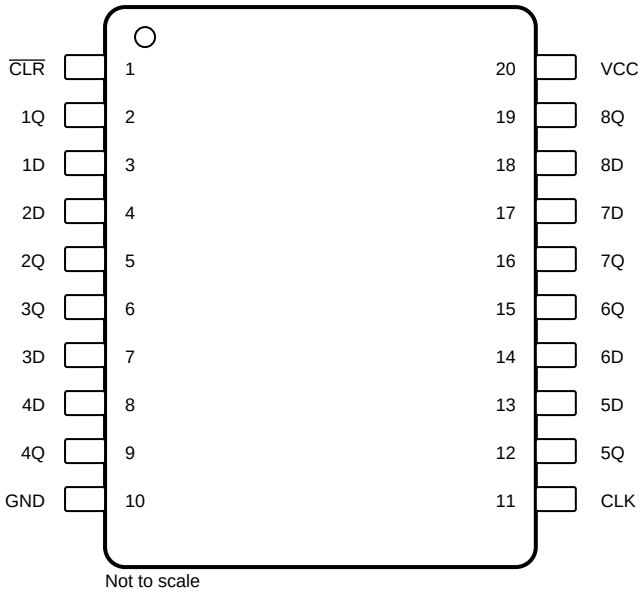
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (August 2003) to Revision E **Page**

- Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Removed *Ordering Information* table, see POA at the end of the data sheet ... 1
- Added Military Disclaimer to *Features* ... 1
- Changed $R_{\theta JA}$ for DB package from 70°C/W : to 90.3°C/W ... 5
- Changed $R_{\theta JA}$ for DW package from 58°C/W : to 77.4°C/W ... 5
- Changed $R_{\theta JA}$ for N package from 69°C/W : to 45.1°C/W ... 5
- Changed $R_{\theta JA}$ for NS package from 60°C/W : to 72.6°C/W ... 5
- Changed $R_{\theta JA}$ for PW package from 83°C/W : to 98.3°C/W ... 5

5 Pin Configuration and Functions

J, W, DB, DW N, NS, or PW Package
CDIP, CFP, SSOP, SOIC, SO, PDIP, or TSSOP
Top View



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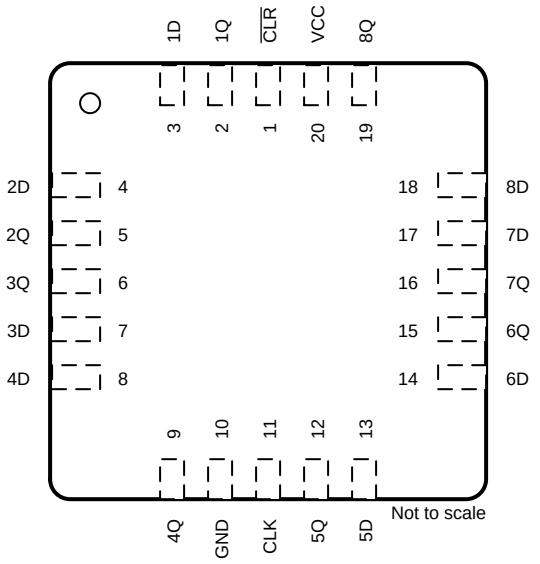
FK Package
20-Pin LCCC
Top View



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Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$\overline{\text{CLR}}$	I	Active low clear input
2	1Q	O	Output 1
3	1D	I	Input 1
4	2D	I	Input 2
5	2Q	O	Output 2
6	3Q	O	Output 3
7	3D	I	Input 3
8	4D	I	Input 4
9	4Q	O	Output 4
10	GND	—	Ground
11	CLK	I	Clock input
12	5Q	O	Output 5
13	5D	I	Input 5
14	6D	I	Input 6
15	6Q	O	Output 6
16	7Q	O	Output 7
17	7D	I	Input 7
18	8D	I	Input 8
19	8Q	O	Output 8
20	V_{CC}	—	Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current(2)	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings – SN74HC273

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 6 V	4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 6 V			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise and fall time	V_{CC} = 2 V			1000	ns
		V_{CC} = 4.5 V			500	
		V_{CC} = 6 V			400	
T_A	Operating free-air temperature	SN54HC273	–55		125	°C
		SN74HC273	–40		85	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*.

6.4 Thermal Information

THERMAL METRIC[1]		SN74HC273					UNIT
		DB (SSOP)	DW (SOIC)	N (PDIP)	NS (SO)	PW (TSSOP)	
		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	90.3	77.4	45.1	72.6	98.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.7	42.8	31.1	38.9	33.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.5	45.2	26	40.1	49.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.7	16.7	16.6	15.7	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.1	44.7	25.9	39.7	48.7	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 µA	V_{CC} = 2 V	1.9	1.998		V
			V_{CC} = 4.5 V	4.4	4.499		
			V_{CC} = 6 V	5.9	5.999		
		I_{OH} = –4 mA, V_{CC} = 4.5 V		3.98	4.3		
		I_{OH} = –5.2 mA, V_{CC} = 6 V		5.48	5.8		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	V_{CC} = 2 V		0.002	0.1	V
			V_{CC} = 4.5 V		0.001	0.1	
			V_{CC} = 6 V		0.001	0.1	
		I_{OL} = 4 mA, V_{CC} = 4.5 V			0.17	0.26	
		I_{OL} = 5.2 mA, V_{CC} = 6 V			0.15	0.26	
I_I	$V_I = V_{CC}$ or 0, V_{CC} = 6 V				±0.1	±100	nA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0, V_{CC} = 6 V					8	µA
C_i	V_{CC} = 2 V to 6 V				3	10	pF

6.6 Electrical Characteristics – SN54HC273

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 µA	V_{CC} = 2 V	1.9			V
			V_{CC} = 4.5 V	4.4			
			V_{CC} = 6 V	5.9			
		I_{OH} = –4 mA, V_{CC} = 4.5 V		3.7			
		I_{OH} = –5.2 mA, V_{CC} = 6 V		5.2			
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	V_{CC} = 2 V			0.1	V
			V_{CC} = 4.5 V			0.1	
			V_{CC} = 6 V			0.1	
		I_{OL} = 4 mA, V_{CC} = 4.5 V				0.4	
		I_{OL} = 5.2 mA, V_{CC} = V				0.4	
I_I	$V_I = V_{CC}$ or 0, V_{CC} = 6 V					±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0, V_{CC} = 6 V					160	µA
C_i	V_{CC} = 2 V to 6 V					10	pF

6.7 Electrical Characteristics – SN74HC273

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -20$ µA	$V_{CC} = 2$ V	1.9			V
			$V_{CC} = 4.5$ V	4.4			
			$V_{CC} = 6$ V	5.9			
		$I_{OH} = -4$ mA, $V_{CC} = 4.5$ V		3.84			
		$I_{OH} = -5.2$ mA, $V_{CC} = 6$ V		5.34			
V_{OL}	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 20$ µA	$V_{CC} = 2$ V			0.1	V
			$V_{CC} = 4.5$ V			0.1	
			$V_{CC} = 6$ V			0.1	
		$I_{OL} = 4$ mA, $V_{CC} = 4.5$ V				0.33	
		$I_{OL} = 5.2$ mA, $V_{CC} = 6$ V				0.33	
I_I	$V_I = V_{CC}$ or 0, $V_{CC} = 6$ V					±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$, $V_{CC} = 6$ V					80	µA
C_i	$V_{CC} = 2$ V to 6 V					10	pF

6.8 Timing Requirements

$T_A = 25°C$ (unless otherwise noted)

				MIN	MAX	UNIT
f_{clock}	Clock frequency		$V_{CC} = 2$ V		5	MHz
			$V_{CC} = 4.5$ V		27	
			$V_{CC} = 6$ V		32	
t_w	Pulse duration	$\overline{CLR}$ low	$V_{CC} = 2$ V	80		ns
			$V_{CC} = 4.5$ V	16		
			$V_{CC} = 6$ V	14		
		CLK high or low	$V_{CC} = 2$ V	80		
			$V_{CC} = 4.5$ V	16		
			$V_{CC} = 6$ V	14		
t_{su}	Setup time before CLK↑	Data	$V_{CC} = 2$ V	100		ns
			$V_{CC} = 4.5$ V	20		
			$V_{CC} = 6$ V	17		
		$\overline{CLR}$ inactive	$V_{CC} = 2$ V	100		
			$V_{CC} = 4.5$ V	20		
			$V_{CC} = 6$ V	17		
t_h	Hold time, data after CLK↑		$V_{CC} = 2$ V	0		ns
			$V_{CC} = 4.5$ V	0		
			$V_{CC} = 6$ V	0		

6.9 Timing Requirements – SN54HC273

over recommended operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
f_{clock}	Clock frequency		V_{CC} = 2 V		4	MHz
			V_{CC} = 4.5 V		18	
			V_{CC} = 6 V		21	
t_w	Pulse duration	$\overline{CLR}$ low	V_{CC} = 2 V	120		ns
			V_{CC} = 4.5 V	24		
			V_{CC} = 6 V	20		
		CLK high or low	V_{CC} = 2 V	120		
			V_{CC} = 4.5 V	24		
			V_{CC} = 6 V	20		
t_{su}	Setup time before CLK↑	Data	V_{CC} = 2 V	150		ns
			V_{CC} = 4.5 V	30		
			V_{CC} = 6 V	25		
		$\overline{CLR}$ inactive	V_{CC} = 2 V	150		
			V_{CC} = 4.5 V	30		
			V_{CC} = 6 V	25		
t_h	Hold time, data after CLK↑		V_{CC} = 2 V	0		ns
			V_{CC} = 4.5 V	0		
			V_{CC} = 6 V	0		

6.10 Timing Requirements – SN74HC273

over recommended operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
f_{clock}	Clock frequency		V_{CC} = 2 V		4	MHz
			V_{CC} = 4.5 V		21	
			V_{CC} = 6 V		25	
t_w	Pulse duration	$\overline{CLR}$ low	V_{CC} = 2 V	100		ns
			V_{CC} = 4.5 V	20		
			V_{CC} = 6 V	17		
		CLK high or low	V_{CC} = 2 V	100		
			V_{CC} = 4.5 V	20		
			V_{CC} = 6 V	17		
t_{su}	Setup time before CLK↑	Data	V_{CC} = 2 V	125		ns
			V_{CC} = 4.5 V	25		
			V_{CC} = 6 V	21		
		$\overline{CLR}$ inactive	V_{CC} = 2 V	125		
			V_{CC} = 4.5 V	25		
			V_{CC} = 6 V	21		
t_h	Hold time, data after CLK↑		V_{CC} = 2 V	0		ns
			V_{CC} = 4.5 V	0		
			V_{CC} = 6 V	0		

6.11 Switching Characteristics

T_A = 25°C and C_L = 50 pF (unless otherwise noted; see Figure 2)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}		V_{CC} = 2 V	5	11		MHz
		V_{CC} = 4.5 V	27	50		
		V_{CC} = 6 V	32	60		
t_{PHL}	From $\overline{CLR}$ (input) to any (output)	V_{CC} = 2 V		55	160	ns
		V_{CC} = 4.5 V		15	32	
		V_{CC} = 6 V		12	27	
t_{pd}	From CLK (input) to any (output)	V_{CC} = 2 V		56	160	ns
		V_{CC} = 4.5 V		15	32	
		V_{CC} = 6 V		13	27	
t_t	To any (output)	V_{CC} = 2 V		38	75	ns
		V_{CC} = 4.5 V		8	15	
		V_{CC} = 6 V		6	13	

6.12 Switching Characteristics – SN54HC273

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted; see Figure 2)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
f_{max}		V_{CC} = 2 V	4		MHz
		V_{CC} = 4.5 V	18		
		V_{CC} = 6 V	21		
t_{PHL}	From $\overline{CLR}$ (input) to any (output)	V_{CC} = 2 V		240	ns
		V_{CC} = 4.5 V		48	
		V_{CC} = 6 V		41	
t_{pd}	From CLK (input) to any (output)	V_{CC} = 2 V		240	ns
		V_{CC} = 4.5 V		48	
		V_{CC} = 6 V		41	
t_t	To any (output)	V_{CC} = 2 V		110	ns
		V_{CC} = 4.5 V		22	
		V_{CC} = 6 V		19	

6.13 Switching Characteristics – SN74HC273

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted; see Figure 2)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
f_{max}		V_{CC} = 2 V	4		MHz
		V_{CC} = 4.5 V	21		
		V_{CC} = 6 V	25		
t_{PHL}	From $\overline{CLR}$ (input) to any (output)	V_{CC} = 2 V		200	ns
		V_{CC} = 4.5 V		40	
		V_{CC} = 6 V		34	
t_{pd}	From CLK (input) to any (output)	V_{CC} = 2 V		200	ns
		V_{CC} = 4.5 V		40	
		V_{CC} = 6 V		34	
t_t	To any (output)	V_{CC} = 2 V		95	ns
		V_{CC} = 4.5 V		19	
		V_{CC} = 6 V		16	

6.14 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	No load	35	pF

6.15 Typical Characteristics

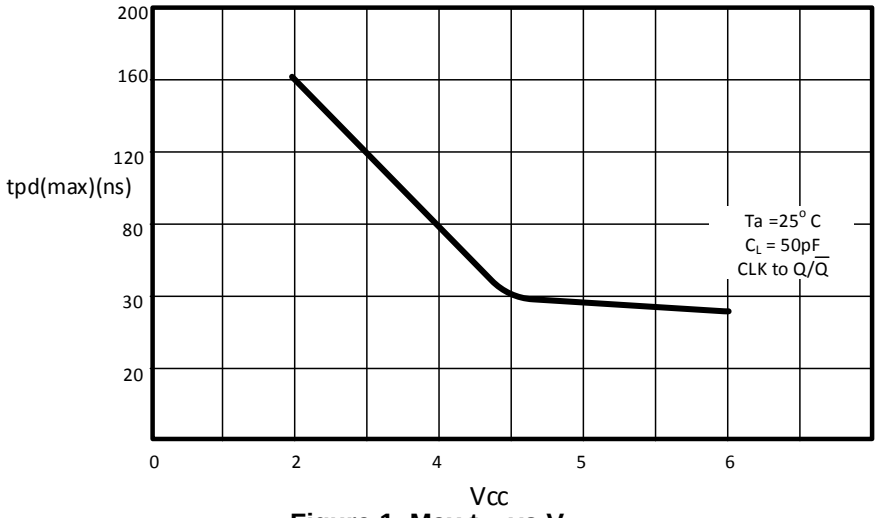
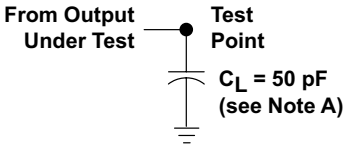
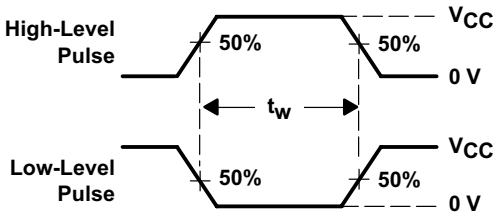


Figure 1. Max t_{pd} vs V_{CC}

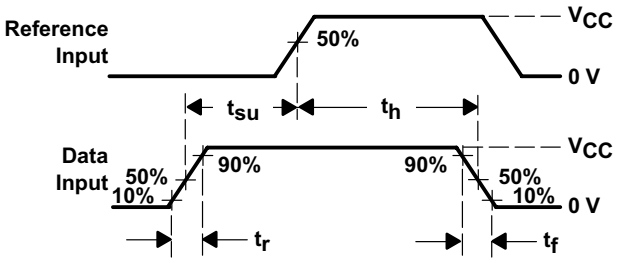
7 Parameter Measurement Information



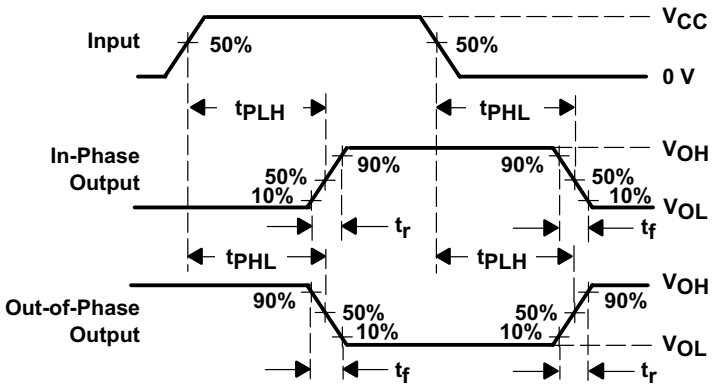
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

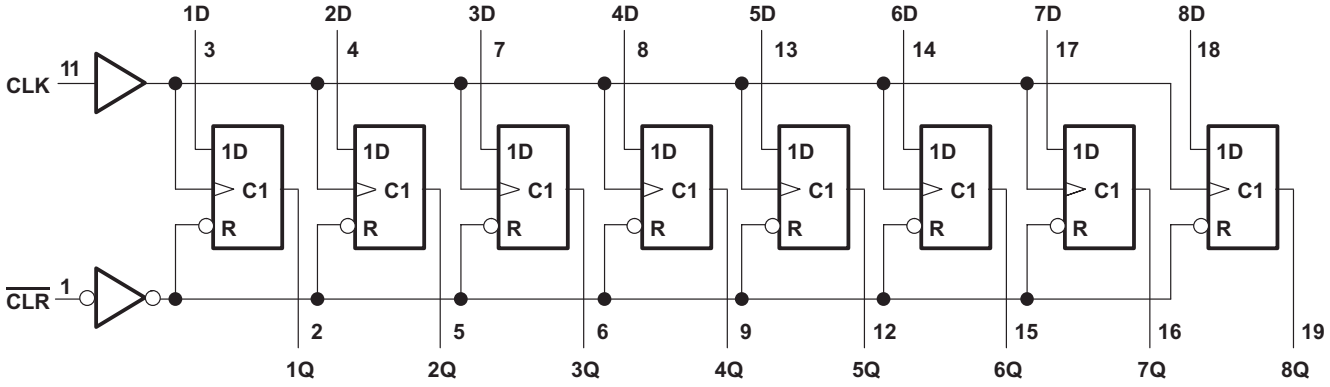
Figure 2. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SNx4HC273 contains eight flip-flops with single-rail outputs with individual data input to each flip-flop. The outputs can drive up to 10 LSTTL loads. The device has direct active low clear input.

8.2 Functional Block Diagram



8.3 Feature Description

The SNx4HC273 has low power consumption with a maximum $_{CC}$ of 80 µA.

The typical t_{pd} for the SNx4HC273 is 12 ns and the output drive is ±4 mA at 5 V.

The SNx4HC273 also has very low input current, with the maximum set at 1 µA.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SNx4HC273.

Table 1. Function Table (Each Flip-Flop)

INPUTS			OUTPUT Q
$\overline{CLR}$	CLK	D	
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

9 Application and Implementation

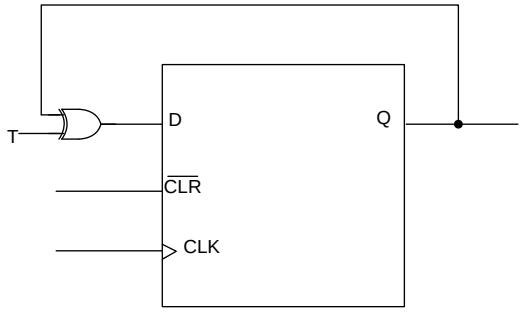
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SNx4HC273 is octal D Flip flop with active low clear input. It has low input current and low power consumption. The D flip-flop can be used as a Toggle flip flop using an XOR gate at the input. The output toggles from the previous state whenever the T input is high.

9.2 Typical Application



9.2.1 Design Requirements

This SNx4Hc273 device uses CMOS technology and has balanced output drive.

9.2.2 Detailed Design Procedure

1. Recommended input conditions:
   - Rise time and fall time specifications: see ($\Delta t/\Delta V$) in *Recommended Operating Conditions*.
   - Specified high and low levels: see (V_{IH} and V_{IL}) in *Recommended Operating Conditions*.
   - Inputs are not overvoltage tolerant and must not be above any valid V_{CC} as per *Recommended Operating Conditions*.
2. Absolute maximum output conditions:
   - Continuos output currents must not exceed (I_O max) per output and must not exceed total current (continuous current through V_{CC} or GND) for the part. These limits are located in the *Absolute Maximum Ratings*.
   - Outputs must not be pulled above V_{CC}.

Typical Application (continued)

9.2.3 Application Curve

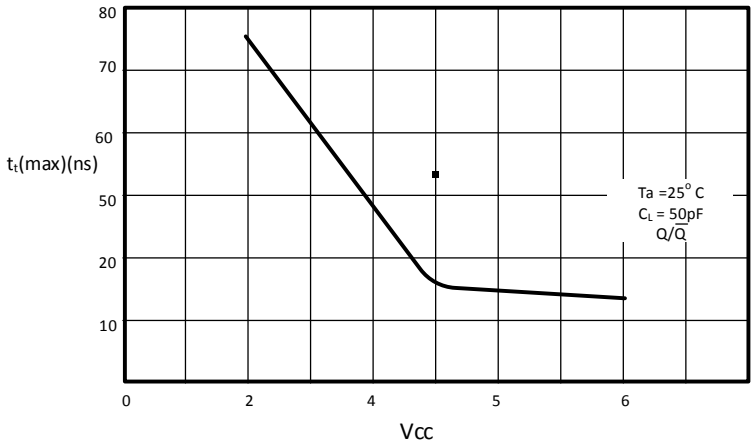


Figure 3. Max Transition Time vs V_{CC}

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions*.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF capacitor. If there are multiple V_{CC} pins, TI recommends a 0.01-µF or 0.022-µF capacitor for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs must not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances:

- All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating.
- The logic level that must be applied to any particular unused input depends on the function of the device.
- Generally they are tied to GND or V_{CC} whichever make more sense or is more convenient.

11.2 Layout Example

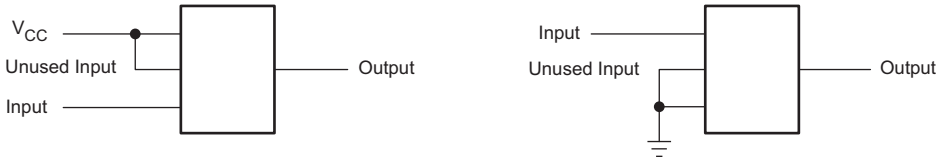


Figure 4. SNx4HC273 Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54HC273	Click here	Click here	Click here	Click here	Click here
SN74HC273	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8409901VRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8409901VR A SNV54HC273J	Samples
5962-8409901VSA	ACTIVE	CFP	W	20	25	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8409901VS A SNV54HC273W	Samples
84099012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84099012A SNJ54HC 273FK	Samples
8409901RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8409901RA SNJ54HC273J	Samples
8409901SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8409901SA SNJ54HC273W	Samples
JM38510/65601BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 65601BRA	Samples
JM38510/65601BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 65601BSA	Samples
M38510/65601BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 65601BRA	Samples
M38510/65601BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 65601BSA	Samples
SN54HC273J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54HC273J	Samples
SN74HC273DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC273	Samples
SN74HC273DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC273	Samples
SN74HC273DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	HC273	Samples
SN74HC273DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC273	Samples
SN74HC273DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC273	Samples
SN74HC273N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC273N	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC273NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC273N	Samples
SN74HC273NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC273	Samples
SN74HC273PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC273	Samples
SN74HC273PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC273	Samples
SN74HC273PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC273	Samples
SN74HC273PWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC273	Samples
SNJ54HC273FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84099012A SNJ54HC 273FK	Samples
SNJ54HC273J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8409901RA SNJ54HC273J	Samples
SNJ54HC273W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8409901SA SNJ54HC273W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54HC273, SN54HC273-SP, SN74HC273 :

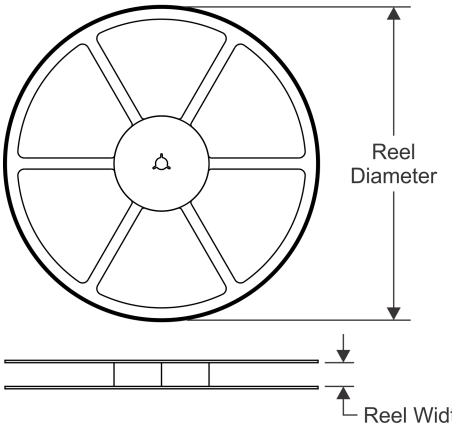
- Catalog: SN74HC273, SN54HC273
- Automotive: SN74HC273-Q1, SN74HC273-Q1
- Military: SN54HC273
- Space: SN54HC273-SP

NOTE: Qualified Version Definitions:

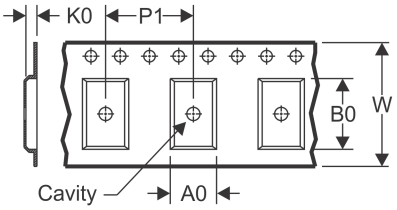
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

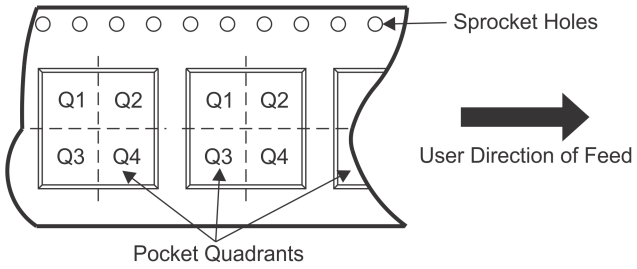


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

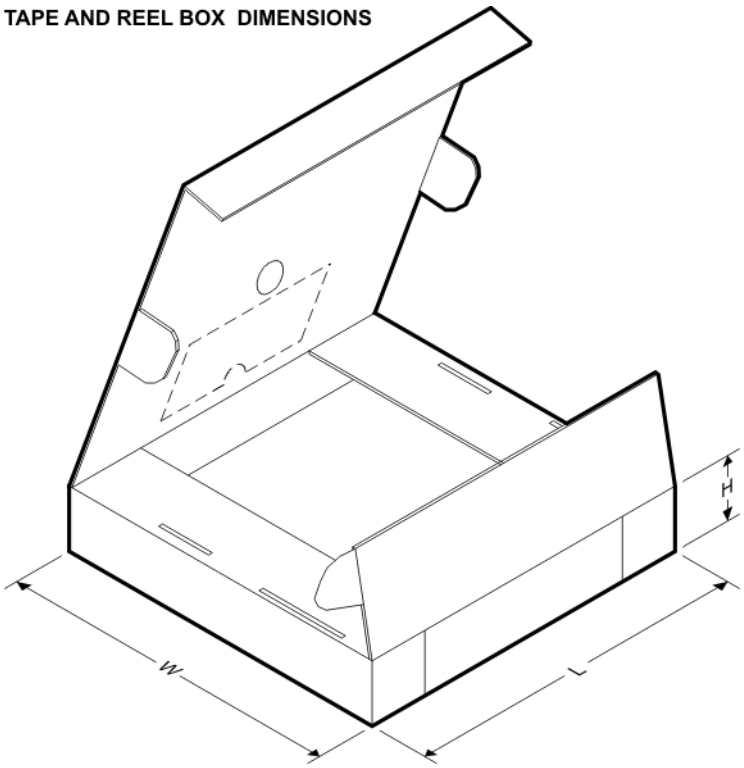
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC273DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74HC273DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74HC273DWRG4	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74HC273NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74HC273PWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

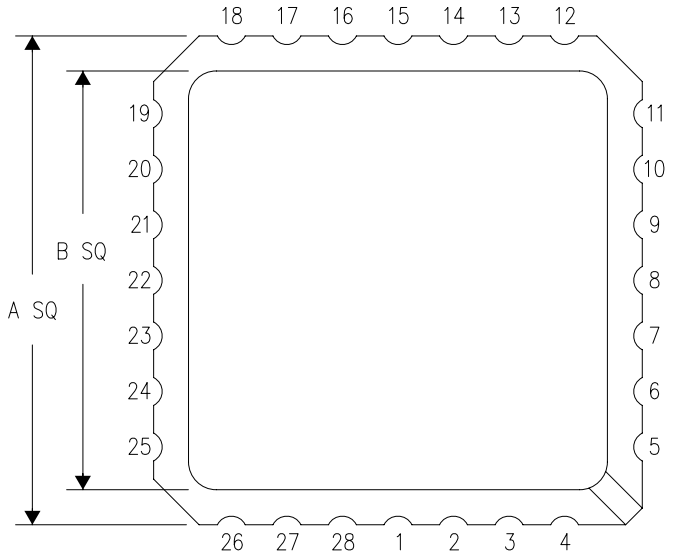


*All dimensions are nominal

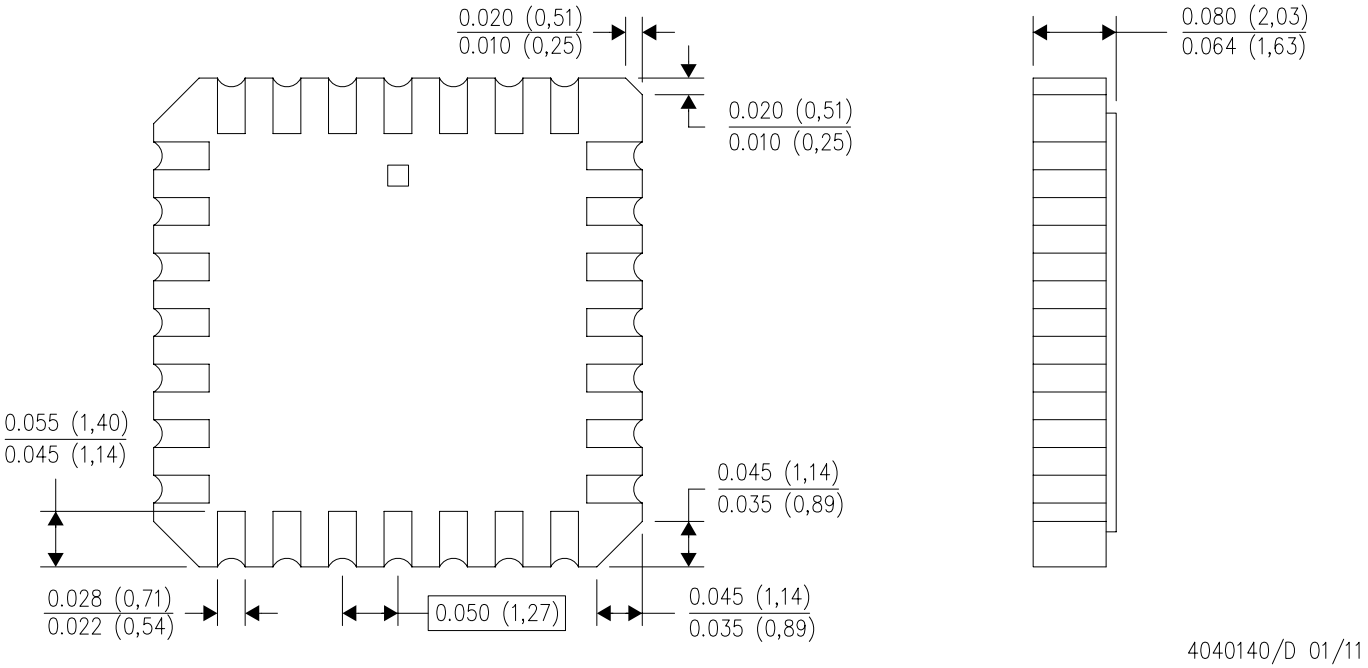
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC273DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74HC273DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74HC273DWRG4	SOIC	DW	20	2000	367.0	367.0	45.0
SN74HC273NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74HC273PWT	TSSOP	PW	20	250	367.0	367.0	38.0

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



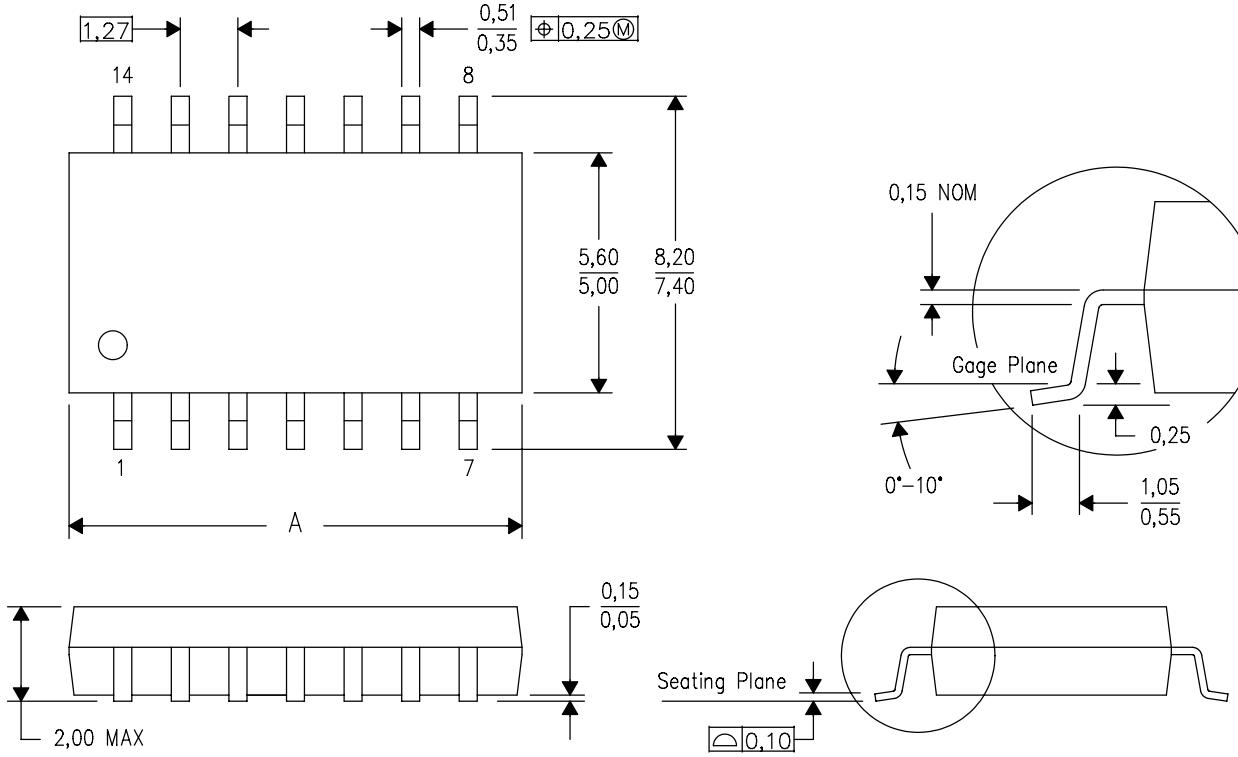
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

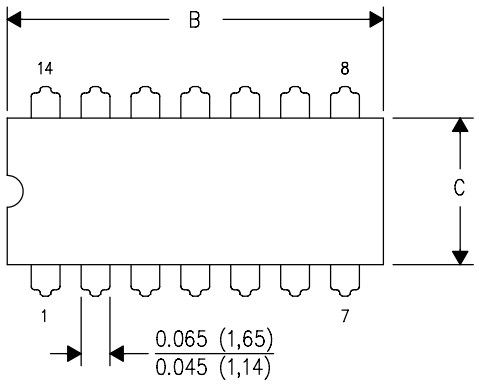
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

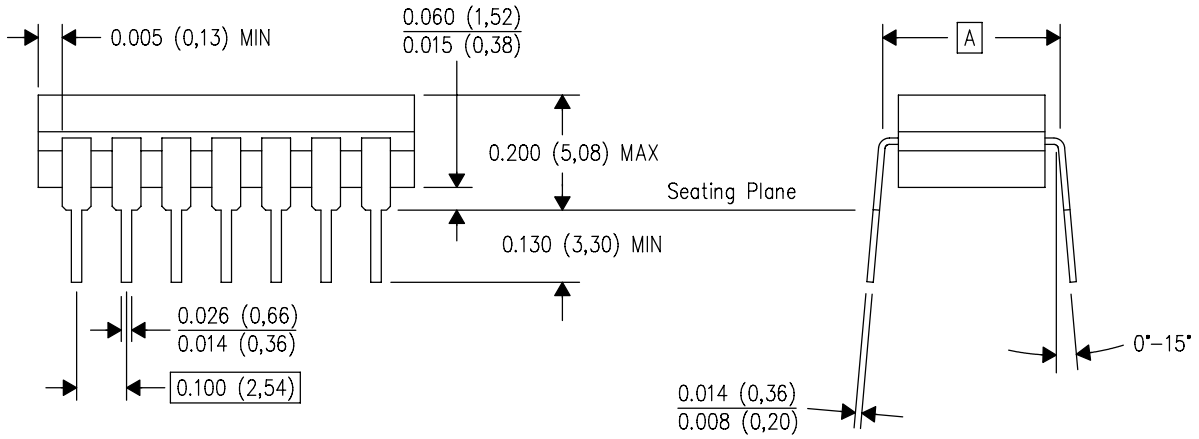
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



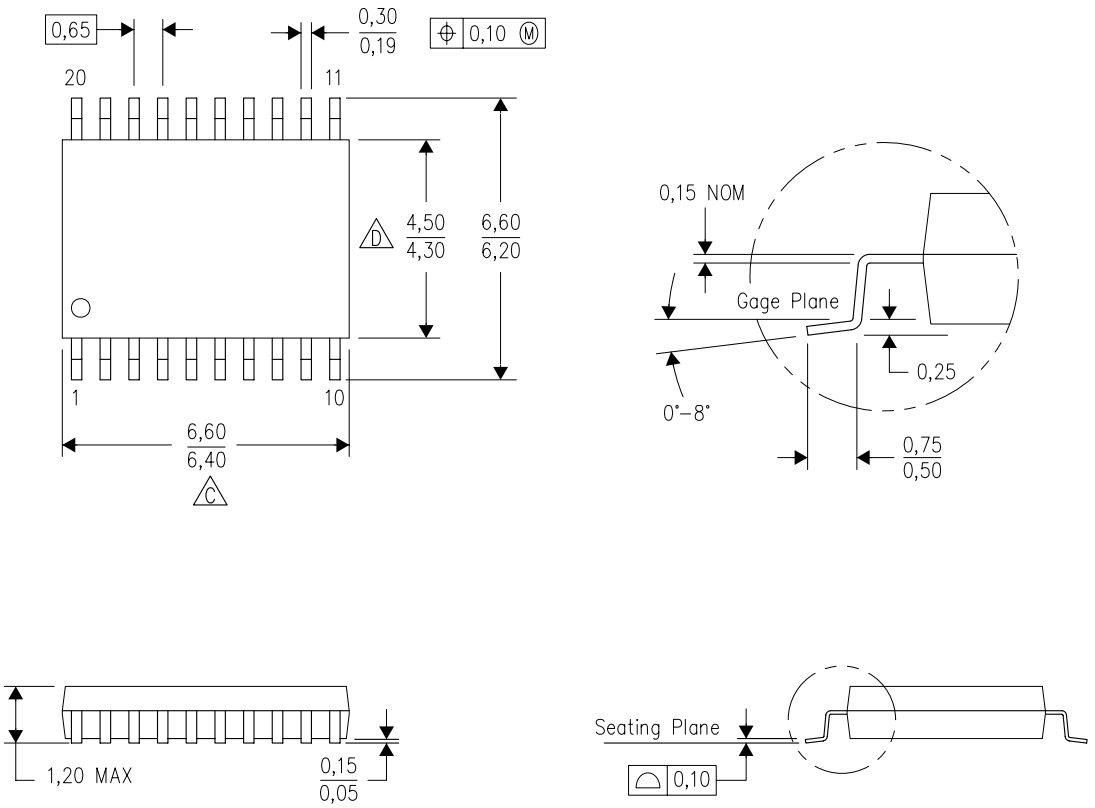
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

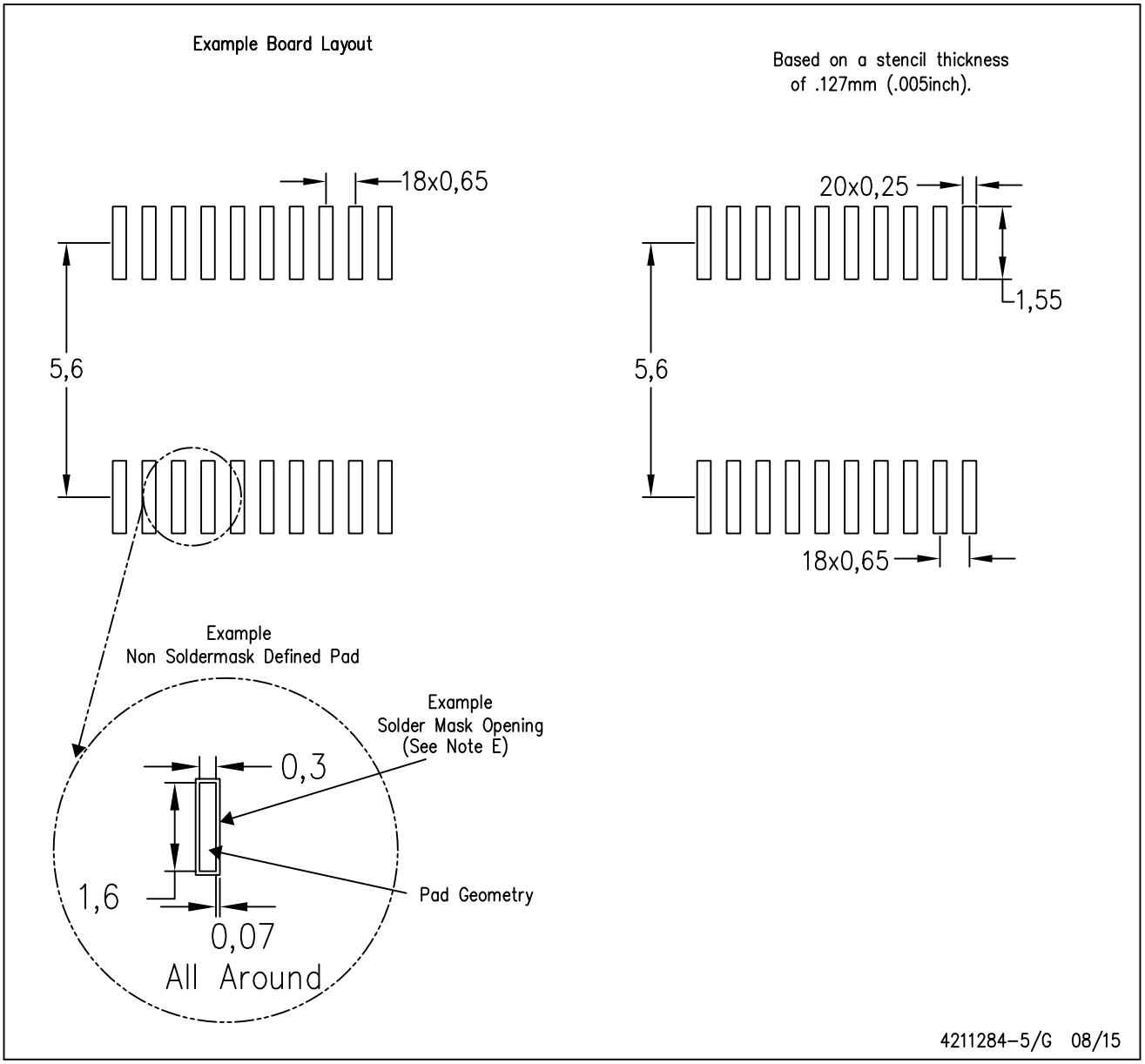
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



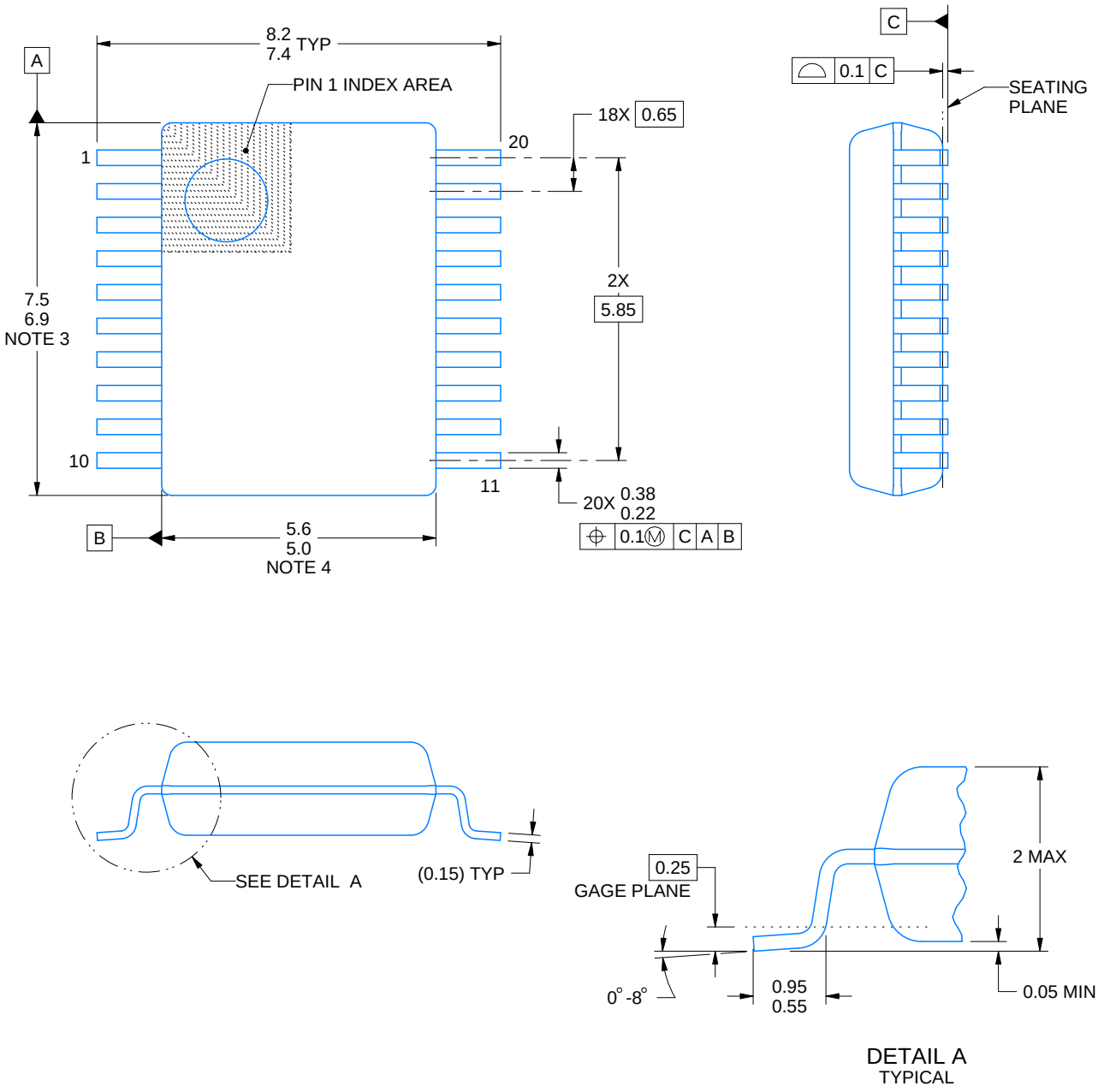
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

DB0020A

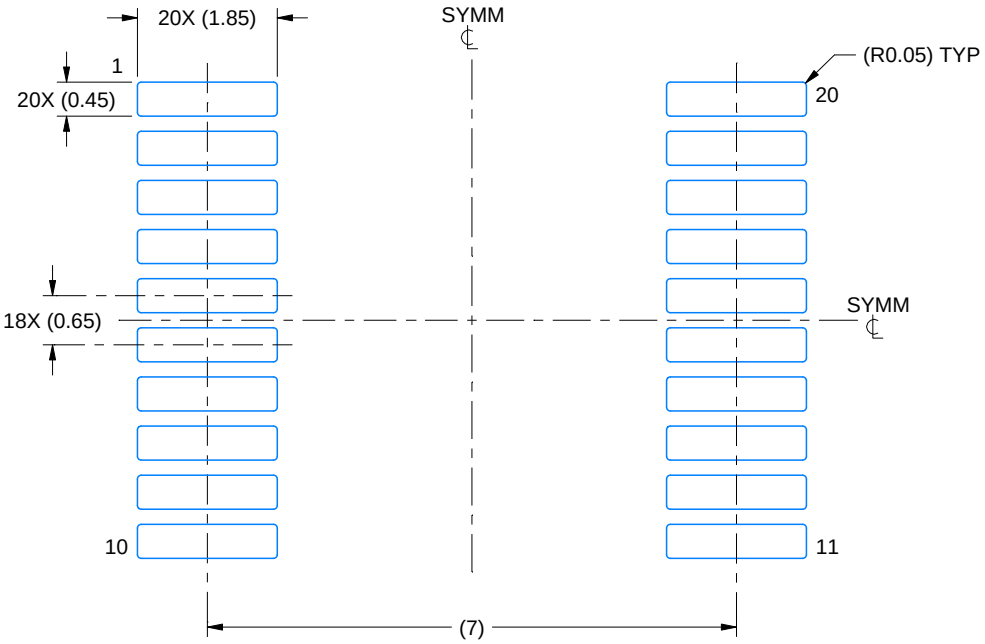
TSSOP - 2 mm max height

SMALL OUTLINE PACKAGE

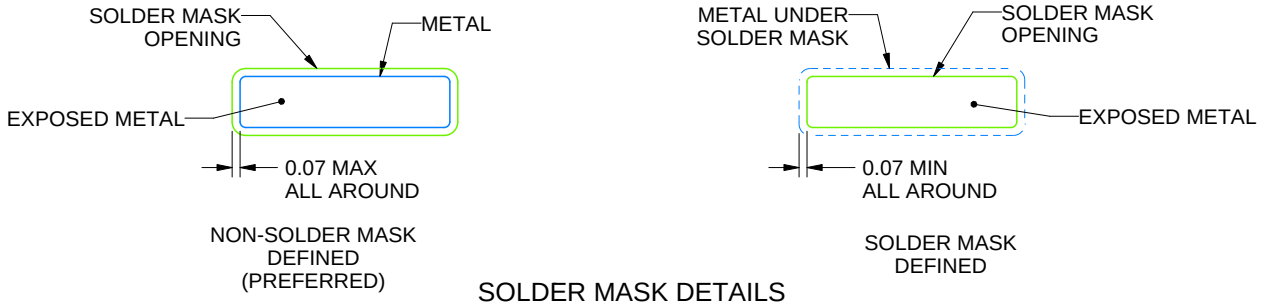


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

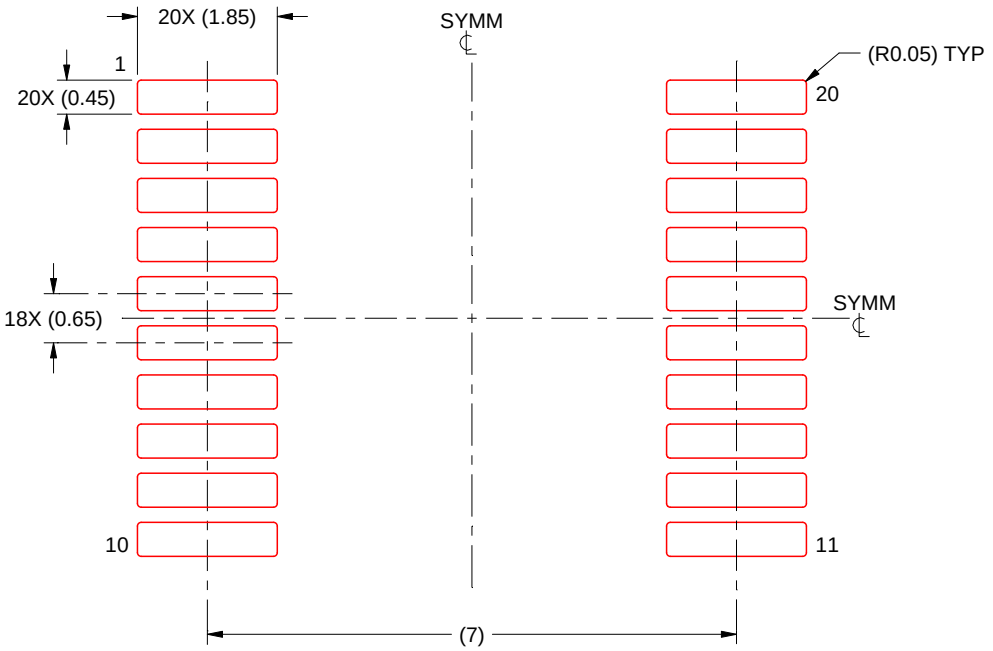


SOLDER MASK DETAILS

4214851/A 12/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/A 12/2017

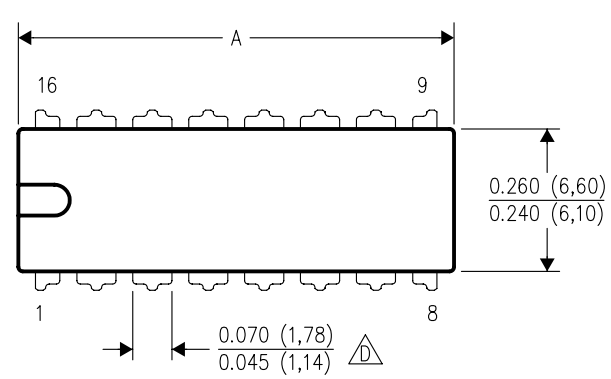
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

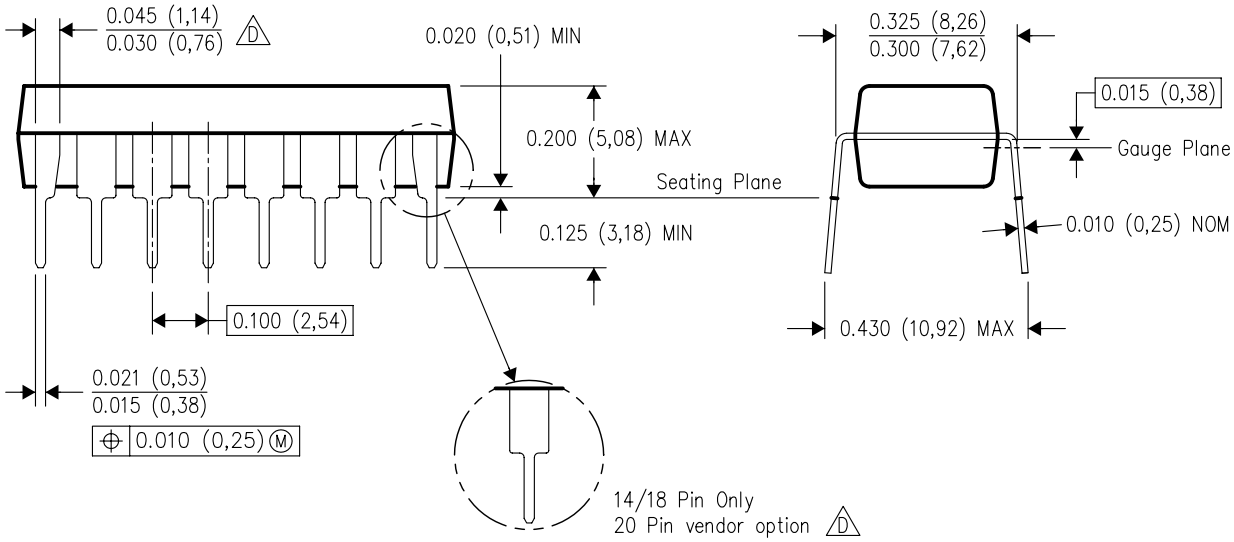
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

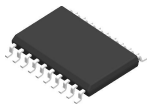


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

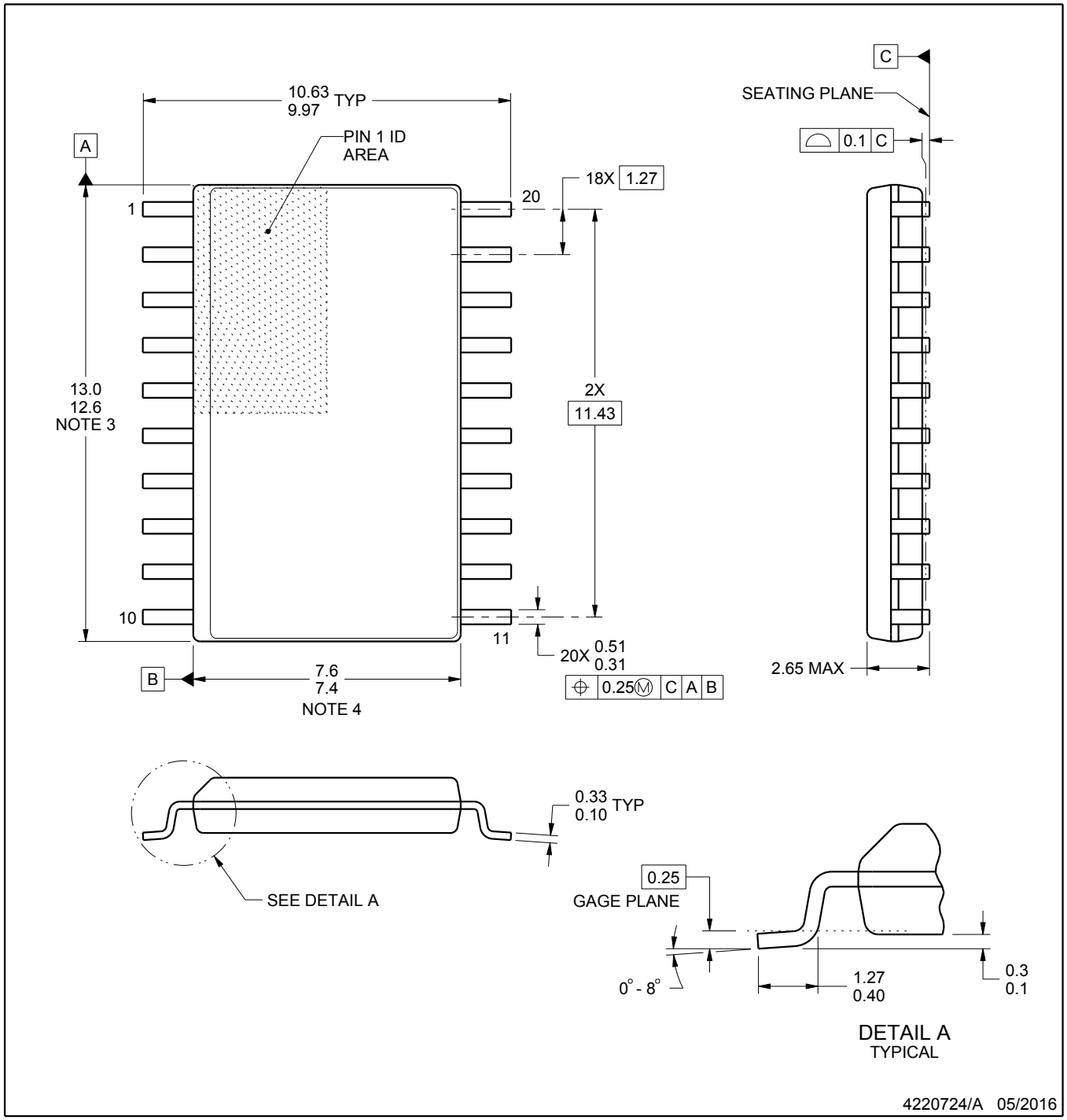


PACKAGE OUTLINE

DW0020A

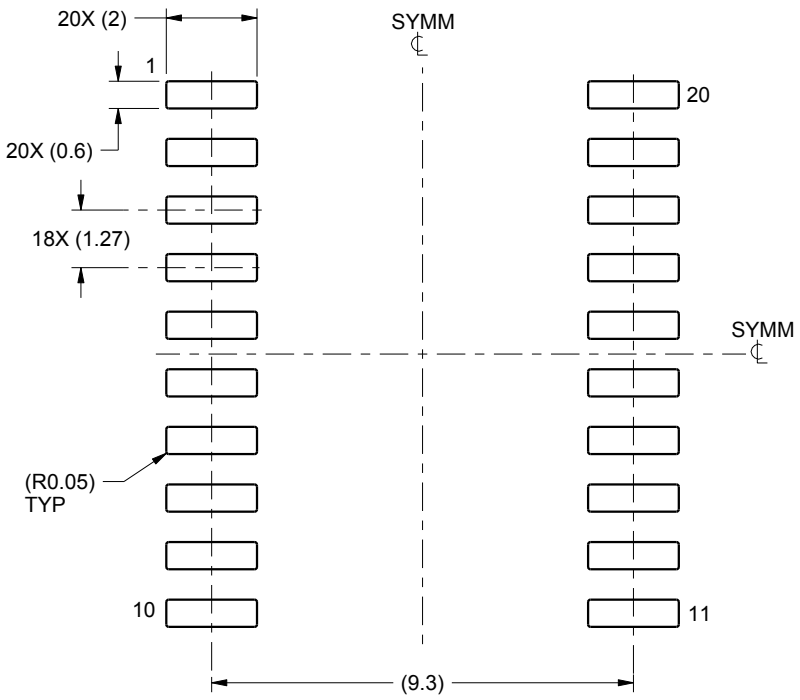
SOIC - 2.65 mm max height

SOIC

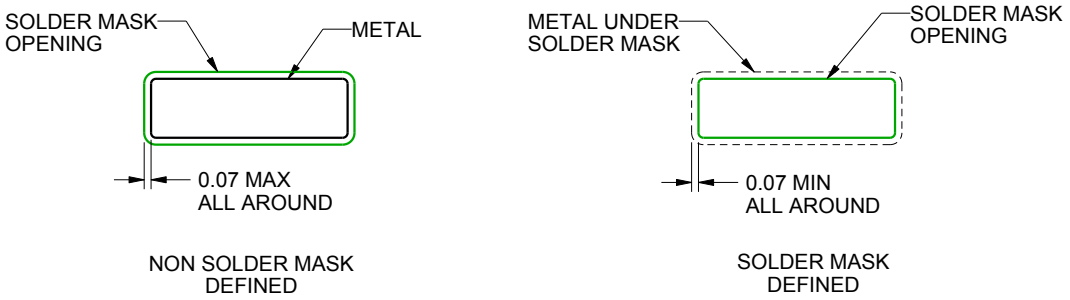


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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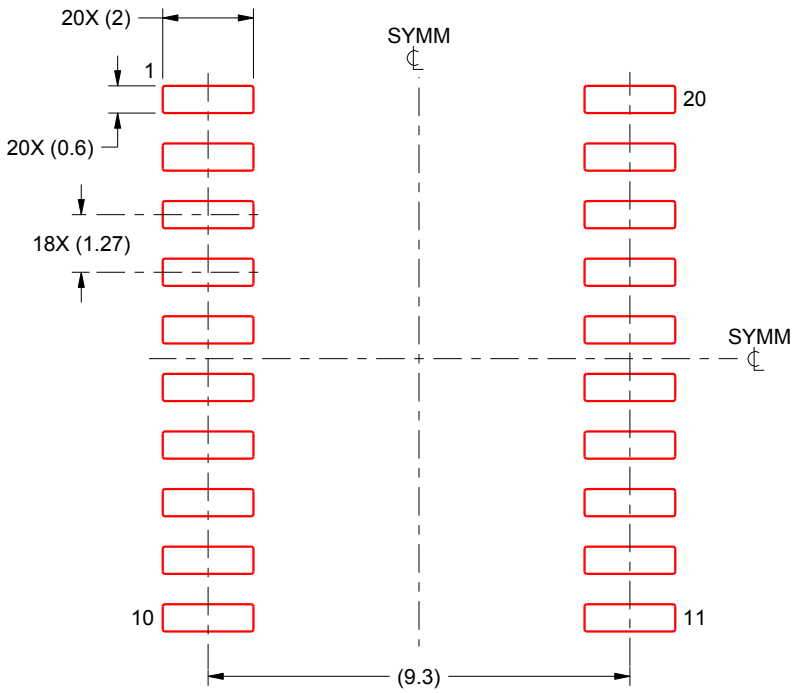
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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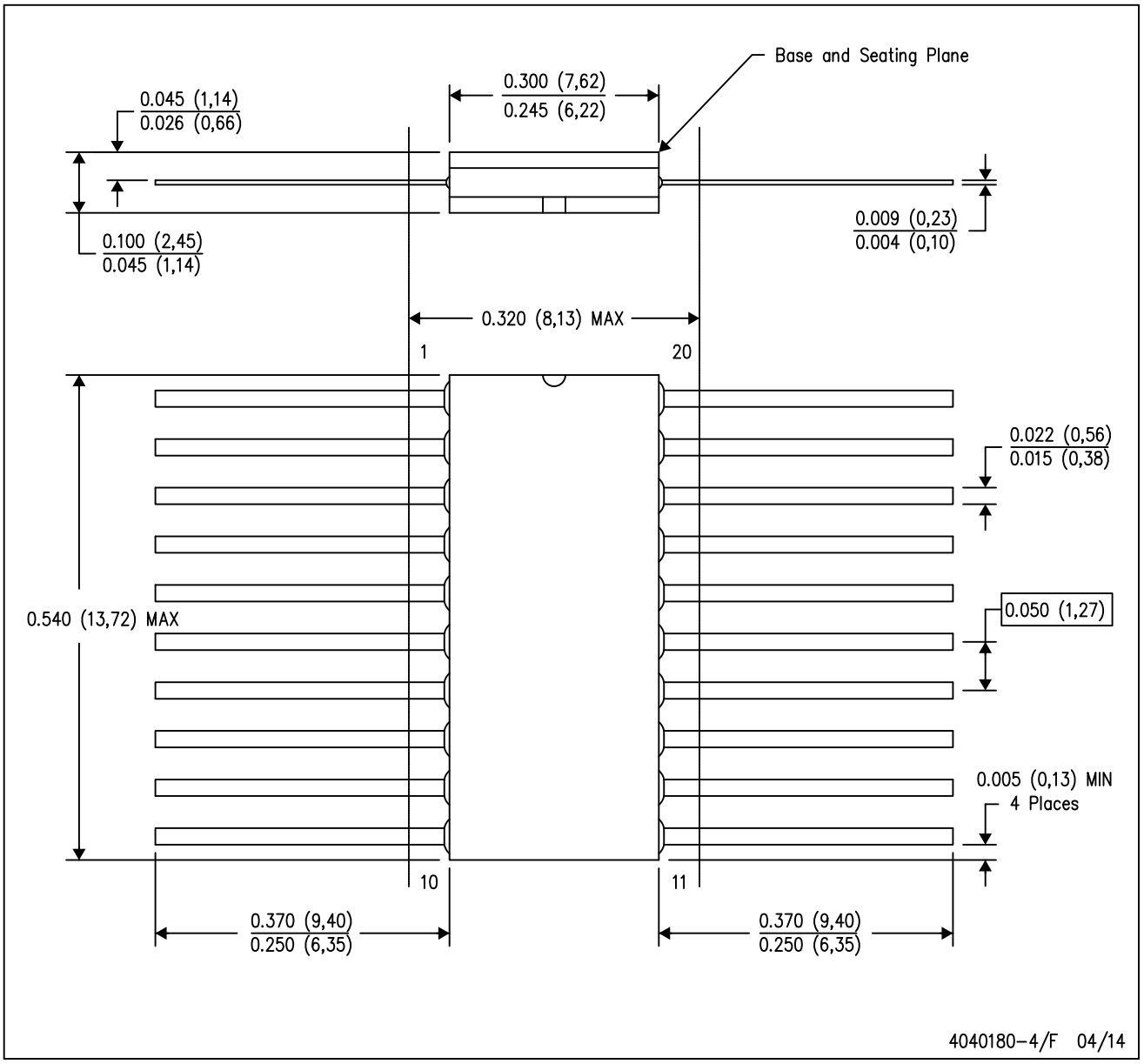
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

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