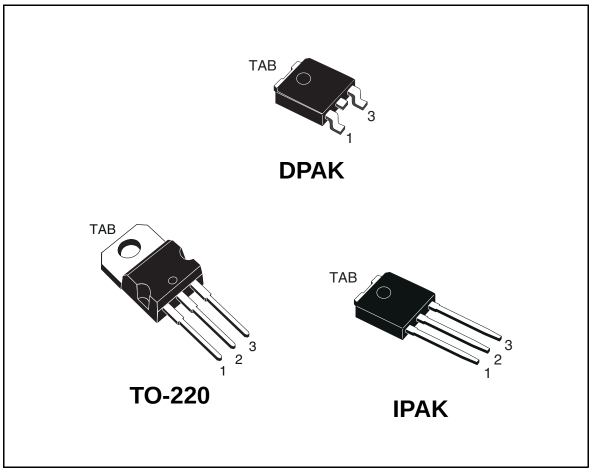
STD5N60M2, STP5N60M2, STU5N60M2

N-channel 600 V, 1.26 Ω typ., 3.5 A MDmesh II Plus™ low Qg Power MOSFETs in DPAK, TO-220 and IPAK packages

Datasheet - production data



Features

Order codes	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STD5N60M2	650 V	1.4 Ω	3.5 A
STP5N60M2			
STU5N60M2			

- Extremely low gate charge
- Lower $R_{DS(on)}$ x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using a new generation of MDmesh™ technology: MDmesh II Plus™ low Qg. These revolutionary Power MOSFETs associate a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. They are therefore suitable for the most demanding high efficiency converters.

Figure 1. Internal schematic diagram

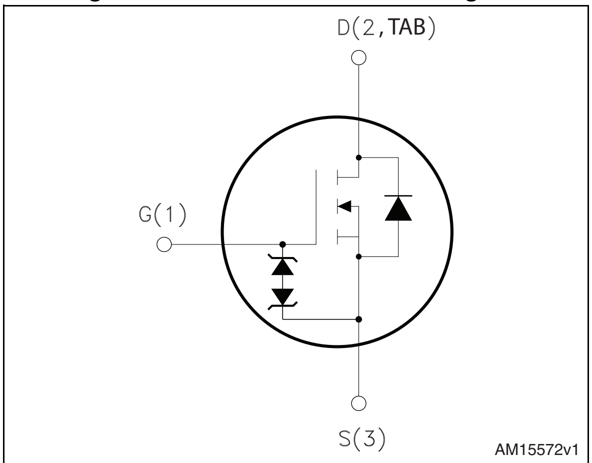


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD5N60M2	5N60M2	DPAK	Tape and reel
STP5N60M2		TO-220	Tube
STU5N60M2		IPAK	

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	3.5	A
I_D	Drain current (continuous) at T_C = 100 °C	2.2	A
I_{DM} (1)	Drain current (pulsed)	14	A
P_{TOT}	Total dissipation at T_C = 25 °C	45	W
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	

1. Pulse width limited by safe operating area..
2. I_{SD} ≤ 3.5 A, di/dt ≤ 400 A/µs; $V_{DS\ peak}$ < $V_{(BR)DSS}$, V_{DD}=400 V
3. V_{DS} ≤ 480 V

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		DPAK	TO-220	IPAK	
$R_{thj-case}$	Thermal resistance junction-case max	2.08			°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb max(1)	50			°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max			100	°C/W

1. When mounted on 1 inch² FR-4, 2 Oz copper board

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	0.5	A
E_{AS}	Single pulse avalanche energy (starting T_j=25°C, I_D= I_{AR}; V_{DD}=50)	80	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 600 V			1	µA
		V_{DS} = 600 V, T_C=125 °C			100	µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 1.7 A		1.3	1.4	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	211	-	pF
C_{oss}	Output capacitance		-	13	-	pF
C_{rss}	Reverse transfer capacitance		-	0.75	-	pF
Coss eq.(1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0	-	19.5	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	6.2	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 3.5 A, V_{GS} = 10 V (see *Figure 19*)	-	8.5	-	nC
Q_{gs}	Gate-source charge		-	1.6	-	nC
Q_{gd}	Gate-drain charge		-	5	-	nC

1. Coss eq. is defined as a constant equivalent capacitance giving the same charging time as Coss when VDS increases from 0 to 80% VDSS

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 1.75 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 18* and *Figure 23*)	-	11.8	-	ns
t_r	Rise time		-	3	-	ns
$t_{d(off)}$	Turn-off delay time		-	70	-	ns
t_f	Fall time		-	15	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		3.5	A
I_{SDM} [1]	Source-drain current (pulsed)		-		14	A
V_{SD} [2]	Forward on voltage	I_{SD} = 3.5 A, V_{GS} = 0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 3.5 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 20*)	-	221		ns
Q_{rr}	Reverse recovery charge		-	1.05		µC
I_{RRM}	Reverse recovery current		-	9.5		A
t_{rr}	Reverse recovery time	I_{SD} = 3.5 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 20*)	-	314		ns
Q_{rr}	Reverse recovery charge		-	1.5		µC
I_{RRM}	Reverse recovery current		-	9.5		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for DPAK

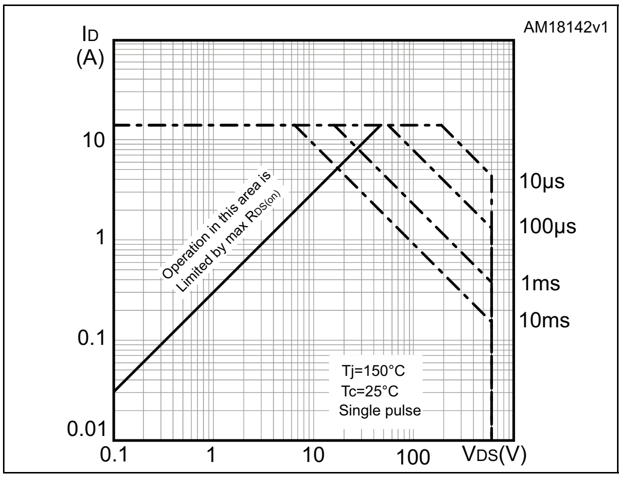


Figure 3. Thermal impedance for DPAK

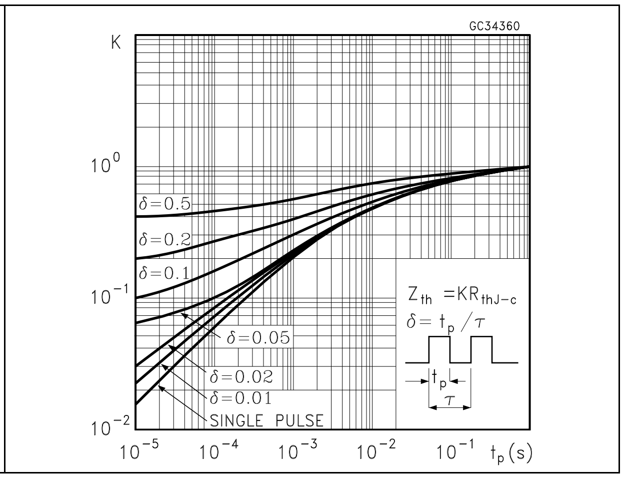


Figure 4. Safe operating area for TO-220

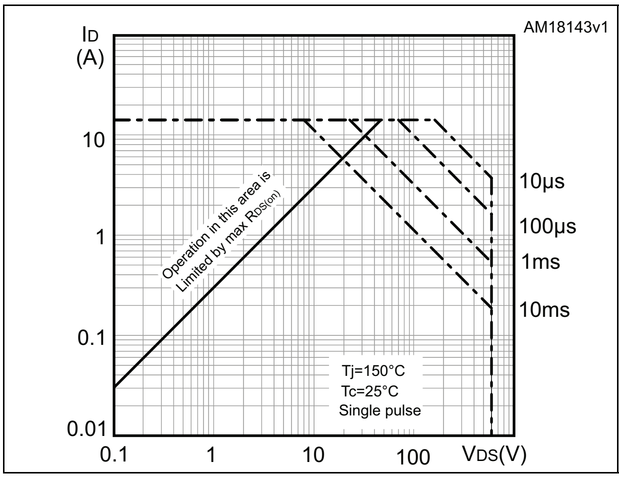


Figure 5. Thermal impedance for TO-220

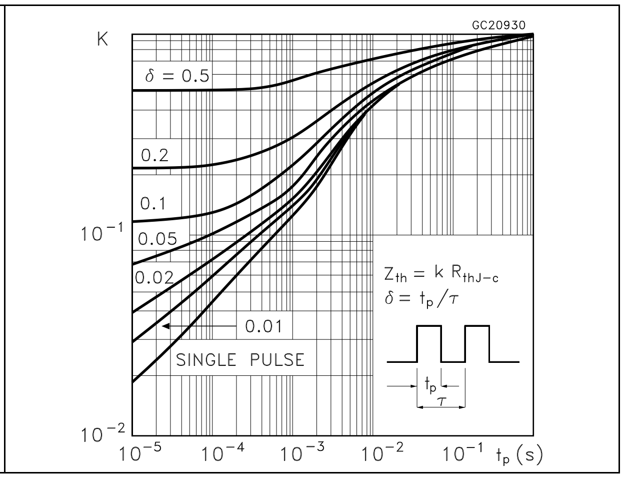


Figure 6. Safe operating area for IPAK

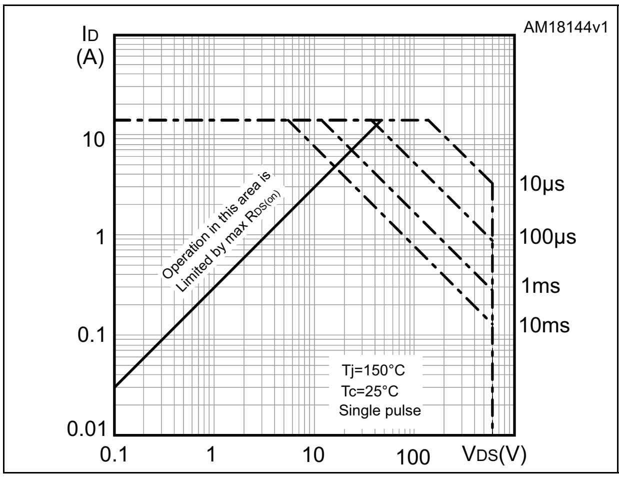


Figure 7. Thermal impedance for IPAK

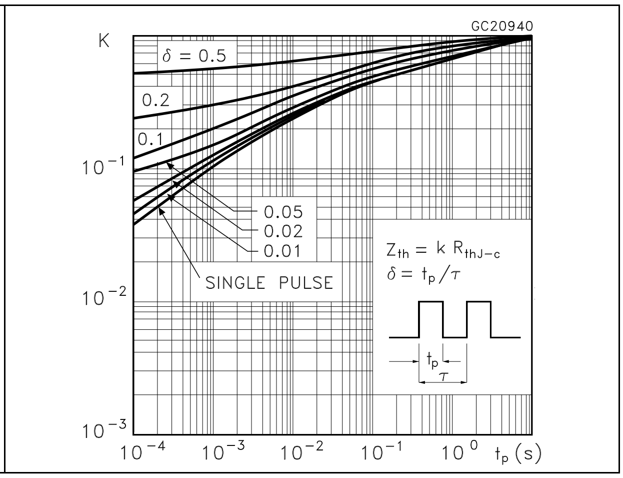


Figure 8. Output characteristics

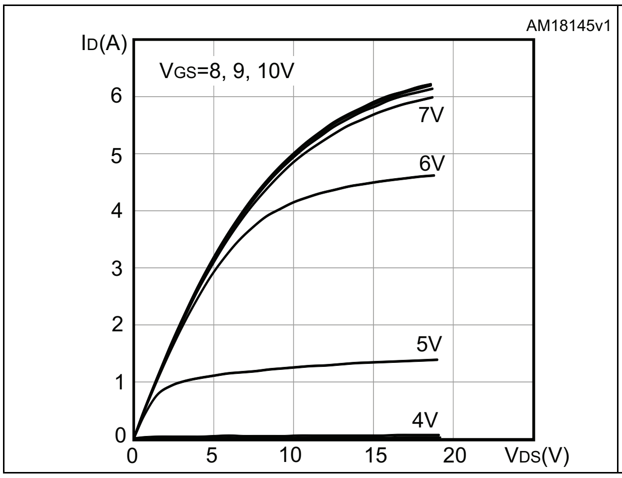


Figure 9. Transfer characteristics

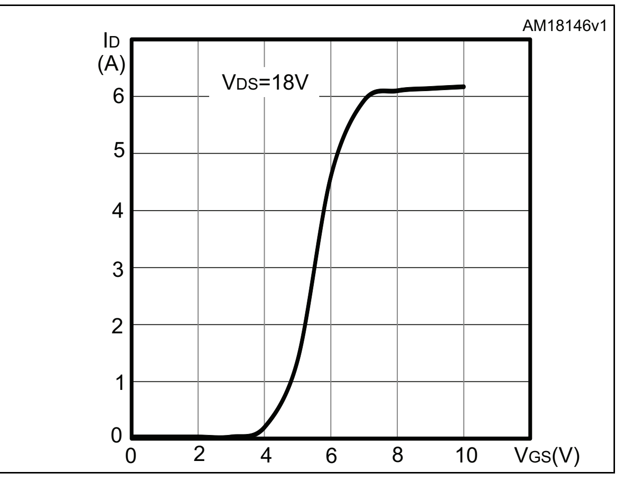


Figure 10. Gate charge vs gate-source voltage

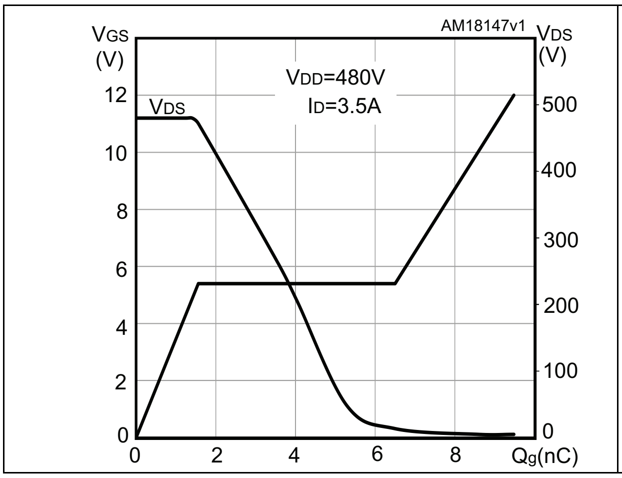


Figure 11. Static drain-source on-resistance

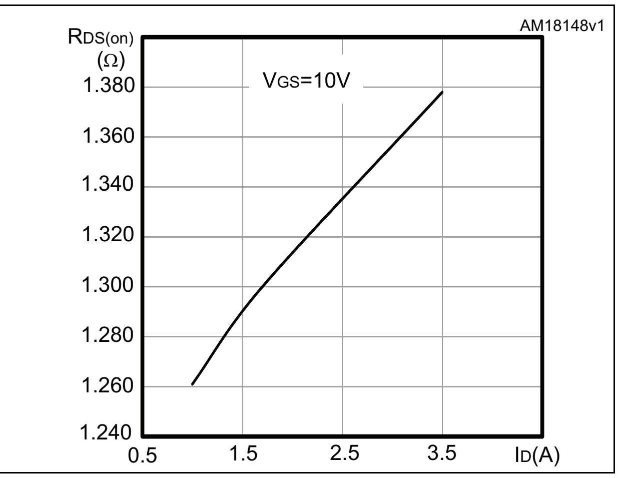


Figure 12. Capacitance variations

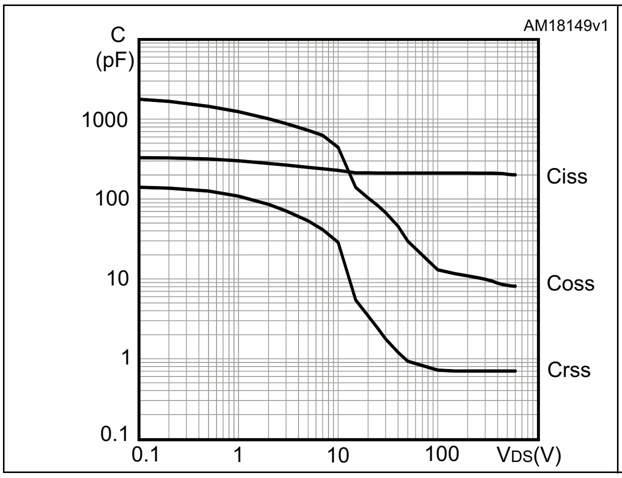


Figure 13. Output capacitance stored energy

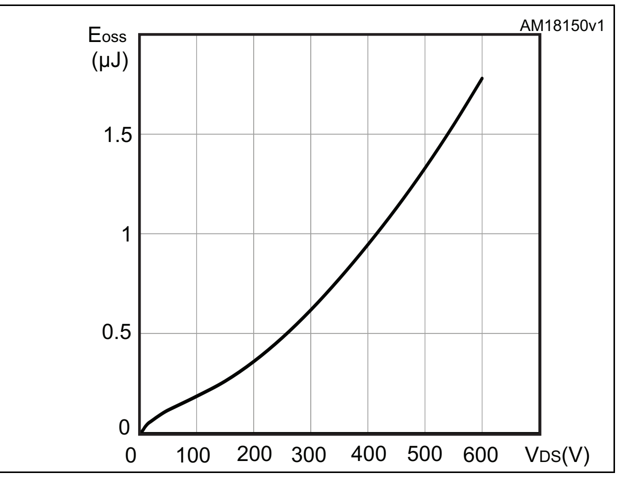


Figure 14. Normalized gate threshold voltage vs temperature

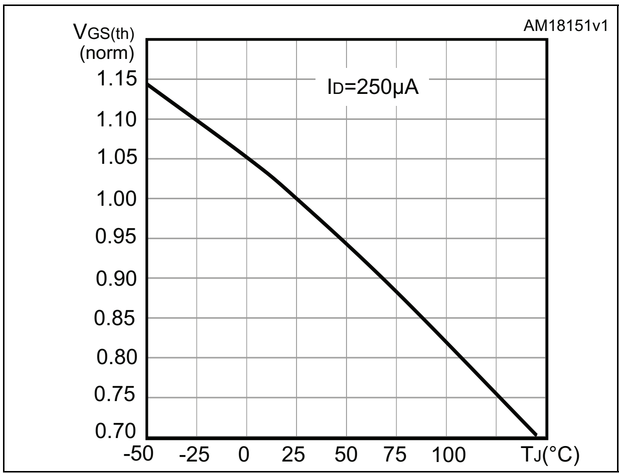


Figure 15. Normalized on-resistance vs temperature

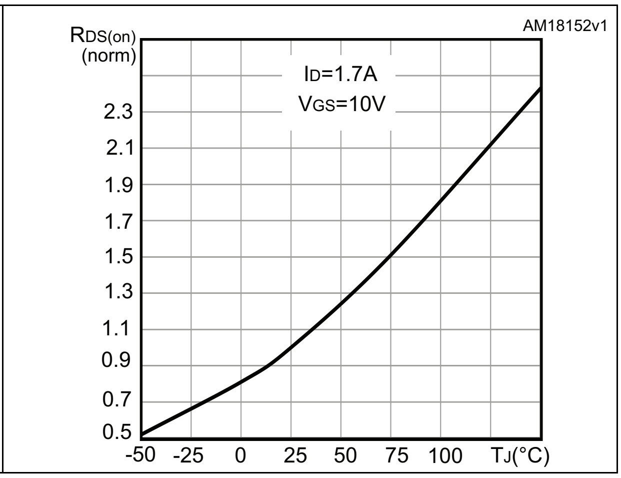


Figure 16. Normalized $V_{(BR)DSS}$ vs temperature

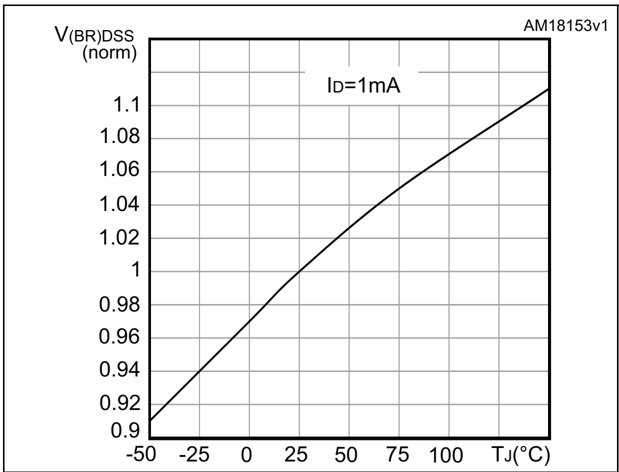
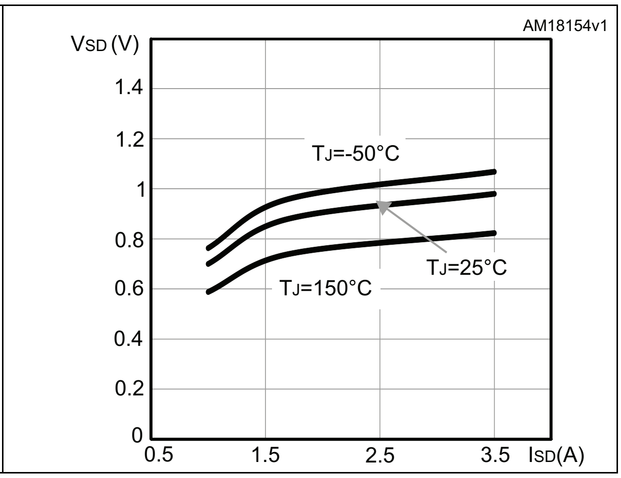


Figure 17. Source-drain diode forward characteristics



3 Test circuits

Figure 18. Switching times test circuit for resistive load

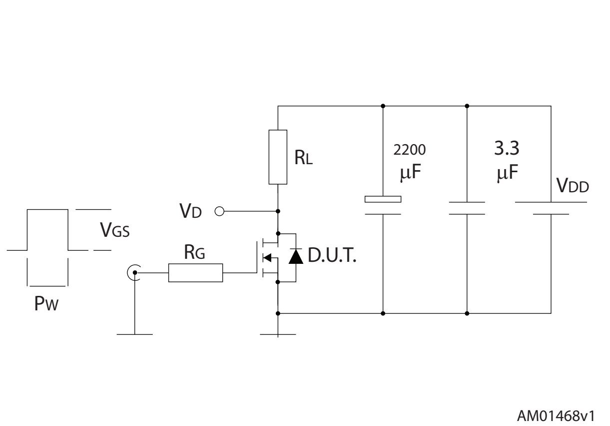


Figure 19. Gate charge test circuit

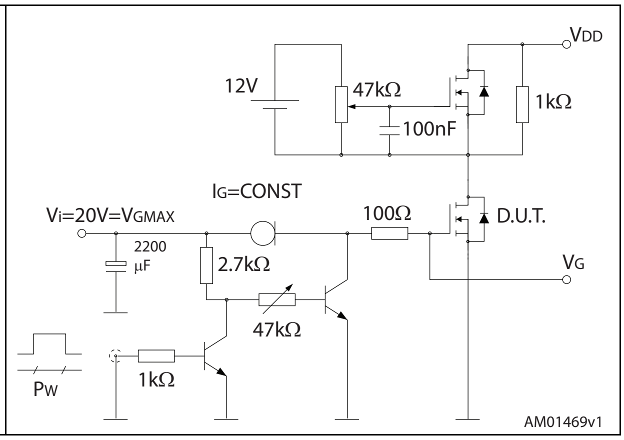


Figure 20. Test circuit for inductive load switching and diode recovery times

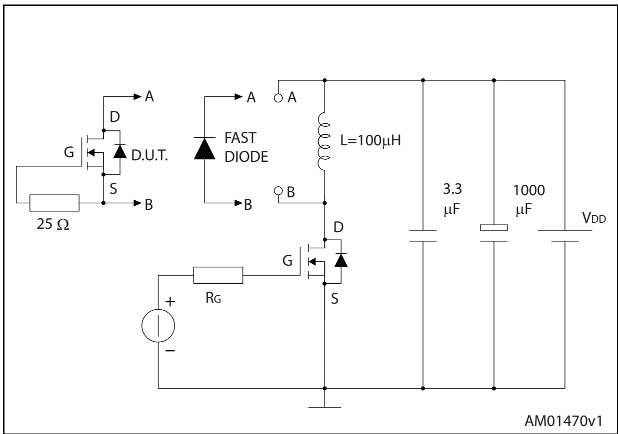


Figure 21. Unclamped inductive load test circuit

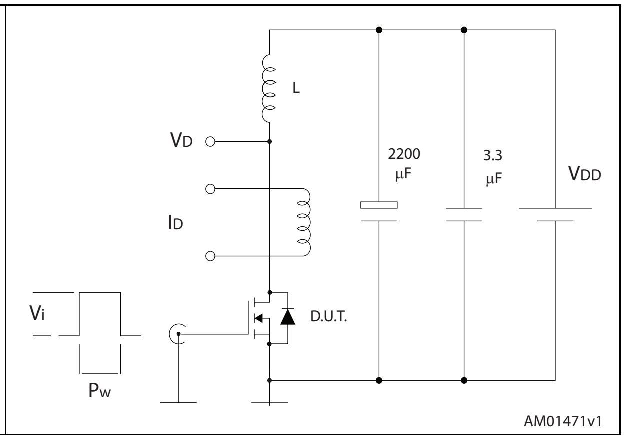


Figure 22. Unclamped inductive waveform

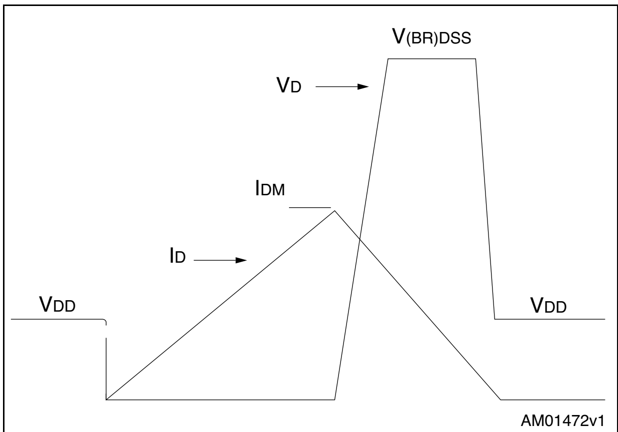
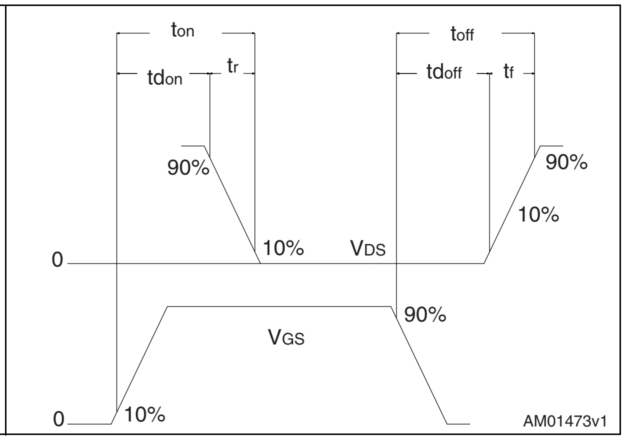


Figure 23. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.1 DPAK, STD5N60M2

Figure 24. DPAK (TO-252) type A drawing

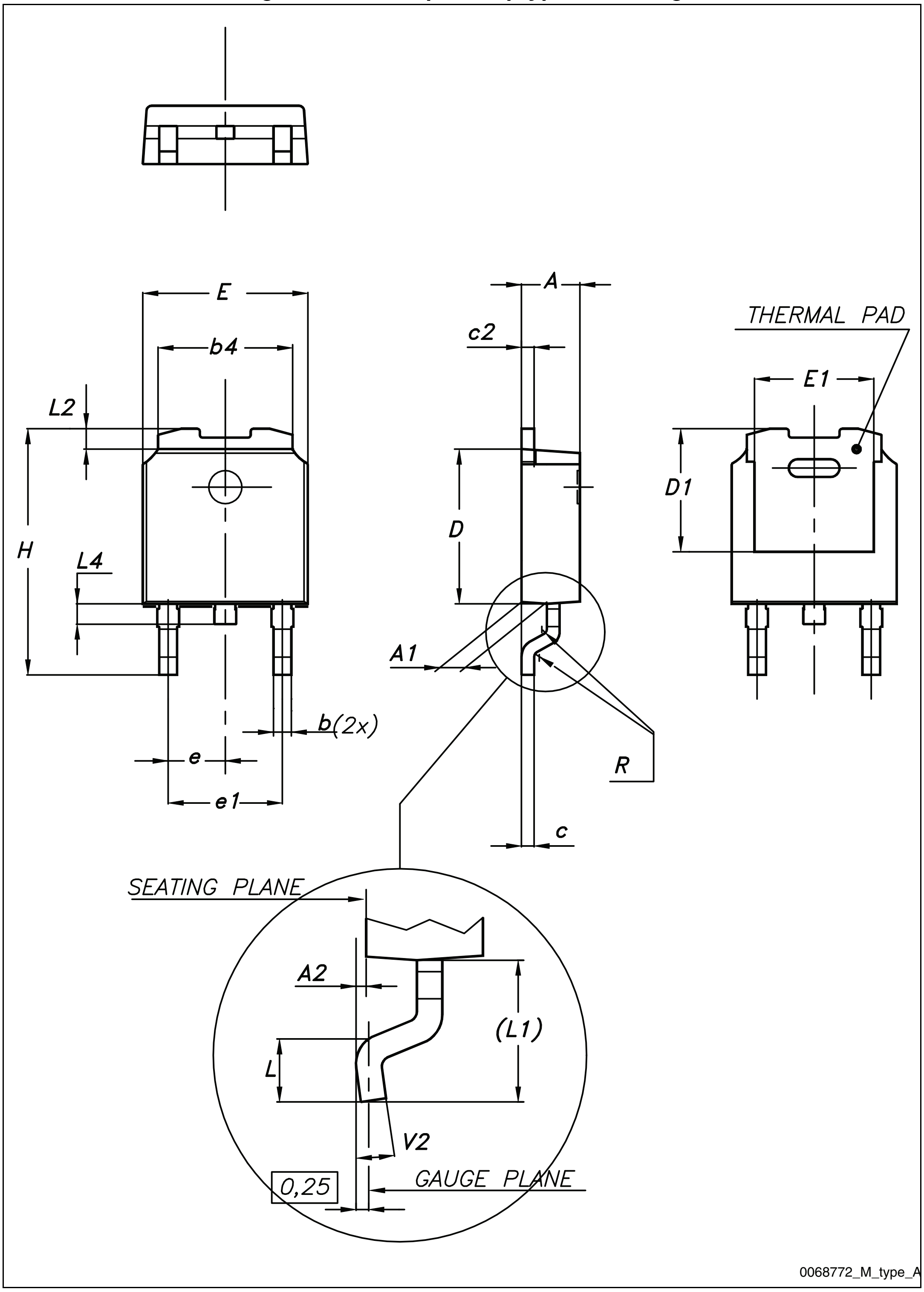
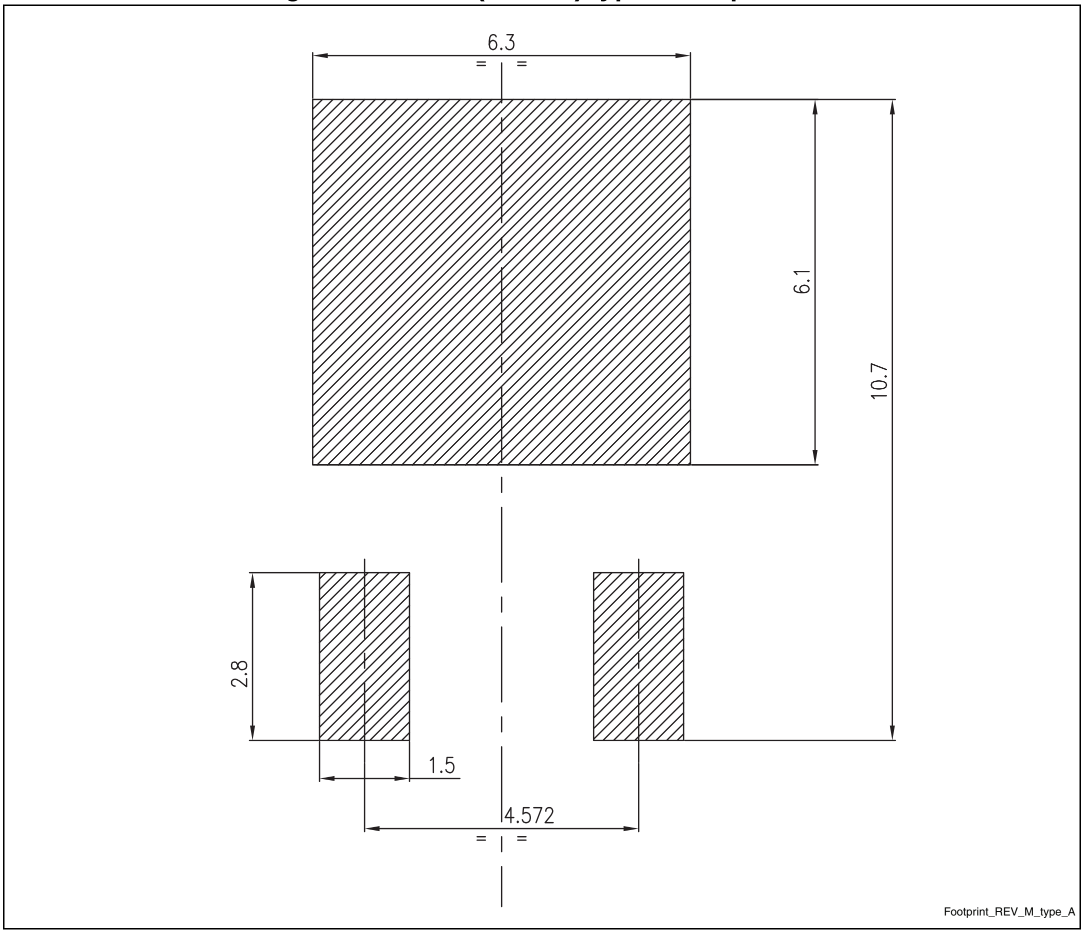


Table 9. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 25. DPAK (TO-252) type A footprint [(a)]



a. All dimensions are in millimeters

4.2 TO-220, STP5N60M2

Figure 26. TO-220 type A drawing

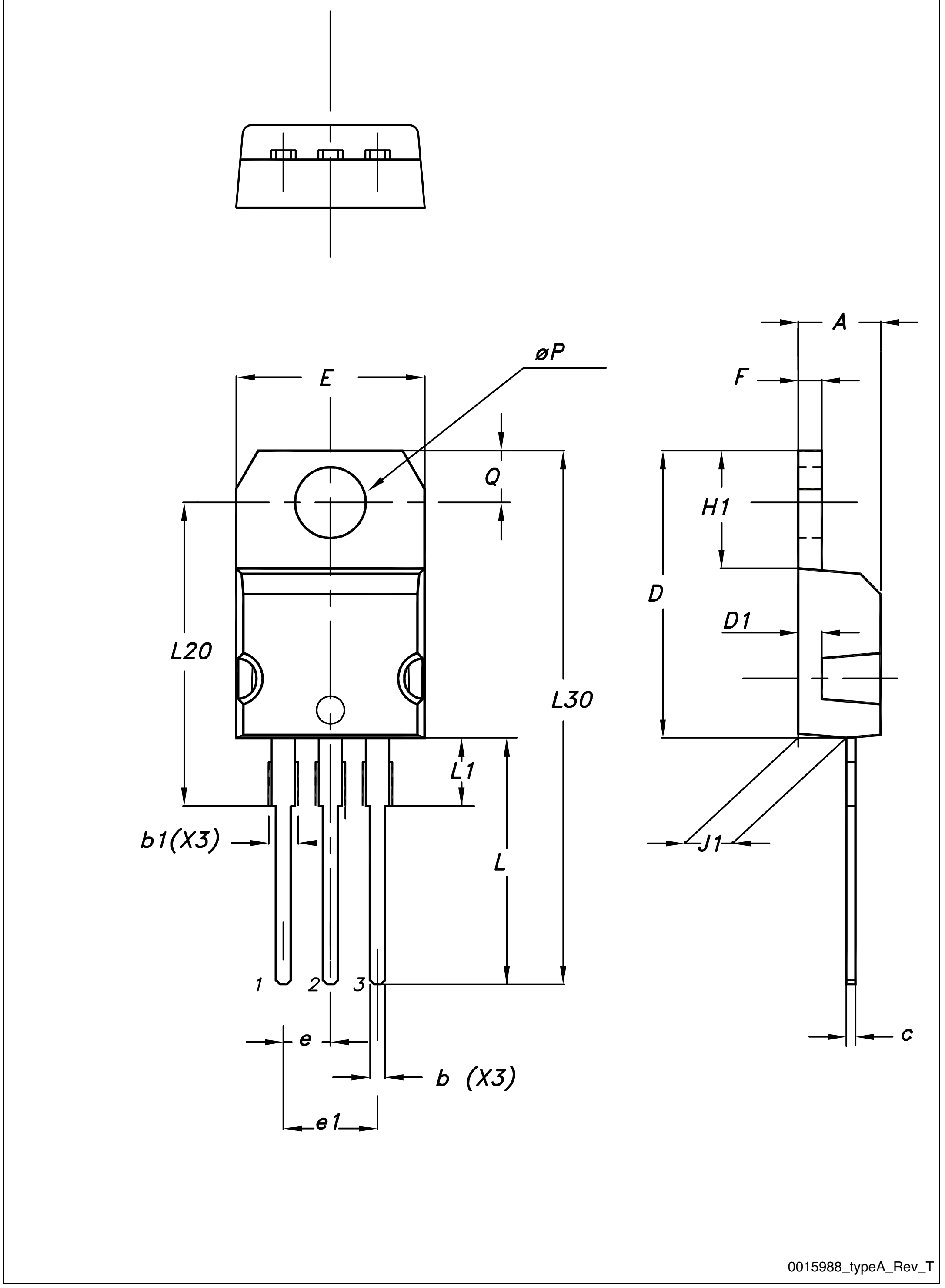


Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ÆP	3.75		3.85
Q	2.65		2.95

4.3 IPAK, STU5N60M2

Figure 27. IPAK (TO-251) drawing

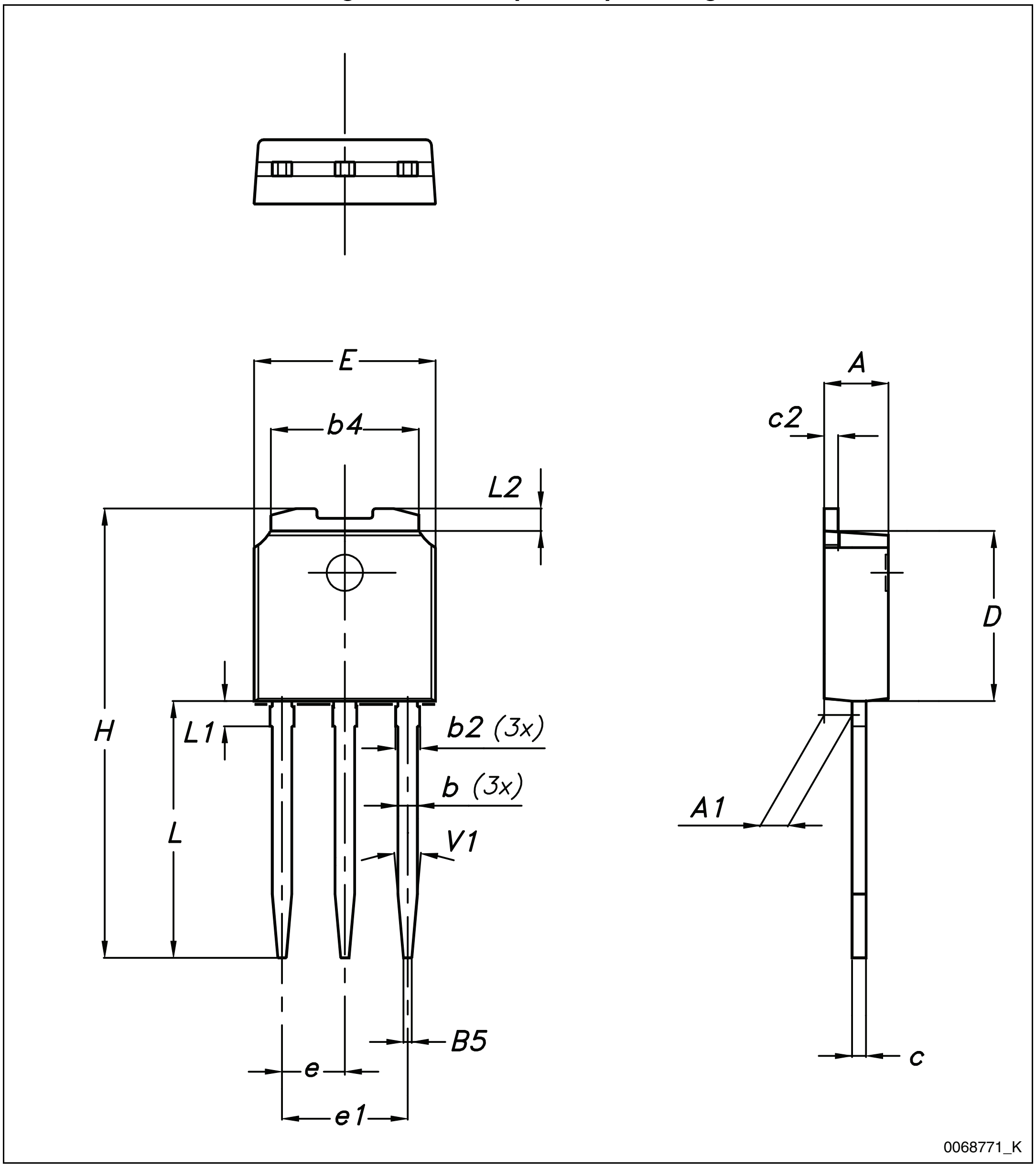


Table 11. IPAK (TO-251) mechanical data

DIM	mm.		
	min.	typ.	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

5 Packaging mechanical data

Figure 28. Tape

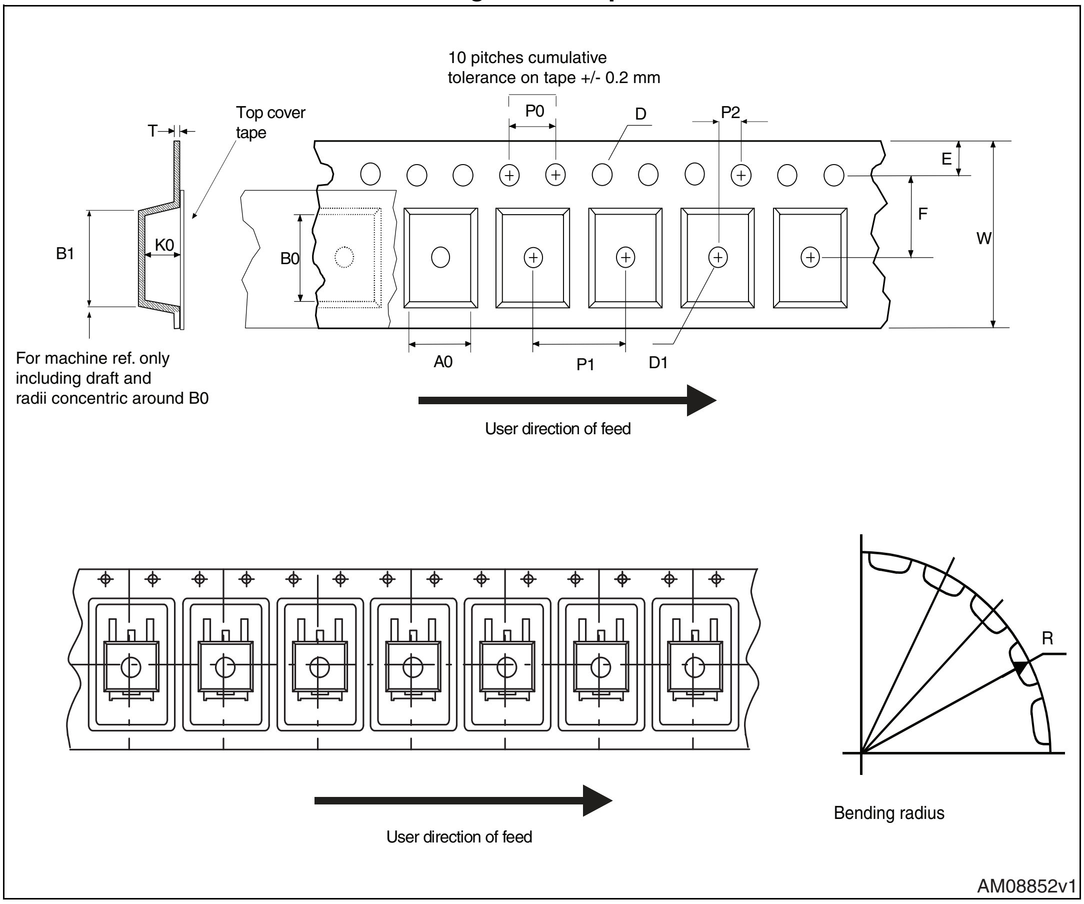


Figure 29. Reel

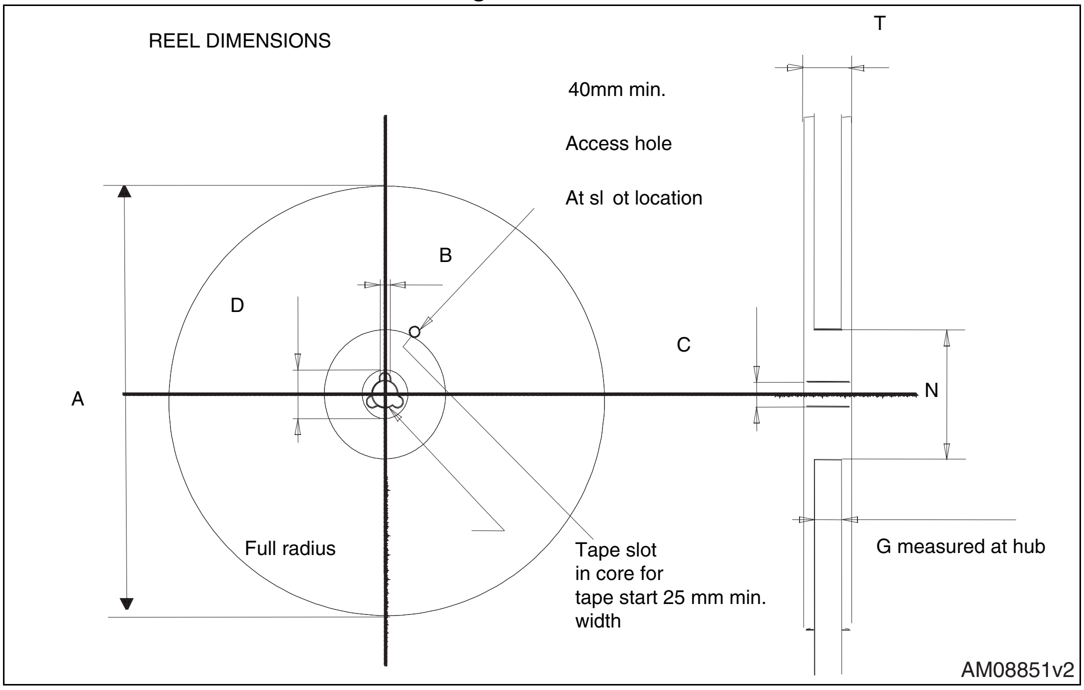


Table 12. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

6 Revision history

Table 13. Document revision history

Date	Revision	Changes
30-Sep-2013	1	First release.
20-Mar-2014	2	– Modified: I_D, I_{DM} and *note 2* values in *Table 2* – Modified: the entire values in *Table 4* – Modified: $R_{DS(on)}$ typical and I_D values in *Table 5* – Modified: the entire typical values, I_{SD} and I_{SDM} in *Table 6*, *7* and *8* – Updated: *Section 4.1: DPAK, STD5N60M2* – Minor text changes