LSF0102-Q1 Automotive 2-Channel Auto Bidirectional Multi-Voltage Level Translator

1 Features

- AEC-Q100 Qualified for Automotive Applications
  - Temperature Grade 1: –40°C ≤ T_A ≤ 125°C
  - Device HBM ESD Classification Level 2
  - CDM ESD Classification Level C6
- Provides Bidirectional Voltage Translation With No Direction Pin
- Supports open drain and push-pull applications such as I^2C, SPI, UART, MDIO, SDIO, and GPIO
- Supports Up to 100 MHz Up Translation and Greater Than 100 MHz Down Translation at ≤ 30pF Cap Load and Up To 40 MHz Up/Down Translation at 50 pF Cap Load
- Enables Bidirectional Voltage Level Translation Between
  - 0.95 V ↔ 1.8/2.5/3.3/5 V
  - 1.2 V ↔ 1.8/2.5/3.3/5 V
  - 1.8 V ↔ 2.5/3.3/5 V
  - 2.5 V ↔ 3.3/5 V
  - 3.3 V ↔ 5 V
- Low Standby Current
- 5 V Tolerant I/O Ports to Support TTL Voltage Levels
- Low r_{on} Provides Less Signal Distortion
- High-Impedance I/O pins when EN = Low
- Flow-Through Pinout for Ease of PCB Trace Routing
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

2 Applications

- Infotainment Head Unit
- Graphical Cluster
- ADAS Fusion
- ADAS Front Camera
- HEV Battery Management System

3 Description

The LSF0102-Q1 device is an auto bidirectional voltage translator that translates among a wide range of supplies without the need for a directional pin. The LSF0102-Q1 supports up to 100 MHz up translation and greater than 100 MHz down translation with capacitive loads ≤ 30 pF. Additionally, the LSF0102-Q1 supports up to 40 MHz up and down translation at 50 pF capacitance load, which enables the LSF0102-Q1 device to support a wide variety of standard interfaces commonly found in automotive applications such as I^2C, SPI, GPIO, SDIO, UART, and MDIO.

The LSF0102-Q1 device has 5-V tolerant data inputs. This makes the device compatible with TTL voltage levels. Furthermore, the LSF0102-Q1 supports mixed-mode voltage translation, allowing the device to up translate and down translate to different supply levels on each channel.

Device Information(1)

PART NUMBER	PACKAGE(PINS)	BODY SIZE (NOM)
LSF0102QDCURQ1	VSSOP (8)	2.30 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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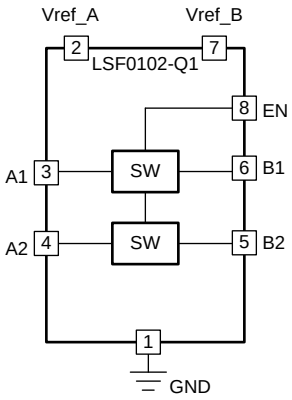

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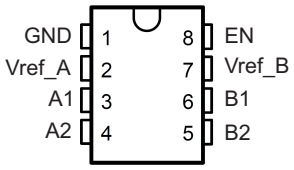
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2018	*	Initial release.

5 Pin Configuration and Functions

LSF0102-Q1 DCU Package
8-Pin VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	DCU		
A1	3	I/O	Input/Output A port for Channel 1
A2	4	I/O	Input/Output A port for Channel 2
B1	6	I/O	Input/Output B port for Channel 1
B2	5	I/O	Input/Output B port for Channel 2
EN	8	I	I/O enable input; see Figure 7 for typical setup. Should be tied directly to Vref_B to be enabled or pulled LOW to disable all I/O pins.
GND	1	—	Ground
Vref_A	2	—	A side reference supply voltage; see *Application and Implementation* for setup and supply voltage range.
Vref_B	7	—	B side reference supply voltage. Must be connected to supply through 200 kΩ; see *Application and Implementation* for setup and supply voltage range.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage(2), V_I		–0.5	7	V
Input/output voltage(2), $V_{I/O}$		–0.5	7	V
Continuous channel current			128	mA
Input clamp current, I_{IK}	$V_I < 0$		–50	mA
Storage temperature range, T_{stg}		–65	150	°C
Operating junction temperature, T_J			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and input/output negative-voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage		5	V
$V_{ref\_A/B/EN}$	Reference voltage		5	V
I_{PASS}	Pass transistor current		64	mA
T_A	Operating free-air temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LSF0102-Q1 DCU (US8) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	229.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	106.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	141.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	35.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	141.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA, V_{EN} = 0				–1.2	V
I_{IH}	I/O input high leakage	V_I = 5 V, V_{EN} = 0				5.0	µA
I_{CCBA}	V_{ref_B} to V_{ref_A} leakage	V_{ref_B} = V_{EN} = 5.5 V, V_{ref_A} = 4.5 V, I_O = 0, V_I = V_{CC} or GND			1		µA
$C_{I(ref\_A/B/EN)}$	Input capacitance	V_I = 3 V or 0			11		pF
$C_{io(off)}$	I/O pin off-state capacitance	V_O = 3 V or 0, V_{EN} = 0			4.0	6.0	pF
$C_{io(on)}$	I/O Pin on-state capacitance	V_O = 3 V or 0, V_{EN} = 3 V			10.5	12.5	pF
r_{on}(2)	On-state resistance	V_I = 0, I_O = 64 mA	V_{ref_A} = 3.3 V; V_{ref_B} = V_{EN} = 5 V		8.0		Ω
			V_{ref_A} = 1.8 V; V_{ref_B} = V_{EN} = 5 V		9.0		
			V_{ref_A} = 1.0 V; V_{ref_B} = V_{EN} = 5 V		10		
		V_I = 0, I_O = 32 mA	V_{ref_A} = 1.8 V; V_{ref_B} = V_{EN} = 5 V		10		Ω
			V_{ref_A} = 2.5 V; V_{ref_B} = V_{EN} = 5 V		15		
		V_I = 1.8 V, I_O = 15 mA	V_{ref_A} = 3.3 V; V_{ref_B} = V_{EN} = 5 V		9.0		Ω
		V_I = 1.0 V, I_O = 10 mA	V_{ref_A} = 1.8 V; V_{ref_B} = V_{EN} = 3.3 V		18		Ω
		V_I = 0 V, I_O = 10 mA	V_{ref_A} = 1.0 V; V_{ref_B} = V_{EN} = 3.3 V		20		Ω
		V_I = 0 V, I_O = 10 mA	V_{ref_A} = 1.0 V; V_{ref_B} = V_{EN} = 1.8 V		30		Ω

(1) All typical values are at T_A = 25°C.
(2) Measured by the voltage drop between the A and B pins at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) pins.

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6.6 Switching Characteristics (Translating Down): V_{GATE} = 3.3 V

over recommended operating free-air temperature range, V_{GATE} = 3.3 V, V_{IH} = 3.3 V, V_{IL} = 0, and V_M = 1.15 V (unless otherwise noted) (see *Parameter Measurement Information* table)

PARAMETER		TEST CONDITIONS	C_L = 50 pF			C_L = 30 pF			C_L = 15 pF			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high output	From (input) A or B to (output) B or A		1.1			0.7			0.3		ns
t_{PHL}	Propagation delay time, high-to-low output	From (input) A or B to (output) B or A		1.2			0.8			0.4		

6.7 Switching Characteristics (Translating Down): V_{GATE} = 2.5 V

over recommended operating free-air temperature range, V_{GATE} = 2.5 V, V_{IH} = 2.5 V, V_{IL} = 0, and V_M = 0.75 V (unless otherwise noted) (see *Parameter Measurement Information* table)

PARAMETER		TEST CONDITIONS	C_L = 50 pF			C_L = 30 pF			C_L = 15 pF			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high output	From (input) A or B to (output) B or A		1.2			0.8			0.35		ns
t_{PHL}	Propagation delay time, high-to-low output	From (input) A or B to (output) B or A		1.3			1			0.5		

6.8 Switching Characteristics Translating Up): V_{GATE} = 3.3 V

over recommended operating free-air temperature range, V_{GATE} = 3.3 V, V_{IH} = 2.3 V, V_{IL} = 0, V_T = 3.3 V, V_M = 1.15 V and R_L = 300 (unless otherwise noted) (see *Parameter Measurement Information* table)

PARAMETER		TEST CONDITIONS	C_L = 50 pF			C_L = 30 pF			C_L = 15 pF			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high output	From (input) A or B to (output) B or A		1			0.8			0.4		ns
t_{PHL}	Propagation delay time, high-to-low output	From (input) A or B to (output) B or A		1			0.9			0.4		

6.9 Switching Characteristics (Translating Up): V_{GATE} = 2.5 V

over recommended operating free-air temperature range, V_{GATE} = 2.5 V, V_{IH} = 1.5 V, V_{IL} = 0, V_T = 2.5 V, V_M = 0.75 V and R_L = 300 (unless otherwise noted) (see *Parameter Measurement Information* table)

PARAMETER		TEST CONDITIONS	C_L = 50 pF			C_L = 30 pF			C_L = 15 pF			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high output	From (input) A or B to (output) B or A		1.1			0.9			0.45		ns
t_{PHL}	Propagation delay time, high-to-low output	From (input) A or B to (output) B or A		1.3			1.1			0.6		

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6.10 Typical Characteristics

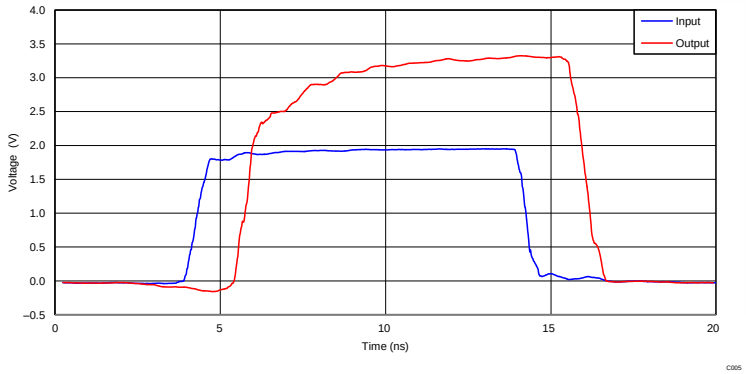

Figure 1. Signal Integrity (1.8 to 3.3 V Translation Up at 50 MHz)

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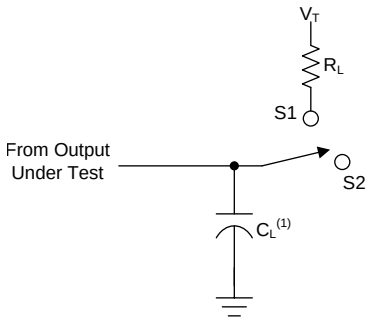
7 Parameter Measurement Information

The outputs are measured one at a time, with one transition per measurement. All input pulses are supplied by generators that have the following characteristics:

- PRR ≤ 10 MHz
- Z_O = 50 Ω
- t_r ≤ 2 ns
- t_f ≤ 2 ns



(1) C_L includes probe and jig capactictance.

Figure 2. Load Circuit

USAGE	SWITCH
Translating Up Translating Down	S1 S2

Figure 3. Translating Up and Down Table

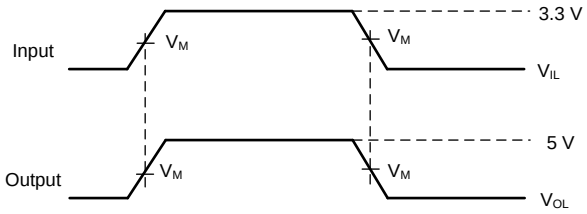


Figure 4. Translating Up

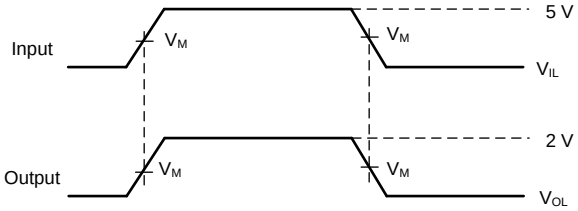


Figure 5. Translating Down

ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

The LSF0102-Q1 device can be used in level translation applications for interfacing devices or systems operating at different interface voltages. The LSF0102-Q1 device is ideal for use in applications where an open-drain driver is connected to the data I/Os. With appropriate pull-up resistors and layout, the LSF0102-Q1 device can achieve 100 MHz. The LSF0102-Q1 can also be used in applications where a push-pull driver is connected to the data I/Os.

8.2 Functional Block Diagrams

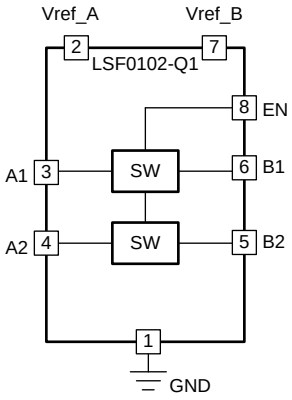


Figure 6. LSF0102-Q1 Functional Block Diagram

8.3 Feature Description

8.3.1 Auto Bidirectional Voltage Translation

The LSF0102-Q1 device is an auto bidirectional voltage level translator that operates from 0.95 to 4.5 V on Vref_A and 1.8 to 5.5 V on Vref_B. This allows bidirectional voltage translation between 0.95 V and 5.5 V without the need for a direction pin in open-drain or push-pull applications. The LSF0102-Q1 device supports level translation applications with transmission speeds greater than 100 Mbps for open-drain systems using a 250-Ω pullup resistor with a 30-pF capacitive load.

8.3.2 Output Enable

When EN is HIGH, the translator switch is on, and the An I/O is connected to the Bn I/O, respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state exists between ports. To enable the I/O pins, the EN input should be tied directly to Vref_B. To ensure the high-impedance state during power-up or power-down, EN must be LOW. For additional details on how to use the enable pin, see the *Using the Enable Pin with the LSF Family* video.

Table 1. Enable Function Table

INPUT EN(1) PIN	FUNCTION
Tied directly to Vref_B	An = Bn
L	Hi-Z

(1) EN is controlled by V_{ref_B} logic levels and should be at least 1 V higher than V_{ref_A} for best translator.

8.3.3 Mixed-Mode Voltage Translation

The supply voltage (Vpu#) for each channel can be individually set up with a pull-up resistor. For example, CH1 can be used in up-translation mode (1.2 V ↔ 3.3 V) and CH2 in down-translation mode (2.5 V ↔ 1.8 V). For additional details on how to use the LSF0102-Q1 for mixed-mode voltage translation, see the *Multi-Voltage Translation with the LSF Family* video.

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8.4 Device Functional Modes

When the An or Bn port is LOW, the switch is in the ON-state and a low resistance connection exists between the An and Bn ports. The low R_{on} of the switch allows connections to be made with minimal propagation delay and signal distortion. Assuming the higher voltage is on the Bn port when the Bn port is HIGH, the voltage on the An port is limited to the voltage set by Vref_A. When the An port is HIGH, the Bn port is pulled to the drain pull-up supply voltage ($V_{pu\#}$) by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for direction control. For additional details on the functional operation of the LSF0102-Q1, see the *Down Translation with the LSF Family* and *Up Translation with the LSF Family* videos.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

ADVANCE INFORMATION

9.1 Application Information

The LSF0102-Q1 device is able to perform voltage translation for open-drain or push-pull interfaces such as I^2C, SPI, UART, MDIO, SDIO, and GPIO.

9.2 Typical Application

9.2.1 Bidirectional Translation

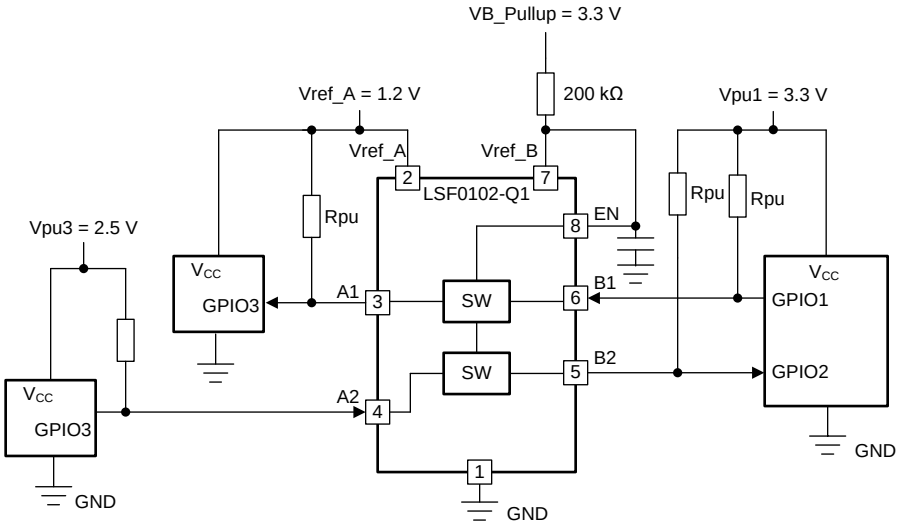

Figure 7. Bidirectional Translation to Multiple Voltage Levels

9.2.1.1 Design Requirements

9.2.1.1.1 Enable, Disable, and Reference Voltage Guidelines

The LSF0102-Q1 device has an EN input that is used to disable the device by setting EN LOW, which places all I/Os in the high-impedance state. Since LSF family is switch-type voltage translator, the power consumption is very low. It is recommended to always enable LSF0102-Q1 device for bidirectional applications by connecting the EN pin to the Vref_B pin, as shown in Figure 7. For additional details on setting up the Vref_A, Vref_B, and EN pins, see the *Understanding the Bias Circuit for the LSF Family* video.

Typical Application (continued)

Table 2. Application Operating Condition

PARAMETER		MIN	TYP	MAX	UNIT
Vref_A (1)	reference voltage (A)	0.95		4.5	V
Vref_B	reference voltage (B)	Vref_A + 0.8		5.5	V
$V_{I(EN)}$	input voltage on EN pin	Vref_A + 0.8	Vref_B	5.5	V
Vpu	pull-up supply voltage	0		Vref_B	V

(1) Vref_A is required to be the lowest voltage level across all inputs and outputs.

The 200 kΩ, pull-up resistor is required to allow Vref_B to regulate the EN input. A filter capacitor on Vref_B is recommended. Also Vref_B and $V_{I(EN)}$ are recommended to be 1.0 V higher than Vref_A for best signal integrity.

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Bidirectional Translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to Vref_B and both pins pulled to HIGH side Vpu through a pull-up resistor (typically 200 kΩ), as shown in Figure 7. This allows Vref_B to regulate the EN input. A filter capacitor on Vref_B is recommended. The master output driver can be push-pull or open-drain (pull-up resistors may be required) and the slave device output can be push-pull or open-drain (pull-up resistors are required to pull the Bn outputs to Vpu).

If either output is push-pull, data must be unidirectional or the outputs must be tri-state and be controlled by some direction-control mechanism to prevent HIGH-to-LOW contention in either direction. If both outputs are open-drain, no direction control is needed.

In Figure 7, the reference supply voltage (Vref_A) is connected to the processor core power supply voltage. When Vref_B is connected through a 200 kΩ resistor to a 3.3 V Vpu power supply, and Vref_A is set 1.2 V. The output of A1 has a maximum output voltage equal to Vref_A, and the bidirectional interface on channel 2 has a maximum output voltage equal to Vpu.

9.2.1.2.2 Pull-up Resistor Sizing

To maintain an appropriate output low voltage, the pull-up resistor value should limit the current through the pass transistor when it is in the ON state to less than 15 mA. This ensures a pass voltage of 260 mV to 350 mV. To set the current through each pass transistor at 15 mA, the pull-up resistor value can be calculated using the following equation:

$$Rpu = (Vpu – 0.35\ V) / 0.015\ A \quad (1)$$

The appropriate pull up resistor will depend on the current requirements of the application. Table 3 summarizes resistor values, reference voltages, and currents at 15 mA, 10 mA, and 3 mA. The resistor value shown in the +10% column (or a larger value) should be used to ensure that the pass voltage of the transistor is 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the LSF0102-Q1 device at 0.175 V, although the 15 mA applies only to current flowing through the LSF0102-Q1.

Table 3. Pull-up Resistor Values (1) (2)

V_{DPU}	15 mA		10 mA		3 mA	
	NOMINAL (Ω)	+10% (3) (Ω)	NOMINAL (Ω)	+10% (3) (Ω)	NOMINAL (Ω)	+10% (3) (Ω)
5 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

(1) Calculated for V_{OL} = 0.35 V
(2) Assumes output driver V_{OL} = 0.175 V at stated current
(3) +10% to compensate for V_{DD} range and resistor tolerance

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9.2.1.3 Application Curve

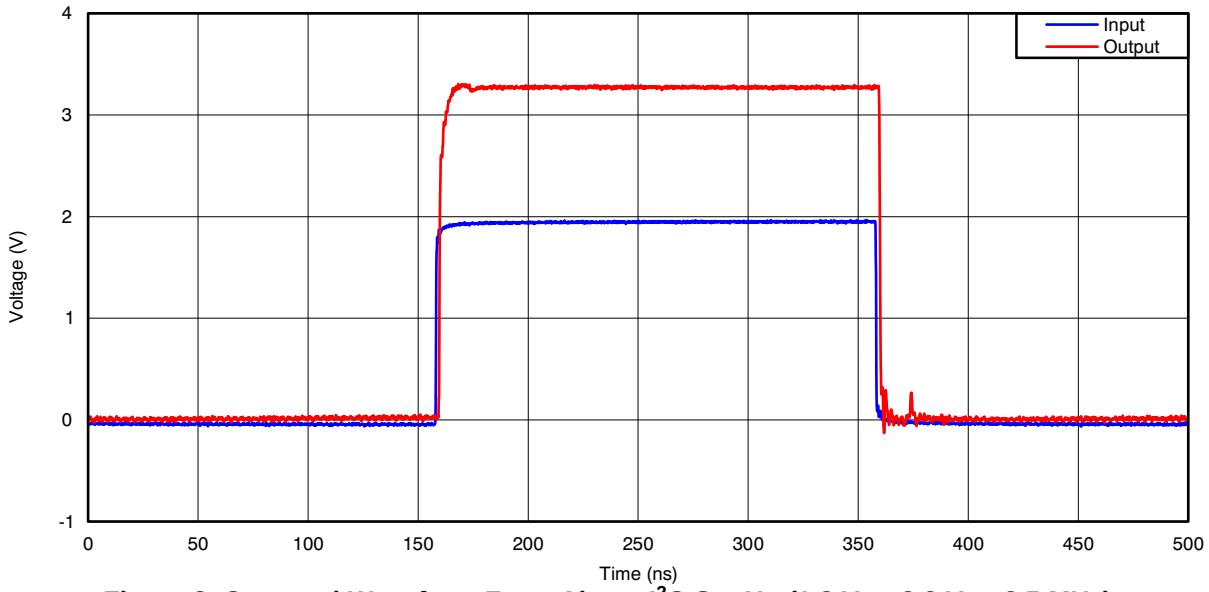

Figure 8. Captured Waveform From Above I^2C Set-Up (1.8 V to 3.3 V at 2.5 MHz)

ADVANCE INFORMATION

10 Power Supply Recommendations

There are no power sequence requirements for the LSF family. For recommended operating voltages for all supply and input pins, see Table 5.

Table 4. Recommended Operating Voltages

PARAMETER		MIN	TYP	MAX	UNIT
Vref_A (1)	reference voltage (A)	0.95		4.5	V
Vref_B	reference voltage (B)	Vref_A + 0.8		5.5	V
$V_{I(EN)}$	input voltage on EN pin	Vref_A + 0.8		5.5	V
Vpu	pull-up supply voltage	0		Vref_B	V

(1) Vref_A is required to be the lowest voltage level across all inputs and outputs.

11 Layout

11.1 Layout Guidelines

Because the LSF0102-Q1 device is a switch-type level translator, the signal integrity is dependent upon the pull-up resistor value and PCB board parasitics. Consider the following recommendations when designing with the LSF0102-Q1.

- Minimize the signal trace length to reduce capacitance
- Avoid using stubs in the signal path to reduce parasitics.
- Place the LSF0102-Q1 device near the high voltage side.
- Select the appropriate pull-up resistor that applies to translation levels and driving capability of transmitter.

11.2 Layout Example

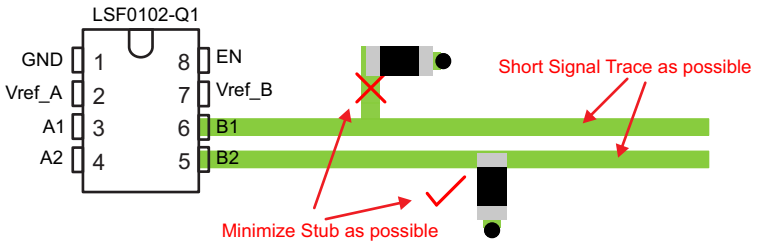

Figure 9. Short Trace Layout

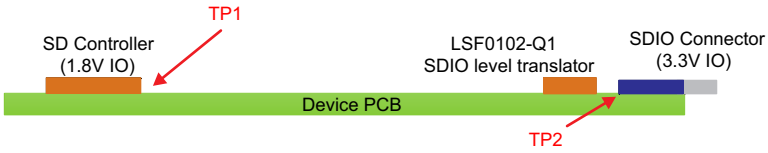

Figure 10. Device Placement

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, TI Logic Minute: *Introduction – Voltage Level Translation with the LSF Family* video
- Texas Instruments, *Voltage-Level Translation With the LSF Family* application report

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LSF0102	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LSF0102QDCURQ1	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	NG2SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

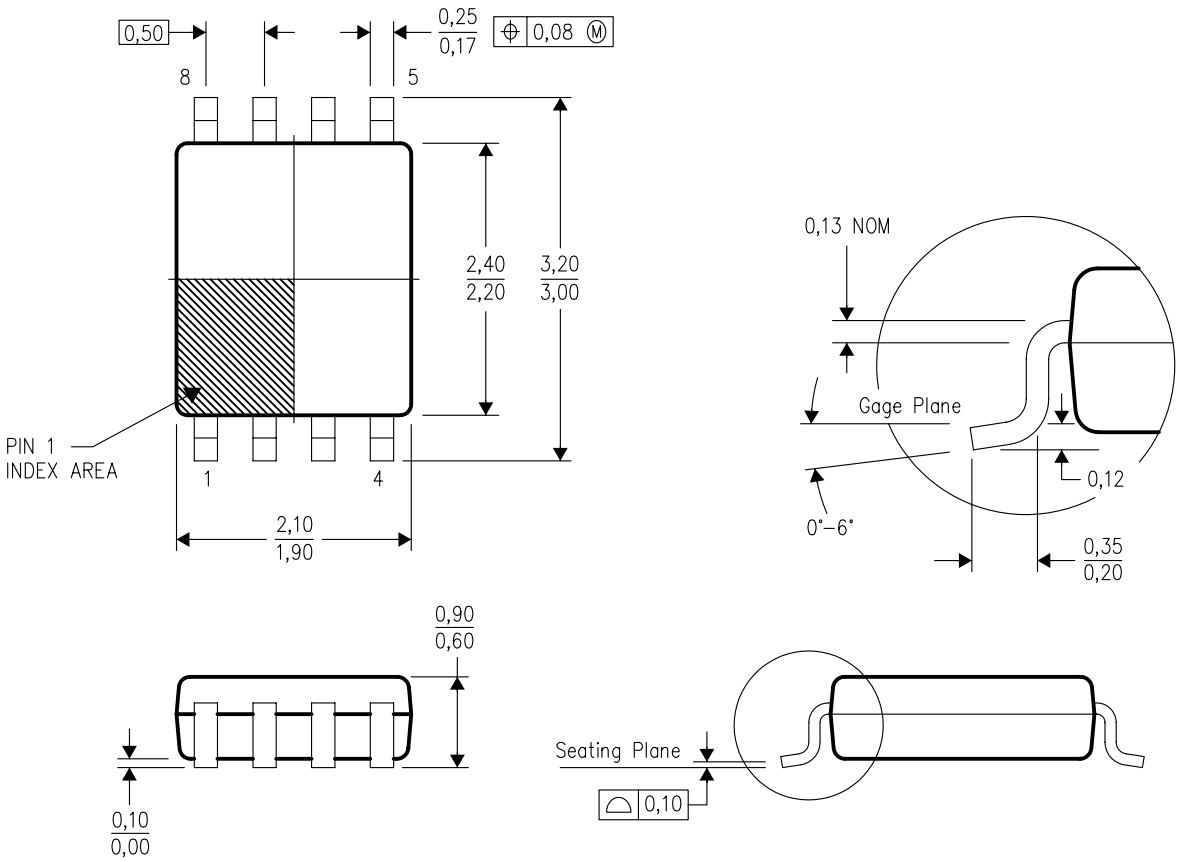
OTHER QUALIFIED VERSIONS OF LSF0102-Q1 :

- Catalog: LSF0102

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

DCU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–187 variation CA.

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